Aug. 2, 1966 G. B. PARKINSON 3,264,637

LOGARITHMIC CONVERTERS

Filed May 31, 1963 3 Sheets-Sheet 1

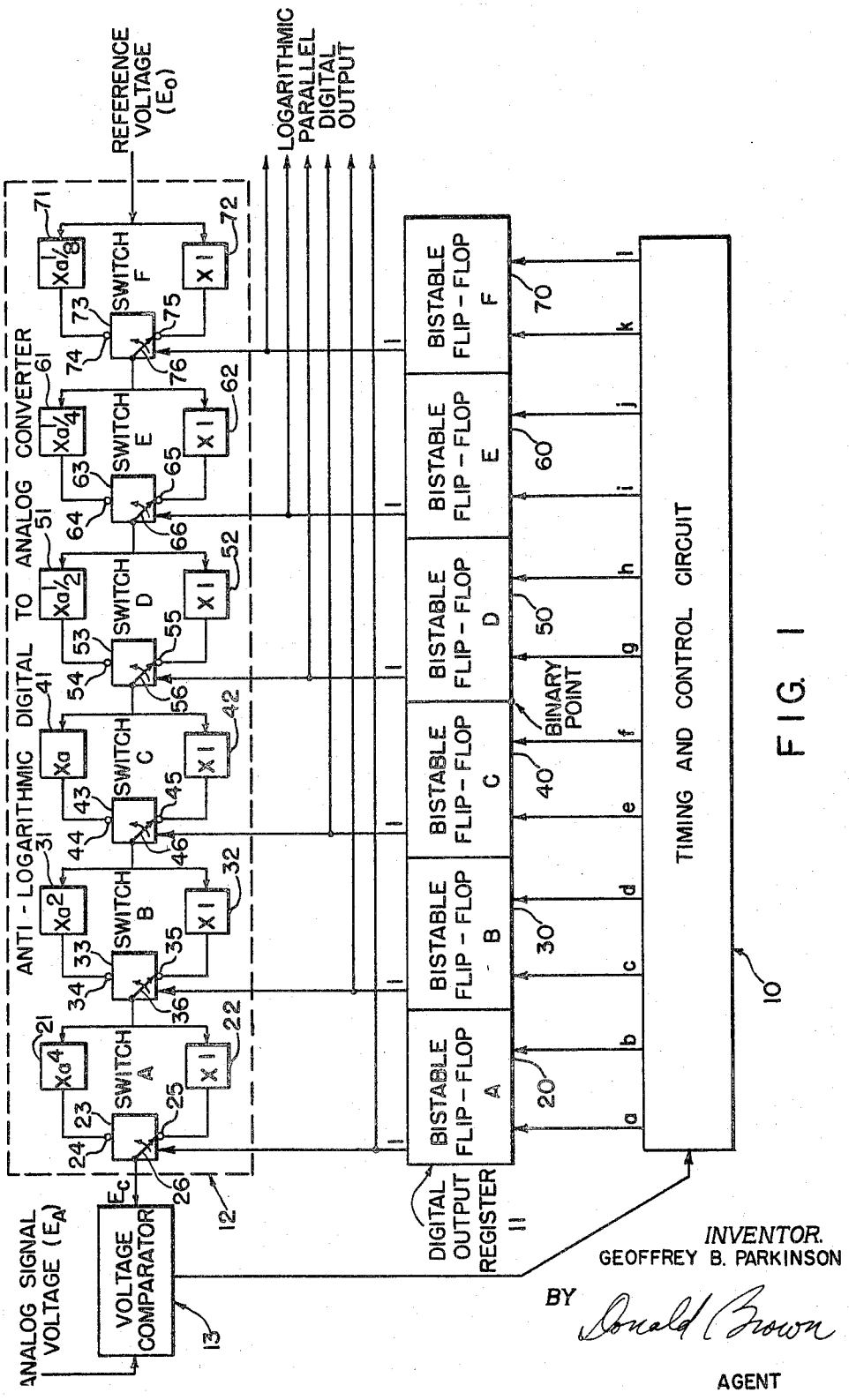


FIG. 1

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Aug. 2, 1966 G. B. PARKINSON 3,264,637

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Filed May 31, 1963 3 Sheets-Sheet 2

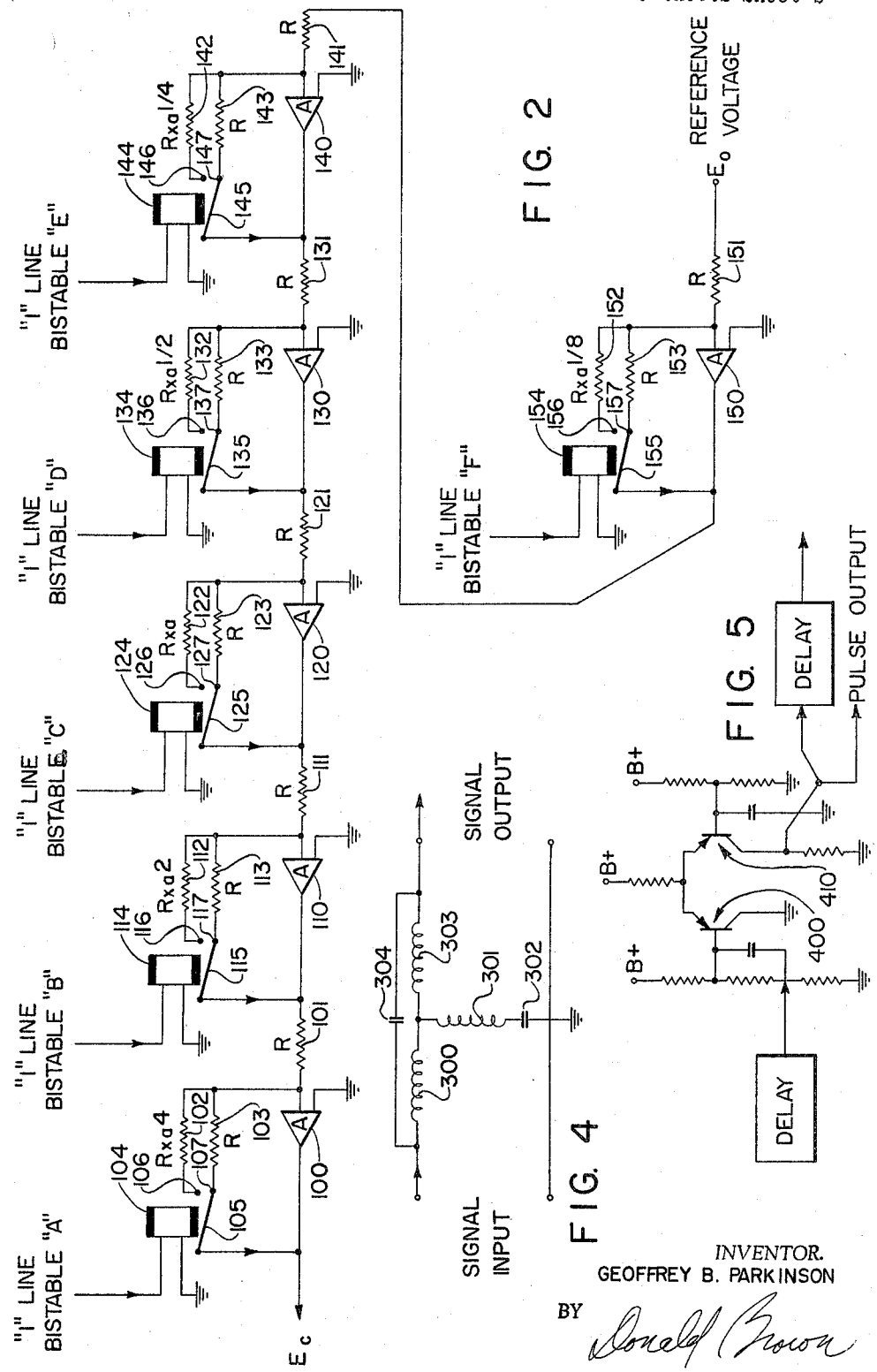


FIG. 2

FIG. 4

FIG. 5

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LOGARITHMIC CONVERTERS

Filed May 31, 1963 3 Sheets-Sheet 3

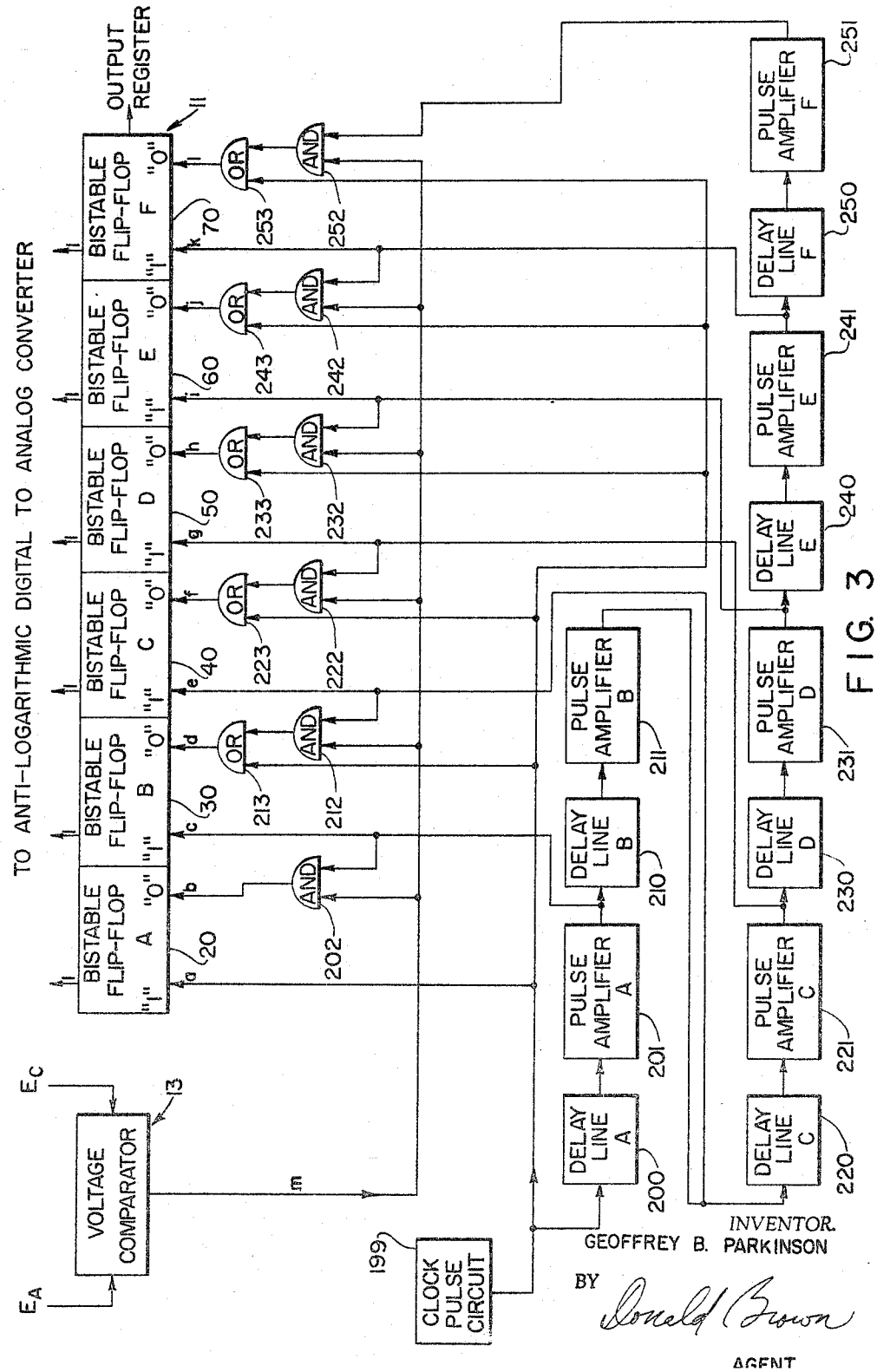


FIG. 3

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3,264,637

LOGARITHMIC CONVERTERS

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Filed May 31, 1963, Ser. No. 284,483
7 Claims. (Cl. 340—347)

The present invention relates to converter systems and more particularly to encoding systems for effecting the conversion of analog signals to provide a digital logarithmic representation of said analog signals. Additionally, this invention relates to a converter system for effecting conversion of a logarithmic digital signal to obtain an analog signal representative of said logarithmic digital signal.

Various means have heretofore been proposed in the prior art for converting analog information to digital information and vice versa. Prior art logarithmic conversion systems generally relate to mechanical devices such as, for example, cathode ray raster techniques to provide a logarithmic digital signal representative of an analog input. Additionally, mechanically rotated encoded disks have been provided which operate on an analog signal to provide a digital representation in logarithmic form of said analog signal.

Other prior art systems have disclosed the use of an analog device for providing a logarithmic analog signal representative of an analog input signal in combination with a linear or other type of analog to digital converter, thereby obtaining a digital signal representative of the logarithmic analog input signal. This above-mentioned type of device using the combination of a logarithmic analog device and linear analog to digital converter has required an undesirable complexity of equipment to provide this logarithmic digital output.

Accordingly, it is an object of this invention to provide a new, useful and improved converter for effecting the conversion of an analog signal to a digital signal without the requirement of a logarithmic analog device in combination with an analog to digital device.

It is a further object of this invention to provide an improved electrical device for converting an analog signal varying over a wide dynamic range to its logarithmic digital representation.

It is an additional object of this invention to quantize an analog signal in accordance with feedback principles to provide a logarithmic digital representation of said analog signal.

A further object of this invention is to provide an anti-logarithmic device which converts a logarithmic digital signal to obtain an analog signal representative of said logarithmic digital signal.

In accordance with this invention, electrical means for converting an analog signal or voltage to a logarithmic digital signal including means for obtaining the product of a signal and a factor is provided without the requirement of a separate analog to logarithmic analog conversion device in combination with an analog to digital conversion device. In the preferred embodiment of this invention, an analog signal input voltage to be converted is applied to a voltage comparator device where it is compared with a comparison signal. The anti-logarithmic digital to analog conversion device for providing this voltage comparison signal operates utilizing feedback encoding techniques wherein a logically controlled register or storage device provides signals for selectively and sequentially operating and stepping a plurality of switches of said digital to analog conversion device. This technique permits a reference signal to be selectively multiplied by either a constant or a factor which is the base of the desired logarithmic to a power,

thereby obtaining a comparison signal substantially equal in magnitude to the analog signal. The digital register is then sampled after the comparison process is completed to obtain a digital signal representative of the logarithmic of the analog signal.

The above-mentioned and other features and objects of this invention and the manner of obtaining them will best be understood by reference to the following description of an embodiment of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram of a particular system for producing a binary code representative of the logarithm to any particular base of a given analog signal;

FIG. 2 illustrates the details of the anti-logarithmic digital to analog converter of FIG. 1;

FIG. 3 shows a logical flow diagram of the timing and control circuit of FIG. 1;

FIG. 4 shows a typical delay line section in schematic form; and

FIG. 5 is a schematic diagram of a typical pulse amplifier for use in the timing and control circuits of FIG. 3.

Although the principle of operation of the present invention is applicable to any number of bits to provide a digital output number representative of the logarithm of an analog signal to any desired logarithmic base, apparatus supplying six bits to represent a number 7.875 is considered sufficient for illustrative purposes and will be described herein by way of example.

In FIG. 1 an input analog signal or voltage the amplitude of which contains information, such as that which could be obtainable in the monitoring of chemical or other types of processes, is applied to a voltage sampler or comparator **13** wherein it is compared with a comparison signal or voltage E_c in order to determine whether or not the input analog voltage E_A is greater or less than the comparison voltage. The voltage comparator **13** could be of the type found in chapter 15 of the book "Pulse and Digital Circuits" by Millman and Taub, published by the McGraw Hill Book Company in 1956 and more particularly could be the difference amplifier shown on page 467 of this book.

The output signal from the voltage comparator **13** is provided to a timing and control circuit **10** for providing a plurality of logical signals from its output lines *a, b, c, d, e, f, g, h, i, j, k* and *l* to control a digital output register **11**. The timing and control circuit **10** is shown in FIG. 3 and operation will be discussed in conjunction with a description of FIG. 3. The digital output register **11** operates to selectively provide a plurality of signals to actuate an anti-logarithmic digital to analog converter which is used to generate the aforementioned comparison signal E_c. Additionally, at the completion of the comparison the digital output register **11** can be sampled utilizing standard digital techniques in order to obtain a logarithmic digital output representative of the analog input signal. The digital output register **11** comprises six bi-stable flip-flops referred to as bi-stable flip-flop A, shown as **20**, bi-stable flipflop B, shown as **30**, bi-stable flip-flop C, shown as **40**, bi-stable flip-flop D, shown as **50**, bi-stable flip-flop E, shown as **60** and bi-stable flip-flop F, shown as **70**. Each of these flip-flops is shown having its "1" output coupled to a plurality of switches in the logarithmic digital to analog converter **12** to provide control signals to said switches in accordance with control signals from the timing and control circuit **10**. The bi-stable flip-flops could be of the type shown in chapter 5 of the book "Pulse and Digital Circuits" referred to above in conjunction with the voltage comparator and, more particularly, could be the circuit shown on page 142 of the above-referenced book.

The aforementioned anti-logarithmic digital to analog converter **12** is shown for providing a comparison voltage E_c by selectively multiplying a reference signal or voltage E_o by a plurality of multiplication factors in accordance with signals provided by said digital register **11**. For purposes of explanation, the anti-logarithmic digital to analog converter **12** will first be described with relation to the block diagram of FIG. 1, and will be further described after completion of this description with reference to the schematic diagram of FIG. 2 in order to set forth a particular circuit which is capable of operating as an anti-logarithmic digital to analog converter. Referring to FIG. 1, the anti-logarithmic digital to analog converter **12** comprises a plurality of two position switches, such as switch A, **23**, having contacts **24** and **25** with an arm **26** able to be closed on either contact **24** or **25**. Switch **23**, which is shown coupled to bi-stable flip-flop A, has its arm **26** positioned on contact **25** in the absence of a signal or voltage on the "1" line from bi-stable flip-flop A and has its arm **26** positioned on contact **24** in the presence of a signal or voltage on the "1" line of bi-stable flip-flop A. While switch A comprises a relay as shown in FIG. 2, other embodiments could utilize electronic switches comprising diode or transistor networks. Shown coupled to switch A at contacts **24** and **25** are two multiplication factor devices shown as blocks **21** and **22**. Devices for providing multiplication factors could comprise the operational amplifier circuit shown in FIG. 2, or alternatively could be constructed utilizing resistive attenuation networks and other types of operational amplifier circuits known to the analog computer art. Block **21** represents a device for multiplying a signal by "a^4," wherein "a" represents the base of the required logarithm. Block **22** is shown for multiplying a signal such as E_o times "1." Depending upon the position of arm **26** of switch A, a signal such as E_o will be multiplied by either "a^4," or "1" and thus the comparison signal E_c, which is equal to E_o times a factor, will be a function of the position of the arm **26** of switch A.

There is also shown a switch B, **33**, functioning the same as switch A and having contacts **34** and **35** and a moving arm **36** which is positioned either at contact **34** or **35** in accordance with an output from bi-stable flip-flop B. Coupled to switch B are two blocks **31** and **32** representing the multiplication factors "1" and "a^2". These blocks **31** and **32** affect the input reference voltage E_o in the same manner as described with relation to blocks **21** and **22**, thus affecting the magnitude of the generated comparison voltage E_c. A third switch C, **43**, is also shown having contacts **44** and **45** with an arm **46** responsive to an output signal from bi-stable flip-flop C. A block **41** is shown for providing a multiplication factor "a" in one path and a multiplication factor "1" in another path. This device functions similarly as described with relation to blocks **31** and **32** and affects the magnitude of the comparison voltage E_c depending upon the position of arm **46**. Further, a switch E, **53**, having contacts **54** and **55** with a movable arm **56**, responsive to the presence of an output signal from bi-stable flip-flop D, is shown having connected to it a block **51** providing a multiplication factor "$a^{1/2}$" in one path and a multiplication factor of "1" in another path. Switch D in blocks **51** and **52** operates in the same manner as described with relation to blocks **41** and **42** in switch C above, and accordingly affect the magnitude of the comparison signal E_c.

A fifth switch E, **63**, is shown having contacts **64** and **65** and a movable arm **66**, which is responsive to an output signal provided from bi-stable flip-flop E. Block **61** is shown in one signal path coupled to switch E for providing a multiplication factor "$a^{1/4}$" and a block **62** is shown for providing a multiplication factor "1" in another signal path. Switch E and blocks **61** and **62** perform in the same manner as described with relation to switch D and blocks **51** and **52** mentioned above, and therefore, accordingly affect the magnitude of the comparison signal E_c.

The sixth switch F, **73**, having contacts **74** and **75** with a movable arm **76** responds to an output signal from bi-stable flip-flop F. In one signal path there is shown a block **71** for providing a multiplication factor "$a^{1/8}$" and a block **72** in another signal path for providing a multiplication factor "1." Blocks **71** and **72** are shown coupled to a reference voltage E_o. Switch F and blocks **71** and **72** operate similarly as described with reference to blocks **61** and **62** and switch E above, and thus, accordingly affect the magnitude of the comparison voltage E_c. From this it can thus be seen that if a reference voltage E_o is applied to the logarithmic digital to analog converter **12**, a comparison voltage E_c is generated which is a function of the position of the arms **26**, **36**, **46**, **56**, **66** and **76** of switches A, B, C, D, E and F, respectively, of converter **12**. Thus, by selectively and sequentially utilizing this comparison feedback technique, at balance the analog input signal E_a and the comparison voltage E_c will be substantially equal, and thus by sampling the register flip-flops A, B, C, D, E and F, a logarithmic digital output number representative of the analog input signal can be obtained as will be described below.

Referring again to FIG. 1 for the principle of operation, a logarithmic base "a" is chosen and represents the base of the desired logarithm. For example, "a" could represent the natural log to the base e or the log to the base **10**. The output register **11**, which will hold the binary number resulting from the conversion process, is shown for representing six bits corresponding to the number 7.785 (i.e. 111.111 in binary digital code) and having its binary point between the flip-flop C and the flip-flop D of the output register **11**. Further, it will be observed that the presence of an output digit or a "1" in the register **11** controls a two position switch which selects either of two signal paths. A multiplication factor of "1" is selected when the corresponding digit of the bi-stable flip-flop is in a "0" state, and a factor which is an appropriate power of "a" is selected when the corresponding digit of the bi-stable flip-flop to which it is coupled is in a "1" state. The power of "a" controlled by a particular digit is

$$a^{2^r}$$

where r is the power of 2 represented by that digit in the register. In other words, r designates the position of the digit in any register, relative to the binary point; digits to the left of the point corresponding to values of r equal to 0, 1, 2, etc. and digits to the right of the point corresponding to r equal to -1, -2, -3, etc., respectively.

It can be seen that the application of the comparison output voltage E_c and the voltage from the logarithmic digital to analog converter voltage E_a applied to the voltage comparative circuit **13** will produce an output signal indicating whether the input analog voltage E_a exceeds the comparison voltage E_c, or vice versa.

Each conversion operation or sampling of the input analog voltage E_a consists of an ordered sequence of m tests where m is the total number of digits in the output register. For the first test all the digits in the register **11** are set in the "0" state except the first bi-stable flip-flop A, which represents the most significant digit. This flip-flop A is set to the "1" state. The timing and control circuit **10** performs this function and will be described at a later time with reference to FIG. 3. Due to the bi-stable flip-flop A being placed in the "1" state an output will be applied to the switch **23** so that the a^4 multiplication factor will be applied to the reference voltage E_o. All the other switches will at the same time connect the "times 1" factor in the logarithmic digital to analog converter **12**. Then, if the decision signal out of the voltage comparator **13** indicates that the analog signal voltage E_a exceeds the comparison voltage E_c, the first digit in the digital output register **11** is permitted to remain at

"1" and we then proceed to the second test; if the comparison indicates that E_c is greater than E_a, the bi-stable flip-flop A will be re-set to the "0" state before proceeding to the next test. The required value for the first digit having thus been determined, the remaining digits of the digital register **11** are maintained at "0," that is flip-flops C, D, E and F are maintained in the "0" state except that flip-flop B, representing the next most significant digit, is set to a "1." Now, if the decision signal, that is the signal from the voltage comparator **13**, indicates that the voltage E_a exceeds the comparison voltage E_c, bi-stable flip-flop B, that is the second most significant digit, is allowed to remain at "1"; if not, the second digit is re-set to "0" before proceeding to the next test. Subsequent tests follow a similar procedure, each one determining the value of the most significant remaining digit. After m tests all the digits will have been determined unambiguously. It is thus seen that the comparison voltage E_c consists of a product of a number of contributions, the magnitude of each contribution being determined by the corresponding digit in the output register **11**. Furthermore, it is seen that at balance $E_a=E_0a^N$ and therefore N, the number in the digital output register **11**, is equal to

$$\log_a \frac{E_a}{E_0}$$

or $\log_a E_a - \log_a E_0$, where E_0 is the reference signal or voltage whose magnitude determines the scale factor of the conversion. This explanation is intended to cover the main feature of operation of this device and purposely omits such minor points as the correct rounding off of the output number and the provision of sample and hold circuits for detecting a varying input voltage, all of which are the same as would be applicable to the standard linear A–D converters presently available on the market.

Referring now to FIG. 2, there is shown details of an embodiment of an anti-logarithmic digital to analog converter in schematic form in accordance with the anti-logarithmic digital to analog converter of FIG. 1. Reference voltage E_0 is applied at one end of the anti-logarithmic digital to analog converter device to provide a conversion voltage E_c. This device comprises a plurality of operational amplifiers **100, 110, 120, 130, 140** and **150**. The operational amplifiers could be of that type described in the book "Analog Methods," Second Edition, authored by Karplus and Soroka, published by the McGraw-Hill Book Company in 1959, particularly that described in chapter 2, secs. 2.9–2.15. A plurality of input resistors **101, 111, 121, 131, 141** and **151** is shown coupled to each of these operational amplifiers referred to above. There is also shown a plurality of feedback resistors coupled across each operational amplifier. For example, operational amplifier **100** is provided with a feedback resistor **102** which is weighted to represent the value of the resistance **101** times a^4 and is also provided with a feedback resistor **103** which is equal to the magnitude of resistor **101**. By the use of the relay **104**, an arm **105** can be moved from a contact **107** coupled to the "times 1" path, to contact **106**, which is coupled to the a^4 multiplication path. Thus, by providing an output on the "1" line from bi-stable flip-flop A, a multiplication factor can be selected in accordance with a number set in the respective flip-flops of the digital register. Operational amplifier **100** is also shown having multiplication factor resistors **112** and **113** with a relay device **114** for selectively controlling the appropriate multiplication factor in accordance with a signal from bi-stable flip-flop B. This device operates similarly as described with reference to the multiplication factors coupled across operational amplifier **110**.

The third multiplication factor, that is either "a" or "1" is provided across operational amplifier **120** by the combination of resistors **122** and **123**. By applying an appropriate signal from bi-stable flip-flop C, relay **124** can move arm **125** between contacts **126** and **127**, thereby selectively controlling the multiplication factor provided across operational amplifier **120**.

A fourth multiplication factor that is representative of either "$a^{1/4}$" or "1" is provided by resistors **132** and **133**. By appropriately controlling relay **134** with a signal from bi-stable flip-flop D, movable arm **135** can be positioned between the contacts **136** and **137** to selectively choose the required multiplication factor.

A fifth pair of multiplication factors are provided by a resistor **142** representing "$a^{1/4}$" and a resistor **143** representing "times 1." By appropriately operating relay **144** in accordance with a signal provided by bi-stable flip-flop E, relay arm **145** can be selectively positioned at either contact **146** or **147** to provide the required multiplication factor in the manner described above.

The last multiplication factor for this particular six digital system is provided by a resistor **152** representing the multiplication factor "$a^{1/8}$" and a resistor **153** representing "times 1" by selectively providing an output signal from bi-stable flip-flop F to relay **154**, arm **155** can be coupled to either contact **156** or **157** to selectively choose the required multiplication factor. It is thus seen that an input voltage E_0 will be selectively operated on by a digital signal in such a manner that a logarithmic digital number can be converted to an analog signal representative of said logarithmic digital number. Therefore, this particular digital-analog conversion device can be utilized either as an element in a logarithmic A–D converter or as an output device for providing a conversion of a digital signal to obtain an analog output signal. It is also seen that any digital number, whether representative of a logarithm or not, can be converted to an analog signal representative of the selective multiplication of an input reference signal.

Referring now to FIG. 3, there is shown a logical flow diagram of the timing and control circuit of this invention in block diagram form. The voltage comparator **13** and the output register **12** comprising flip-flops **20, 30, 40, 50, 60** and **70** are also shown in block form. The timing and control circuit referred to as block **10** in FIG. 1 comprises a clock circuit for providing timing pulses to initiate operation of this system. This clock is of the well known pulse type. A plurality of delay line-pulse amplifier combinations shown as delay line **200** and pulse amplifier **201**, delay line **210** and pulse amplifier **211**, delay line **220** and pulse amplifier **221**, delay line **230** and pulse amplifier **231**, delay line **240** and pulse amplifier **241**, and delay line **250** and pulse amplifier **251** are serially coupled to each other and to the clock pulse circuit **199**. This serial combination of delay lines and pulse amplifiers provides sequential and selective actuating pulses which are applied to control the bi-stable flip-flops of the output register **12**. Coupled to the voltage comparator **13** are a plurality of "AND" gates **202, 212, 222, 232, 242** and **252** for logically gating the result of a comparison between E_a and E_c to selectively actuate the flip-flops of output register **12**. These comparison signals are gated in accordance with pulses obtained from the delay line pulse amplifier serial combination referred to above. There is also shown a plurality of "OR" circuits **213, 223, 233, 243** and **253**, coupled respectively to bi-stable flip-flops **30, 40, 50, 60** and **70**. It is noted that bi-stable flip-flop **20** does not have an "OR" circuit coupled to it inasmuch as it is not required for the logical operation of this system. Referring again to FIG. 3 for the principle of operation, the clock circuit **199** provides a signal which initiates three occurrences. Bi-stable flip-flop **20** is set in the "1" state and bi-stable flip-flops **30, 40, 50, 60** and **70** are placed in the "0" state. Additionally, this signal from the clock circuit **199** is applied to the delay line **200** and thus initiates a signal flow through the delay line and pulse amplifier serial combination.

The setting of bi-stable flip-flop **20** in the "1" state causes a comparison signal E_c to be provided to the voltage comparator **13** in accordance with the mode of operation described with reference to FIGS. 1 and 2. The voltage comparator **13** then compares the analog input

signal E_a with the comparison signal E_c. If E_c is less than E_a, voltage comparator **13** will not provide an output signal. If E_c is greater than E_a, an output signal will be provided over line *m*. This output signal is an indication that the generated comparison voltage E_c is greater than E_a. Thus, bi-stable flip-flop **20** will have to be re-set to the "0" state. This is accomplished by the simultaneous application of the delayed signal which passes through delay line **200** and pulse amplifier **201**, and the signal generated from the result of the comparison of E_c and E_a being applied to "AND" circuit **202**. The application of these two signals will cause bi-stable flip-flop **20** to be set to the "0" state. Additionally, the output from pulse amplifier **201** will cause bi-stable flip-flop **30** to be placed in the "1" state in order to generate the second comparison signal in accordance with the operation described with reference to FIGS. 1 and 2. The remainder of the operation, that is the remainder of the sequenced comparison tests, is completed in a similar fashion as described with reference to bi-stable flip-flop **20**. This type of control circuit, described above, is typically shown as a block diagram control circuit, page 489, FIG. 11–8(*a*) in the book "Digital Computer Components and Circuits," by R. K. Richards, published by D. Van Nostrand Co., Inc., in November of 1957.

Referring now to FIG. 4, there is shown a typical logical low-pass all-pass lumped parameter delay line section adapted to pass the clock pulses and which could be utilized as one of a plurality of sections of the delay lines **200**, **210**, **220**, **230**, **240** and **250**, shown in FIG. 3. The delay line section comprises a plurality of inductances **300**, **303** serially coupled and a third inductance **301** coupled at one end to the junction of inductances **300** and **303**. Coupled to the other end of inductance **301** is a capacitor **302**, and coupled across the serial combination of inductances **300** and **303** is a capacitor **304**. Other well known delay line sections could be substituted in place of this delay line section.

With reference to FIG. 5, a typical delay line pulse amplifier circuit is shown comprising PNP transistors **400** and **410**. This typical pulse amplifier circuit is utilized for rejuvenating the attenuated signal provided from the delay line circuits of FIG. 3. Other types of pulse amplifier circuits for producing this result are well known in the prior art.

Since many changes could be made in the above-described construction and many apparently widely different embodiments of the present invention could be made without departing from the scope thereof, it is maintained that all matter contained in the above description or shown in the accompanying drawings should be interpreted as illustrative and not in a limiting sense.

What is claimed is:

1. A converter for changing an analog signal representation to a digital logarithm representation having a predetermined base, comprising a comparator circuit to compare an analog signal with a generated comparison signal, a control circuit operating in response to said comparison signal, said control circuit providing a pluralty of sequential actuating signals, a register having a plurality of storage devices each representing a value of two to a different power and being responsive to said actuating signals for providing a plurality of selection signals, and an anti-logarithmic digital to analog converter responsive to said selection signals including a plurality of multiplier means for selectively multiplying a reference signal by a plurality of successive weighted constants to generate said comparison signal, each of said multiplier means being coupled to a different one of said storage devices for multiplying, in response thereto, by a weighted constant having a value of said base to a power equal to the value represented by the coupled storage device.

2. An anti-logarithmic digital to analog conversion device comprising means for storing a number represented by a binary digital word and in accordance with said binary word providing a plurality of selection signals, and means for multiplying a reference signal by a serially coupled plurality of multiplication factors in accordance with the magnitude of the number represented by said binary digital word comprising a plurality of means each including at least two multiplier means with one of said multiplier means operative to multiply said reference signal by a factor equal to a predetermined logarithm base to a power of two to a power and a second one of said multiplier means operative to multiply said reference signal by a factor of one, and a switching means responsive to one of said selection signals for selecting one of said at least two multiplier means.

3. A system for changing an analog signal representation to a digital logarithm representation having a predetermined base comprising means to receive an analog input signal, means for comparing said input signal with a comparison signal to generate an intermediate signal, a digital register responsive to said intermediate signal for storing a digital number and in response thereto producing a plurality of selection signals, and means responsive to said selection signals for selectively multiplying a reference signal and a plurality of serially coupled weighted constants to generate said comparison signal comprising a plurality of means each including at least two multiplier means with one of said multiplier means operative to multiply said reference signal by a factor equal to said base to a power of two to a power and a second one of said multiplier means operative to multiply said reference signal by a factor of one, and a switching means responsive to one of said selection signals for selecting one of said at least two multiplier means.

4. The invention according to claim **1** and wherein:
said register is operative to store a binary word having a plurality of digits with each digit being stored in a different storage device.

5. The invention according to claim **1** and wherein:
said register is operative to store a binary word having a plurality of digits with each digit being stored in a different storage device; and,
said control circuit includes a plurality of delay means serially connected.

6. The invention according to claim **2** and wherein:
said means for storing a number comprises a plurality of flip-flops, each operative in first and second states and producing a different selection signal in each state of operation.

7. The invention according to claim **3** and wherein:
said digital register comprises a plurality of flip-flops, each operative in first and second states and producing a different selection signal in each state of operation.

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