Title: GETTERING AGENTS IN MEMORY CHARGE STORAGE STRUCTURES

Abstract: Memory cells including a charge storage structure having a gettering agent therein can be useful for non-volatile memory devices. Providing for gettering of oxygen from a charge-storage material of the charge storage structure can facilitate a mitigation of detrimental oxidation of the charge-storage material.
GETTERING AGENTS IN MEMORY CHARGE STORAGE STRUCTURES

TECHNICAL FIELD OF THE INVENTION

[0001] The present disclosure relates generally to semiconductor memories and, in particular, in one or more embodiments, the present disclosure relates to memory cells for non-volatile memory devices, the memory cells with charge storage structures having gettering agents incorporated therein.

BACKGROUND OF THE INVENTION

[0002] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash memory.

[0003] Flash memory devices have developed into a popular source of non-volatile memory for a wide range of electronic applications. Flash memory devices typically use a one-transistor memory cell that allows for high memory densities, high reliability, and low power consumption. Changes in threshold voltage of the cells, through programming (which is sometimes referred to as writing) of charge storage structures (e.g., floating gates or charge traps) or other physical phenomena (e.g., phase change or polarization), determine the data value of each cell. Common uses for flash memory include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, cellular telephones, and removable memory modules.

[0004] A NAND flash memory device is a common type of flash memory device, so called for the logical form in which the basic memory cell configuration is arranged. Typically, the array of memory cells for NAND flash memory devices is arranged such that the control gate of each memory cell of a row of the array is connected together to form an access line, such as a word line. Columns of the array include strings (often termed NAND strings) of memory cells connected together in series, source to drain, between a pair of select lines, a source select line and a drain select line. A "column" refers to a group of memory cells that are commonly coupled to a local data line, such as a local bit line. It does not require any particular orientation or linear relationship, but instead refers to the logical
relationship between memory cell and data line. The source select line includes a source select gate at each intersection between a NAND string and the source select line, and the drain select line includes a drain select gate at each intersection between a NAND string and the drain select line. Each source select gate is connected to a source line, while each drain select gate is connected to a data line, such as column bit line.

[0005] As memory densities increase, issues with data retention, program saturation and trap-up tend to worsen. For example, while polysilicon (sometimes referred to as polycrystalline silicon) charge storage structures have been commonly used for years, they tend to become impracticable as their thickness becomes too thin, e.g., around 60Å (6nm) or less. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternative memory charge storage structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a simplified block diagram of a memory device coupled to a processor as part of an electronic system, according to an embodiment of the disclosure.

[0007] Figure 2 is a schematic of a portion of an example NAND memory array as might be found in the memory device of Figure 1.

[0008] Figures 3A-3E depict a portion of a memory array during various stages of fabrication in accordance with an embodiment of the disclosure.

[0009] Figures 4A-4B depict a portion of a memory cell during various stages of fabrication of a charge storage structure in accordance with an embodiment of the disclosure.

[0010] Figures 5A-5B shows conceptually concentration of metal across a charge-storage material in accordance with embodiments of the disclosure.

[0011] Figures 6A-6B depict a portion of a memory cell during various stages of fabrication of a charge storage structure in accordance with an embodiment of the disclosure.

[0012] Figures 7A-7B depict a portion of a memory cell during various stages of fabrication of a charge storage structure in accordance with an embodiment of the disclosure.
DETAILED DESCRIPTION

[0013] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments. In the drawings, like numerals describe substantially similar components throughout the several views. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present disclosure. The term semiconductor can refer to, for example, a layer of material, a wafer, or a substrate, and includes any base semiconductor structure. "Semiconductor" is to be understood as including silicon on sapphire (SOS) technology, silicon on insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a semiconductor in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure. The following detailed description is, therefore, not to be taken in a limiting sense.

[0014] Traditional floating gate NAND flash structures often use a thick polysilicon (sometimes referred to as polycrystalline silicon) floating gate which can have the control gate wrapped around it, allowing it to program and erase with a silicon dioxide intergate dielectric on the polysilicon. However, this geometry may soon be impracticable to sustain in smaller devices because there may not be enough room to wrap the intergate dielectric and control gate around the polysilicon floating gate. Using this same materials stack in a planar geometry is generally unsatisfactory and may even fail to program. To address this issue, an intergate dielectric using a high-k dielectric may be required. These high-k dielectrics are primarily oxides, and depositing these oxides on polysilicon can oxidize the polysilicon, reducing its ability to function as a charge storage structure.

[0015] Various embodiments include memory cells having a charge storage structure between a first dielectric, e.g., a tunnel dielectric, and a second dielectric, e.g., an intergate dielectric, and memory devices and systems including such memory cells. Memory cells of this type are often referred to as floating-gate memory cells or charge trap memory cells. Charge storage structures of various embodiments include a charge-storage material and a gettering agent. As used herein, a gettering agent is an element or compound that is expected, in the case of unreacted oxygen, to preferentially react with that oxygen over the
charge-storage material under the process conditions experienced by that charge-storage material; or that is expected, in the case of oxidized charge-storage material, to either pull the reacted oxygen away from the oxidized charge-storage material or to further react with the oxidized charge-storage material to produce a compound that is either conductive or is a dielectric compound having a higher k value than the oxidized charge-storage material. Some gettering agents may meet only one of these criteria, while others may meet more than one of these criteria. Such memory cells are useful in non-volatile memory devices.

[0016] Various embodiments use gettering agents to mitigate the oxidation risk of a charge-storage material of a charge storage structure. For example, metal doping and silicidation of a silicon-containing charge-storage material provides such gettering agents, e.g., metal silicides. For one or more embodiments, the metals incorporated into the charge-storage material thermodynamically react with SiO$_2$ to form either MSiO$_x$ (M = metal) or MO$_x$+Si. For example, the elements used to getter oxygen from silicon may do so because their reaction products will have a lower Gibbs Free Energy than SiO$_2$, and high temperatures supplied during gate stack anneals, e.g., often over 900°C, may overcome the kinetic barriers that would prevent these reactions from occurring. Examples of metals that are theoretically known to work are zirconium (Zr), beryllium (Be), and magnesium (Mg). Additional metals which are expected to work are calcium (Ca), strontium (Sr), scandium (Sc), yttrium (Y), the rare earth metals (e.g. lanthanum (La)), thorium (Th), uranium (U), hafnium (Hf), and aluminum (Al). Beyond these theoretically functional metals, there is experimental evidence in the literature that other metals, such as titanium (Ti), will thermodynamically remove oxygen from silicon.

[0017] Such metals doped into a thin polysilicon floating gate could enable integration of the thin polysilicon floating gate with other oxide based materials by acting as an in situ getter for oxygen that is exposed to the polysilicon. As the oxygen reaches the polysilicon, it may either be preferentially bound to the doping metal, or if it does react with silicon to form SiO$_2$, later, during integration and high temperature anneals, a metal element may diffuse to the SiO$_2$ site, and pull the oxygen away from the Si to form MO$_x$ (metal oxide) or MSiO$_x$ (metal silicon oxide).

[0018] Having the oxygen bound to the metal accrues multiple benefits. Continuing the example of a polysilicon floating gate, one benefit is that it helps to ensure there is enough silicon to function as a charge storage structure. If too much of the silicon is oxidized, then
the silicon may no longer function effectively as a floating gate. A second concern is that SiO$_2$ is a low-k dielectric which can add significant equivalent oxide thickness (EOT) to the gate stack. The voltage that is available to these gate stacks may be severely limited and this additional amount of EOT can cause additional amounts of voltage to be required to program and erase the charge storage structure and can make these devices unsuitable for memory products. Many of the described metals have oxides whose dielectric constants are high, e.g. HfO$_2$ has $k=20$ and TiO$_2$ has $k=80$. By converting the oxide from SiO$_2$, where $k=3.9$, to a high-k oxide, the EOT of the stack would be reduced.

[0019] One additional benefit of metal doping or silicidation of a polysilicon floating gate is that doping such thin polysilicon materials can be quite challenging. Additionally, even if such thin polysilicon materials were to be doped, the dopant species may diffuse out during thermal cycling. Metals described herein generally would not diffuse as easily and may still be available to ensure a sufficient number of electrons are available in the charge storage structure for proper program and erase functions.

[0020] Various embodiments incorporate into or on top of the charge-storage material a component that intrinsically scavenges oxygen while prior strategies relied on a barrier layer to prevent the charge-storage material from being exposed to an oxidant. The problem with such prior solutions is that layers of typical gate stacks will oxidize to some degree and such layers are generally permeable to oxygen at some level, increasing the risk that the charge-storage material will eventually become oxidized from available oxygen within the gate stack, thus degrading the cell stack EOT and degrading the electrical properties of the charge-storage material itself. By accepting the likely inevitability of oxygen reaching the charge-storage material, and by incorporating an element in the charge-storage material that will react with the oxygen and remove or inhibit the formation of undesirable oxidation products in situ, e.g., SiO$_2$, from a silicon-containing charge-storage material, improvements over prior solutions may be facilitated.

[0021] Figure 1 is a simplified block diagram of a memory device 100, as one example of an integrated circuit device, in communication with (e.g., coupled to) a processor 130 as part of an electronic system, according to an embodiment of the disclosure. Some examples of electronic systems include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, digital recorders, games, appliances, vehicles, wireless devices, cellular telephones and the like. The processor 130 may be, for example, a memory
controller or other external processor for use in the control and access of the memory device 100.

[0022] Memory device 100 includes an array of memory cells 104 logically arranged in rows and columns. At least one memory cell of the array of memory cells 104 includes a charge storage structure in accordance with an embodiment of the disclosure. Although various embodiments will be described primarily with reference to NAND memory arrays, the various embodiments are not limited to a specific architecture of the memory array 104. Some examples of other array architectures suitable for the present embodiments include NOR arrays, AND arrays or other arrays.

[0023] A row decode circuitry 108 and a column decode circuitry 110 are provided to decode address signals. Address signals are received and decoded to access memory array 104. Memory device 100 also includes input/output (I/O) control circuitry 112 to manage input of commands, addresses and data to the memory device 100 as well as output of data and status information from the memory device 100. An address register 114 is coupled between I/O control circuitry 112 and row decode circuitry 108 and column decode circuitry 110 to latch the address signals prior to decoding. A command register 124 is coupled between I/O control circuitry 112 and control logic 116 to latch incoming commands. Control logic 116 controls access to the memory array 104 in response to the commands and generates status information for the external processor 130. The control logic 116 is coupled to row decode circuitry 108 and column decode circuitry 110 to control the row decode circuitry 108 and column decode circuitry 110 in response to the addresses.

[0024] Control logic 116 is also coupled to a cache register 118. Cache register 118 latches data, either incoming or outgoing, as directed by control logic 116 to temporarily store data while the memory array 104 is busy writing or reading, respectively, other data. During a write operation, data is passed from the cache register 118 to data register 120 for transfer to the memory array 104; then new data is latched in the cache register 118 from the I/O control circuitry 112. During a read operation, data is passed from the cache register 118 to the I/O control circuitry 112 for output to the external processor 130; then new data is passed from the data register 120 to the cache register 118. A status register 122 is coupled between I/O control circuitry 112 and control logic 116 to latch the status information for output to the processor 130.
Memory device 100 receives control signals at control logic 116 from processor 130 over a control link 132. The control signals may include a chip enable CE#, a command latch enable CLE, an address latch enable ALE, and a write enable WE#. Memory device 100 receives command signals (which represent commands), address signals (which represent addresses), and data signals (which represent data) from processor 130 over a multiplexed input/output (I/O) bus 134 and outputs data to processor 130 over I/O bus 134.

Specifically, the commands are received over input/output (I/O) pins [7:0] of I/O bus 134 at I/O control circuitry 112 and are written into command register 124. The addresses are received over input/output (I/O) pins [7:0] of bus 134 at I/O control circuitry 112 and are written into address register 114. The data are received over input/output (I/O) pins [7:0] for an 8-bit device or input/output (I/O) pins [15:0] for a 16-bit device at I/O control circuitry 112 and are written into cache register 118. The data are subsequently written into data register 120 for programming memory array 104. For another embodiment, cache register 118 may be omitted, and the data are written directly into data register 120. Data are also output over input/output (I/O) pins [7:0] for an 8-bit device or input/output (I/O) pins [15:0] for a 16-bit device.

It will be appreciated by those skilled in the art that additional circuitry and signals can be provided, and that the memory device of Figure 1 has been simplified. It should be recognized that the functionality of the various block components described with reference to Figure 1 may not necessarily be segregated to distinct components or component portions of an integrated circuit device. For example, a single component or component portion of an integrated circuit device could be adapted to perform the functionality of more than one block component of Figure 1. Alternatively, one or more components or component portions of an integrated circuit device could be combined to perform the functionality of a single block component of Figure 1.

Additionally, while specific I/O pins are described in accordance with popular conventions for receipt and output of the various signals, it is noted that other combinations or numbers of I/O pins may be used in the various embodiments.

Figure 2 is a schematic of a NAND memory array 200, e.g., as a portion of memory array 104. Memory array 200 may be formed in a common conductively doped region (e.g., a common p-well) formed in a semiconductor.
As shown in Figure 2, the memory array 200 includes access lines, commonly referred to as word lines (which may comprise commonly coupled control gates 2021 to 202N) and intersecting data lines, such as bit lines 2041 to 204M. For ease of addressing in the digital environment, the number of word lines 202 and the number of bit lines 204 are generally each some power of two.

Memory array 200 includes NAND strings 2061 to 206M. Each NAND string includes transistors 2081 to 208N, each located at an intersection of a word line 202 and a bit line 204. The transistors 208, depicted as floating-gate transistors in Figure 2, represent non-volatile memory cells for storage of data. At least one transistor 208 has a gate stack having a charge storage structure in accordance with an embodiment of the disclosure. The floating-gate transistors 208 of each NAND string 206 are connected in series source to drain between one or more source select gates 210, e.g., a field-effect transistor (FET), and one or more drain select gates 212, e.g., an FET. Each source select gate 210 is located at an intersection of a local bit line 204 and a source select line 214, while each drain select gate 212 is located at an intersection of a local bit line 204 and a drain select line 215.

A source of each source select gate 210 is connected to a common source line 216. The drain of each source select gate 210 is connected to the source of the first floating-gate transistor 208 of the corresponding NAND string 206. For example, the drain of source select gate 2101 is connected to the source of floating-gate transistor 2081 of the corresponding NAND string 2061. A control gate of each source select gate 210 is connected to source select line 214. If multiple source select gates 210 are utilized for a given NAND string 206, they would be coupled in series between the common source line 216 and the first floating-gate transistor 208 of that NAND string 206.

The drain of each drain select gate 212 is connected to a local bit line 204 for the corresponding NAND string at a drain contact. For example, the drain of drain select gate 2121 is connected to the local bit line 2041 for the corresponding NAND string 2061 at a drain contact. The source of each drain select gate 212 is connected to the drain of the last floating-gate transistor 208 of the corresponding NAND string 206. For example, the source of drain select gate 2121 is connected to the drain of floating-gate transistor 208N of the corresponding NAND string 2061. If multiple drain select gates 212 are utilized for a given NAND string 206, they would be coupled in series between the corresponding bit line 204 and the last floating-gate transistor 208N of that NAND string 206.
Typical construction of floating-gate transistors 208 includes a source 230 and a drain 232, a floating gate 234 as a charge storage structure, and a control gate 236, as shown in Figure 2. Floating-gate transistors 208 have their control gates 236 coupled to a word line 202 (e.g., the control gates may be commonly coupled to form a word line). A column of the floating-gate transistors 208 are those NAND strings 206 coupled to a given local bit line 204. A row of the floating-gate transistors 208 are those transistors commonly coupled to a given word line 202.

Figures 3A-3E depict a portion of a memory array during various stages of fabrication. Figure 3A depicts a portion of a memory array after several processing steps have occurred. In general, Figure 3A may depict a semiconductor 305 upon which portions of future gate stacks of non-volatile memory cells are formed. For one embodiment, the semiconductor 305 is a monocrystalline silicon. For a further embodiment, semiconductor 305 is a conductively-doped monocrystalline silicon. Other embodiments may include amorphous silicon, polysilicon or other semiconductor materials. Semiconductor 305 may be conductively doped to a first conductivity type, e.g., a p-type conductivity.

As further depicted in Figure 3A, a tunnel dielectric 310, a charge storage structure 315 having one or more gettering agents in accordance with an embodiment of the disclosure, an intergate dielectric 320, a control gate 325 and a dielectric cap 330 have been formed on the semiconductor 305. These elements will form the gate stacks of future memory cells.

Formation of the structure of Figure 3A can include formation of the tunnel dielectric 310 over an active region of the semiconductor 305, e.g., an area over which memory cells will be formed. For example, the active region of the semiconductor 305 may include a conductively-doped well of a semiconductor wafer. The tunnel dielectric 310 is generally one or more dielectric materials. The tunnel dielectric 310 might be formed, for example, by thermal oxidation of the semiconductor 305. Alternatively, the tunnel dielectric 310 could be formed by a blanket deposition of a dielectric material, such as by chemical vapor deposition (CVD), physical vapor deposition (PVD) or atomic layer deposition (ALD). Example dielectric materials for tunnel dielectric 310 include silicon oxides (SiOx), silicon nitride (SiNx), silicon oxynitrides (SiOxNy), aluminum oxides (AlOx), hafnium oxides (HfOx), hafnium aluminum oxides (HfAlOx), lanthanum oxides (LaOx), tantalum oxides...
(TaOx), zirconium oxides (ZrOx), zirconium aluminum oxides (ZrAlOx), etc., and combinations thereof.

[0038] The charge storage structure 315 is then formed over the tunnel dielectric 310. Formation of the charge storage structure 315 will be described in more detail with reference to Figures 4A-7B. The charge storage structure 315 can be used to store a charge indicative of a data state of the future memory cells. The charge storage structure 315 is a semiconductive to a conductive structure.

[0039] The intergate dielectric 320 is then formed over the charge storage structure 315. The intergate dielectric 320 is generally one or more dielectric materials. For example, the intergate dielectric 320 may include one or more layers of dielectric materials including high K dielectric materials. Example high-k dielectric materials for intergate dielectric 320 include aluminum oxides (AlOx), hafnium oxides (HfOx), hafnium aluminum oxides (HfAlOx), hafnium silicon oxides (HfSiOx), lanthanum oxides (LaOx), tantalum oxides (TaOx), zirconium oxides (ZrOx), zirconium aluminum oxides (ZrAlOx), yttrium oxide (Y2O3), etc. For one embodiment, the intergate dielectric 320 includes an ozone-based formation of hafnium silicon oxide followed by water-based formation of hafnium oxide. For a further embodiment, the intergate dielectric 320 includes a high-k dielectric material over silicon nitride.

[0040] The control gate 325 is formed over the intergate dielectric 320. In general, the control gate 325 includes one or more conductive materials. For one embodiment, the control gate 325 contains a conductively-doped polysilicon. For another embodiment, the control gate 325 contains a metal-containing material. For a further embodiment, the control gate 325 includes a metal-containing material over polysilicon, e.g., a refractory metal silicide formed on a conductively-doped polysilicon. The metals of chromium (Cr), cobalt (Co), hafnium (Hf), molybdenum (Mo), niobium (Nb), tantalum (Ta), titanium (Ti), tungsten (W), vanadium (V), zirconium (Zr), and metal nitrides (including, for example, titanium nitride, tantalum nitride, tantalum carbon nitride, tungsten nitride) for metal gates are generally recognized as refractory metal materials. For another embodiment, the control gate 325 contains multiple metal-containing materials, e.g., a titanium nitride (TiN) barrier over the intergate dielectric 320, titanium (Ti) as an adhesion material over the barrier, and tungsten (W) over the adhesion material.
[0041] The dielectric cap 330 can be formed over the control-gate 325 to act as an insulator and barrier layer to protect the control gate 325 during subsequent processing. The dielectric cap 330 contains one or more dielectric materials and may include, for example, such dielectrics as silicon oxides (SiOx), silicon nitride (SiNx), and silicon oxynitrides (SiOxNy). For one embodiment, the dielectric cap 330 is a silicon nitride, formed, for example, by such methods as CVD. It is noted that additional layers may be used to form the gate stack, such as barrier materials to inhibit diffusion between opposing materials or adhesion materials to promote adhesion between opposing materials.

[0042] In Figure 3B, a mask 335 is formed and patterned over the dielectric cap 330. As one example, a photolithographic resist material could be deposited overlying the dielectric cap 330, exposed to a radiation source, such as UV light, and developed to define areas overlying the dielectric cap 330 for removal.

[0043] Following this patterning of the mask 335, exposed portions of the dielectric cap 330 and underlying portions are removed in Figure 3C, such as by etching or other removal process, to expose the semiconductor 305. More than one removal process may be used where the chosen removal process is ineffective at removing an underlying material. Following removal, one or more gate stacks 337 for word lines are defined. Although Figures 3A-3E depict only memory cells, the select gates (not shown in Figures 3A-3E) may be formed of the same gate stacks 337.

[0044] In Figure 3D, source/drain regions 340 are formed generally adjacent the tunnel dielectric 310, such as by conductive doping of portions of the semiconductor 305 exposed in Figure 3C. A channel region of a memory cell is defined by the area of the semiconductor 305 between the source/drain regions 340. Source/drain regions 340 will generally have a conductivity type different than the conductivity type of the semiconductor 305. The conductivity types may be opposites. For example, for a p-type semiconductor 305, the source/drain regions 340 might have an n+-type conductivity.

[0045] In Figure 3E, dielectric spacers 345 may also be formed. As one example, a blanket deposit of some dielectric material, e.g., silicon nitride, is formed overlying the gate stacks 337, followed by an anisotropic removal of the blanket deposit to form the dielectric spacers 345. The resulting structure depicted in Figure 3E includes series-coupled memory cells, such as those of a NAND string. However, it will be readily apparent that memory cells may be formed for an alternate array architecture using the gate stacks 337.
Figures 4A-4B depict a portion of a memory cell during various stages of fabrication of a charge storage structure 315 in accordance with an embodiment of the disclosure. In Figure 4A, a charge-storage material 450 is formed over the tunnel dielectric 310 overlying the semiconductor 305. The charge-storage material 450 generally contains one or more materials capable of storing a charge. For at least some embodiments, the charge-storage material includes a silicon-containing material. Examples of silicon-containing charge-storage material include polysilicon, amorphous silicon and monocrystalline silicon. The charge-storage material 450 may be an undoped or conductively doped silicon-containing material. For example, the charge-storage material 450 might be a polysilicon material having a p-type conductivity. Conductively doping semiconductor materials, such as monocrystalline silicon, amorphous silicon and polysilicon, may be performed subsequent to formation or concurrent with formation.

For one embodiment, the charge-storage material 450 has a thickness of approximately 10 Å to 100 Å (1nm to 10nm). For a further embodiment, the charge-storage material 450 has a thickness of approximately 30 Å to 50 Å (3nm to 5nm). It is recognized that the variability of industrial fabrication will inherently produce minor variations in thickness such that a process seeking a particular thickness, e.g., 30 Å (3nm), will likely produce thicknesses cell-to-cell that are above and below that particular value.

In Figure 4B, one or more gettering agents, as represented by arrows 455, are incorporated into the charge-storage material 450 of the resulting charge storage structure 315. Various embodiments described herein will use the example of metals as the gettering agents 455 as certain of these are expected to be gettering agents for commonly used polysilicon floating gates. However, for charge-storage materials 450 other than silicon-containing materials, it will be understood that other elements or compounds may meet the gettering agent criteria described above. The metals 455 may be incorporated, for example, by ionic implantation, plasma, sputtering or other physical deposition process. Alternatively, the metals 455 may be incorporated into the charge-storage material 450 during formation of the charge-storage material 450, such as by chemical vapor deposition (CVD). Concentration of the metals may range, for example, from 1E19/cm³ to stoichiometric levels and above, and the metal concentration may be greater than 50 atomic percent (at%). Following incorporation of the metals 455, the device may be annealed to cause at least a portion of the metals 455 to react with the charge-storage material 450 to form the charge storage structure.
315. For certain embodiments, the charge storage structure 315 consists essentially of silicon and one or more of a metal silicon oxide, a metal silicide, a metal oxide and a metal. For certain additional embodiments, the charge storage structure 315 consists essentially of a metal silicon oxide and one or more of a metal silicide, a metal oxide and a metal. For certain further embodiments, the charge storage structure 315 consists essentially of a metal silicide and one or more of a metal silicon oxide, a metal oxide and a metal. The anneal for various embodiments may be performed prior to the formation of a subsequent intergate dielectric 320, as a part of the processing for formation of the subsequent intergate dielectric 320, or after processing for formation of the subsequent intergate dielectric 320. At concentrations of metals 455 above the stoichiometric levels, layers or pockets of unreacted metals 455 may occur within the charge storage structure 315.

[0049] The concentration of the metals 455 may be a gradient across the charge-storage material 450, or it may be uniform across the charge-storage material 450. Figures 5A-5B show conceptually concentration of metal across a charge-storage material 450 from point A, corresponding to an interface between the charge-storage material 450 and the dielectric 310, to a point B, corresponding to an interface between the charge-storage material 450 and the intergate dielectric 320. For various embodiments, the concentration of metals 455 is higher nearer point B. It is expected that oxidation risk is greater nearer this interface, and higher concentrations of metals 455 may be desirable nearer point B. The concentration of metals 455 may be a gradient, such as depicted in Figure 5A. The gradient may be uniform as depicted by line 572, it may have a higher slope nearer point A than point B as depicted by line 574, it may have a higher slope nearer point B than point A as depicted by line 576, or it may be stepped as depicted by line 578. Alternatively, the concentration may be substantially uniform (e.g., uniform) from point A to point B as depicted by line 580. Other concentration curves will be apparent, such as concentrations curves having a lower concentration of metals 455 nearer point B, and the embodiments are not limited to a particular concentration curve.

[0050] For certain embodiments, at least some of the charge-storage material 450 is formed to be substantially devoid (e.g., devoid) of metals 455. For example, polysilicon may be devoid of metals as formed. Figures 6A-6B depict a portion of a memory cell during various stages of fabrication of a charge storage structure 315 in accordance with an embodiment of the disclosure. In Figure 6A, a charge-storage material 450 is formed over the tunnel dielectric 310 overlying the semiconductor 305. In Figure 6B, metals 455 are
incorporated into only a portion 460 of the charge-storage material 450. For example, in ionic implantation, plasma deposition or other physical deposition processes, implantation depth can generally be controlled by varying the amount of power applied. Alternatively, in a CVD process, during a first portion of formation, precursors for only the charge-storage material 450 could be supplied to the reaction until a particular thickness had been formed, then the reaction could continue by concurrently supplying precursors for the metals 455 with precursors for the charge-storage material 450. Alternatively, a barrier could be formed after forming the portion of charge-storage material 450 devoid of metals 455 and before forming the portion 460 of charge-storage material 450 having metals 455 incorporated therein. As with the embodiment of Figures 4A-4B, an anneal could be performed to react at least a portion of the metals 455 with the charge-storage material 450 of portion 460. For certain embodiments, the portion 460 consists essentially of silicon and one or more of a metal silicon oxide, a metal silicide, a metal oxide and a metal. For certain other embodiments, the portion 460 consists essentially of one or more of a metal silicon oxide, a metal silicide, and a metal. For additional embodiments, reaction products of portion 460 separate the remaining portion of charge-storage material 450 from the intergate dielectric 320. Formation of a memory cell using the charge storage structure 315 of Figure 6B can proceed as described with reference to Figures 3A-3E.

[0051] Figures 7A-7B depict a portion of a memory cell during various stages of fabrication of a charge-storage structure 315 in accordance with an embodiment of the disclosure. The example of Figures 7A-7B show how metals 455 could be incorporated into the charge-storage material 450 in a sequential process. In Figure 7A, a first charge-storage material 450i is formed over the tunnel dielectric 310 overlying the semiconductor 305 and a first metal 455i is formed over the first charge-storage material 450i. Subsequently, a second charge-storage material 4502 is formed over the first metal 455i and a second metal 4552 is formed over the second charge-storage material 4502. Subsequently, a third charge-storage material 4503 is formed over the second metal 4552 and a third metal 4553 is formed over the third charge-storage material 4503. Fewer or additional layers may be formed in this manner.

[0052] In the example depicted in Figure 7A, each successive formation of charge-storage material 450 is thinner, while each successive formation of metals 455 is thicker. Upon reacting at least a portion of the metals 455 with the charge-storage material 450 in this example, a gradient having a higher concentration nearer the top, i.e., nearer the intergate
dielectric 320, will result, such as depicted in Figure 7B. It is noted that similar results could be obtained by forming various layers of charge-storage material 450 having uniform thickness while increasing the thickness of subsequent layers of metals 455, or by forming various layers of metals 455 having uniform thickness while decreasing the thickness of subsequent layers of charge-storage material 450. If the ratio of metals 455 to charge-storage materials 450 is greater than a stoichiometric amount, layers of unreacted metals 455 may occur. Similarly, if the ratio of metals 455 to charge-storage materials 450 is less than a stoichiometric amount, layers of unreacted charge-storage material 450 may occur. For some embodiments, reaction products of the metals 455 separate any remaining charge-storage material 450 from the intergate dielectric 320, i.e., no portion of charge-storage material 450 is in contact with intergate dielectric 320. Formation of a memory cell using the charge storage structure 315 of Figure 7B can proceed as described with reference to Figures 3A-3E. It will be apparent that the process depicted in Figure 7A could be used to form portion 460 of the embodiment depicted in Figure 6B.

Conclusion

[0053] Memory cells including a charge storage structure having one or more gettering agents can be useful in non-volatile memory devices. Various embodiments provide for gettering of oxygen from a charge-storage material of the charge storage structure to facilitate a mitigation of detrimental oxidation of the charge-storage material.

[0054] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the embodiments will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the embodiments.
What is claimed is:

1. A memory cell, comprising:
   a first dielectric over a semiconductor;
   a charge storage structure over the first dielectric;
   a second dielectric over the charge storage structure;
   a control gate over the second dielectric; and
   source/drain regions in the semiconductor generally adjacent the first dielectric;
   wherein the charge storage structure comprises a charge-storage material and a gettering agent.

2. The memory cell of claim 1, wherein the charge-storage material is a silicon-containing material.

3. The memory cell of claim 2, wherein the silicon-containing material is selected from the group consisting of amorphous silicon, monocrystalline silicon and polycrystalline silicon.

4. The memory cell of claim 1, wherein the gettering agent comprises a plurality of gettering agents.

5. The memory cell of claim 1, wherein the gettering agent comprises an oxygen gettering agent.

6. The memory cell of claim 1, wherein the gettering agent comprises an element or compound meeting at least one criteria, under process conditions experienced by the charge-storage material, selected from the group consisting of preferentially reacting with unreacted oxygen over the charge-storage material, pulling reacted oxygen away from an oxidized charge-storage material, further reacting with oxidized charge-storage material to produce a compound that is conductive, and further reacting with oxidized charge-storage material to produce a dielectric compound that has a higher k value than the oxidized charge-storage material.
7. The memory cell of claim 1, wherein the gettering agent comprises a metal.

8. The memory cell of claim 7, wherein the metal is selected from the group consisting of zirconium, beryllium and magnesium.

9. The memory cell of claim 7, wherein the metal is selected from the group consisting of zirconium, beryllium, magnesium, calcium, strontium, scandium, yttrium, rare earth metals, lanthanum, thorium, uranium, hafnium and aluminum.

10. The memory cell of claim 7, wherein the metal is selected from the group consisting of zirconium, beryllium, magnesium, calcium, strontium, scandium, yttrium, rare earth metals, lanthanum, thorium, uranium, hafnium, aluminum and titanium.

11. The memory cell of claim 7, wherein the gettering agent comprises a silicide of the metal.

12. The memory cell of claim 1, wherein a concentration of the metal is greater than a stoichiometric amount in at least a portion of the charge-storage material.

13. The memory cell of claim 1, wherein at least a portion of the gettering agent is incorporated into the charge-storage material.

14. The memory cell of claim 13, wherein the gettering agent is incorporated into only a portion of the charge-storage material.

15. The memory cell of claim 1, wherein the gettering agent is on the charge-storage material and separates the charge-storage material from the second dielectric.

16. The memory cell of claim 1, wherein a concentration of the gettering agent is greater nearer the second dielectric than a concentration of the gettering agent nearer the first dielectric.
17. The memory cell of claim 1, wherein the charge-storage material is devoid of the gettering agent in a portion nearer the first dielectric.

18. The memory cell of claim 1, wherein the charge storage structure comprises a silicon-containing material and a metal.

19. The memory cell of claim 18, wherein the charge storage structure comprises a silicon-containing material and one or more metals.

20. The memory cell of claim 19, wherein a concentration of the one or more metals is greater than or equal to $1 \times 10^{19}/\text{cm}^3$.

21. The memory cell of claim 20, wherein the concentration is greater than 50 atomic percent.

22. The memory cell of claim 20, wherein the concentration is greater than a stoichiometric amount.

23. The memory cell of claim 1, wherein the charge storage structure comprises polysilicon and a metal silicide.

24. The memory cell of claim 23, wherein the charge storage structure further comprises an elemental metal incorporated therein.

25. The memory cell of claim 23, wherein at least a portion of the metal silicide is incorporated into the polysilicon.

26. The memory cell of claim 23, wherein the metal silicide separates the polysilicon from the second dielectric.

27. The memory cell of claim 1, wherein the charge storage structure consists essentially of a silicon-containing material and at least one component selected from the group consisting of a metal silicon oxide, a metal silicide, a metal oxide and a metal.
28. The memory cell of claim 27, wherein the at least one component separates the silicon-containing material from the second dielectric.

29. The memory cell of claim 27, wherein at least a portion of the at least one component is incorporated into the silicon-containing material.

30. The memory cell of claim 1, wherein the charge storage structure consists essentially of a metal silicon oxide and at least one component selected from the group consisting of a metal silicide, a metal oxide and a metal.

31. The memory cell of claim 1, wherein the charge storage structure consists essentially of a metal silicide and at least one component selected from the group consisting of a metal silicon oxide, a metal oxide and a metal.

32. A method of forming a memory cell, comprising:
   forming a first dielectric over a semiconductor;
   forming a charge storage structure over the first dielectric;
   forming a second dielectric over the charge storage structure;
   forming a control gate over the second dielectric; and
   forming source/drain regions in the semiconductor generally adjacent the first dielectric;
wherein forming the charge storage structure comprises:
   forming a charge-storage material; and
   incorporating a gettering agent into the charge storage structure.

33. The method of claim 32, wherein incorporating a gettering agent into the charge storage structure comprises incorporating the gettering agents using a process selected from the group consisting of ionic implantation, sputtering, plasma, and chemical vapor deposition.

34. The method of claim 32, wherein the gettering agent comprises an oxygen gettering agent.
35. The method of claim 32, wherein the gettering agent is incorporated at more than a stoichiometric amount.

36. The method of claim 32, wherein forming a charge storage structure comprises forming a charge storage structure that has a conductivity selected from the group consisting of semiconductive and conductive.

37. The method of claim 32, wherein incorporating a gettering agent into the charge storage structure comprises incorporating the gettering agent into the charge-storage material.

38. The method of claim 37, wherein incorporating the gettering agent into the charge-storage material comprises incorporating the gettering agent into only a portion of the charge-storage material.

39. The method of claim 32, wherein incorporating a gettering agent into the charge storage structure comprises forming the gettering agent on top of the charge-storage material.

40. The method of claim 32, further comprising:
   wherein forming a charge-storage material comprises forming a silicon-containing material over the first dielectric; and
   wherein incorporating a gettering agent into the charge storage structure comprises incorporating a metal into the silicon-containing material and annealing to react at least a portion of the metal with the silicon-containing material, thereby defining the charge storage structure.

41. The method of claim 40, wherein incorporating a metal into the silicon-containing material comprises incorporating a sufficient amount of the metal such that unreacted metal remains in the charge storage structure after annealing to react the at least a portion of the metal with the silicon-containing material.
42. The method of claim 40, wherein annealing to react at least a portion of the metal with the silicon-containing material comprises forming at least one compound selected from the group consisting of a metal silicon oxide, a metal silicide and a metal oxide.

43. The method of claim 40, wherein the silicon-containing material contains a silicon oxide and further comprising reacting the at least a portion of the metal with the silicon-containing material to convert at least a portion of the silicon oxide to a metal silicon oxide, or silicon and a metal oxide.

44. The method of claim 40, wherein the silicon-containing material contains a silicon oxide and further comprising reacting the at least a portion of the metal with the silicon-containing material to convert at least a portion of the silicon oxide to a compound that is either conductive or has a dielectric constant greater than a dielectric constant of silicon dioxide.

45. The method of claim 40, further comprising:
preferentially reacting oxygen with at least a further portion of the metal over the silicon-containing material.

46. The method of claim 32, further comprising:
wherein forming a charge-storage material comprises forming an instance of charge-storage material over the first dielectric; and
wherein incorporating a gettering agent into the charge storage structure comprises:
forming an instance of metal, wherein the instance of metal is formed over the instance of charge-storage material, reacting the instance of charge-storage material with at least a portion of the instance of metal, thereby defining a charge storage structure.

47. The method of claim 46, wherein reacting the instance of charge-storage material with the at least a portion of the instance of metal occurs during or after forming the second dielectric.
48. The method of claim 46, wherein forming an instance of charge-storage material over the first dielectric comprises forming one or more instances of charge-storage material over the first dielectric, wherein forming an instance of metal comprises forming one or more instances of metal, and wherein each instance of metal is formed over one of the one or more instances of charge-storage material.
FIG. 3C

FIG. 3D
FIG. 3E