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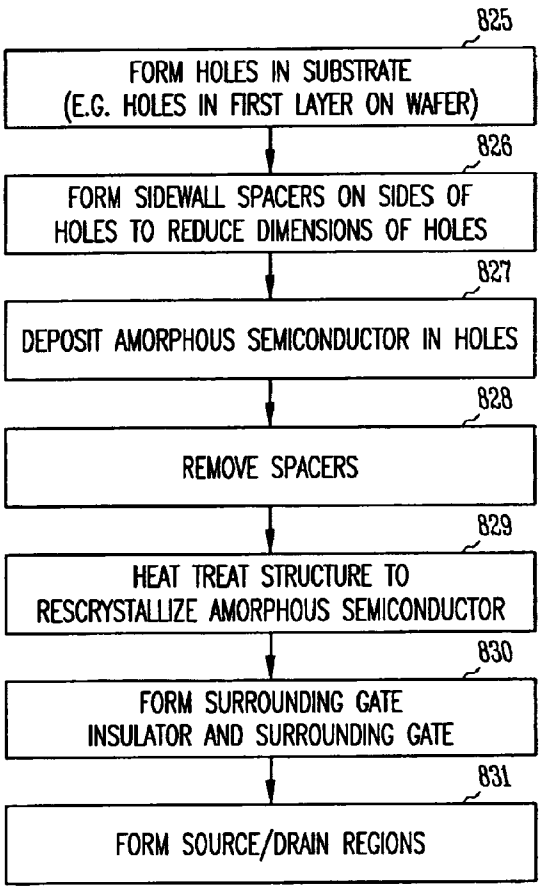
(54) Title: NANOWIRE TRANSISTOR WITH SURROUNDING GATE



(57) Abstract: One aspect of the present subject matter relates to a method for forming a transistor. According to an embodiment of the method, a pillar of amorphous semiconductor material is formed on a crystalline substrate, and a solid phase epitaxy process is performed to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth. The pillar has a sublithographic thickness. A transistor body is formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region. A surrounding gate insulator is formed around the semiconductor pillar, and a surrounding gate is formed around and separated from the semiconductor pillar by the surrounding gate insulator. Other aspects are provided herein.

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NANOWIRE TRANSISTOR WITH SURROUNDING GATE

Cross Reference To Related Applications

Benefit of priority is hereby claimed to "Grown Nanofin Transistors," U.S. Application Serial No. 11/397,430, filed on April 4, 2006; "Etched Nanofin Transistors," U.S. Application Serial No. 11/397,358, filed on April 4, 2006; "DRAM With Nanofin Transistors," U.S. Application Serial No. 11/397,413, filed on April 4, 2006; and "Tunneling Transistor With Sublithographic Channel," U.S. Application Serial No. 11/397,406, filed April 4, 2006, which applications are herein incorporated by reference.

Technical Field

This disclosure relates generally to semiconductor devices, and more particularly, to nanowire transistors that have a surrounding gate.

Background

The semiconductor industry has a market driven need to reduce the size of devices, such as transistors, and increase the device density on a substrate. Some product goals include lower power consumption, higher performance, and smaller sizes. FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k. The continuous scaling of MOSFET technology to the deep sub-micron region where channel lengths are less than 0.1 micron (100 nm or 1000 Å) causes significant problems in the conventional transistor structures. For example, junction depths should be much less than the channel length. Thus, with reference to the transistor 100 illustrated in FIG. 1, the junctions depths 101 should be on the order of a few hundred Angstroms for channels lengths 102 that are approximately 1000 Å long. Such shallow junctions are difficult to form by conventional implantation and diffusion techniques. Extremely high levels of channel doping are required to suppress short-channel effects such as drain induced barrier lowering, threshold

voltage roll off, and sub-threshold conduction. Sub-threshold conduction is particularly problematic in DRAM technology as it reduces the charge storage retention time on the capacitor cells. These extremely high doping levels result in increased leakage and reduced carrier mobility. Thus, the expected improved performance attributed to a shorter channel is negated by the lower carrier mobility and higher leakage attributed to the higher doping.

Leakage current is a significant issue in low voltage and lower power battery-operated CMOS circuits and systems, and particularly in DRAM circuits. The threshold voltage magnitudes are small to achieve significant overdrive and reasonable switching speeds. However, as illustrated in FIG. 2, the small threshold results in a relatively large sub-threshold leakage current.

Some proposed designs to address this problem use transistors with ultra-thin bodies, or transistors where the surface space charge region scales as other transistor dimensions scale down. Dual-gated or double-gated transistor structures also have been proposed to scale down transistors. As commonly used in the industry, "dual-gate" refers to a transistor with a front gate and a back gate which can be driven with separate and independent voltages, and "double-gated" refers to structures where both gates are driven when the same potential. An example of a double-gated device structure is the FinFET. "TriGate" structures and surrounding gate structures have also been proposed. In the "TriGate" structure, the gate is on three sides of the channel. In the surrounding gate structure, the gate surrounds or encircles the transistor channel. The surrounding gate structure provides desirable control over the transistor channel, but the structure has been difficult to realize in practice.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, and front and back gates separated from a semiconductor body by gate insulators, and also illustrates an electric field generated by the drain. Some characteristics of the dual-gated and/or double-gated MOSFET are better than the conventional bulk silicon MOSFETs, because compared to a single gate the two gates better screen the electric field generated by the drain electrode from the source-end of the

channel. The surrounding gate further screens the electric field generated by the drain electrode from the source. Thus, sub-threshold leakage current characteristics are improved, because the sub-threshold current is reduced more quickly as the gate voltage is reduced when the dual-gate and/or double gate MOSFET turns off. FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, or surrounding gate MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

Advances have been made in the growth of II-V compound semiconductor nanowires and in the fabrication of III-V compound semiconductor nanowire transistors. The growth of the II-V compound semiconductor transistors is achieved by vapor-liquid-solid (VLS) epitaxial growth of vertical nanowires on gold dots. Silicon nanowire transistors have been previously described by vapor phase epitaxial growth through a hole or by solid phase epitaxial growth over a polysilicon DRAM capacitor plate to make a polycrystalline nanowire transistor.

Summary

An embodiment of the present subject matter provides nanowire transistors from amorphous semiconductor nanorods that are recrystallized on the surface of a semiconductor wafer. The silicon nanorods are formed with dimensions smaller than lithographic dimensions by a sidewall spacer technique. The recrystallization of the amorphous nanorods uses solid phase epitaxial growth. The resulting nanowires can be used as the body regions of transistors where both the thickness of the body of the transistor and channel length have dimensions smaller than lithographic dimensions. The nanowire transistors have a wraparound gate. Various nanowire transistor embodiments use silicon nanowires.

One aspect of the present subject matter relates to a method for forming a transistor. According to an embodiment of the method, a pillar of amorphous

semiconductor material is formed on a crystalline substrate, and a solid phase epitaxy process is performed to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth. The pillar has a sublithographic thickness. A transistor body is formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region. A surrounding gate insulator is formed around the semiconductor pillar, and a surrounding gate is formed around and separated from the semiconductor pillar by the surrounding gate insulator.

An aspect relates to a transistor. A transistor embodiment includes a crystalline substrate, a first source/drain region formed in the crystalline substrate, and a crystalline semiconductor pillar formed on the substrate in contact with the first source/drain region. The transistor includes a second source/drain region formed in a top portion of the pillar, a gate insulator formed around the pillar, and a surrounding gate formed around and separated from the pillar by the gate insulator. The pillar has cross-section dimensions less than a minimum feature size.

These and other aspects, embodiments, advantages, and features will become apparent from the following description of the present subject matter and the referenced drawings.

Brief Description of the Drawings

FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k.

FIG. 2 illustrates sub-threshold leakage in a conventional silicon MOSFET.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, front and back gates separated from a semiconductor body by gate insulators, and an electric field generated by the drain.

FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, or surrounding gate MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

FIGS. 5A-5H illustrate an embodiment of a process to form crystalline nanorods with surrounding gates.

FIGS. 6A-6C illustrate an embodiment of a process to form isolated transistors with source, drain and gate contacts, using the nanorods with wraparound gates illustrated in FIGS. 5A-5H.

FIGS. 7A-7C illustrate an embodiment of a process to form an array of transistors, using the nanorods with wraparound gates illustrated in FIGS. 5A-5H.

FIG. 8 illustrates a flow diagram for forming a nanowire transistor with surrounding gates, according to various embodiments of the present subject matter.

FIG. 9 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter.

FIG. 10 illustrates a diagram for an electronic system having nanowire transistors, according to various embodiments.

FIG. 11 depicts a diagram of an embodiment of a system having a controller and a memory.

Detailed Description

The following detailed description refers to the accompanying drawings which show, by way of illustration, specific aspects and embodiments in which the present subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present subject matter. The various embodiments of the present subject matter are not necessarily mutually exclusive as aspects of one embodiment can be combined with aspects of another embodiment. Other embodiments may be utilized and

structural, logical, and electrical changes may be made without departing from the scope of the present subject matter. In the following description, the terms "wafer" and "substrate" are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art. The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side", "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The following discussion refers to silicon nanowire transistor embodiments. Those of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to use the teaching contained herein to form nanowire transistors using other semiconductors.

FIGS. 5A-5H illustrate an embodiment of a process to form crystalline nanorods with surrounding gates. FIG. 5A illustrates a first layer 503 on a substrate 504, with holes 505 formed in the first layer. The first layer is able to be etched to define the holes within the layer. According to various embodiments, the holes 505 are formed in a silicon nitride layer 503 on a silicon substrate 504, such that the holes extend through the silicon nitride layer to the silicon substrate. In the illustrated embodiment, the holes are formed with dimensions corresponding to the minimum feature size. The center of each hole

corresponds to the desired location of the nanowire transistor. An array of nanowire transistors can have a center-to-center spacing between rows and columns of 2F.

A layer of oxide is provided to cover the first layer after the holes have been etched therein. Various embodiments form a silicon oxide over the silicon nitride layer. Some embodiments deposit the silicon oxide by a chemical vapor deposition (CVD) process.

FIG. 5B illustrates the structure after the oxide is directionally etched to leave oxide sidewalls 506 on the sides of the hole, which function to reduce the dimensions of the resulting hole, and the resulting structure is planarized. In 100 nm technology, for example, the oxide sidewalls reduce the dimensions of the hole to about 30 nm. In this example, the thickness of the body region for the transistor will be on the order of 1/3 of the feature size. Some embodiments planarize the structure using a chemical mechanical polishing (CMP) process.

FIG. 5C illustrates a thick layer of an amorphous semiconductor material 507 formed over the resulting structure. The amorphous material fills the hole defined by the sidewalls 506. Various embodiments deposit amorphous silicon as the amorphous material. FIG. 5D illustrates the resulting structure after it is planarized, such as by CMP, to leave amorphous semiconductor material only in the holes.

FIG. 5E illustrates the resulting structure after the sidewalls (e.g. silicon oxide sidewalls) are removed. The structure is heat treated to crystallize the amorphous semiconductor 507 (e.g. a-silicon) into crystalline nanorods (represented as 507-C) using a process known as solid phase epitaxy (SPE). The amorphous semiconductor pillar 507 is in contact with the semiconductor wafer (e.g. silicon wafer), and crystal growth in the amorphous semiconductor pillar is seeded by the crystals in the wafer. The crystal formation from the SPE process is illustrated by the arrows 508 in FIG. 5E.

FIG. 5F illustrates the structure after the first layer (e.g. silicon nitride) is removed, leaving crystalline nanorods 507-C extending away from the substrate

surface, and after a gate insulator 509 is formed over the resulting structure. An embodiment forms the gate insulator by a thermal oxidation process. Thus, for an embodiment in which the wafer is a silicon wafer and the nanorods are crystalline silicon nanorods, the gate insulator is a silicon oxide. Other gate insulators, such as high K insulators, may be used.

FIG. 5G illustrates a side view and FIG. 5H illustrates a cross-section view along 5H-5H of FIG. 5G view of the structure after a gate material 510 is formed on the sidewalls of the crystalline nanorods 507-C. An embodiment deposits the gate material and etches the resulting structure to leave the gate material only on the sidewalls of the nanorods. Polysilicon is used as the gate material, according to various embodiments. The height of the pillars, which determines the channel length of the transistors, can be less than the minimum lithographic dimensions. Various embodiments provide a channel length on the order of approximately 100 nm. These nanorods with wraparound gates can be used to form nanowire transistors with surrounding or wraparound gates. The process continues in FIGS. 6A-6C for some embodiments of standalone transistors, and continued in FIGS. 7A-7C for some embodiments of transistor arrays.

FIGS. 6A-6C illustrate an embodiment of a process to form isolated transistors with source, drain and gate contacts, using the nanorods with wraparound gates illustrated in FIGS. 5A-5H. The illustrated structure includes a crystalline nanorod 607-C, a gate insulator 609, and a surrounding gate 610. Gate contacts 611 for the wraparound gates are patterned. Various embodiments deposit polysilicon to function as gate contacts for the wraparound gates. Both the wraparound gate and the gate contact, also referred to as a gate pad, are recessed below the top of the nanowire. A directional etching process may be used to recess the wraparound gate and the gate pad. As illustrated in FIG. 6B, the resulting structure is filled with an insulator fill (e.g. oxide) 612 and planarized to the top of the nanowires. The top of the nanowires are exposed by removing the gate insulator from the top of the nanowire. For example, an etch

can be used to remove silicon oxide from the top of the nanowire. The top of the nanowires can be doped and contact areas defined. The doped top portion 613 of the nanowires can function as a drain region. The substrate is appropriately doped to diffuse under the crystalline nanorod, and extend up into a bottom portion of the nanorod. This doped region can function as a source region. This doped region 614 also extends to a contact area. The doped region can be formed before the first layer is deposited and holes formed therein. The dopant can also be implanted and diffused before the surrounding gate is formed. Appropriate doping can be provided to provide NMOS or PMOS transistors. As illustrated in FIG. 6C, a contact 615 can be etched to the buried source, a contact 616 can be etched to the buried gate pad, and a contact 617 can also be formed for the drain. Those of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that other stand alone transistor designs may be used.

FIGS. 7A-7C illustrate an embodiment of a process to form an array of transistors, using the nanorods with wraparound gates illustrated in FIGS. 5A-5H. FIG. 7A illustrates a top view of adjacent transistors in a row of an embodiment of a transistor array. According to the illustrated embodiment, one word line 719 is formed adjacent to one row of transistors, such that the wraparound gates 710 of each transistor 718 in the row are in contact with the adjacent word line. FIB. 7B illustrates a top view of adjacent transistors in a row of another embodiment of a transistor array. According to various embodiments, polysilicon or gate material can be used for the gate wiring, a buried doped region can form a source region 720 and the source wiring 721, and metal contacts 722 and metal used for the drain wiring 723. In some embodiments, the nanowire structure with only wraparound gates is then backfilled with oxide and patterned and etched to leave oxide 724 between the pillars in one direction and expose the wrap around gates on the side. Polysilicon can be deposited and directionally etched to leave only on the sidewalls of the oxide blocks and exposed gate sides. As described with respect to FIG. 6C, the wraparound gates

can be further directionally etched to recess them below the top of the nanowire transistors. This will form the gate contacts and wiring. The structure can be planarized and backfilled with oxide and the top of the nanowires doped and contacted for the drain wiring using conventional techniques. Those of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that other transistor array designs may be used.

FIG. 8 illustrates a flow diagram for forming a nanowire transistor with surrounding gates, according to various embodiments of the present subject matter.

At 825, holes are formed in a substrate. For example, the substrate can include a first layer on a wafer, such as a layer of silicon nitride on a silicon wafer, and the holes are formed in the first layer to expose the wafer. The holes are defined by walls formed by the first layer. At 826, spacer sidewalls are formed within the holes against the walls formed by the first layer to effectively reduce the dimensions of the holes. An example of a spacer sidewall is silicon oxide. At 827, the holes are filled by an amorphous semiconductor (e.g. a-silicon). The spacer sidewalls are removed at 828, leaving pillars of amorphous semiconductor extending away from the wafer. The resulting structure is heat-treated or annealed at 829 to recrystallize the amorphous semiconductor, using the wafer to seed the crystalline growth. The recrystallization process is referred to as solid phase epitaxy (SPE). The resulting structure includes crystalline nanowires extending away from the wafer. At 830, a surrounding gate insulator and a surrounding gate are formed around the crystalline nanowires. Source/drain regions are formed at 831. The bottom of the nanowire is doped to form a first source/drain region, and the top of the nanowire is doped to form a second source/drain region. The first source/drain region can be formed by doping the substrate before depositing the first layer and patterning and etching the holes. The first source/drain can also be formed by implanting dopants adjacent to the nanorod before the gate is formed. These implanted dopants are capable of

diffusing completely under the nanorod because the nanorods are very thin. This doping can be performed after the first layer is removed off of the substrate.

FIG. 9 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter. The illustrated memory device 932 includes a memory array 933 and read/write control circuitry 934 to perform operations on the memory array via communication line(s) or channel(s) 935. The illustrated memory device 932 may be a memory card or a memory module such as a single inline memory module (SIMM) and dual inline memory module (DIMM). One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that semiconductor components in the memory array and / or the control circuitry are able to be fabricated using the nanowire transistors with surrounding gates, as described above. The structure and fabrication methods for these devices have been described above.

The memory array 933 includes a number of memory cells 936. The memory cells in the array are arranged in rows and columns. In various embodiments, word lines 937 connect the memory cells in the rows, and bit lines 938 connect the memory cells in the columns. The read/write control circuitry 934 includes word line select circuitry 939 which functions to select a desired row, bit line select circuitry 940 which functions to select a desired column, and read circuitry 941 which functions to detect a memory state for a selected memory cell in the memory array 933.

FIG. 10 illustrates a diagram for an electronic system 1042 having one or more nanowire transistors with surrounding gates, according to various embodiments. The electronic system includes a controller 1043, a bus 1044, and an electronic device 1045, where the bus provides communication channels between the controller and the electronic device. In various embodiments, the controller and/or electronic device include nanowire transistors as previously discussed herein. The illustrated electronic system may include, but is not limited to, information handling devices, wireless systems, telecommunication

systems, fiber optic systems, electro-optic systems, and computers.

FIG. 11 depicts a diagram of an embodiment of a system 1146 having a controller 1147 and a memory 1148. The controller and/or memory may include nanowire transistors. The illustrated system also includes an electronic apparatus 1149 and a bus 1150 to provide communication channel(s) between the controller and the electronic apparatus, and between the controller and the memory. The bus may include an address, a data bus, and a control bus, each independently configured; or may use common communication channels to provide address, data, and/or control, the use of which is regulated by the controller. In an embodiment, the electronic apparatus 1149 may be additional memory configured similar to memory 1148. An embodiment may include a peripheral device or devices 1151 coupled to the bus. Peripheral devices may include displays, additional storage memory, or other control devices that may operate in conjunction with the controller and/or the memory. In an embodiment, the controller is a processor. Any of the controller, the memory, the electronic apparatus, and the peripheral devices may include nanowire transistors. The system may include, but is not limited to, information handling devices, telecommunication systems, and computers. Applications containing nanowire transistors as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

The memory may be realized as a memory device containing nanowire transistors according to various embodiments. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash

memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM). Various emerging memory technologies are capable of using nanowire transistors.

This disclosure includes several processes, circuit diagrams, and structures. The present subject matter is not limited to a particular process order or logical arrangement. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover adaptations or variations of the present subject matter. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing and understanding the above description. The scope of the present subject matter should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method for forming a transistor, comprising:

forming a transistor body, including:

forming a pillar of amorphous semiconductor material on a crystalline substrate, the pillar having a sublithographic thickness; and

performing a solid phase epitaxy (SPE) process to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth, the transistor body being formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region;

forming a surrounding gate insulator around the semiconductor pillar; and

forming a surrounding gate around and separated from the semiconductor pillar by the surrounding gate insulator.

2. The method of claim 1, wherein forming a pillar of amorphous semiconductor material on a crystalline substrate includes forming a pillar of amorphous silicon on a crystalline silicon substrate.

3. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

4. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon gate.

5. The method of claim 1, wherein forming a surrounding gate includes forming a metal gate.

6. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the pillar.

7. The method of claim 1, further comprising forming the first source/drain region in the substrate and forming the second source/drain region in a top portion of the pillar.

8. A method for forming a transistor, comprising:

forming a transistor body, including:

forming silicon nitride on a silicon wafer;

etching a hole in the silicon nitride, the hole having a minimum feature size and extending through the silicon nitride to the silicon wafer;

reducing a dimension of the hole to less than the minimum feature size, including forming silicon oxide sidewall spacers on sides of the silicon nitride that define the hole;

filling the hole with an amorphous silicon;

removing the silicon oxide sidewall spacers to leave an amorphous silicon pillar in contact with and extending from the wafer; and

crystallizing the silicon pillar to form a crystalline silicon pillar, the transistor body being formed in the crystalline silicon pillar between a first source/drain region and a second source/drain region;

forming a surrounding gate insulator around the semiconductor pillar; and

forming a surrounding gate around and separated from the semiconductor pillar by the surrounding gate insulator.

9. The method of claim 8, wherein the height of the crystalline silicon pillar is less than the minimum feature size.

10. The method of claim 8, wherein forming a surrounding gate insulator includes oxidizing the crystalline silicon pillar.

11. The method of claim 8, further comprising etching source, gate and drain contacts for a stand-alone transistor.

12. The method of claim 8, further comprising forming a source line, at least one gate line, and a drain contact for a transistor array.

13. A method for forming a transistor, comprising:

forming a transistor body, including:

forming silicon nitride on a silicon wafer;

etching a hole in the silicon nitride, the hole having a minimum feature size and extending through the silicon nitride to the silicon wafer;

forming silicon oxide sidewall spacers on sides of the silicon nitride that define the hole;

filling the hole with an amorphous silicon, the amorphous silicon being in contact with the silicon wafer;

removing the silicon oxide sidewall spacers to leave an amorphous silicon pillar in contact with and extending from the wafer; and

crystallizing the silicon pillar to form a crystalline silicon pillar, the transistor body being formed in the crystalline silicon

pillar between a first source/drain region and a second source/drain region;

forming a surrounding gate insulator around the silicon pillar; and

forming a surrounding gate around and separated from the silicon pillar by the surrounding gate insulator.

14. The method of claim 13, further comprising forming a first contact on the wafer in contact with the first source/drain region, forming a gate contact in contact with the surrounding gate, and forming a second contact on the silicon pillar in contact with the second source/drain region.

15. The method of claim 13, wherein forming a surrounding gate insulator includes oxidizing the silicon pillar.

16. A method, comprising:

forming a silicon nitride layer on a silicon wafer;

etching a hole in the silicon nitride layer, the hole having a minimum feature size and extending through the silicon nitride to the silicon wafer;

forming silicon oxide sidewall spacers within the hole in contact with the silicon nitride;

filling the hole with an amorphous silicon, the amorphous silicon being in contact with the silicon wafer;

removing the silicon oxide sidewall spacers to leave an amorphous silicon pillar in contact with and extending from the wafer;

crystallizing the silicon pillar to form a crystalline silicon pillar;

removing the silicon nitride from the wafer;

forming an insulator layer on the wafer and the silicon pillar;

forming a surrounding gate around and separated from the silicon pillar by the surrounding gate insulator;

forming a first source/drain diffusion region in the wafer;

forming a gate contact adjacent to the surround gate;

etching a top surface of the surrounding gate and a top surface of the gate contact to be below a top surface of the pillar;

filling the structure with an insulator;

forming a second source/drain diffusion region in a top portion of the pillar; and

forming contacts through the insulator to the first source/drain region, the second source/drain region and the gate contact.

17. The method of claim 16, wherein forming an insulator on the wafer and the silicon pillar includes oxidizing the wafer and the silicon pillar.

18. The method of claim 16, wherein forming a surrounding gate includes forming a polysilicon gate.

19. A method, comprising:

forming at least one buried source conductor in a silicon wafer;

forming a silicon nitride layer on the silicon wafer;

etching a plurality of holes in the silicon nitride, the plurality of holes being arranged in an array of rows and columns, each hole having a minimum feature size and extending through the silicon nitride to the silicon wafer, at least two of the plurality of holes being formed over the buried source conductor;

forming silicon oxide sidewall spacers within each hole in contact with the silicon nitride;

filling each hole with an amorphous silicon, the amorphous silicon being in contact with the silicon wafer, the amorphous silicon in at least two of the plurality of holes being in contact with the buried source conductor in the silicon wafer;

removing the silicon oxide sidewall spacers to leave amorphous silicon pillar in contact with and extending from the wafer, the amorphous silicon pillar having cross-sectional dimensions less than the minimum feature size; and

crystallizing the silicon pillar to form a crystalline silicon pillar;

removing the silicon nitride from the wafer;

forming an insulator layer on the wafer and the silicon pillar;

forming a surrounding gate around and separated from the silicon pillar by the surrounding gate insulator;

forming at least one gate line adjacent to each row, the at least one gate line being in contact with each surrounding gate in the row;

etching a top surface of the surrounding gate and a top surface of the gate contact to be below a top surface of the pillar;

filling the structure with an insulator;

forming a second source/drain diffusion region in a top portion of the pillar; and

forming a contact to the second source/drain region.

20. The method of claim 19, wherein forming an insulator on the wafer and the silicon pillar includes oxidizing the wafer and the silicon pillar.

21. The method of claim 19, wherein forming a surrounding gate includes forming a polysilicon gate.

22. The method of claim 19, wherein forming at least one buried source conductor in a silicon wafer includes implanting a dopant in the silicon wafer.

23. A transistor, comprising:

a crystalline substrate;

a first source/drain region formed in the crystalline substrate;

a crystalline semiconductor pillar formed on the substrate in contact with the first source/drain region, the semiconductor pillar having cross-section dimensions less than a minimum feature size;

a second source/drain region formed in a top portion of the pillar;

a gate insulator formed around the pillar; and

a surrounding gate formed around and separated from the pillar by the gate insulator.

24. The transistor of claim 23, wherein the semiconductor pillar has a cross-section dimension on the order of one third of the minimum feature size.

25. The transistor of claim 23, wherein the semiconductor pillar has a cross-section dimension on the order of 30 nm.

26. The transistor of claim 23, wherein the gate insulator includes silicon oxide.

27. The transistor of claim 23, wherein the gate includes a polysilicon gate.

28. The transistor of claim 23, wherein the gate includes a metal gate.

29. A transistor, comprising:

a crystalline silicon substrate;

a first source/drain region formed in the crystalline silicon substrate;

a crystalline silicon pillar formed on the substrate in contact with the first source/drain region, the silicon pillar having cross-section dimensions less than a minimum feature size;

a second source/drain region formed in a top portion of the pillar;

a gate insulator formed around the pillar;

a surrounding gate formed around and separated from the pillar by the gate insulator; and

a gate contact positioned adjacent to and in contact with the surrounding gate, the surrounding gate and the gate contact being etched to have a top surface below a top surface of the pillar.

30. The transistor of claim 29, wherein the semiconductor pillar has a cross-section dimension on the order of one third of the minimum feature size.

31. The transistor of claim 29, wherein the semiconductor pillar has a cross-section dimension on the order of 30 nm.

32. A transistor, comprising:

a crystalline silicon substrate;

a first source/drain region formed in the crystalline silicon substrate;

a crystalline silicon pillar formed on the substrate in contact with the first source/drain region, the silicon pillar having cross-section dimensions less than a minimum feature size;

a second source/drain region formed in a top portion of the pillar;

a gate insulator formed around the pillar;

a surrounding gate formed around and separated from the pillar by the gate insulator; and

at least one gate line positioned adjacent to and in contact with the surrounding gate, the surrounding gate and the gate line being etched to have a top surface below a top surface of the pillar.

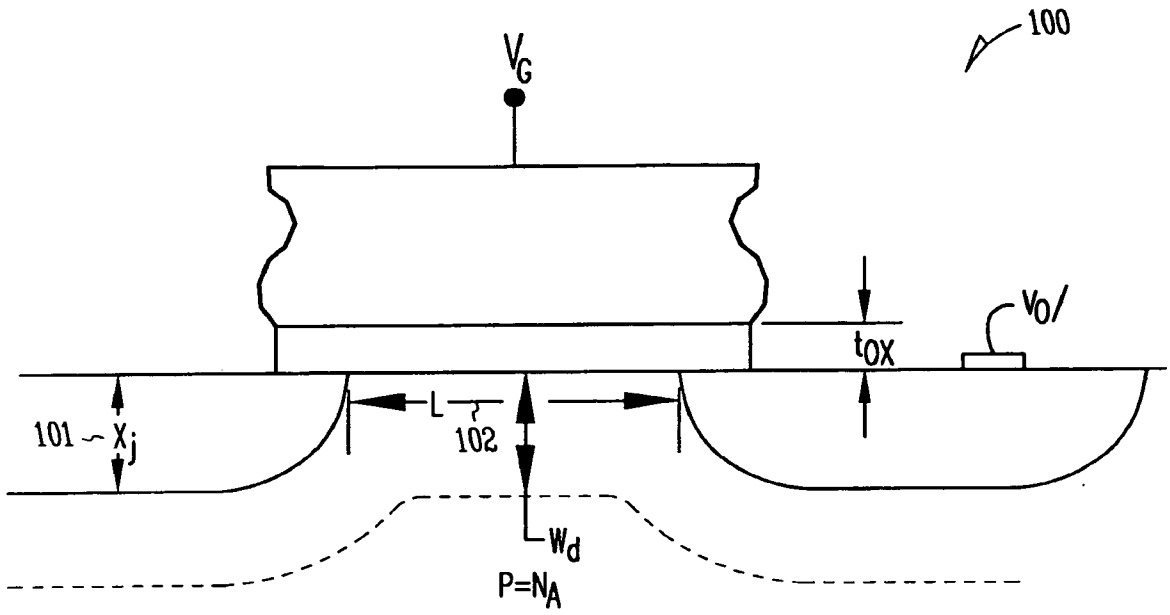
33. The transistor of claim 32, wherein the at least one gate line includes first and second gate lines adjacent to and in contact with the surrounding gate on opposing sides of the pillar.

34. A semiconductor structure, comprising:

a crystalline substrate; and

a semiconductor pillar formed on the substrate in contact with the first source/drain region, the semiconductor pillar having cross-section dimensions less than a minimum feature size, the semiconductor pillar having a crystallized bottom portion and an amorphous top portion indicative of a partially-completed solid phase epitaxy (SPE) process.

35. The structure of claim 34, further comprising a silicon nitride layer on the substrate, the silicon nitride layer being separated from the pillar by a void.



$V_G \longrightarrow V_G/k$ $\quad V_O \longrightarrow V_O/k$

$t_{OX} \longrightarrow t_{OX}/k$

$L \longrightarrow L/k$

$X_j \longrightarrow X_j/k$ JUNCTION DEPTH DECREASED

$W_d \longrightarrow W_d/k$

$N_A \longrightarrow k\ N_A$ SUBSTRATE DOPING INCREASED

FIG. 1

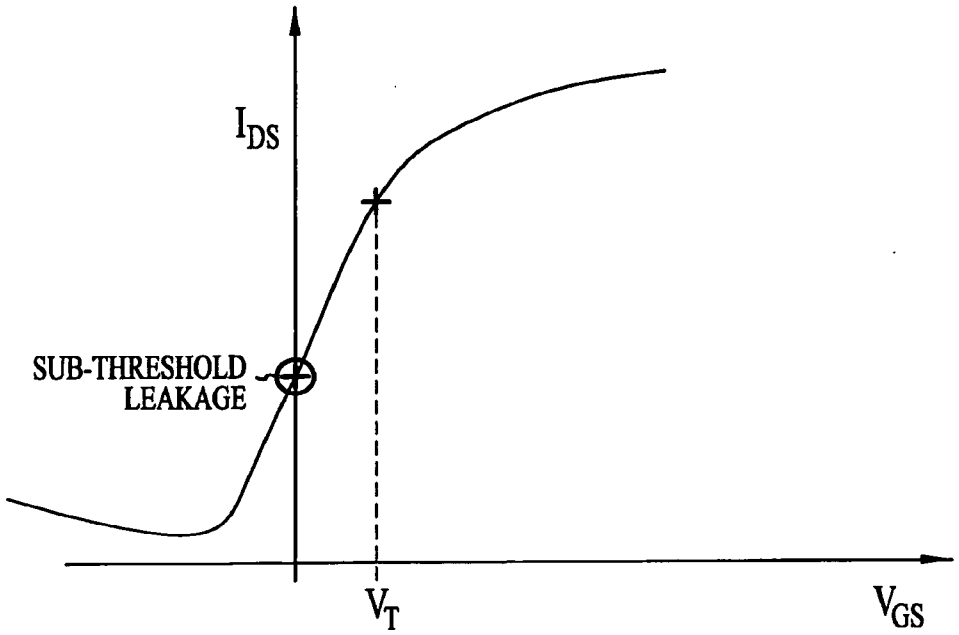

I_{DS}
SUB-THRESHOLD LEAKAGE
V_T
V_{GS}

FIG. 2

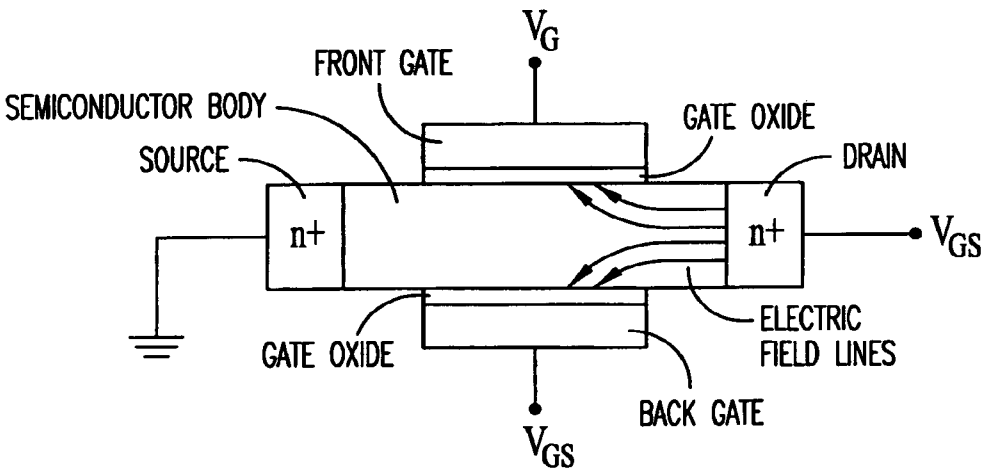

V_G
FRONT GATE
SEMICONDUCTOR BODY
GATE OXIDE
SOURCE
DRAIN
n+
n+
V_{GS}
ELECTRIC FIELD LINES
GATE OXIDE
BACK GATE
V_{GS}

FIG. 3

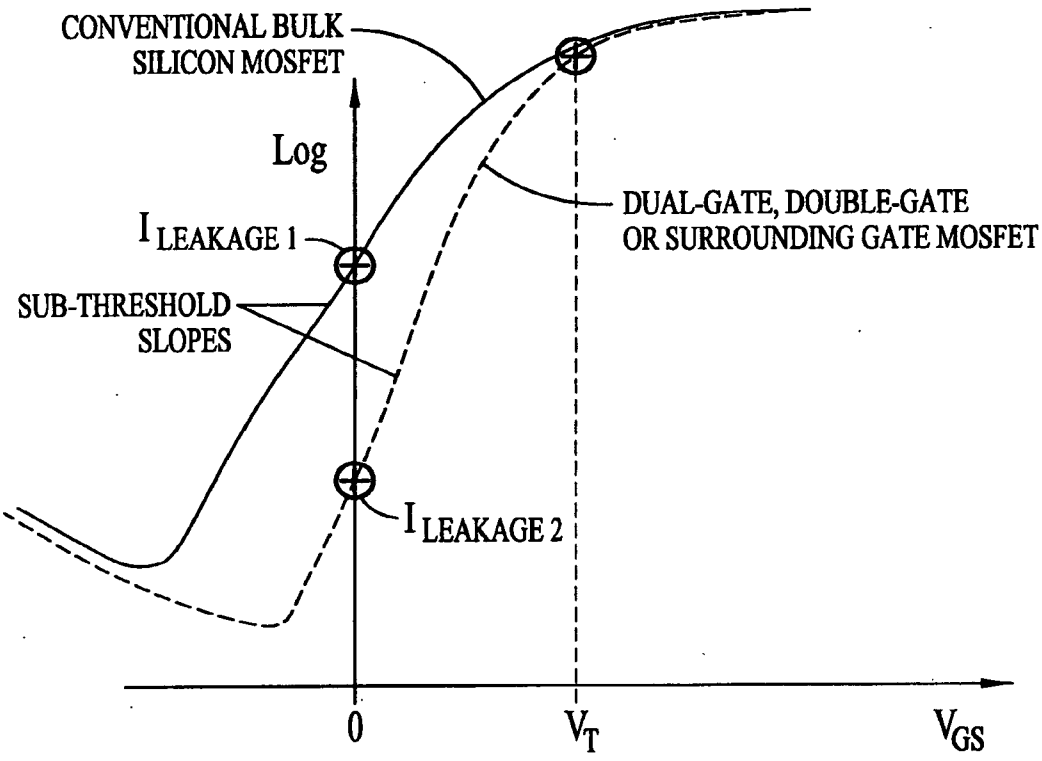
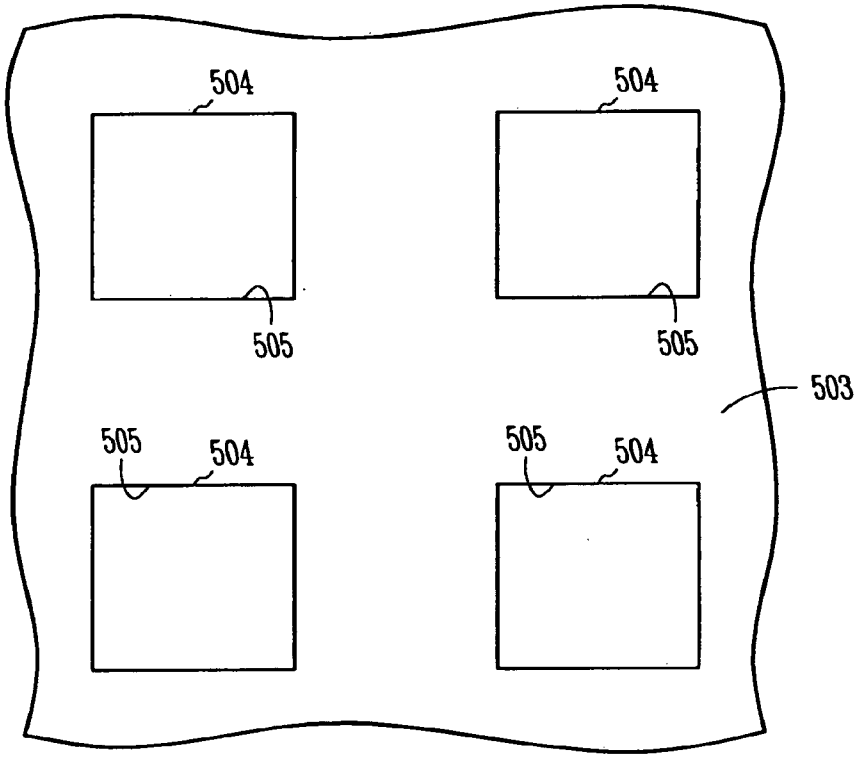

CONVENTIONAL BULK
SILICON MOSFET
Log
I LEAKAGE 1
SUB-THRESHOLD
SLOPES
DUAL-GATE, DOUBLE-GATE
OR SURROUNDING GATE MOSFET
I LEAKAGE 2
0
V_T
V_{GS}

FIG. 4


504
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505
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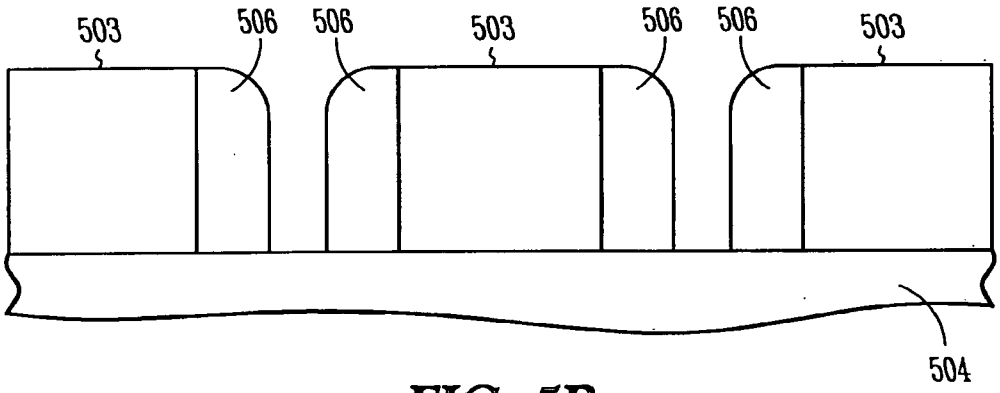
503
505
504
505
504

FIG. 5A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506
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503
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506
503
504

FIG. 5B

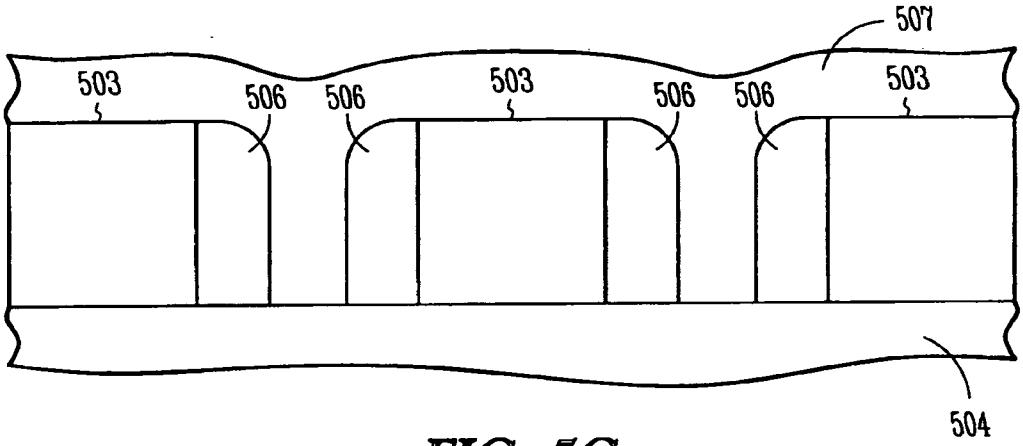
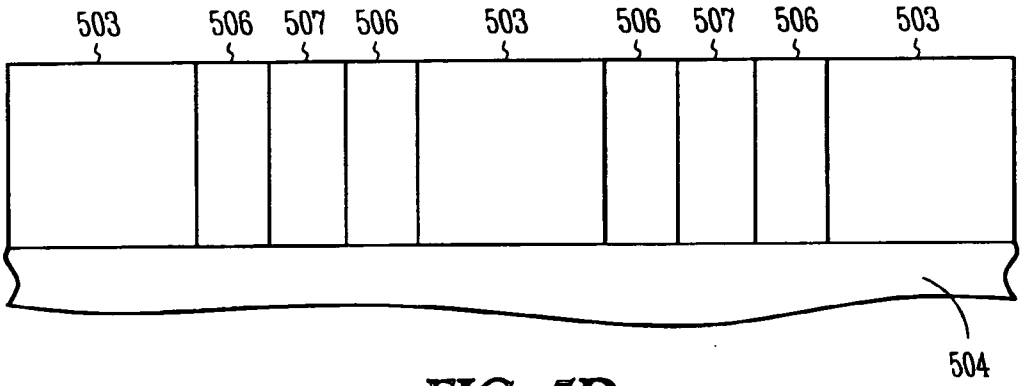

507
503
506
506
503
506
506
503
504

FIG. 5C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506
507
506
503
506
507
506
503
504

FIG. 5D

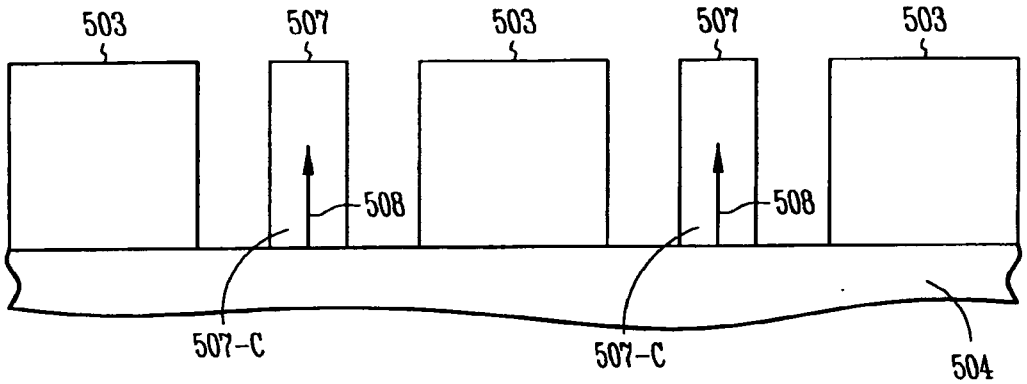


FIG. 5E

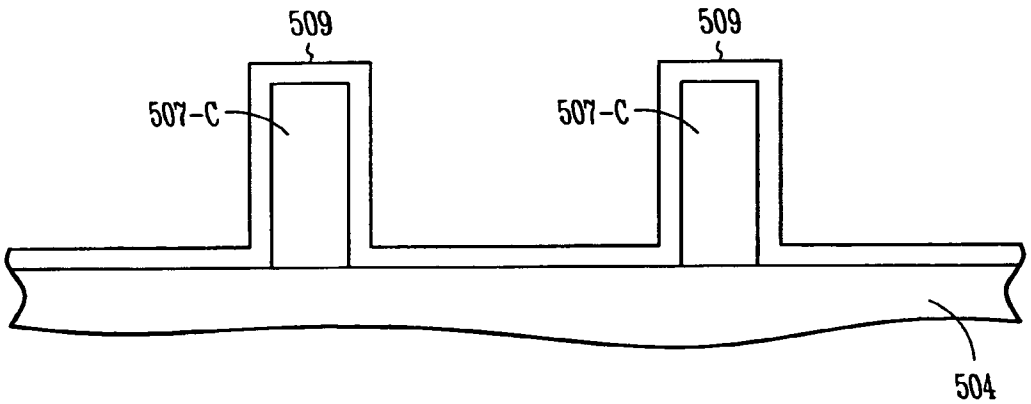


FIG. 5F

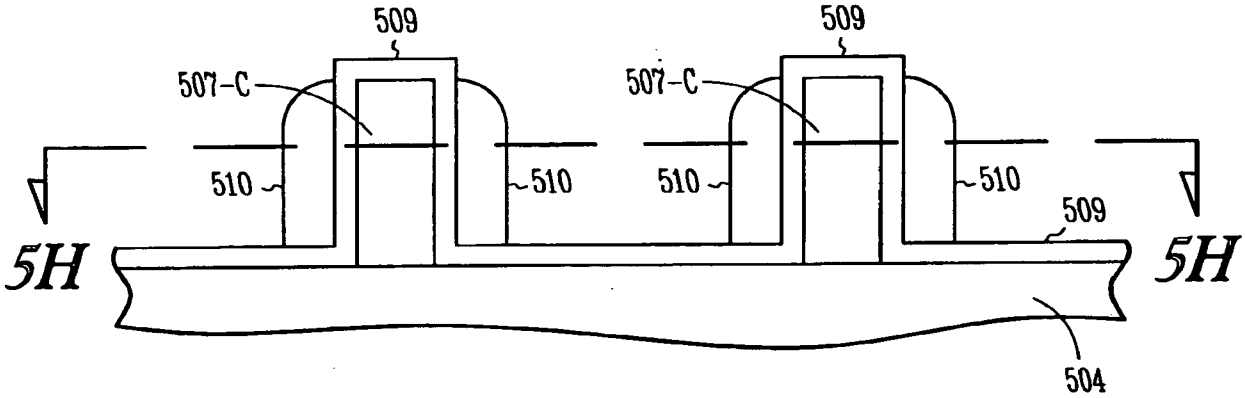

509
509
507-C
507-C
510
510
510
510
509
5H
5H
504

FIG. 5G

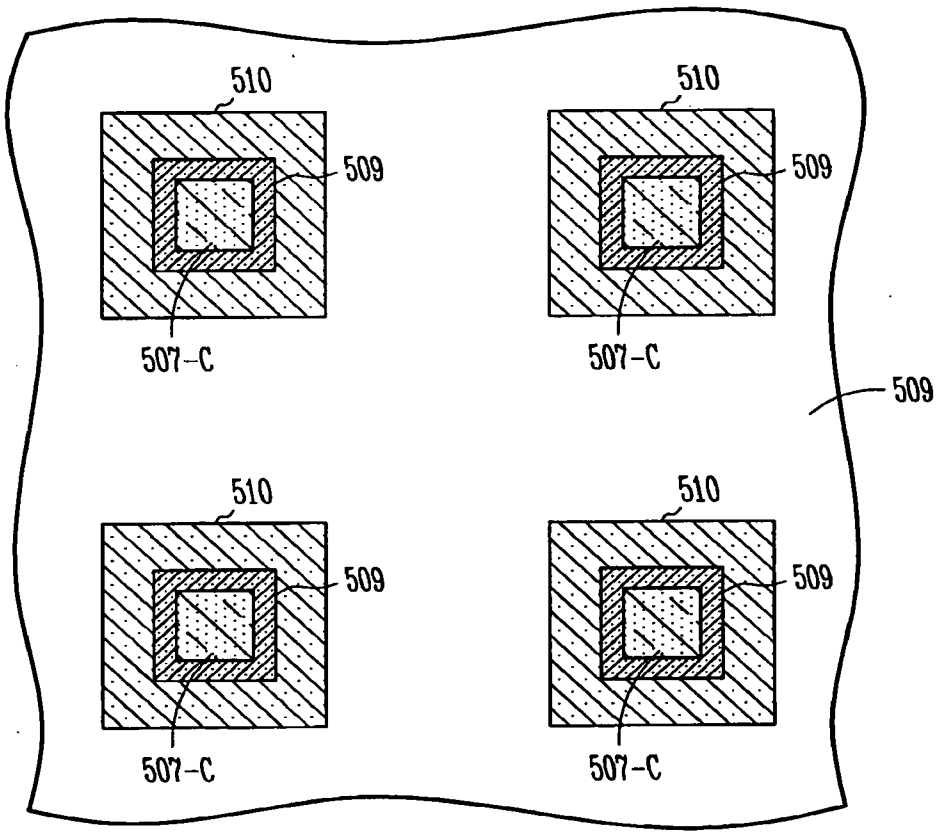

510
510
509
509
507-C
507-C
509
510
510
509
509
507-C
507-C

FIG. 5H

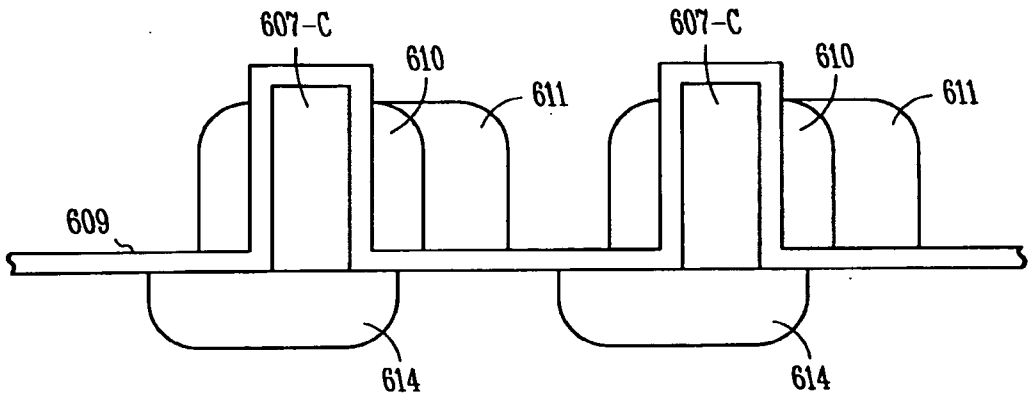


FIG. 6A

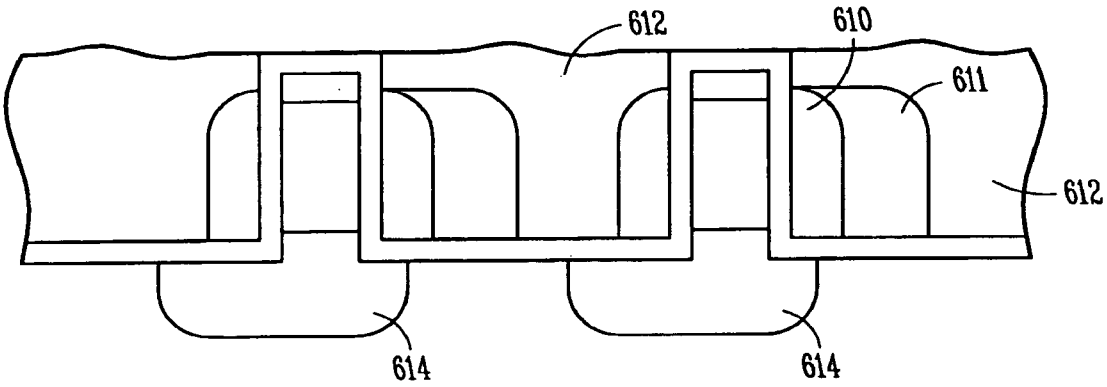


FIG. 6B

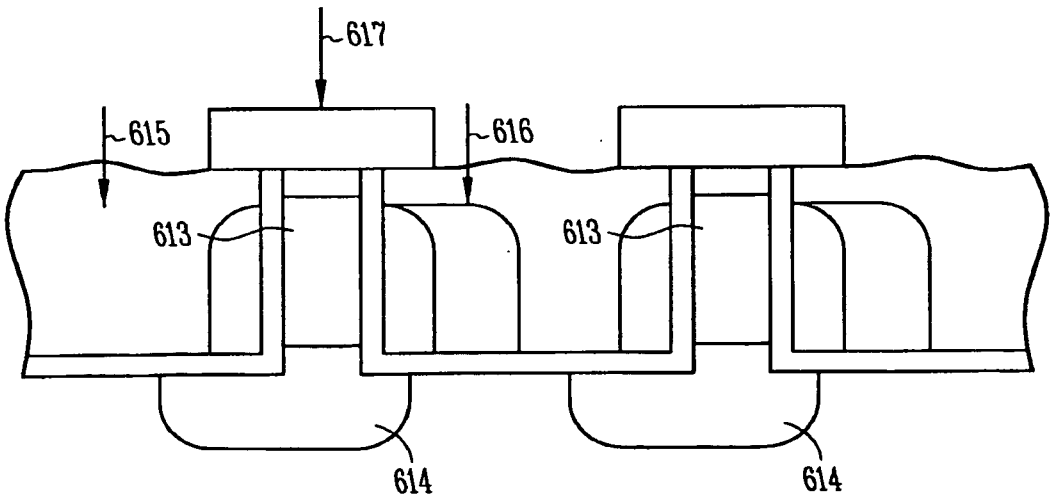


FIG. 6C

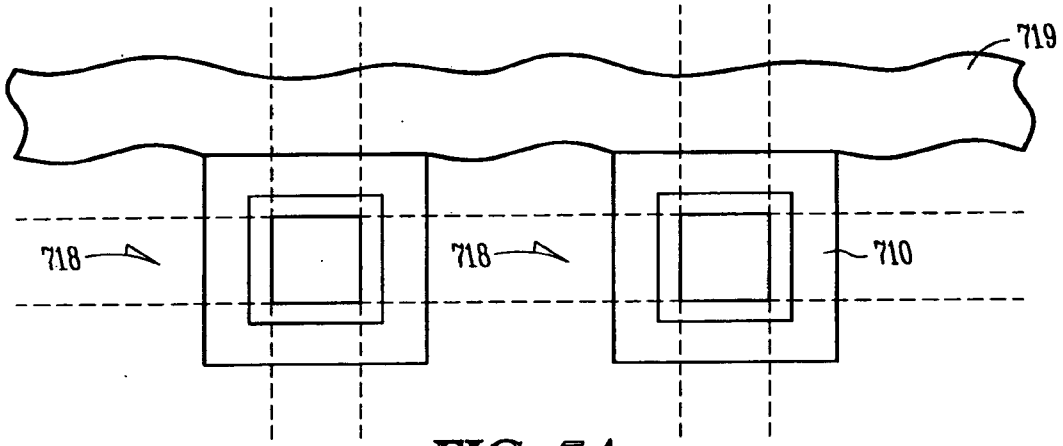

719
718
718
710

FIG. 7A

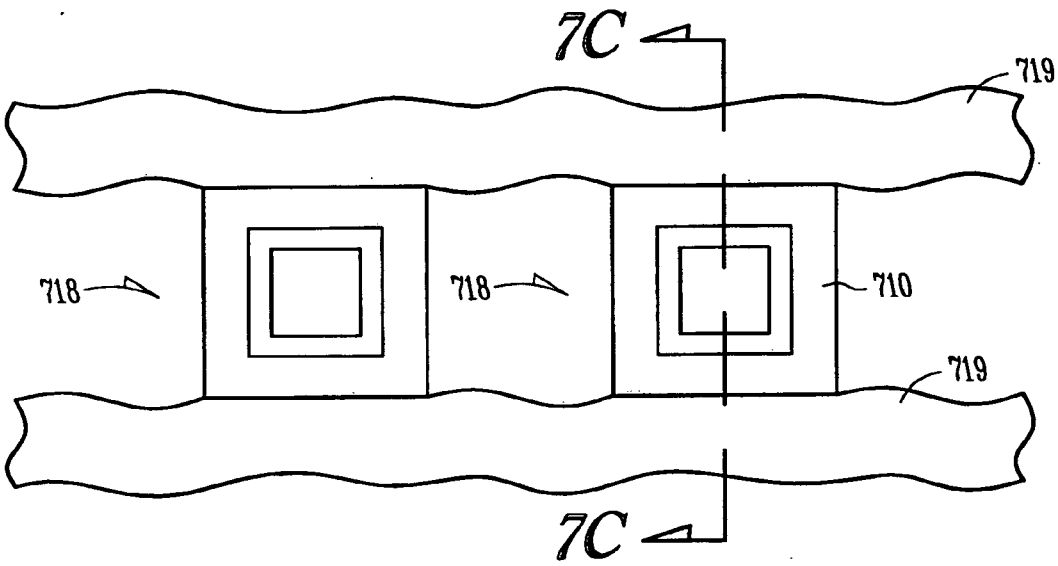
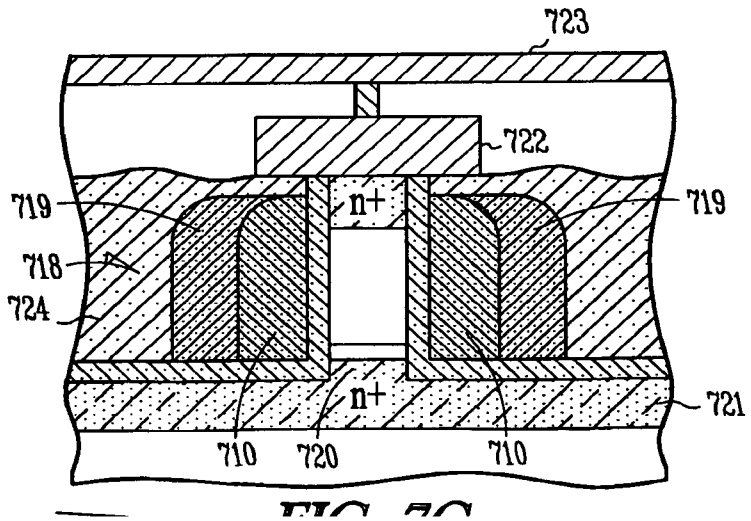

7C
719
718
718
710
719
7C

FIG. 7B


723
722
719
n+
719
718
724
n+
721
710
720
710

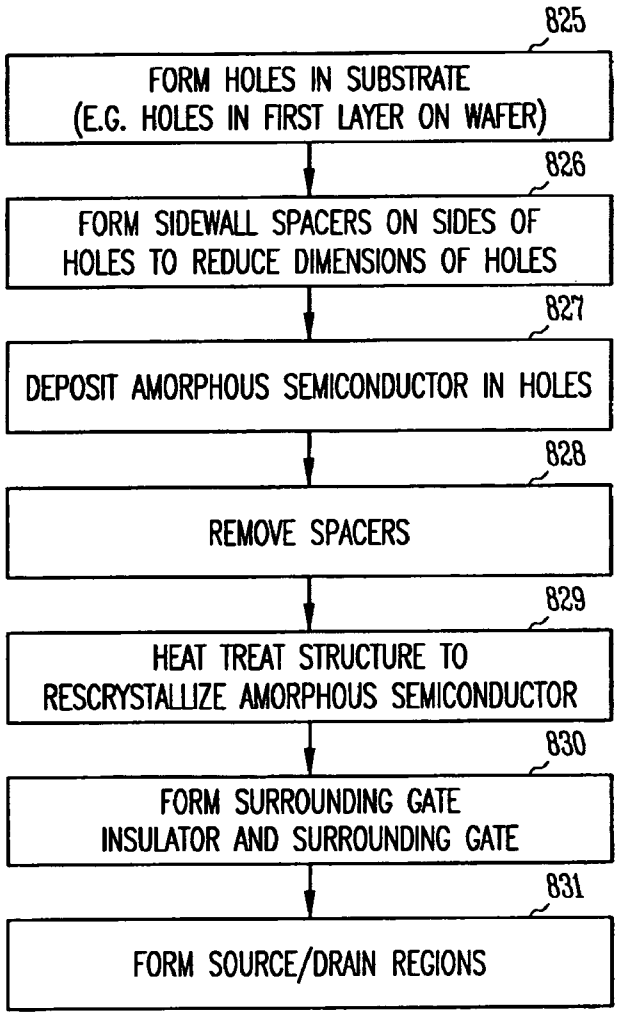

825
FORM HOLES IN SUBSTRATE (E.G. HOLES IN FIRST LAYER ON WAFER)
826
FORM SIDEWALL SPACERS ON SIDES OF HOLES TO REDUCE DIMENSIONS OF HOLES
827
DEPOSIT AMORPHOUS SEMICONDUCTOR IN HOLES
828
REMOVE SPACERS
829
HEAT TREAT STRUCTURE TO RESCRYSTALLIZE AMORPHOUS SEMICONDUCTOR
830
FORM SURROUNDING GATE INSULATOR AND SURROUNDING GATE
831
FORM SOURCE/DRAIN REGIONS

FIG. 8

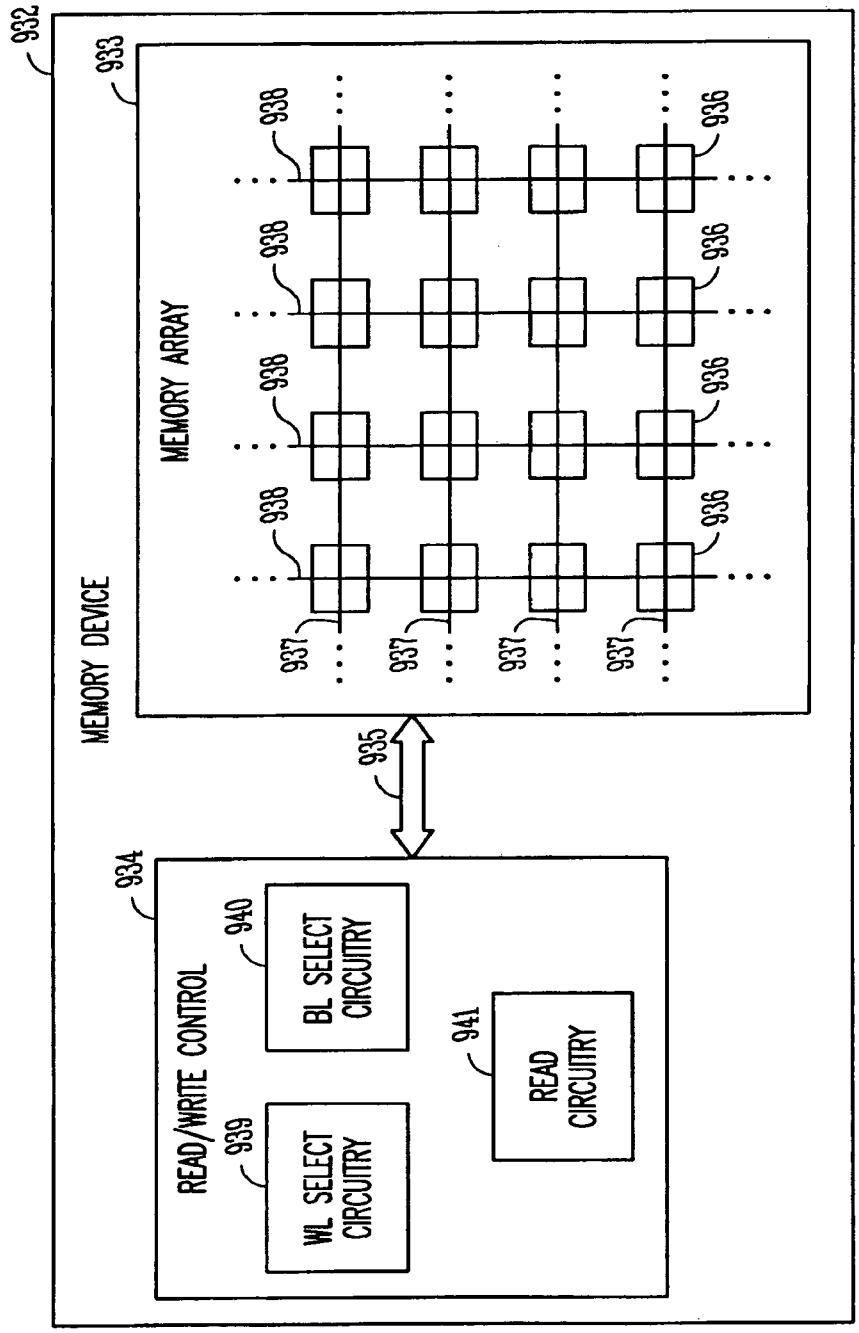

932
MEMORY DEVICE
933
MEMORY ARRAY
936
937
938
935
934
READ/WRITE CONTROL
939
WL SELECT CIRCUITRY
940
BL SELECT CIRCUITRY
941
READ CIRCUITRY

FIG. 9

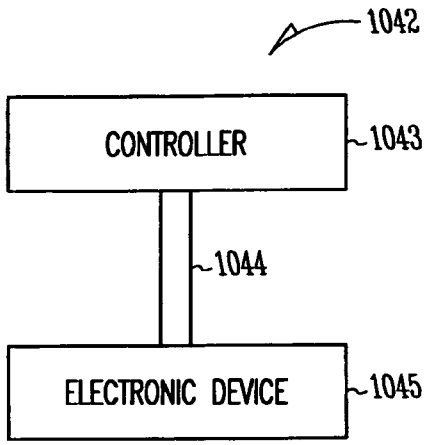

1042
CONTROLLER
1043
1044
ELECTRONIC DEVICE
1045

FIG. 10

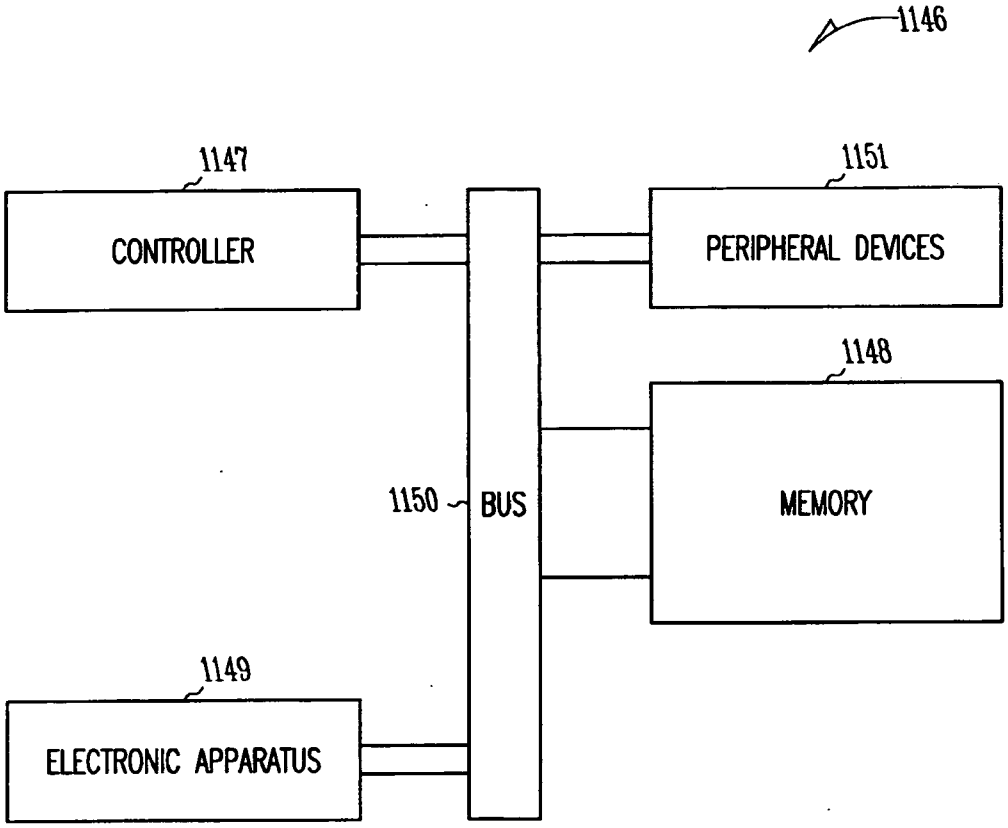

1146
1147
CONTROLLER
1151
PERIPHERAL DEVICES
1148
MEMORY
1150
BUS
1149
ELECTRONIC APPARATUS

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/008123

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/336 H01L29/06 H01L29/786 H01L21/8242 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2005/032297 A1 (KAMINS THEODORE I [US]) 10 February 2005 (2005-02-10) paragraphs [0041] - [0047]; figure 1	23-34 1-22
X	US 2006/046391 A1 (TANG SANH D [US] ET AL) 2 March 2006 (2006-03-02) paragraphs [0117] - [0119]; figures 7B-10B	23-34
X	US 6 855 582 B1 (DAKSHINA-MURTHY SRIKANTESWARA [US] ET AL) 15 February 2005 (2005-02-15) figures 12-14	23-34
Y	DE 199 43 390 A1 (HANSCH WALTER [DE]) 3 May 2001 (2001-05-03) column 4, line 36 - line 44	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 August 2007	21/08/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, Andreas

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/008123

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005032297 A1	10-02-2005	NONE	
US 2006046391 A1	02-03-2006	US 2007048943 A1	01-03-2007
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DE 19943390 A1	03-05-2001	NONE	