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(54) Title: METHOD AND APPARATUS FOR INITIALIZING MULTIPLE PROCESSORS RESIDING IN AN INTEGRATED CIRCUIT

(57) Abstract:



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**METHOD AND APPARATUS FOR INITIALIZING MULTIPLE
PROCESSORS RESIDING IN AN INTEGRATED CIRCUIT**

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DESCRIPTION

The present invention generally relates to integrated circuits, and more specifically, to integrated circuits having multiple processors that are to be initialized during the powering on of the integrated circuit.

Description of Related Art

Consumers continuously challenge the electronic industry to produce increasingly smaller devices while introducing even greater functionality. It has become an expectation of the consumer that these devices will become instantly available upon turning the power on.

These devices typically contain a myriad of integrated circuits each supporting numerous functional capabilities with the assistance of one or more processors. The initialization of these processors has been accomplished using several different solutions. The previous solutions were developed without the time constraints presented by the current instantaneous expectations of the consumer.

It would, therefore, be a distinct advantage to have a method and system that would initialize multiple processors residing in an integrated circuit in a time and code efficient manner.

SUMMARY OF THE PRESENT INVENTION

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The present invention initializes multiple processors in an integrated circuit. Boot code is written for initialization of the processors so that there is a general/common section and specific sections for processor specific code. Each one of the processors is uniquely identifiable (in the preferred embodiment of the present invention, the strapping of a unique value to a register is used). During execution of the general section of boot code, the identity of the processor is used to

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execute any specific code for the identified processor in the specific section of boot code.

BRIEF DESCRIPTION OF THE DRAWINGS

5 A preferred embodiment of the present invention will now be described in detail, by way of example only, with reference to the following drawings in which:

10 Figure 1 is a block diagram illustrating an integrated circuit 102 having multiple processors P1-Pn that are initialized in a preferred embodiment of the present invention; and

15 Figure 2, a flow chart is shown illustrating the method for initializing the processors P1-Pn of Figure 1 in a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE PRESENT INVENTION

20 The present invention initializes multiple processors, residing in an integrated circuit, by providing each processor with a unique identification value. This unique identification value is then used by the boot code to identify specific code to initialize the identified processor. The incorporation of the identity of the processor into the boot code allows each of the processors to contain the same
25 address for the boot code (i.e. starting point), and to reuse common portions of the boot code as explained in greater detail below in connection with the corresponding figures.

30 Reference now being made to Figure 1, a block diagram is shown illustrating an integrated circuit 102 having multiple processors P1-Pn that are initialized according to a preferred embodiment of the present invention. Integrated circuit 102 includes multiple processors P1 - Pn, a shared cache 110, memory 112, processor bus 114, and system bus 116.

35 The processors P1-Pn can be, for example, the PowerPC 405 processor from International Business Machines or any other processor capable of being incorporated into an integrated circuit. In the preferred embodiment of the present invention, each of the processors P1-Pn include a register that is strapped or otherwise provided with a value

to uniquely identify the processor P1-Pn. Each one of the processors P1-Pn is provided with the capability of transferring and receiving data via processor bus 114.

5 Shared Cache 110 is a standard shared cache implementation invention as explained in greater detail with the other elements of integrated circuit 102. It should be noted, however, that shared cache 110 is optional and not a necessary requirement in embodiments of the present invention, but merely enhances the speed and operation where such
10 speed and operation are desirable (e.g. large number of processors). Shared Cache 110 is coupled to the processor bus 114 and the system bus 116.

 Shared memory 112 is a typical memory having a sufficient size to store the boot code for the processors P1-Pn, and is coupled to system
15 bus 116. The boot code should be located at an address that is consistent with the address provided to the processors P1-Pn for initialization. A pseudo code example of the boot code is provided in Table 1 below.

TABLE 1

20 // General Initialization Code//
 perform code routines here that are common for all processors.
 Read unique identification value of processor
 Jump/branch to processor specific code as identified by unique
 identifier
25 //Processor Specific Code //
 Processor specific code resides here

 Reference now being made to Figure 2, a flow chart is shown illustrating the method for initializing the processors P1-Pn of Figure 1 according to a preferred embodiment of the present invention. The method begins (step 200) by providing each one the processors P1-Pn with a unique
30 identification (step 202). In the preferred embodiment of the present invention, the unique identification is provided by strapping a register, such as a DCR register. The method continues by executing a particular
35 start sequence for the processors P1-Pn (step 204) where each of the processors P1-Pn executes the boot code residing either in memory 112 or shared cache 110 (if retrieved by a previous processor P1-Pn) (step 204). The unique identification is used in the boot code to initialize the processor P1-Pn with any processor P1-Pn specific code.

CLAIMS

1. A method of initializing a plurality of processors in an integrated circuit, the method comprising the steps of:

identifying each one of the processors;

executing boot code for initializing each one of the processors, the boot code containing specific code for at least one of the processors and common code that is common for each one of the processors, the specific code being accessed according to the identity of the processor executing the boot code.

2. The method of claim 1 wherein the step of identifying includes the step of:

assigning a unique value to each one of the processors.

3. The method of claim 2 wherein each one of the processors includes a register and the step of assigning includes the step of:

providing a unique value to the register of the processor.

4. An apparatus for initializing a plurality of processors in an integrated circuit, the apparatus comprising:

means for identifying each one of the processors;

means for executing boot code for initializing each one of the processors, the boot code containing specific code for at least one of the processors and common code that is common for each one of the processors, the specific code being accessed according to the identity of the processor executing the boot code.

5. The apparatus of claim 4 wherein the means for identifying includes:

means for assigning a unique value to each one of the processors.

6. The apparatus of claim 5 wherein each one of the processors includes a register and the means for assigning includes:

means for providing a unique value to the register of the processor.

7. An integrated circuit comprising:

a plurality of processors each having a unique identifier;

a bus for providing data to and from each one of the processors;

a memory, coupled to the bus, having boot code for initializing each one of the processors, the boot code using the unique identifier of each processor to access code that is unique to the identified processor.

5 8. The integrated circuit of claim 7 wherein each one of the processors has at least one register, and the at least one register is used to store a unique identifier.

10 9. The integrated circuit of claim 7 further comprising a cache shared between the plurality of processors.

10. A method of initializing multiple processors in an integrated circuit, the method comprising the steps of:

15 creating boot code for initializing the processors, the boot code having code that is common for each one of the processors, and code that is specific for each one of the processors;

20 assigning each one of the processors a unique identifier; and
executing the boot code and accessing code that is specific for a processor using the unique identifier of the processor.

11. The method of claim 10 wherein the step of assigning includes the step of:

storing a unique value into a register of each one of the processors.

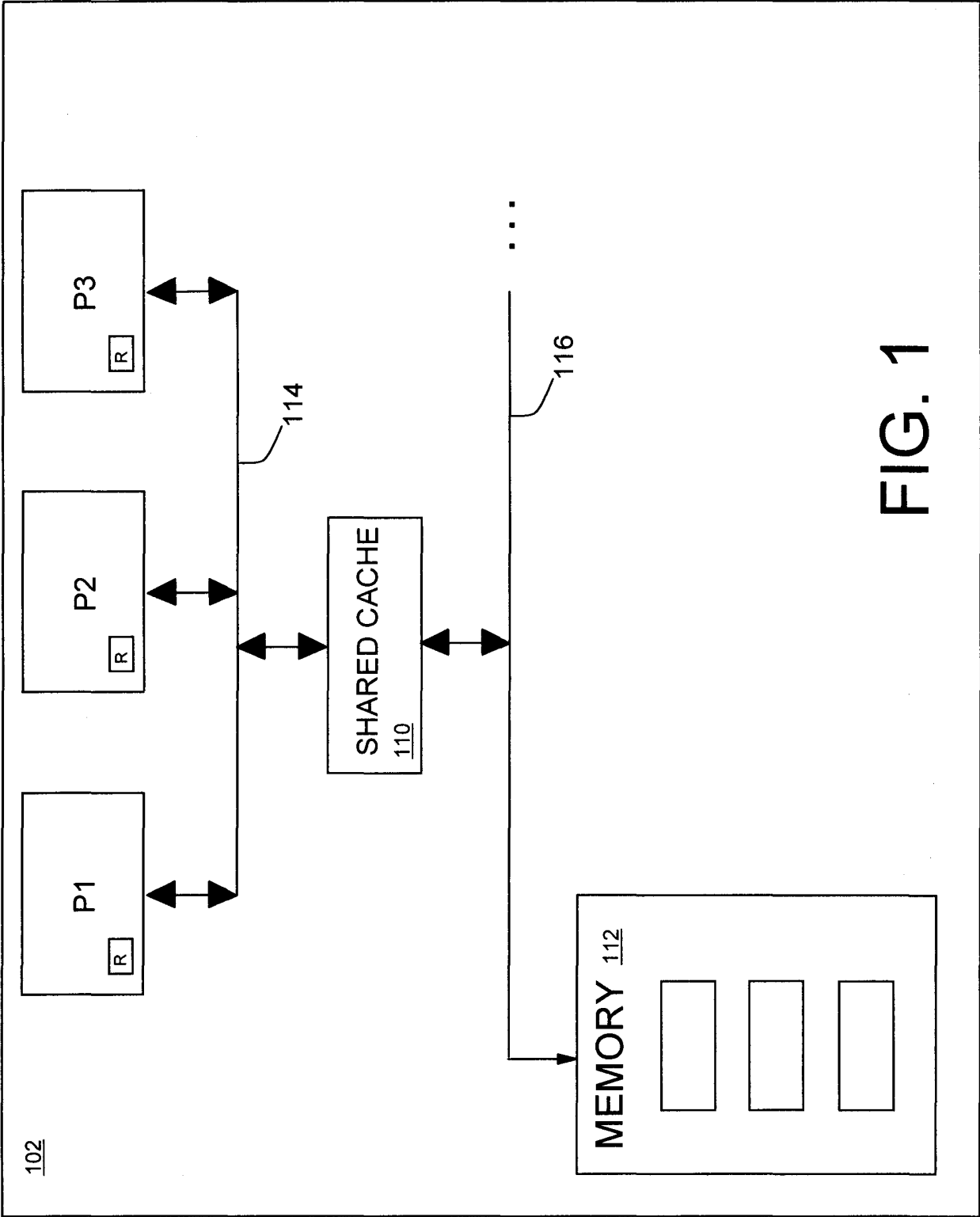


FIG. 1

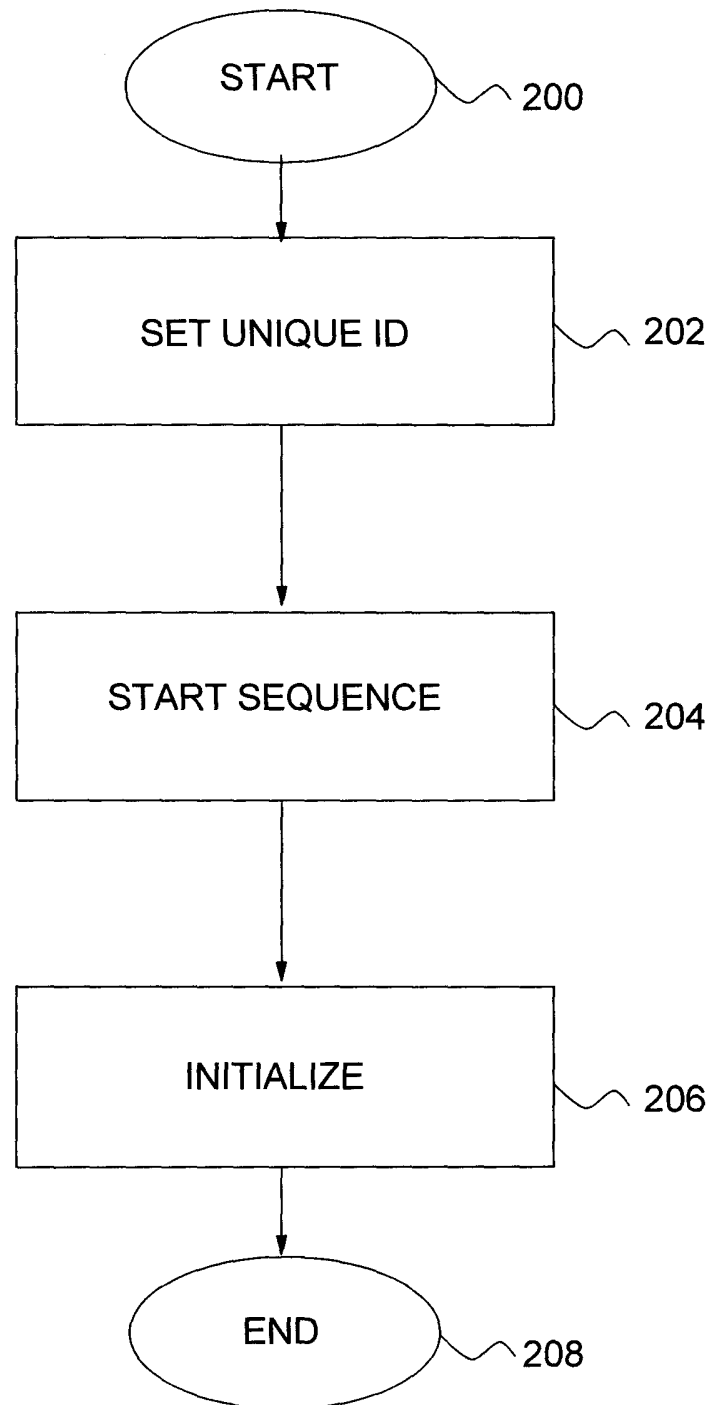


FIG. 2

PATENT COOPERATION TREATY

PCT

DECLARATION OF NON-ESTABLISHMENT OF INTERNATIONAL SEARCH REPORT

(PCT Article 17(2)(a), Rules 13ter.1(c) and Rule 39)

Applicant's or agent's file reference BUR030020	IMPORTANT DECLARATION	Date of mailing(day/month/year) 11/01/2006
International application No. PCT/EP2005/054300	International filing date(day/month/year) 01/09/2005	(Earliest) Priority date(day/month/year) 01/09/2004
International Patent Classification (IPC) or both national classification and IPC G06F15/18		
Applicant INTERNATIONAL BUSINESS MACHINES CORPORATION		

This International Searching Authority hereby declares, according to Article 17(2)(a), that **no international search report will be established** on the international application for the reasons indicated below

1. ☐ The subject matter of the international application relates to:
 - a. ☐ scientific theories.
 - b. ☐ mathematical theories
 - c. ☐ plant varieties.
 - d. ☐ animal varieties.
 - e. ☐ essentially biological processes for the production of plants and animals, other than microbiological processes and the products of such processes.
 - f. ☐ schemes, rules or methods of doing business.
 - g. ☐ schemes, rules or methods of performing purely mental acts.
 - h. ☐ schemes, rules or methods of playing games.
 - i. ☐ methods for treatment of the human body by surgery or therapy.
 - j. ☐ methods for treatment of the animal body by surgery or therapy.
 - k. ☐ diagnostic methods practised on the human or animal body.
 - l. ☐ mere presentations of information.
 - m. ☐ computer programs for which this International Searching Authority is not equipped to search prior art.
2. ☒ The failure of the following parts of the international application to comply with prescribed requirements prevents a meaningful search from being carried out:

☒ the description ☒ the claims ☐ the drawings
3. ☐ The failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions prevents a meaningful search from being carried out:

☐ the written form has not been furnished or does not comply with the standard.
☐ the computer readable form has not been furnished or does not comply with the standard.
4. ☐ The failure of the tables related to the nucleotide and/or amino acid sequence listing to comply with the technical requirements provided for in Annex C-bis of the Administrative Instructions prevents a meaningful search from being carried out:

☐ the written form has not been furnished.
☐ the computer readable form has not been furnished or does not comply with the technical requirements.
5. Further comments:

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FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 203

The claims define methods and apparati for initializing a plurality of processors in an integrated circuit which are defined by reference to desirable properties, namely to identify each one of the processors and to execute a boot code for initializing each of the processors. The claims cover all methods and apparati having these properties, whereas the application does not provide any support within the meaning of Article 6 PCT and disclosure within the meaning Article 5 PCT.

In particular, the claims are drafted in an extremely generic and functional manner, setting out the result to be achieved, but not defining the concrete technical features in order to achieve the envisaged technical effect.

In the whole description no disclosure is given in how to identify each of the processors (it is only stated that it may be implemented by a DCR register). There is also lack of disclosure concerning how a boot code is accessed by each one of the processors.

Consequently, the description does not set forth any mode for carrying out the claimed subject-matter and does not enable the skilled person to carry out the invention (produce said apparatus, carry out the method). Hence the application does not fulfill the requirements of Rule 5(a)(v) and Article 5 PCT.

Independent of the above reasoning, the claims also lack clarity (Article 6 PCT). An attempt is made to define the methods and apparati by reference to a result to be achieved.

This lack of clarity and support in the present case is such as to render a meaningful search impossible (Article 17(2)(a)(ii) PCT).

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.