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(54) METHOD FOR CONSTRUCTING A MAGNETO-RESISTIVE ELEMENT

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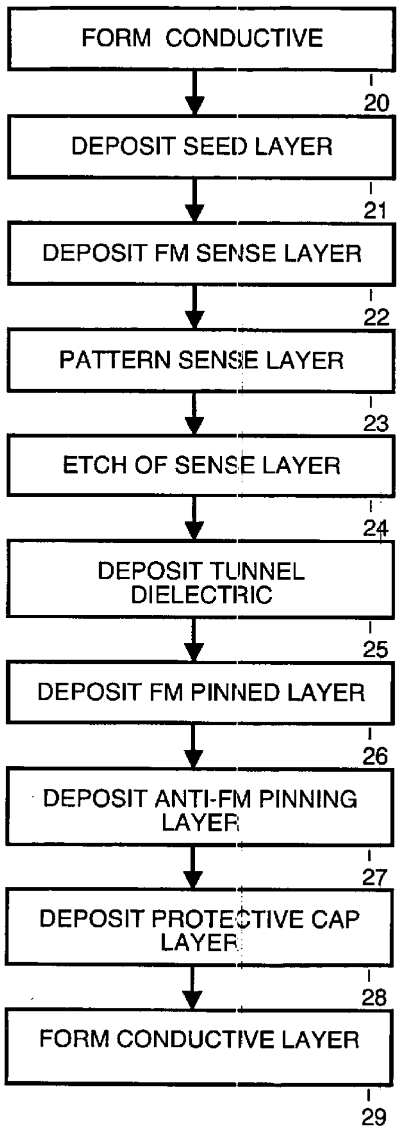
(52) U.S. Cl. **438/3**

(57) **ABSTRACT**

A magneto-resistive element is constructed. A ferromagnetic sense layer is deposited on a surface. The ferromagnetic sense layer is patterned. An etch is performed in preparation for depositing a dielectric layer. The dielectric layer is deposited over the sense layer. A ferromagnetic pinned layer is deposited over the dielectric layer.



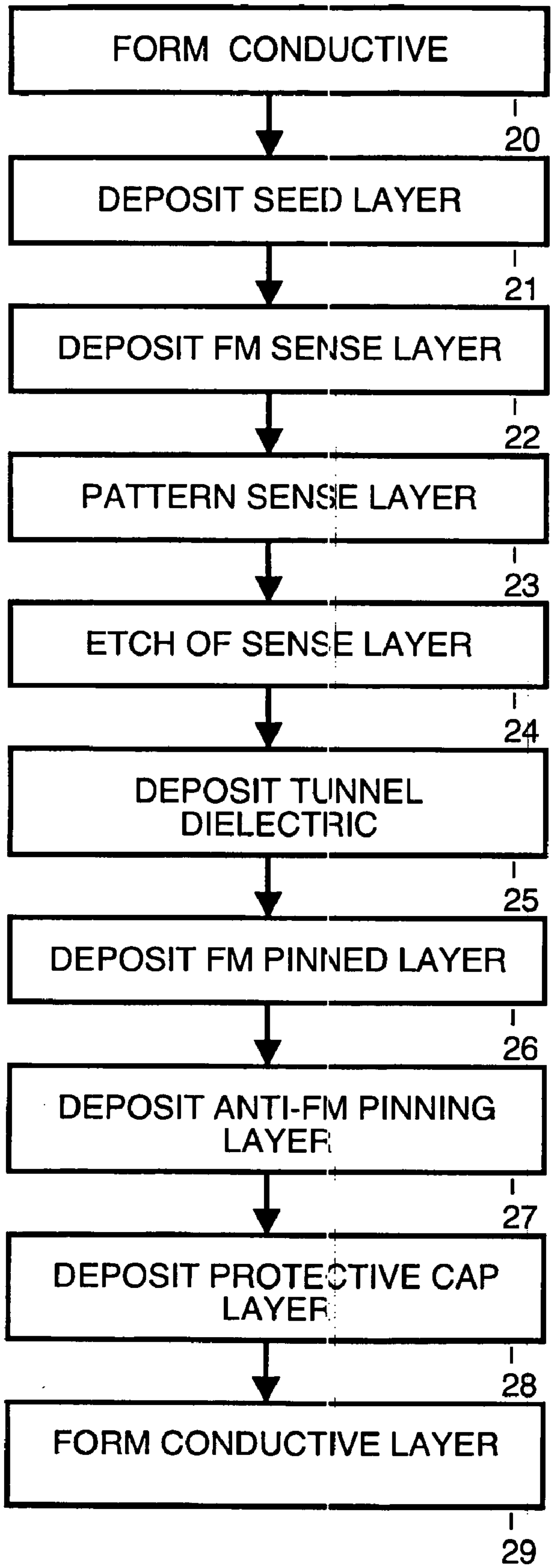

FORM CONDUCTIVE
20
DEPOSIT SEED LAYER
21
DEPOSIT FM SENSE LAYER
22
PATTERN SENSE LAYER
23
ETCH OF SENSE LAYER
24
DEPOSIT TUNNEL DIELECTRIC
25
DEPOSIT FM PINNED LAYER
26
DEPOSIT ANTI-FM PINNING LAYER
27
DEPOSIT PROTECTIVE CAP LAYER
28
FORM CONDUCTIVE LAYER
29

FIGURE 1

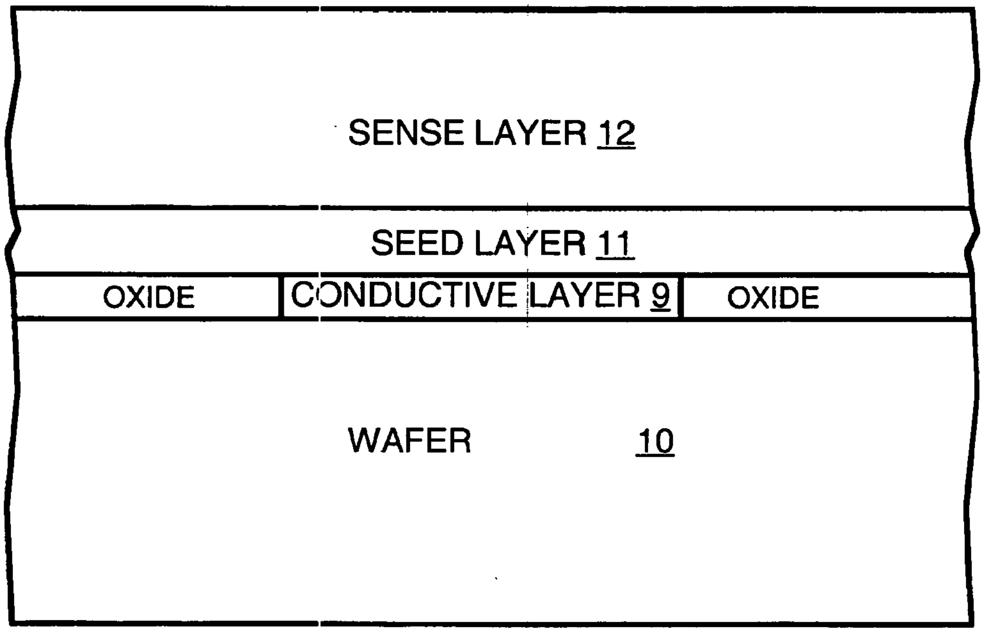

SENSE LAYER 12
SEED LAYER 11
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER 10

FIGURE 2

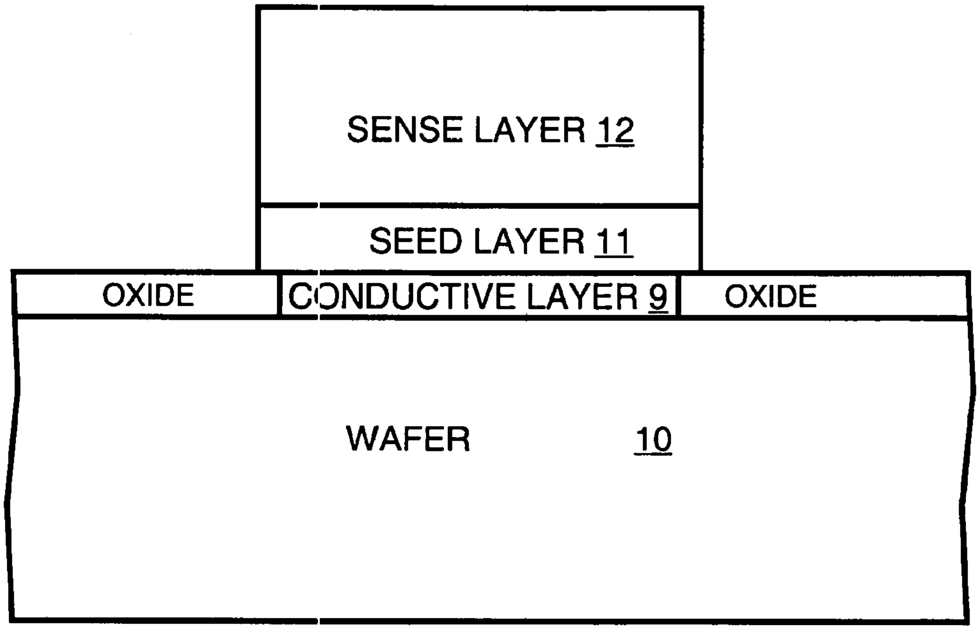

SENSE LAYER 12
SEED LAYER 11
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER
10

FIGURE 3

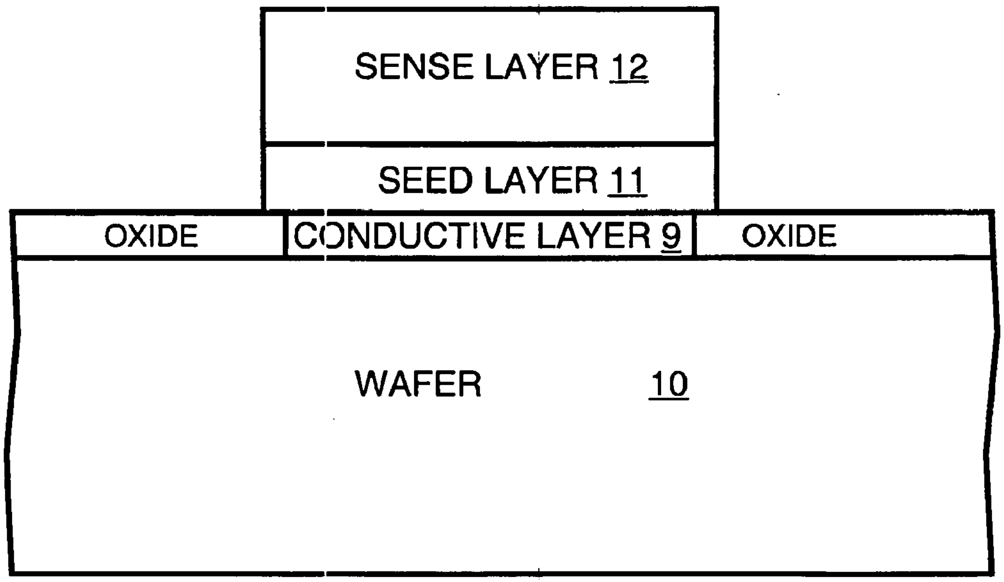

SENSE LAYER 12
SEED LAYER 11
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER 10

FIGURE 4

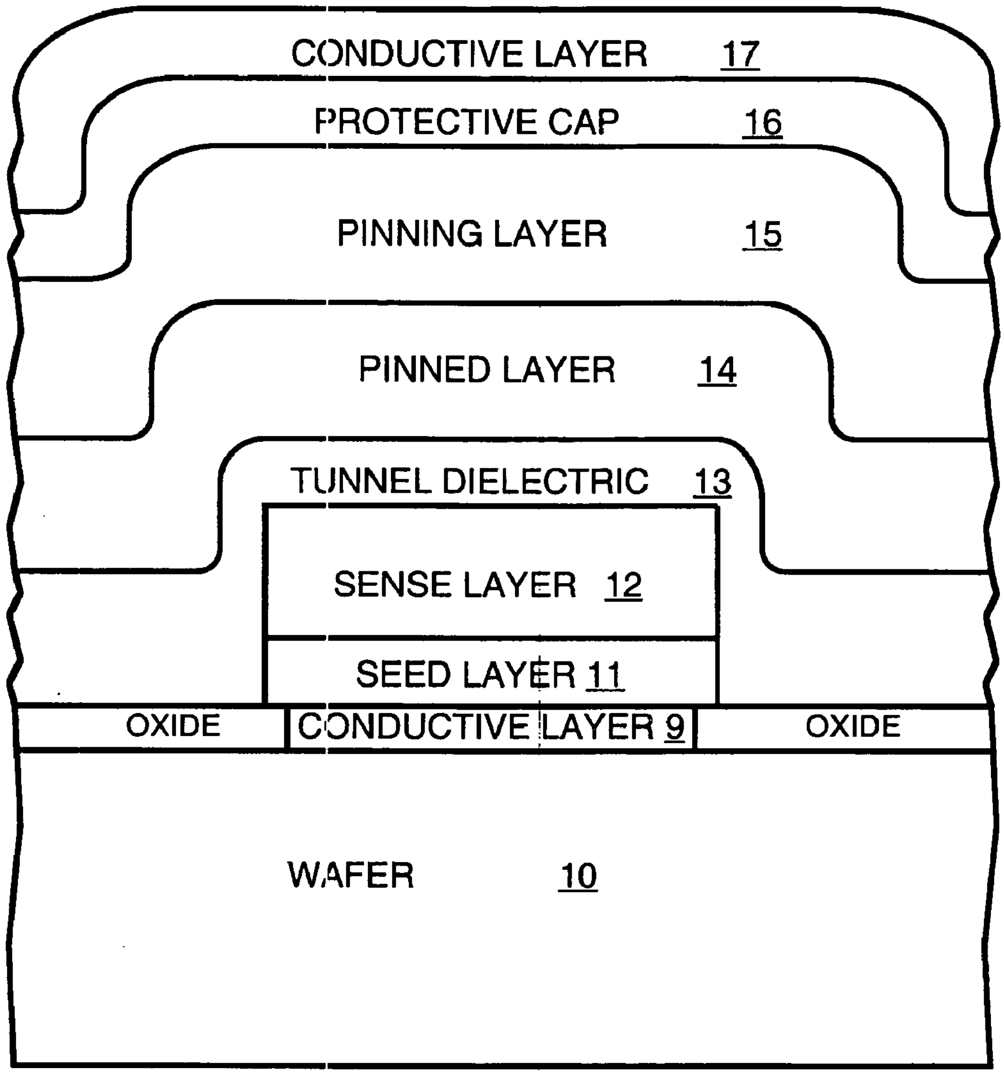

CONDUCTIVE LAYER 17
PROTECTIVE CAP 16
PINNING LAYER 15
PINNED LAYER 14
TUNNEL DIELECTRIC 13
SENSE LAYER 12
SEED LAYER 11
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER 10

FIGURE 5

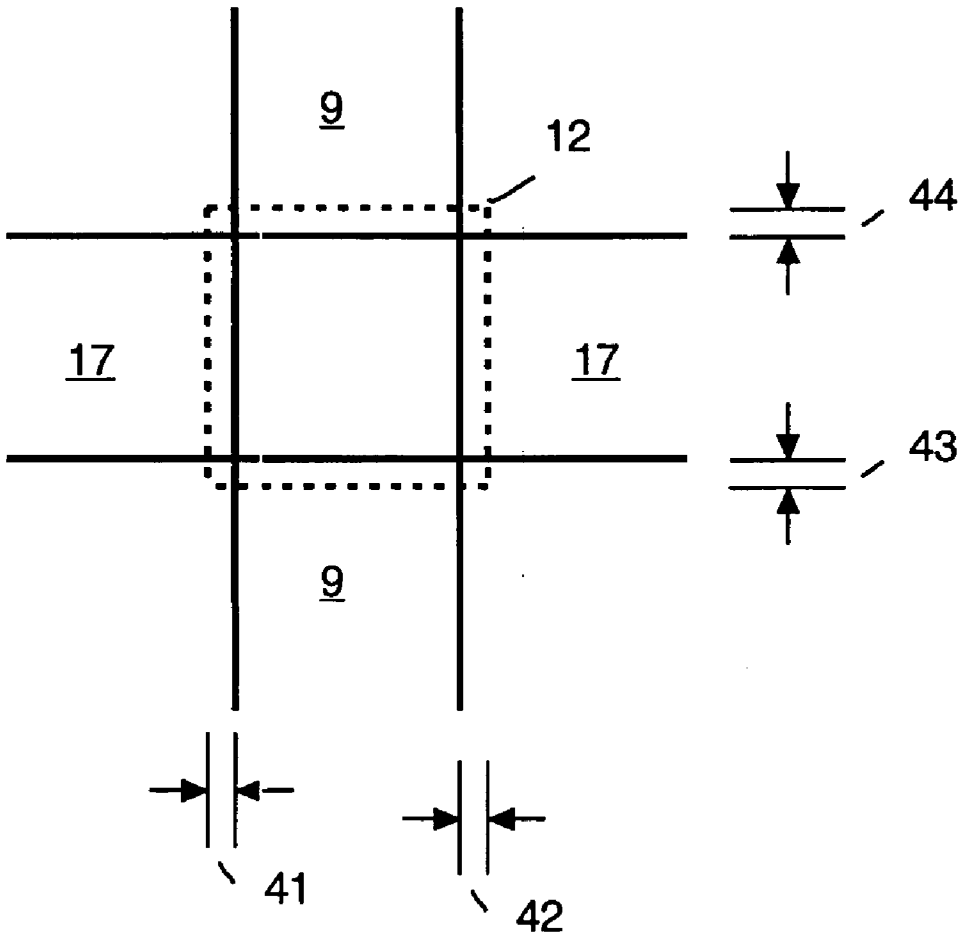


FIGURE 6

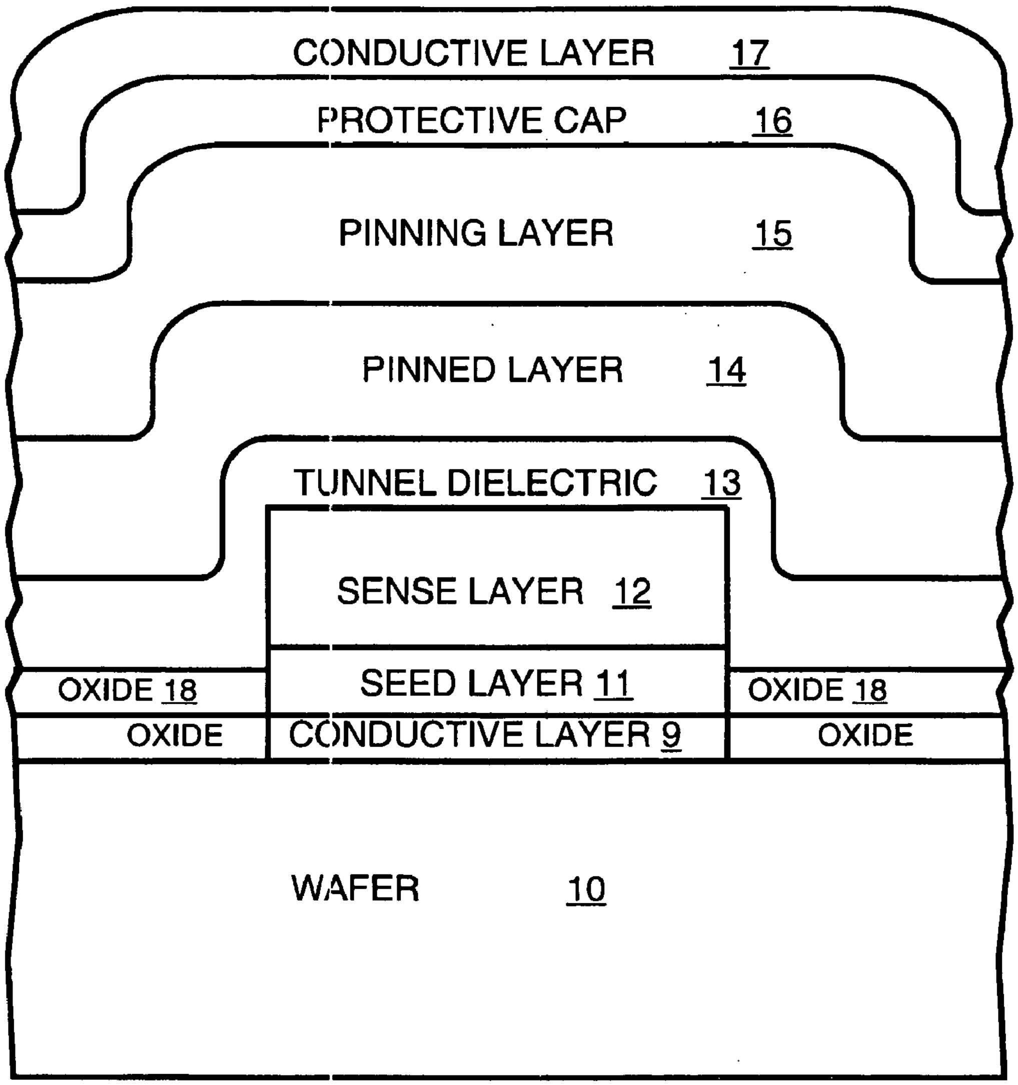

CONDUCTIVE LAYER 17
PROTECTIVE CAP 16
PINNING LAYER 15
PINNED LAYER 14
TUNNEL DIELECTRIC 13
SENSE LAYER 12
OXIDE 18
SEED LAYER 11
OXIDE 18
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER 10

FIGURE 7

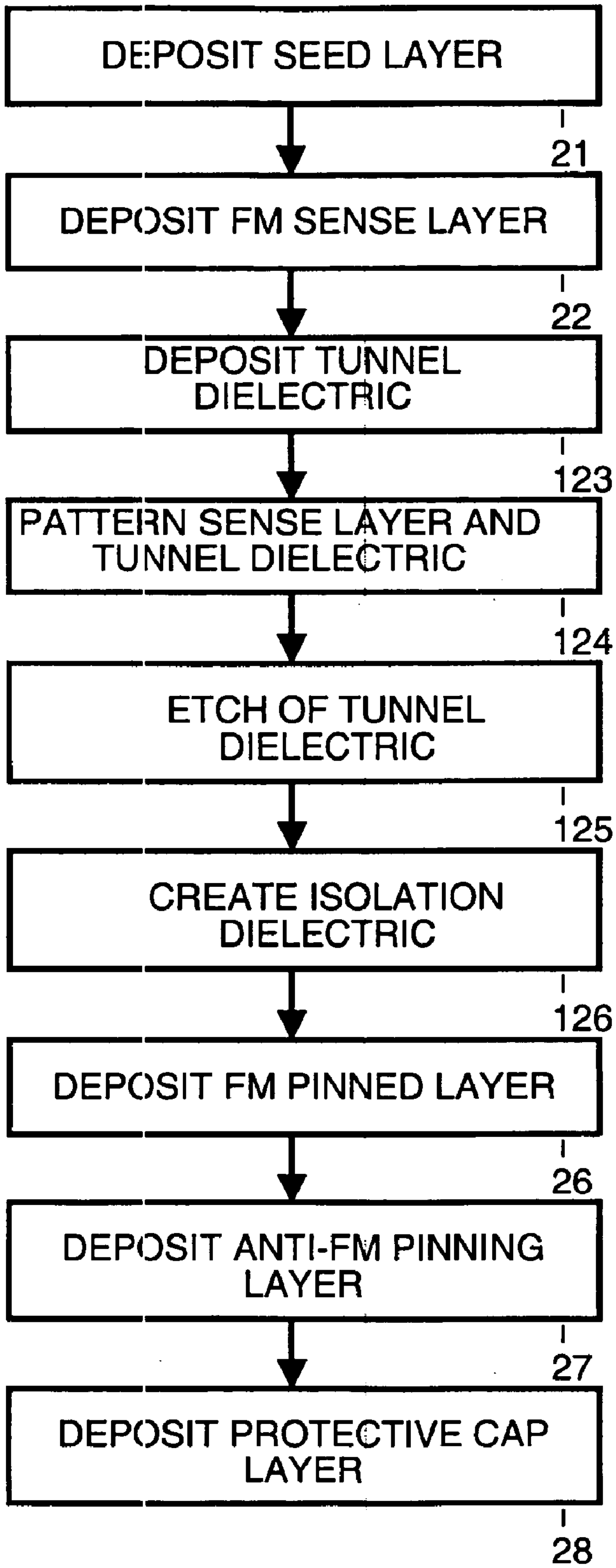

DEPOSIT SEED LAYER
21
DEPOSIT FM SENSE LAYER
22
DEPOSIT TUNNEL DIELECTRIC
123
PATTERN SENSE LAYER AND TUNNEL DIELECTRIC
124
ETCH OF TUNNEL DIELECTRIC
125
CREATE ISOLATION DIELECTRIC
126
DEPOSIT FM PINNED LAYER
26
DEPOSIT ANTI-FM PINNING LAYER
27
DEPOSIT PROTECTIVE CAP LAYER
28

FIGURE 8

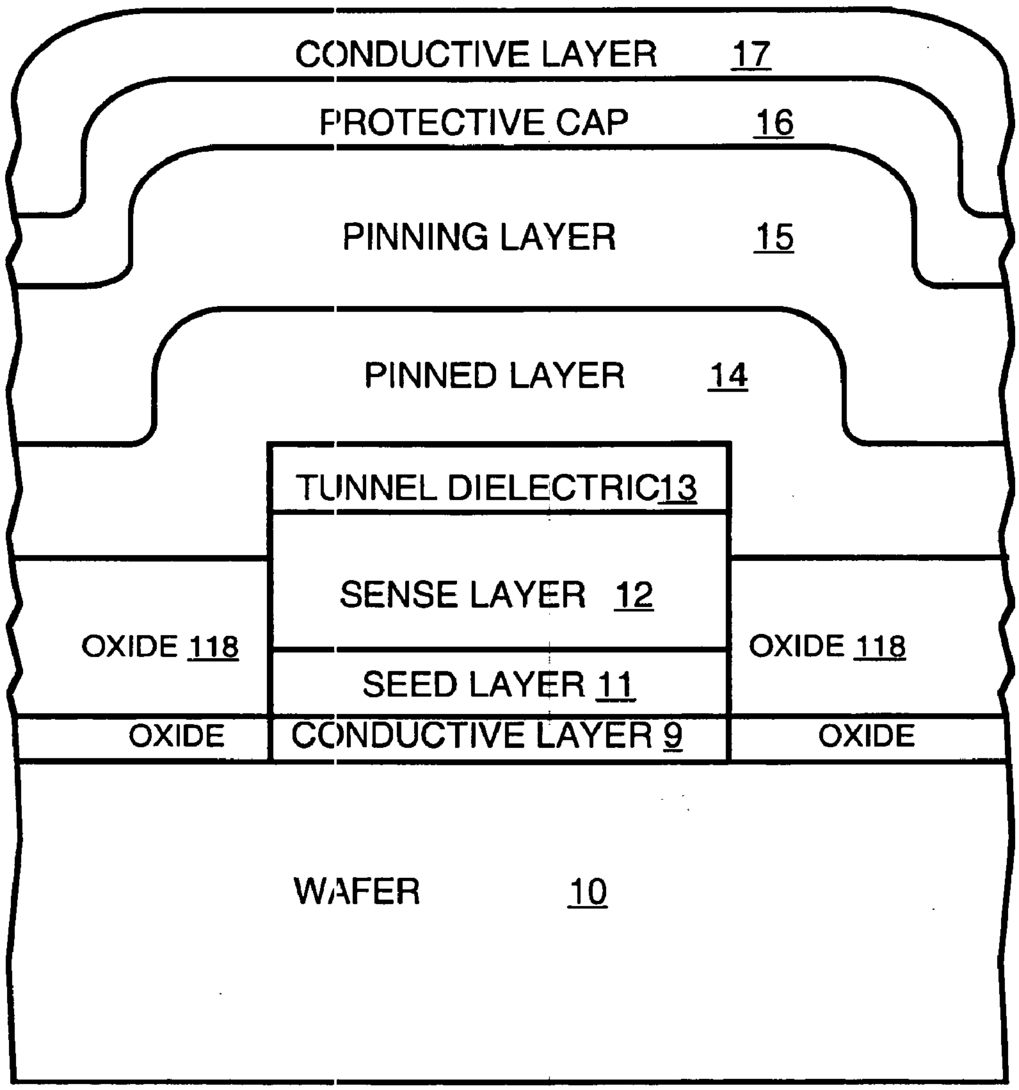

CONDUCTIVE LAYER 17
PROTECTIVE CAP 16
PINNING LAYER 15
PINNED LAYER 14
TUNNEL DIELECTRIC 13
SENSE LAYER 12
OXIDE 118
OXIDE 118
SEED LAYER 11
OXIDE
CONDUCTIVE LAYER 9
OXIDE
WAFER 10

FIGURE 9

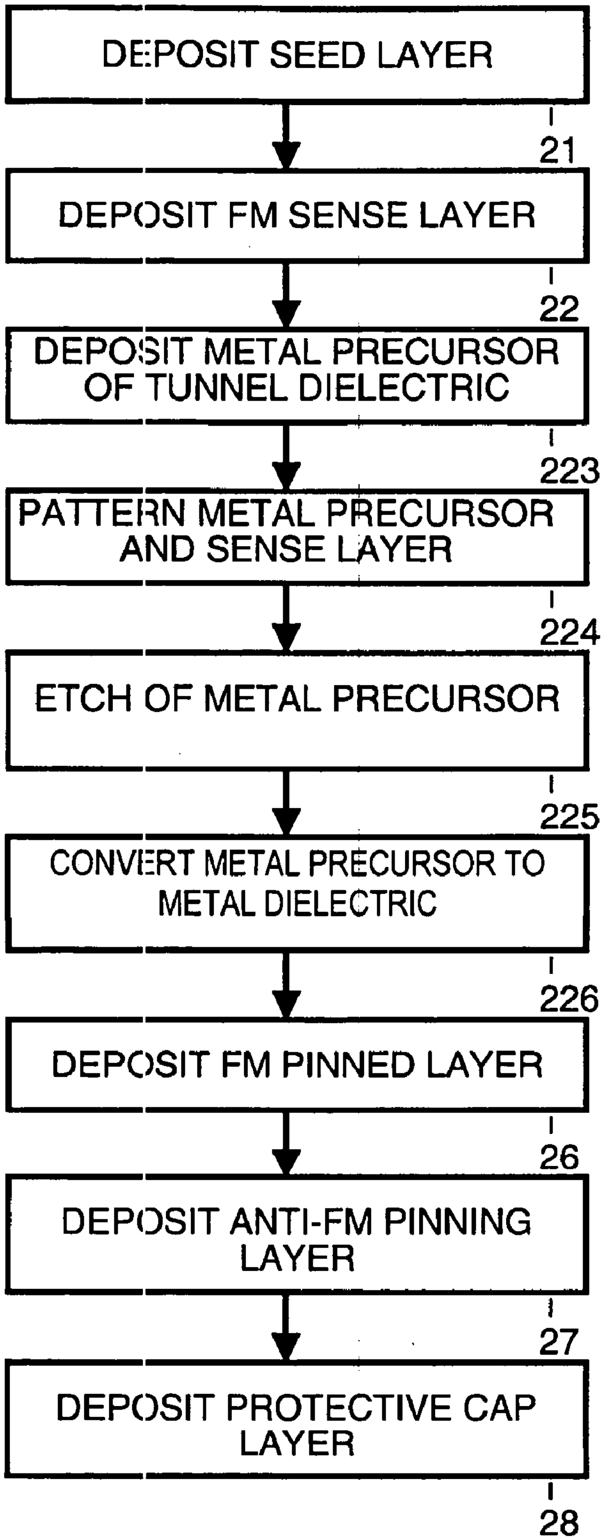

DEPOSIT SEED LAYER
21
DEPOSIT FM SENSE LAYER
22
DEPOSIT METAL PRECURSOR OF TUNNEL DIELECTRIC
223
PATTERN METAL PRECURSOR AND SENSE LAYER
224
ETCH OF METAL PRECURSOR
225
CONVERT METAL PRECURSOR TO METAL DIELECTRIC
226
DEPOSIT FM PINNED LAYER
26
DEPOSIT ANTI-FM PINNING LAYER
27
DEPOSIT PROTECTIVE CAP LAYER
28

FIGURE 10

METHOD FOR CONSTRUCTING A MAGNETO-RESISTIVE ELEMENT

BACKGROUND

[0001] A magnetic random access memory (MRAM) is a solid-state non-volatile magnetic storage device. Bits of data are stored in small magneto-resistive elements. For example, in a magnetic tunnel junction (MTJ) magneto-resistive element, two ferromagnetic layers, a pinned magnetic layer and a sense magnetic layer, are separated by an insulating tunnel barrier. Magnetoresistance results from the spin-polarized tunneling of conduction electrons between the ferromagnetic layers. The tunneling current depends on the relative orientation of the magnetic moments of the two ferromagnetic layers.

[0002] The magnetization orientation of the sense layer is used for information storage. The resistance is either low or high, depending on the relative orientation of sense magnetic layer with respect to the pinned magnetic layer. The orientation is either parallel (P) or antiparallel (AP).

[0003] In an MRAM array, orthogonal lines pass under and over the magneto-resistive elements, carrying current that produces switching fields. The magneto-resistive elements are designed so that the magnetization of the sense magnetic layer will not switch when current is applied to just one line, but will switch when current is applied to both lines. A magneto-resistive element is manufactured using series of layers of material stacked on top of one another. A pinned layer can be either on the bottom or top of the tunnel junction layer. The sense layer is required to be patterned in two dimensions in order to define a discrete bit. When the pinned layer is on the bottom, the pinned layer can be defined in two dimensions (i.e., is "patterned") or can be defined along one dimension (i.e., is "unpatterned"). What is meant by "unpatterned" is that the pinned layer is defined in only one dimension and not defined in the other dimension so that the resulting structure is a line. When the pinned layer is patterned, it is typically patterned at the point in the manufacturing process when the sense layer is patterned. When the pinned layer is to remain unpatterned, the sense layer is patterned and the patterning process is controlled so that the pinned layer is not patterned by the sense layer patterning process.

[0004] If the pinned layer is patterned, it contributes to the magnetic state of the sense layer. This magnetic contribution is often referred to as the "demagnetization field". This demagnetization field needs to either be eliminated or tightly controlled.

[0005] The pinned layer is generally composed of a set of several material layers that have some lattice mismatch. Strain relaxation and the resultant columnar grain growth creates morphological roughness. This roughness contributes to the magnetic state of the sense layer. This contribution is sometimes referred to as the "coupling field" or "Ne'el coupling". The coupling field also needs to be either eliminated or tightly controlled.

[0006] One solution to reduce the coupling field is to put the sense layer on the bottom of the stack, thereby reducing the Ne'el coupling due to the roughness of the pinned stack. In this case, the pinned layer is patterned in order to perform patterning of the sense layer. As discussed above, the patterned pinned layer will then contribute to the demagnetization field.

[0007] Additionally, when the pinned layer is patterned, the sense layer of the completed magneto-resistive element will switch polarity using different mechanisms. When the sense layer switches from P to AP (low resistance to high resistance state switching), the predominant mechanism is the growth of end domains. When the sense layer switches from AP to P (high resistance to low resistance state switching), the mechanism used is the growth of a domain from somewhere in the middle of the sense layer. The AP to P switching has an unstable nucleation mechanism due to probabilistic switching nucleated by surface irregularities and/or roughness. This unpredictable nucleation mechanism in a patterned pinned layer junction causes variations in the switching field over many bits and also for multiple cycling of the same bit.

[0008] A magneto-resistive element with an unpatterned pinned layer always switches by the same mechanism. Thus, the switching of a magneto-resistive element that has a patterned pinned layer has an increased switching distribution relative to a magneto-resistive element that has an unpatterned pinned layer.

SUMMARY OF THE INVENTION

[0009] In accordance with the preferred embodiment of the present invention a magneto-resistive element is constructed. A ferromagnetic sense layer is deposited on a surface. The ferromagnetic sense layer is patterned. An ion etch is performed in preparation for depositing a dielectric layer. The dielectric layer is deposited over the sense layer. A ferromagnetic pinned layer is deposited over the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] **FIG. 1** is a flowchart that describes construction of a magneto-resistive element in accordance with a preferred embodiment of the present invention.

[0011] **FIG. 2**, **FIG. 3**, **FIG. 4**, **FIG. 5** and **FIG. 6** illustrate construction of the magneto-resistive element in accordance with the preferred embodiment of the present invention.

[0012] **FIG. 7** illustrates construction of the magneto-resistive element in accordance with an alternative preferred embodiment of the present invention.

[0013] **FIG. 8** is a flowchart that describes construction of a magneto-resistive element in accordance with another alternative preferred embodiment of the present invention.

[0014] **FIG. 9** illustrates construction of the magneto-resistive element in accordance with another alternative preferred embodiment of the present invention.

[0015] **FIG. 10** is a flowchart that describes construction of a magneto-resistive element in accordance with another alternative preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] **FIG. 1** is a flowchart that describes construction of a magneto-resistive element. In a processing step **20**, a conductive layer **9** (shown in **FIG. 2**) is formed. For example, conductive layer **9** is formed using a damascene process. In a processing step **21**, a seed layer **11** (Shown in

FIG. 2) is deposited on a conductive layer **9** on a top surface of wafer **10**. For example, seed layer **11** is typically in the range of 2 nanometers (nm) to 5 nm thick and composed of tantalum (Ta), copper (Cu) ruthenium (Ru), tantalum nitride (TaN), titanium (Ti), platinum (Pt) or some other suitable material. Although shown as two distinct layers, it is possible for conductive layer **9** and seed layer **11** to be combined in a single layer.

[**0017**] In a processing step **22**, a ferromagnetic (FM) sense layer **12** (shown in **FIG. 2**) is deposited. FM sense layer **12** is composed of cobalt (Co), iron (Fe), nickel (Ni), an alloy containing one of the aforementioned elements, or some other suitable material. The result is shown in **FIG. 2** where seed layer **11** and FM sense layer **12** are shown deposited on conductive layer **9** on a top surface of wafer **10**.

[**0018**] In processing step **22**, the FM material deposited for sense layer **12** is intentionally deposited thicker than the desired thickness. For example, the desired final thickness of FM sense layer **12** is 3 nm to 6 nm, but the deposited thickness is 5 nm to 10 nm.

[**0019**] In alternative embodiment, FM sense layer **12** consists of two FM materials, the second having a high spin polarization, so as to give a high signal. For example, the first FM material is composed of NiFe and the second FM material is composed of CoFe. For example, the first FM material is deposited to a thickness of 3 nm, and the second FM material is deposited to a thickness of 3 nm which is etched back to 1 nm.

[**0020**] Alternatively, in step **22**, FM sense layer **12** can consist of a synthetic ferrimagnet (SF), also called an artificial anti-ferromagnet (AAF). An SF is typically composed of two ferromagnetic films FM**1** and FM**2** separated by a thin non-magnetic layer where the thickness of the non-magnetic layer is such that the ferromagnetic films are coupled very strongly with their magnetic moments in opposite directions. The non-magnetic layer is typically ruthenium (Ru), rhodium (Rh), silicon (Si) or other suitable material. The thickness of the two ferromagnetic films FM**1** and FM**2** are different, such that the SF has a net magnetic moment that interacts with an applied field.

[**0021**] In a processing step **23**, FM sense layer **12** and seed layer **11** are patterned, for example, by lithographic and etch processes. The result is shown in **FIG. 3** where FM sense layer **12** and seed layer **11** are shown having been patterned. To perform the patterning, wafer **10** is removed from the deposition chamber, typically requiring breaking vacuum. However, breaking vacuum between layer depositions can degrade the quality of subsequent layers due to the formation of native oxide or incorporation of contaminants, defects and impurities. Magnetic tunnel junctions are known to be sensitive to the cleanliness of the interfaces between ferromagnetic and dielectric films in the structure. In the preferred embodiment, the sense layer **12** is patterned slightly larger (in one dimension) than the underlying conductor **9**.

[**0022**] Once returned to the deposition chamber, in a processing step **24**, an etch is performed on sense layer **12** to remove defects and impurities and to achieve the final thickness of 1 nm to 6 nm. For example, the etch can be an ion etch, or some other type of etch, such as neutral atom sputter etch. The thickness of material to be etched back is chosen such that etching the material removes any native oxide or contaminants, and produces a smooth layer. The etch process also smoothes the surface of FM sense layer **12** with the result that the remaining portion of FM sense layer **12** is in a pristine condition, ready for deposition of the remaining materials stack. The result is shown in **FIG. 4**.

[**0023**] In a processing step **25**, a tunnel dielectric **13** (shown in **FIG. 5**) is formed. For example, tunnel dielectric **13** is typically 1 nm to 2 nm thick and composed of aluminum oxide (Al_2O_3), aluminum nitride (AlN), boron nitride (BN), or some other suitable material. Tunnel dielectric **13** can be formed by direct deposition of the insulating material, or by depositing a precursor metal, such as Al, and converting it into a dielectric by chemical reaction. An example of a metallic layer converted is conversion of metallic Al to dielectric Al_2O_3 by reaction of Al with oxygen. Typically, reaction enhancing processes such as generating a plasma, or heating the substrate are employed. Tunnel dielectric **13** coats all exposed surfaces, including sidewalls, of sense layer **12**.

[**0024**] In a processing step **26**, an FM pinned layer **14** (shown in **FIG. 5**) is deposited. For example, pinned layer **14** is 1 nm to 6 nm thick and composed of cobalt (Co), iron (Fe), nickel (Ni), an alloy containing one of the aforementioned elements or some other suitable material.

[**0025**] Alternatively, in step **26**, FM pinned layer **14** can consist of a ferrimagnet (SF). An SF is typically composed of two ferromagnetic films separated by a thin non-magnetic spacer-layer where the thickness of the non-magnetic layer is such that the ferromagnetic films are coupled very strongly with their magnetic moments in opposite directions. The non-magnetic layer is typically ruthenium (Ru) rhodium (Rh), silicon (Si) or other suitable material. Generally, for use in the pinned layer, the two FM films are slightly different thicknesses.

[**0026**] In a processing step **27**, an antiferromagnetic pinning layer **15** (shown in **FIG. 5**) is deposited. For example, pinning layer **15** is 7 nm to 10 nm thick and composed of iridium manganese (IrMn), iron manganese (FeMn), platinum manganese (PtMn) or some other suitable material.

[**0027**] In a processing step **28**, a protective cap layer **16** (shown in **FIG. 5**) is deposited. For example, protective cap layer **16** is approximately 5 nm thick and composed of tantalum (Ta), ruthenium (Ru), tantalum nitride (TaN), titanium (Ti), platinum (Pt) or some other suitable material. Often protective cap layer **16** is composed of the same material as seed layer **21**.

[**0028**] In a processing step **29**, a conductive layer **17** is formed. This is done, for example, by depositing and patterning a conductive material. Typically, pinned layer **14**, pining layer **15** and protective cap **16** are patterned along with the conductive material. The result is shown in **FIG. 5** and **FIG. 6**.

[**0029**] **FIG. 6** shows a top view of the intersection of conductive layer **9** and conductive layer **17**. The patterned geometry of pinned layer **14**, pining layer **15** and protective cap **16** is the same as conductive layer **17**. The geometry of sense layer **12** is shown by a dotted line. As can be seen by the dotted line, sense layer **12** overlaps conductor **17** by a distance **41** and a distance **42**. Sense layer **12** overlaps conductor **9** by a distance **43** and a distance **44**.

[0030] When implementing the process steps shown in **FIG. 1**, it is desirable to minimize electrical conduction between pinned layer **14** and conductive layer **9** (or seed layer **11** if there is no separate conductive layer). One way to minimize conduction is to constrain the geometry of the magnetic tunnel junction so that there is no overlap of pinned layer **14** and conductive layer **9**, as shown in **FIG. 6**.

[0031] Geometric isolation is the simplest method to prevent unwanted electrical conduction, but there are other methods. For example, an additional isolation dielectric layer can be inserted between conductive layer **9** and pinned layer **14** in regions of potential overlap. The additional isolation dielectric layer can be, for example, a deposited film or a portion of a metallic layer converted by chemical reaction. An example of a metallic layer converted by chemical reaction is conversion of metallic Ta to dielectric Ta_2O_5 by reaction of Ta with oxygen. Increasing the thickness of the additional isolation dielectric layer over the conductive layer **9** permits overlap of pinned layer **14** and first conductive layer **9**. Tunneling current across an insulator drops exponentially with increasing insulator thickness, so a very small increase in thickness is sufficient to block conduction between the metal layers.

[0032] For example, in an alternative embodiment, sense layer **12** does not overlap conductor **9** or conductor layer **17**. In this embodiment, an additional oxide deposition or a spacer process after sense layer is patterned in processing step **23**. As discussed above, this is necessary because it is not sufficient to have pinned layer **14** separated from conductive layer **9** only by tunnel dielectric **13**. As shown in **FIG. 7** an additional oxide deposition performed after sense layer results in oxide regions **18** isolating conductive layer **9** from tunnel dielectric **13**. In this embodiment, conductive layer **9** and seed layer **11** can be implemented as a single layer (i.e., the conductive layer also acts as the seed layer).

[0033] **FIG. 8** illustrates an alternative embodiment of the present invention. In the alternative embodiment, processing step **21** and processing step **22** are performed as described above, except however, in processing step **22**, the FM material deposited for FM sense layer **12** is deposited at approximately the desired thickness. In a processing step **123**, tunnel dielectric **13** is deposited over sense layer **12** before patterning is performed. In a step **124**, tunnel dielectric **13** and sense layer **12** are patterned. In step **123**, tunnel dielectric **13** is deposited to greater than the required thickness. Once the wafer is returned to the deposition chamber after patterning, in a step **125**, an etch is performed to remove defects and impurities from tunnel dielectric **13** and to achieve the required thickness of tunnel dielectric **13**. For example, the etch can be an ion etch, or some other type of etch, such as neutral atom sputter etch. In a processing step **126**, isolation dielectric regions **118** are formed, for example, by deposition or oxidation of seed layer **11**. Processing steps **26**, **27** and **28** are then performed, as described above. In another alternative embodiment, in processing step **123**, tunnel dielectric **13** is deposited to the desired thickness and processing step **125** is skipped. The result is shown in **FIG. 9**.

[0034] **FIG. 10** illustrates an alternative embodiment of the present invention. In the alternative embodiment, processing step **21** and processing step **22** are performed as described above, except however, in processing step **22**, the FM material deposited for FM sense layer **12** is deposited at approximately the desired thickness. In a processing step **223**, a metal precursor to tunnel dielectric **13** is deposited over sense layer **12** before patterning is performed. In step **223**, metal precursor of tunnel dielectric **13** is deposited to greater than the required thickness. In a step **224**, metal precursor of tunnel dielectric **13** and sense layer **12** are patterned. Once the wafer is returned to the deposition chamber after patterning, in a step **225**, an etch is performed to remove defects and impurities from metal precursor of tunnel dielectric **13** and to achieve the required thickness of metal precursor to tunnel dielectric **13**. For example, the etch can be an ion etch, or some other type of etch, such as neutral atom sputter etch. In process step **226**, the metal precursor tunnel dielectric **13** is converted into a dielectric by chemical reaction. An example is conversion of metallic Al to dielectric Al_2O_3 by reaction of Al with oxygen. Typically, reaction enhancing processes such as generating a plasma, or heating the substrate are employed. Processing steps **26**, **27** and **28** are then performed, as described above.

[0035] The disclosed embodiments of the present invention result in improvement both to the switching distribution and magnetic coupling properties of the magnetic tunnel junction. The disclosed embodiments of the present invention also provide a way to pattern sense layer **12** without having to pattern pinned layer **14**. The disclosed embodiments of the present invention provide a simplified manufacturing process and produce a simplified structure for an MRAM element.

[0036] The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosure is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

1. (canceled)
2. (canceled)
3. (canceled)
4. (canceled)
5. (canceled)
6. (canceled)
7. (canceled)
8. (canceled)
9. (canceled)
10. (canceled)
11. (canceled)
12. (canceled)
13. (canceled)

14. A method for constructing a magneto-resistive element, the method comprising the followings:

(a) depositing a ferromagnetic sense layer on a surface;

(b) forming a dielectric layer over the ferromagnetic sense layer;

(c) patterning the dielectric layer and ferromagnetic sense layer;

(d) forming isolation dielectric regions on sides of the patterned ferromagnetic sense layer;

(e) performing an etch of the dielectric layer; and, (f) depositing a ferromagnetic pinned layer over the patterned dielectric layer and the isolation dielectric regions.

15. (canceled)

16. A magnetic random access memory comprising:

an array of magneto-resistive elements, each magneto-resistive element including:

a patterned ferromagnetic sense layer deposited on a surface;

a dielectric layer deposited over the sense layer; and,

a ferromagnetic pinned layer deposited over the dielectric layer, wherein the ferromagnetic pinned layer is unpatterned.

17. A magnetic random access memory as in claim 16 wherein each magneto-resistive element additionally includes:

an antiferromagnetic pinning layer deposited over the ferromagnetic pinned layer.

18. A magnetic random access memory as in claim 16 wherein each magneto-resistive element additionally includes:

an antiferromagnetic pinning layer deposited over the ferromagnetic pinned layer; and,

a protective cap layer deposited over the antiferromagnetic pinning layer.

19. A magnetic random access memory as in claim 16 wherein the ferromagnetic pinned layer is a synthetic ferrimagnet.

20. (canceled)

21. (canceled)

22. (canceled)

23. (canceled)

24. (canceled)

25. (canceled)

26. (canceled)

27. (canceled)

28. (canceled)

29. (canceled)

30. (canceled)

31. (canceled)

32. (canceled)

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