United States Patent [19]

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[11] **3,814,937**

[45] **June 4, 1974**

[54] **PULSE PILE-UP REJECTOR WITH LIVE-TIME CORRECTOR CIRCUIT**

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[22] Filed: **Apr. 24, 1972**

[21] Appl. No.: **246,819**

[52] **U.S. Cl.** **250/336,** 250/374

[51] **Int. Cl.** **G01t 1/00**

[58] **Field of Search** ..... 250/83.6 R, 336, 374

[56] **References Cited**

UNITED STATES PATENTS

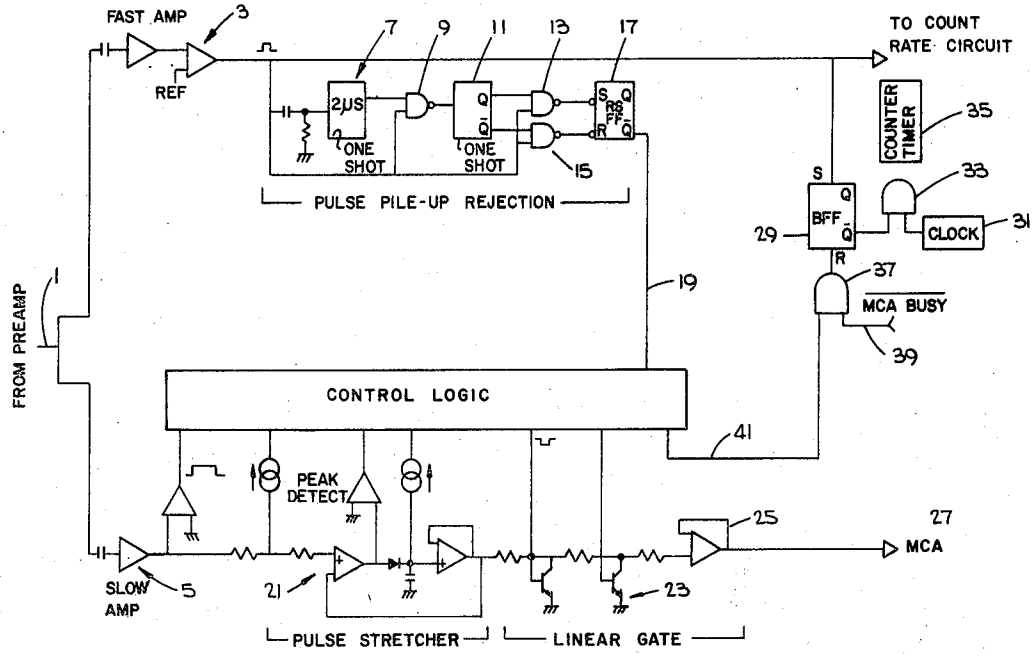
3,037,118	5/1962	Bryant	250/83.6 R
3,382,365	5/1968	Lacour et al.	250/83.6 R
3,573,639	4/1971	Metz et al.	250/83.6 R X

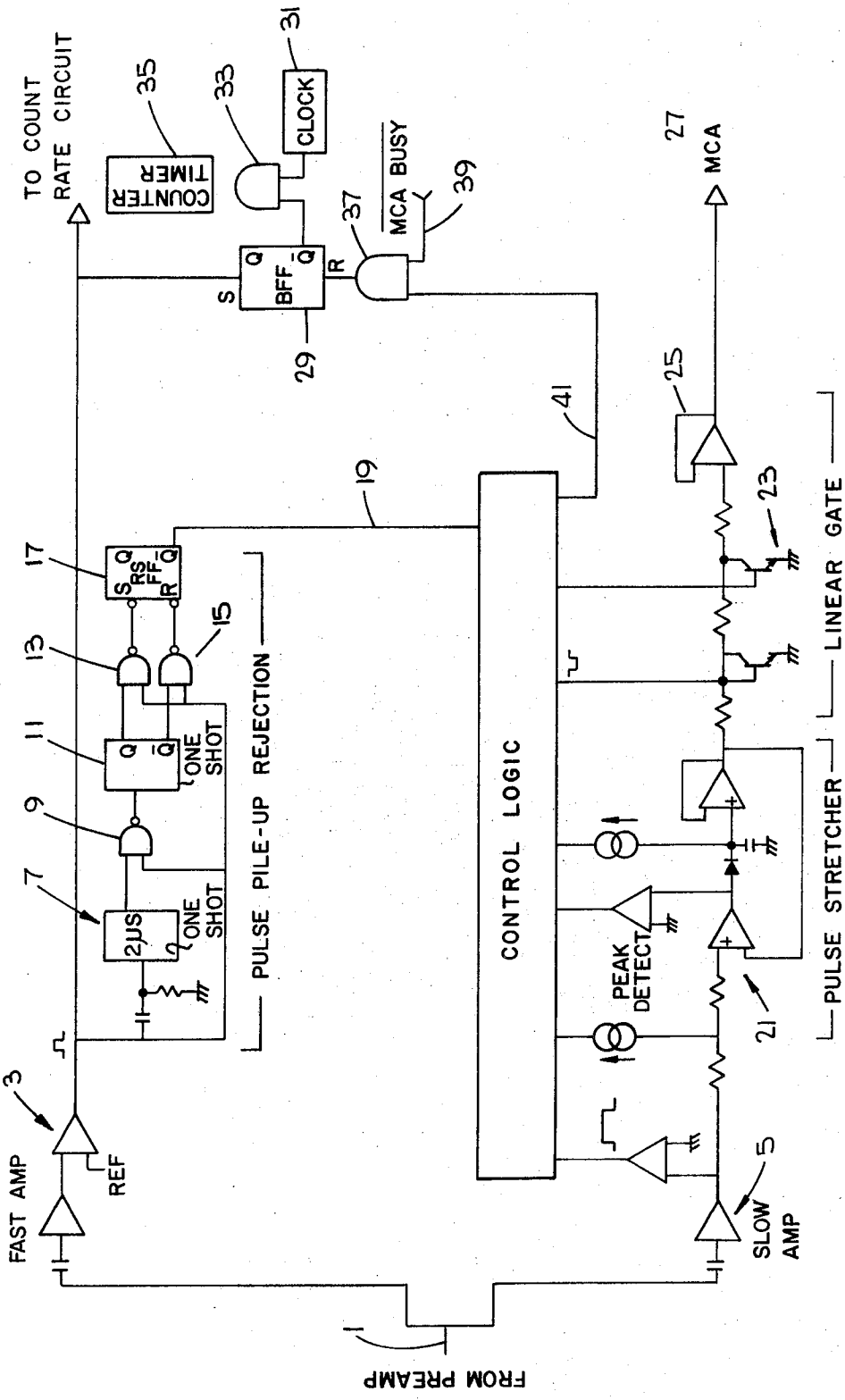
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[57] **ABSTRACT**

A live-time corrector circuit is provided in an x-ray counting device wherein the dead time of the analyzer device as well as dead time caused by overlapping events are compensated for by extending the counting time.

2 Claims, 1 Drawing Figure




TO COUNT RATE CIRCUIT
COUNTER TIMER
35
33
CLOCK
31
MCA BUSY
39
37
BFF
29
27
MCA
25
41
19
23
17
RS FF
15
13
11
ONE SHOT
9
7
2μS ONE SHOT
PULSE PILE-UP REJECTION
CONTROL LOGIC
LINEAR GATE
PULSE STRETCHER
PEAK DETECT
21
3
FAST AMP
REF
5
SLOW AMP
FROM PREAMP
1

PULSE PILE-UP REJECTOR WITH LIVE-TIME CORRECTOR CIRCUIT

SUMMARY OF THE INVENTION

In the analysis of x-ray events by electronic instrumentation, a detector and its associated circuitry are looking for x-ray events which occur randomly in time. Modern high resolution x-ray energy analysis units require that the amplifier must be set for a time constant of 5 or 6 microseconds. Since the number of expected counts may run into the thousands of counts per second, the long duration of the resultant pulses greatly increases the chance of pile-ups, resulting in the data recorded in the pulse height analyzer being stored in the incorrect channel, thus reducing the height of peaks and increasing the general background noise. In other words, when an event occurs, a finite time is required to process the signal and, if during this time a subsequent event occurs, the two signals tend to add or be superimposed on each other. This creates a false signal whose value does not correlate with either of the component signals and which must be disregarded in the analysis. Many electronic schemes have been suggested to prevent the analysis of erroneous signals and the generic term "pulse pile-up rejection circuitry" is common in the industry. The usual process is to examine the events in two channels, one a fast channel which barely detects the occurance of the event and the other a slower channel which may properly process and analyze the signal. In such circuits if a second event occurs during the time when the first event is being processed, the rejection circuitry rejects both signals. Further, during the analysis period in a multiple channel analyzer, no new signals can be accepted for processing. Both of these situations, i.e., two signals arriving so close together than one distorts the other or a second signal arriving while the first signal is being processed, result in dead time.

It is normally desirable to determine the activity of certain events during a definite time period and these results will vary as the live-time to dead time ratio changes. If the system is dead half the time, obviously only about half of the events occuring during the run are being processed.

In accordance with the present invention, this situation is corrected by inhibiting the clock which governs the counting time during the dead time period. In other words, if one wishes to analyze the events of a period such as one minute and the system is dead half the time, the real running time will be two minutes and during this period the actual count is taking place for one minute.

BRIEF DESCRIPTION OF THE DRAWINGS

The sole FIGURE of the drawing is a schematic diagram of an apparatus embodying the present invention.

DESCRIPTION OF THE PREFERRRED EMBODIMENT

Referring now to the drawing by reference characters, each time an x-ray event occurs in the detector (not illustrated) the preamp puts out a signal through line 1 which is passed to both a fast amplifier, generally designated 3, and a slow amplifier generally designated 5. The fast amplifier 3 and its associated capacitor differentiate the signal with a short time constant (suitably 200 ns) and it is then fed to a one-shot multivibrator 7 which puts out a constant amplitude pulse of approximately 1 to 2 microseconds each time an event occurs. The output from the fast discriminator is fed to an NAND gate 9, the output of which is fed to a second one-shot multivibrator 11 having Q and $\bar{Q}$ outputs which are fed to the NAND gates 13 and 15. The time constant of multivibrator 11 is selected to match the full pulse width of the quasi-Gaussian shaped main linear pulse for any particular shaping time-constant and is suitably 10 times the slow amplifier time constant. The output from the NAND gates 13 and 15 is then fed to the set and reset gates respectively of the flip-flop 17. Output is taken from flip-flop 17 from the $\bar{Q}$ output through line 19 and served to actuate the linear gate, later described. It will be seen that enable line 19 will be actuated by a pulse from the fast discriminator unless it is inhibited by a pulse from the one-shot multivibrator 11. Should a second pulse occur during the off-time of 11, no enabling pulse will be sent through line 19. In other words, if the pulses are sufficiently far apart that they can be properly processed, enable line 19 will be activated, while if two pulses occur too close together to be properly processed, line 19 will not be activated.

As was previously mentioned, the signal from the preamplifier at 1 is split in two parts and the second portion goes to the slow or main amplifier 5. The latter will now be described. In the slow amplifier 5 and the pulse stretcher, generally designated 21, the pulse is amplified and stretched to 2 microseconds and the peak of the signal is detected. The peak signal is then passed to the linear gate generally designated 23 and, if the gate is opened by a pulse through line 19, is passed through voltage follower 25 into a multichannel analyzer 27. The exact method of stretching the pulse, detecting the peak and analyzing it in the analyzer 27 is known to those skilled in the art and therefore has not been described in detail.

Each time an event occurs the fast amplifier pulse is also fed to the set terminal of flip-flop 29. The apparatus is provided with a clock oscillator 31 and the output from the clock oscillator and the $\bar{Q}$ output from flip-flop 29 are fed to AND gate 33. The output from AND gate 33 goes to a counter-timer 35 where the number of clock pulses is counted and the operation cut off after the desired time interval. Thus, as a pulse is received at the S terminal of flip-flop 29, the output of the clock 31 is shut off since AND gate 33 is connected to the $\bar{Q}$ output of flip-flop 29.

A second AND gate 37 has its output connected to the reset terminal of slip-flop 29 and one of the inputs of AND gate 37 is connected through line 39 to the multichannel analyzer which puts out a pulse if the analyzer is not busy processing a signal. The other input to AND gate 37 is through line 41 and everytime the linear gate 23 is opened to the analyzer 27, line 41 is pulsed. This will operate the reset of flip-flop 29 providing that the multichannel analyzer is not busy and has put out a signal through line 39. This gives a $\bar{Q}$ output on flip-flop 29 so that the clock pulses 31 are fed into the counter-timer 35.

The overall operation of the circuit will now be apparent. Each time a pulse is received, flip-flop 29 will go to the set condition and the live-time counter 35 will be turned off. Simultaneously the pulse will be pro-

cessed through the slow amplifier side of the circuit and the linear gate **23** will be opened by a pulse from line **19** unless two pulses occur close together. When the gate **23** is opened, the pulse is sent to the multichannel analyzer **27** for processing and, if the analyzer is not busy, an output pulse from line **39** will be added to that of line **41,** resetting flip-flop **29,** causing the clock pulses to be accumulated in **35.**

The design philosophy of this circuit is extremely simple. For a given count rate, the average period between event is

$$T=\frac{1}{n}\sum_{i=1}^{n} T_i = 1/\text{count rate}$$

where T_i is the actual time between events i and $i+1$. Therefore, although T_i varies from event to event, the statistical average over a long period of time is given by the inverse of the count rate. In operation, the live-time counter **35** is enabled only if an event is stored in the analyzer and is again disabled at the next event. If the next event is also stored, the clock is again enabled for one event period, T_i. Therefore, for each event stored, the clock runs for a period T_i. If the count rate is 5,000 counts per second, then $T = 1/5{,}000$ seconds. If a live-time of 100 seconds is desired, there will be 500,000 counts stored on the average but the actual real time required to accumulate these counts will be

$$100 \times [100/100 - \% \text{ dead time}].$$

It will be obvious to those skilled in the art that many variations can be made without departing from the spirit of this invention.

I claim:

1. In an analyzer for x-ray events wherein the amplitude and number of events are recorded in a multichannel analyzer and said events may occur at a rate faster than the events can be processed by said multichannel analyzer, because said analyzer exhibits dead time during processing, the improvement comprising:

a. an input circuit from the pre-amplifier of an x-ray event detector providing a series of pulses,

b. means for dividing the pulses from said input circuit into two parallel paths,

c. the first of said paths being a fast channel which detects pulses,

d. the second of said paths being a slow channel to said multichannel analyzer which processes and gates pulses,

e. a live-time clock for determining the live time period during which a series of counts is made,

f. means whereby said fast circuit actuates a pulse pile-up rejection circuit having means which stops said live-time clock when two pulses are in such close proximity that they cannot be analyzed by said multichannel analyzer, and

g. a second circuit actuated by said multichannel analyzer which shuts off said live-time clock when said multichannel analyzer is busy.

2. The analyzer of claim **1** including the following structure:

a. a pulse pile-up rejection circuit in said fast channel, said circuit having means for opening a linear gate in said slow channel in the absence of overlapping pulses,

b. said fast channel having means for stopping said live-time clock as each pulse is received,

c. said slow channel shaping and passing pulses to a multiple channel recorder,

d. said slow channel actuating one input of an AND gate when a pulse is processed,

e. said multichannel recorder having means to send a not busy signal to the other input of said AND gate when not processing a signal, and

f. the output of said AND gate causing said live-time clock to run.

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