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(54) Title: A SINGLE PHASE INVERTER FOR PHOTOVOLTAIC PANELS

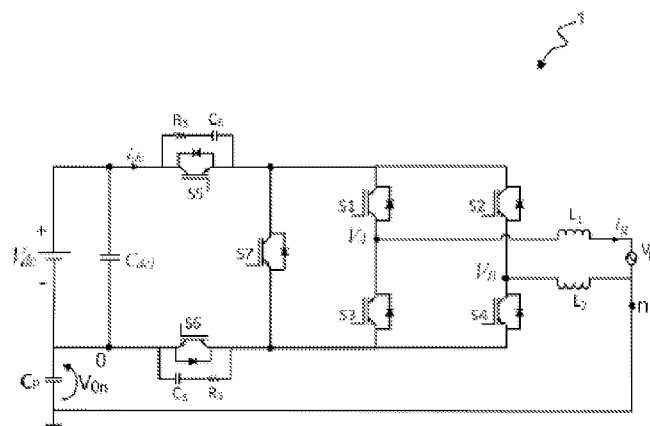


Fig. 7

(57) Abstract: This invention is related to a single phase inverter which enables converting the direct current voltage to alternating current voltage, allowing the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid, connecting to the grid voltage without using a transformer, keeping the leakage current below the standards and keeping the efficiency (ratio between output and input powers) at the rated power value up to 96 %.

A SINGLE PHASE INVERTER FOR PHOTOVOLTAIC PANELS

5 Technical Field

This invention is related to a single phase inverter which enables converting the direct current voltage to alternating current voltage, allowing the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid, connecting to the grid voltage without using a transformer, keeping the leakage current below the standards and keeping the efficiency (ratio between output and input power) at the
10 rated power value up to 96%.

State of the Art

Single phase inverters are used to produce alternating current voltage from direct current voltage. One of these uses is to transmit the direct current voltage obtained
15 from photovoltaic panels to the grid as an alternating current voltage. If the transformer is not used between the grid and the inverter, the leakage current flows between the panels and the ground of the grid must be controlled. Today, H5 and H6 inverter structures that offer transformerless use are widely used. Figure 1 shows H6 inverter, Figure 2 shows H5 inverter, Figure 3 shows optimized H5 (oH5) inverter and Figure 4
20 shows improved H6 inverter circuit diagrams of structures.

In order to connect the photovoltaic panels directly to the grid, the connecting inverters must meet the grid connection standards. In Figure 5, the circuit diagram of the conventional bridge inverter structure and in Figure 6, the circuit diagram of the common mode model of the conventional bridge inverter structures is shown. When the
25 inverter structures shown in Figure 5 and Figure 6 are examined, it is stated in the VDE0126-1-1 standards that in order not to decrease the reliability and the efficiency of the system, the magnitude of the leakage current (i_{cm}) which flows through the parasitic capacitors (C_p) and formed between the photovoltaic panel and the ground does not exceed 300mA (rms). A transformer can be used between the inverter and
30 the grid to prevent leakage current formation. However, the usage of transformers not only increases the cost, volume and weight of the system, but also decreases efficiency of the system. When the inverter is connected to the grid without using the transformer, the voltage on the parasitic capacitor (C_p) must be set to zero or kept constant to prevent leakage current.

The voltage on the parasitic capacitor (V_{on}) is achieved using Thevenin's equivalent and superposition methods, as in equation 1.

(Equation 1)

$$V_{on} = -V_{cm} - \frac{V_{dm}}{2} \left(\frac{L_2 - L_1}{L_1 + L_2} \right) + \frac{V_{gdm}}{2} \left(\frac{L_2 - L_1}{L_1 + L_2} \right) + V_{gcm} + \left(\frac{L_1 L_2}{L_1 + L_2} \right) \frac{di_{cm}}{dt}$$

- 5 In this equation, V_{cm} ((VAO+ VBO)/2) common mode voltage, V_{dm} (VAO-VBO)) inverter output (differential mode) voltage, V_{gcm} grid common mode voltage and V_{gdm} expresses the voltage of the electrical network differential mode.

- 10 Since the common mode (V_{gcm}) and difference mode voltages (V_{gdm}) resulting from the grid are low frequency (50Hz-60Hz), the effects of these voltages on leakage current can be neglected. In addition, inductances (L_1 , L_2) used for current control between the inverter and the grid can be equally selected to eliminate the effect of differential mode. Therefore, in order to prevent leakage current formation, the common mode voltage (V_{cm}) should be kept at a constant value at all levels of inverter output voltage.

- 15 H6 and optimized H5 topologies shown in Figure 1 and Figure 3, in order to keep the common mode voltage constant at all levels of the inverter output voltage, the capacitor (C_{dc1} and C_{dc2}) voltages used on the DC link must be equal. Therefore, the capacitor voltages can be kept equally by using capacitor voltage balancing algorithms. However, these algorithms will bring extra load to system control algorithms and need extra circuit elements (voltage sensors, resistance, diode, etc.) to read capacitor voltages. Another method to keep the capacitor voltages equal is the voltage divider resistance connected to each capacitor in parallel; however, this adversely affects the efficiency of the system.
- 20

- 25 Improved H6 structure shown in Figure 4 utilizes capacitors (IGBT collector – emitter junction capacitors) in the internal structure of semiconductor materials used in circuit topology in order to keep the common mode voltage constant at all levels of the inverter output voltage. Since the values of the capacitors in the internal structure of the semiconductor material can vary according to the working conditions, control of the common mode voltage and therefore the leakage current is difficult. In addition, the resonance that occurs during the operation of the system oscillates the common mode voltage.
- 30

Although H5 inverter given in Figure 2 uses a single capacitor, the common mode voltage carries uncertainty at zero levels of output voltage and can only control the leakage current in this inverter when the power factor of load is one. These restrictions limit the usage of this inverter structure.

- 5 The patent application document No KR101514803 in the literature describes the SPWM-based single phase inverter used in a distributed power supply connected to the renewable energy grid.

- The patent application document No CN108023498 in the literature describes the hybrid H6 photovoltaic single phase inverter structure. While the hybrid H6 single
10 phase photovoltaic inverter works, pulse width modulation performs according to two different modulation strategies.

The patent application document No US10038393 in the literature describes the new single phase, non-insulated inverter with reactive power capability. The inverter in question contains eight switching structures.

- 15 In the patent application document No US2009316458 in the literature, a structure is presented for converting direct current electrical energy into alternative current electrical energy. The feature of this structure is that it is simple, highly efficient and minimizes the problem of electromagnetic compatibility.

- The patent application document No CN107834888 in the literature describes the
20 single-phase photovoltaic inverter of the type without transformers. The inverter in question has up to 98% conversion efficiency.

The inverters described in the above documents have different properties and none of these have the same circuit structure as the single phase inverter subject to the invention.

- 25 Consequently, due to the aforementioned deficiencies, the electrical network, which converts the direct current voltage to alternating current voltage, allows the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid inverter structures that are connected to the voltage without using the transformers, keep the leakage current below the standards and operate at a high conversion
30 efficiency using a single capacitor at the panel output are needed.

The Aim of the Invention

The invention aims to solve the disadvantages mentioned about the existing circuit structures.

The main aim of this invention is to realize the single phase inverter, which converts direct current voltage into alternating current voltage, allowing the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid.

Another aim of this invention is to realize the single phase inverter that connects the voltage of the grid without the use of a transformer.

Another aim of this invention is to realize the single-phase inverter that keeps the leakage current below the standards.

Another aim of this invention is to realize the efficiency of the single phase inverter between the input and output forces at 96% under rated power conditions.

10 Another aim of this invention is to keep the total cost of production low.

Figure Clarifying the Invention

The structural and characteristic features of the invention and all the advantages it offers are more clearly understood in the following ways and detailed explanations.

15 The circuit structures of the single phase inverter developed with the current invention and the single phase inverters in the prior art are shown in attached shapes and in which;

Figure 1 is the circuit diagram of the H6 inverter of the prior art.

Figure 2 is the circuit diagram of the H5 inverter of the prior art.

Figure 3 is the circuit diagram of the optimized H5 (oH5) inverter of the prior art.

20 **Figure 4** is the circuit diagram of the improved inverter of the prior art.

Figure 5 is a circuit diagram of the conventional bridge inverter structure of the prior art.

Figure 6 is a circuit diagram of the common mode model of the traditional bridge inverter structure of the prior art.

25 **Figure 7** is a circuit diagram of the inventive inverter.

Figure 8 is the circuit diagram of the active current mode during the positive cycle of the inventive inverter.

Figure 9 is a circuit diagram of the freewheeling mode during the positive cycle of the inventive inverter.

30 **Figure 10** is a circuit diagram of the active current mode during the negative cycle of the inventive inverter.

Figure 11 is a circuit diagram of the inverter's freewheeling mode during the negative cycle of the inventive inverter.

Figure 12 is the active circuit structure for snubber analysis of the inventive inverter.

The circuit elements and variables in the figures are defined individually and the equivalents of these variables are given below.

1.	Inverter
Vdc.	DC line voltage
5 Idc.	DC line current
Cdc1.	Decoupling capacitor
S1	First semiconductor switch
S2	Second semiconductor switch
S3	Third semiconductor switch
10 S4	Fourth semiconductor switch
S5	Fifth semiconductor switch
S6	Sixth semiconductor switch
S7	Seventh semiconductor switch
Rs.	Snubber resistance
15 Cs.	Snubber capacitor
Is (t).	Snubber Current
VCE,S7.	Collector-absorber voltage of the seventh semiconductor switch
Is7.	Snubber current of the seventh semiconductor switch
0.	Local common ground
20 Cp.	Parasitic capacitor
Von.	Parasitic capacitor voltage
L1.	First inductance
L2.	Second inductance
Vg.	Electrical network voltage
25 Ig.	Electrical network current
Ls	Runaway inductance
Es	Snubber voltage

Detailed Description of the Invention

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In this detailed description, the analysis of the single-phase inverter (1) subject to the invention, the results recorded in operation and the preferred configurations are given only for a better understanding of the subject.

35

This invention is related to a single phase inverter (1) which enables converting the direct current voltage to alternating current voltage, allowing the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid, connecting to the grid voltage (Vg) without using a transformer, keeping the leakage current below the

standards and keeping the efficiency (ratio between output and input powers) at the rated power value up to 96%.

The inverter (1) according to the invention, whose circuit diagram is given in Figure 7, is in the most basic form, comprises the following;

- 5 - a DC connection decoupling capacitor (C_{dc1}), which is connected in parallel to the DC line voltage (V_{dc}) obtained from the photovoltaic panel, thus preventing the need for voltage compensation, keeping the common mode voltage (V_{gcm}) constant and keeping the leakage current below the specified value in the standards,
- 10 - two snubber circuits formed as a result of the series connection of the snubber resistance (R_s), which limits the DC line current (I_{dc}), and the snubber capacitor (C_s) that keeps the common mode voltage (V_{gcm}) constant by charging up to half of the DC line voltage (V_{dc}),
- 15 - a fifth semiconductor switch (S_5), which is connected to the port of the decoupling capacitor (C_{dc1}) with the positive (+) terminal of the DC line voltage (V_{dc}), is parallel to the first snubber circuit, has reduced switching losses due to said snubber circuit, is IGBT or semiconductors with similar switching characteristics,
- 20 - a sixth semiconductor switch (S_6), which is connected to the port of the decoupling capacitor (C_{dc1}) with the negative (-) terminal of the DC line voltage (V_{dc}), is parallel to the second snubber circuit, has reduced switching losses due to said snubber circuit, is IGBT or semiconductors with similar switching characteristics.
- 25 - a seventh semi-conductor (S_7) which is located between the fifth semiconductor switch (S_5) and the sixth semiconductor switch (S_6), is used for active clamping, freewheeling when turned on to maintain common mode voltage (V_{gcm}) constant flowing over a snubber current (I_{s7}) with low average and effective values, at turn off the collector-emitter voltage (V_{CE} , S_7) is equal to the DC line voltage (V_{dc}), is IGBT or semiconductors with similar switching characteristics,
- 30 - the first semiconductor switch (S_1) and the third semiconductor switch (S_3), which are semiconductors with IGBT or similar switching properties, are connected to each other in a serial manner and parallel to the seventh semiconductor switch (S_7),
- the second semiconductor switch (S_2) and the fourth semiconductor switch (S_4), which are semiconductors with IGBT or similar switching properties, are connected

to each other in a serial manner and parallel to the seventh semiconductor switch (S7),

- (Cp) which is between the negative (-) terminal of the DC line voltage (Vdc) and the neutral point of the grid voltage (Vg) and represents the parasitic capacitor of the PV panel,

- a first inductance (L1) which is located between the common end that is between the first semiconductor switch (S1) and the third semiconductor switch (S3) and the grid voltage (Vg) and is used for controlling the mains current (Ig) passes through the grid voltage (Vg) and

- a second inductance (L2) which is located between the common end between the second semiconductor switch (S2) and the fourth semiconductor switch (S4) and the grid voltage (Vg) and is used for controlling the mains current (Ig) that passes through the grid voltage (Vg).

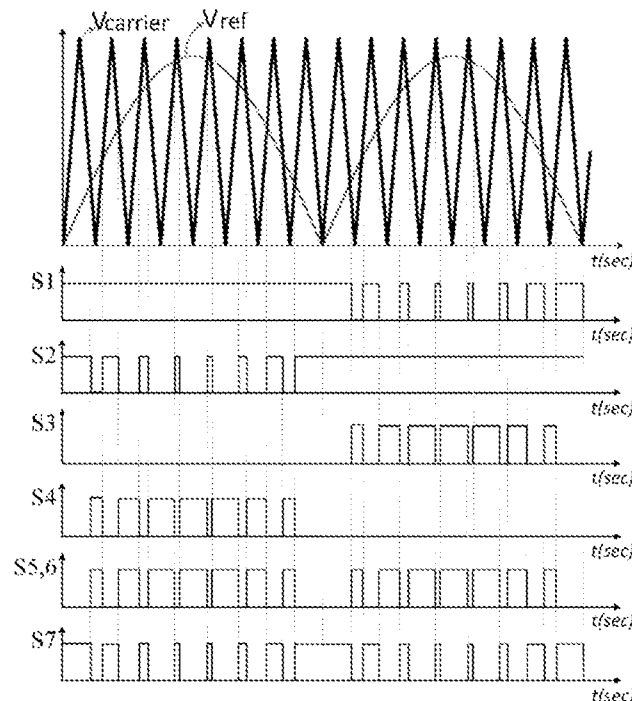
Voltage balancing is not required due to the use of a single capacitor (Cdc1) in the inverter (1) structure of the invention subject. Although the common mode voltages (Vgcm) of H6 and optimized H5 topologies are constant, capacitor voltage balancing is required due to the use of two capacitors in these inverter structures. In the improved H6 inverter structure, the resonance problem based on the use of the internal capacitors (junction capacitors) of semiconductors and the associated common mode voltage (Vgcm) oscillations have been eliminated by the proposed inverter (1) structure. While the common mode voltage (Vgcm) remains constant in the inverter (1) in the inventor's case, the leakage current is kept below the specified value in the standards. In addition, with the proposed inverter (1) structure, oscillations caused by diode clamp circuit and diode reverse recovery current are eliminated. The efficiency of the inverter (1) is around 96% at the rated power value.

The structure of the active clamped snubber-based inverter (1) was created using seven semiconductor switches (S1, S2, S3, S4, S5, S6 and S7), as shown in Figure 7. The seventh semiconductor switch (S7) used for active clamping is only turned on to keep the common mode voltage constant at the moment of freewheeling, so a low average and effective snubber current

(4,6) switch (S7). When the seventh semiconductor switch (S7) is not conduction, the collector-emitter voltage ($V_{CE,S7}$) of this switch ($V_{CE, S7}$) is equal to the DC line voltage (V_{dc}). The Snubber circuit capacitor (C_s) keeps the common mode voltage constant by filling up to half the DC line voltage (V_{dc}). In addition, snubber circuits reduce the switching losses of the fifth and sixth switches (S5 and S6). The parasitic capacitor (C_p) of the photovoltaic panel is located between the

negative terminal of the DC line voltage (V_{dc}) and the neutral point of the grid voltage (V_g).

During a period of grid voltage (V_g), there are four different working modes of the topology of the inventor (1) of the invention subject. The modes in question include; active current mode during the positive cycle, freewheeling mode during the positive cycle, active current mode during the negative cycle and freewheeling mode during the negative cycle. The gate signals of the seven semiconductor switches (S1, S2, S3, S4, S5, S6 and S7) that cause these modes to occur are shown in Figure 1.



Graph 1 - Switching signals (1) for the unipolar switching method for the proposed inverter.

For this proposed inverter (1) topology, the gate signals of the seven semiconductor switches (S1, S2, S3, S4, S5, S6 and S7) supplied in Graph 1 are fully compatible with the PWM ports of the digital signal processors required by the standard unipolar switching method.

The common mode voltage (V_{gcm}) of the inverter of the subject of invention (1) is written in VAO and VBO according to the local common point (0) in the negative terminal of the DC line voltage (V_{dc}). The common mode voltage in question (V_{gcm}) is shown in equation 2. VAO is the voltage difference between the VA terminal and the local common point (0) of the inverter (1). VB0 is the voltage difference between the (1) VB terminal and the local common point (0) of the inverter.

(Equation 2)

$$V_{cm} = \frac{(V_{A0} + V_{B0})}{2}$$

Differential mode voltage (V_{dm}) in the inverter's (1) VA and VB output terminals can be written in VAO and VB0, as shown in equation 3;

(Equation 3)

$$V_{dm} = V_{A0} - V_{B0}$$

VA0; the voltage difference between the VA terminal between the first semiconductor switch (S1) and the third semiconductor switch (S3) and the dc line voltage (V_{dc}) negative (-) terminal and the local common point (0) at the decoupling capacitor (C_{dc1}) port is noted. VB0; the voltage difference between the VB terminal between the second semiconductor switch (S2) and the fourth semiconductor switch (S4) and the dc line voltage (V_{dc}) negative (-) terminal and the local common point (0) at the decoupling capacitor (C_{dc1}) port is noted.

The switching signals for the proposed inverter (1) for sinusoidal pulse width modulation are included in Graph 1. The fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) are running simultaneously, and the seventh semiconductor switch (S7) is switched in the complementary to these switches (S5 and S6). In this case, it is clearly observed from Graph 1 that the first semiconductor switch (S1), the second semiconductor switch (S2), the third semiconductor switch (S3) and the fourth semiconductor switch (S4) are operated with a unipolar switching form.

Common mode voltage (V_{gcm}) can be analyzed in two intervals corresponding to a positive half-cycle of reference sinusoidal signal and a negative half-cycle. As shown in Figure 8, the first semiconductor switch (S1) is in a continuous conduction position during the positive

semi-cycle of the reference sinusoidal signal, while the third semiconductor switch (S3) is in an off position.

The transmission of these two switches (S1 and S3) varies alternately. The fourth semiconductor switch (S4), the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) and the second semiconductor switch (S2) are operated at the frequency of the carrier wave (switch frequency) complementary with each other. The value of the common mode voltage (V_{gcm}) in the meantime is obtained as shown in equation 4.

(Equation 4)

$$V_{cm} = \frac{(V_{dc} + 0)}{2} = \frac{V_{dc}}{2}$$

During the positive half cycle of the reference sinusoidal signal, the fourth semiconductor switch (S4) is opened to obtain the freewheeling path, the second semiconductor switch (S2) is turned on and the inverter (1) output voltage is zero. In addition, the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) are turned off and the seventh semiconductor switch (S7), the active clamping switch, is simultaneously turned on to keep the common mode voltage (V_{gcm}) constant. During the transmission of the seventh semiconductor switch (S7), the current $I_s(t)$ flows through the snubber circuit, as shown in Figure 9, until the voltage value of the snubber capacitor (C_s) reaches half of the DC line voltage (V_{dc}). The value of the common mode voltage (V_{gcm}) in the meantime is obtained as shown in equation 5.

(Equation 5)

$$V_{cm} = \frac{(V_{dc}/2 + V_{dc}/2)}{2} = \frac{V_{dc}}{2}$$

During the negative semi-cycle of the reference sinusoidal signal, the active current path is shown in Figure 10. In this case, the second semiconductor switch (S2) is in continuous conduction and the fourth semiconductor switch (S4) is off state. The second switch (S2) and the fourth semiconductor switch (S4) are commuted alternately. In this mode, the value of common mode voltage (V_{gcm}) is obtained as shown in equation 6.

(Equation 6)

$$V_{cm} = \frac{(0 + V_{dc})}{2} = \frac{V_{dc}}{2}$$

In freewheeling mode during the negative semi-cycle of the reference sinusoidal signal, the constant common mode voltage is achieved as shown in Figure 11. Since the two snubber circuits are equivalent, the voltage value on each is equal to half of the DC line voltage (V_{dc}). Therefore, in this mode, the value of the common mode voltage (V_{gcm}) is obtained as shown in equation 7.

(Equation 7)

$$V_{cm} = \frac{(V_{dc}/2 + V_{dc}/2)}{2} = \frac{V_{dc}}{2}$$

In all operating modes of unipolar switching, the common mode voltage (V_{gcm}) is constant and equals half of the DC line voltage (V_{dc}) ($V_{cm} = V_{dc}/2$).

The snubber circuit allows the inverter (1) to keep constant common mode voltage (V_{gcm}) without oscillations during freewheeling periods. The voltages on the Snubber circuits are shared equally half value through the DC line voltage (V_{dc}) level, ensuring that the seventh semiconductor switch (S7) is turned on. If the seventh semiconductor switch (S7) switch had not been turned on, no current ($I_s(t)$) would flow through the snubber circuits at the time of freewheeling, so the snubber capacitors (C_s) would not be charged.

The active circuit structure for Snubber analysis is shown in Figure 12. Snubber resistance (R_s), snubber condenser (C_s) and stray inductance (L_s) circuit on the DC line side form a circuit. Differential equations analyzing this circuit are shown in equations 8 and equation 9.

(Equation 8)

$$(D^2 + 2\xi\omega_0 D + \omega_0^2)i_s = 0$$

(Equation 9)

$$(R_s C_s D + 1)i_s = C_s D e_s$$

Here $D = d/dt$ and snubber voltage is e_s .

Damping Coefficient $\xi = \frac{R_s}{2} \sqrt{\frac{C_s}{L_s}}$

Resonance frequency, $\omega_0 = 1/\sqrt{L_s C_s}$

The snubber current $i_s(t)$ for the (underdamped) is ($0 < \xi < 1$)

(Equation 10)

$$i_s(t) = \frac{e_s}{R_s} \frac{2\xi}{\sqrt{(1-\xi^2)}} \exp(-\xi\omega_0 t) \sin(\omega t)$$

Here $\omega = \omega_0 \sqrt{(1-\xi^2)}$ current wave forms, $R_s = 1$ ohm and $R_s = 5$ Ohm is recorded at two different snubber resistance value, snubber capacitor (C_s) at 22 nF and when inverter (1) is running at nominal load (1 kW output power).

5

When these snubber parameters are used, underdamped response has been observed in recorded snubber current waveforms. The mathematical expression of the Snubber current waveform is given in equation 10. The stray inductance is calculated as ~~(ω_0)~~ 0.7 μ H using the resonant frequency in the missing underdamped response mode of L_s . The snubber resistance is then fixed to 10 ohm snubber resistance to achieve a critically damped response that causes minimal effect on the icm of the leakage current. The mathematical expression of the snubber current for critically damped response is given in equation 11. The results measured through the snubber circuit designed for the critically damped state are shown in Graph 2 when the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) are turned off. The initial value of the Snubber current is zero and has two critically damped waves in each turning off. The first wave occurs after the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) are simultaneously turned off. The second current wave appears when the seventh semiconductor switch (S7) is turned on after the 1.3 micro second dead time period between the seventh semiconductor switch (S7) and the sixth semiconductor switch (S6). For a critically damped response ($\xi = 1$) state, the snubber current is like $i_s(t)$ in equation 11.

10

15

20

(Equation 11)

$$i_s(t) = e^{-\omega_0 t} (A_1 + A_2 t)$$

25

The initial value of the Snubber current ($i_s(0)$) equals to zero.

Therefore $A_1 = 0$ and $A_2 = \frac{di_s(t)}{dt} \Big|_{t=0^+} = \frac{e_s}{L_s}$

Stored energy in snubber capacitor (C_s) can be calculated as follows;

$$P_{Rs} = C_s \frac{V_{dc}}{2} f_{sw}$$

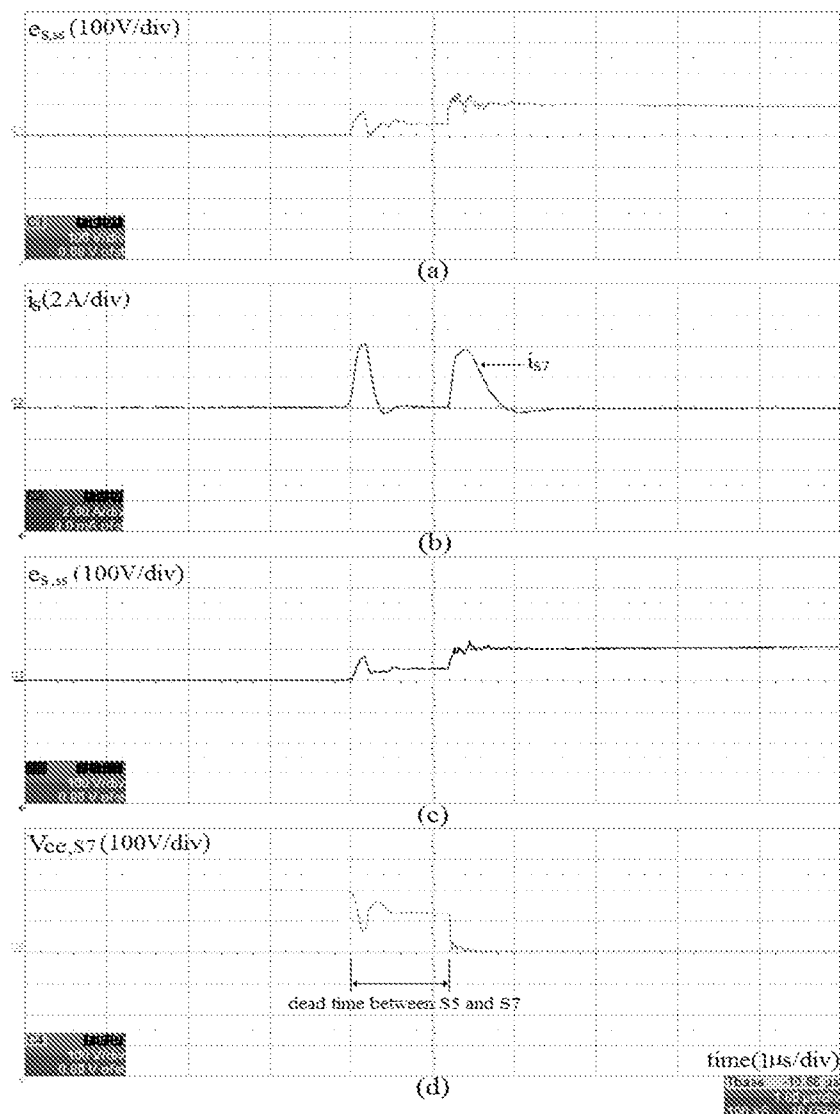
Here, f_{sw} is the switching frequency of IGBTs.

Graph 2 contains results measured through the snubber circuit when the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) are out of transmission. In Graph 2, a) section of the snubber circuit voltage of the sixth semiconductor switch (S6) of the sixth semiconductor switch (S6), b) section of the snubber circuit current (I_s) of the sixth semiconductor switch (S6) of section B, c) section of the snubber circuit voltage of the fifth semiconductor switch (S5) of the c section (E_s) d) section of the collector-absorber voltage (VCE, S7) of the seventh semiconductor switch (S7) is specified.

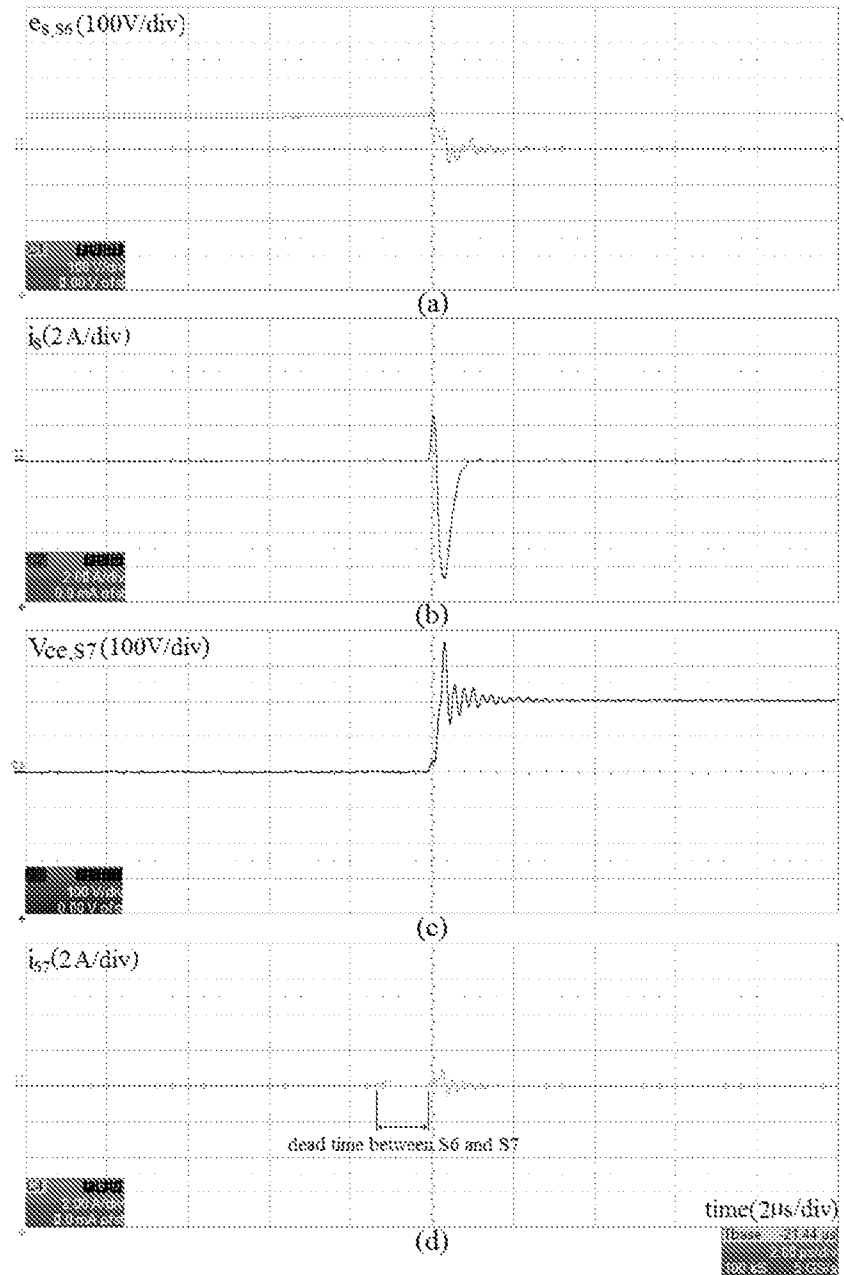
Graph 3 contains the results measured through the snubber circuit during turn on of the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6).

Graph 3 a) section of the snubber circuit voltage of the sixth semiconductor switch (S6), b) section of the snubber circuit current of the sixth semiconductor switch (S6), the c) section of the seventh semiconductor switch (S7) collector-emitter voltage ($V_{CE,S7}$) and d) section of the seventh semiconductor switch (S7) the collector-emitter current (I_{S7}) is indicated.

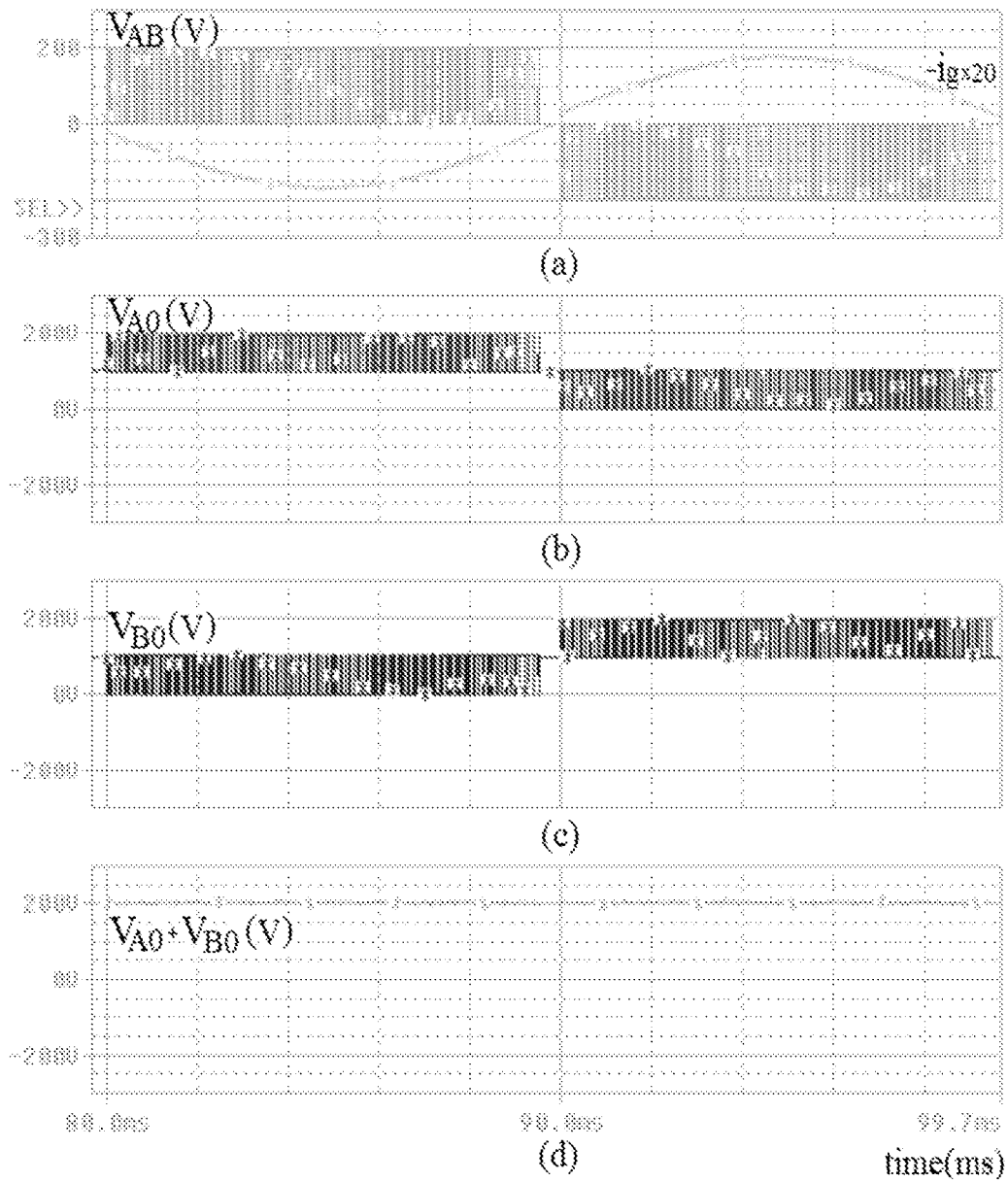
Graph 4 includes simulation of the proposed inverter (1) and experimental results (below) of the proposed inverter (1) in Graph 5. In Graph 4 and Graph 5, a) section of inverter (1) output voltage (V_g) and output current (I_g) (by network), b) section of VA_0 , c) section of VB_0 and d) section of (2x common mode voltage (V_{gcm})) refers to $VA_0 + VB_0$.



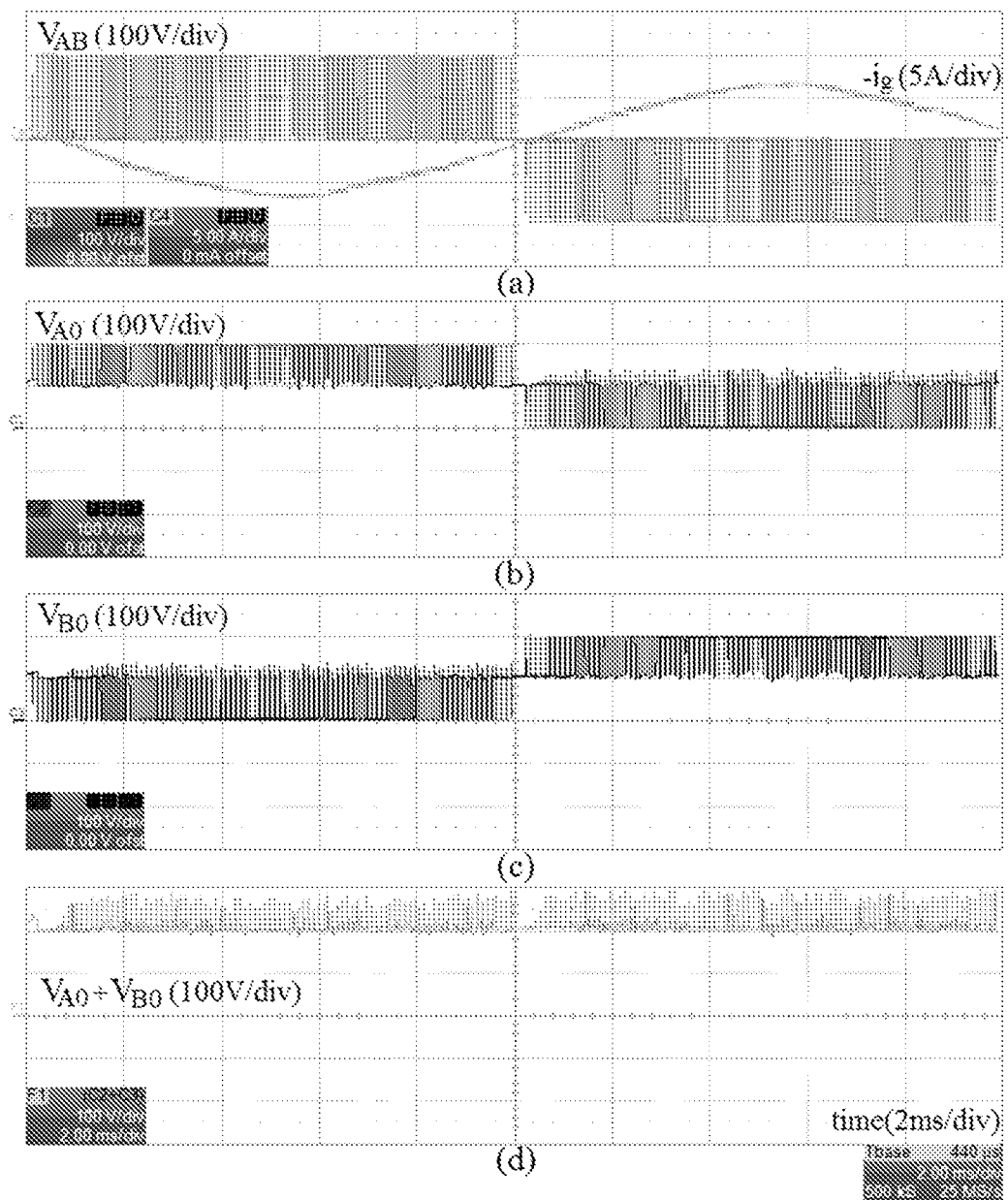
Graph 2- Results measured over the snubber circuit during turn off interval of the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6)



Graph 3 - Results measured over the snubber circuit during turn on interval of the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6)



Graph 4 - Simulation of the proposed inverter (1)



Graph 5 - Experimental results of the proposed inverter (1)

CLAIMS

1. A single phase inverter which enables converting the direct current voltage to alternating current voltage, allowing the energy obtained from photovoltaic (PV) panels to be transferred to the voltage of the grid, connecting to the grid voltage without using a transformer, keeping the leakage current below the standards and keeping the efficiency ratio between output and input powers (efficiency) at the rated power value up to 96%, **characterized in that** it comprises the following;
- 10 - A DC connection decoupling capacitor (C_{dc1}), which is connected in parallel to the DC line voltage (V_{dc}) obtained from the photovoltaic panel, thus preventing the need for voltage compensation, keeping the common mode voltage (V_{gcm}) constant and keeping the leakage current below the specified value in the standards,
 - 15 - Two snubber circuits formed as a result of the series connection of the snubber resistance (R_s), which limits the DC line current (I_{dc}), and the snubber capacitor (C_s), that keeps the common mode voltage (V_{gcm}) constant by filling up to half of the DC line voltage (V_{dc}),
 - 20 - A Fifth semiconductor switch (S_5), which is connected to the port of the decoupling capacitor (C_{dc1}) with the positive (+) terminal of the DC line voltage (V_{dc}), is parallel to the first snubber circuit, has reduced switching losses due to said snubber circuit, is IGBT or semiconductors with similar switching characteristics,
 - 25 - A sixth semiconductor switch (S_6), which is connected to the port of the decoupling capacitor (C_{dc1}) with the negative (-) terminal of the DC line voltage (V_{dc}), is parallel to the second snubber circuit, has reduced switching losses due to said snubber circuit, is IGBT or semiconductors with similar switching characteristics.
 - 30 - A seventh semi-conductor (S_7) which is located between the fifth semiconductor switch (S_5) and the sixth semiconductor switch (S_6) area, is used for active clamping only freewheeling when turned on to maintain common mode voltage (V_{gcm}) constant, flowing over a snubber current (I_{s7}) with low average and effective values, at non conducting state the collector-emitter voltage (V_{CE} , S_7) is

equal to the DC line voltage (V_{dc}), is IGBT or semiconductors with similar switching characteristics,

- the first semiconductor switch (S1) and the third semiconductor switch (S3), which are IGBT or semiconductors with IGBT or similar switching properties, are connected to each other in a serial manner and parallel to the seventh semiconductor switch (S7),
 - the second semiconductor switch (S2) and the fourth semiconductor switch (S4), which are IGBT or semiconductors with IGBT or similar switching properties, are connected to each other in a serial manner and parallel to the seventh semiconductor switch (S7),
 - (C_p) which is between the negative (-) terminal of the DC line voltage (V_{dc}) and the neutral point of the grid voltage (V_g) and represents the parasitic capacitor of the PV panel,
 - the first inductance (L1) which is located between the common end that is between the first semiconductor switch (S1) and the third semiconductor switch (S3) and the grid voltage (V_g) and is used for controlling the mains current (I_g) passes through the electrical network voltage (V_g) and
 - the second inductance (L2) which is located between the common end between the second semiconductor switch (S2) and the fourth semiconductor switch (S4) and the grid voltage (V_g) and is used for controlling the mains current (I_g) that passes through the electrical network voltage (V_g).
2. An inverter (1) according to claim 1, **characterized in that**; in case VA0 states the voltage difference between the VA terminal located between the first semiconductor switch (S1) and the third semiconductor switch (S3) and the negative (-) terminal of the DC line voltage (V_{dc}) and the local common point (0) at the connection point of the decoupling capacitor (C_{dc1}) and VB0 states the voltage difference between VB terminal between the second semiconductor switch (S2) and the fourth semiconductor switch (S4) and the DC line voltage (V_{dc}) negative (-) terminal and the local common point (0) at the connection point of the decoupling capacitor (C_{dc1}), the common mode voltage is the value obtained from the equation

$V_{cm}=(V_{A0}+V_{B0})/2$ and the differential mode voltage (V_{dm}) at the VA and VB output terminals is the value obtained from $V_{dm}=V_{A0}-V_{B0}$.

3. An inverter (1) according to claim 1, **characterized in that**; it comprises for the sinusoidal pulse width modulation, a fifth semiconductor switch (S5) which operates simultaneously and a sixth semiconductor switch (S6), a seventh semiconductor switch (S7) which is switched in complementary to these switches (S5 and S6), a first semiconductor switch (S1), the second semiconductor switch (S2), third semiconductor switch (S3) and fourth semiconductor switch (S4) which are operated with a unipolar switching form.
4. An inverter (1) according to claim 1, **characterized in that**; it comprises seven semiconductor switches (S1, S2, S3, S4, S5, S6 and S7) which form during the period of grid voltage (V_g), four different operating modes as the active current mode during the positive cycle, freewheeling mode during the positive cycle, active current mode during negative cycle and freewheeling mode during negative cycle and which are fully compatible with the PWM ports of the digital signal processors which are required by the standard unipolar switching method of the gate signals.
5. An inverter (1) according to claim 4, **characterized in that**; during the positive semi-cycle of the reference sinusoidal signal, it comprises the first semiconductor switch (S1), whose transmissions change alternately, i.e. one in a conduction position at all time, the other in an off position and third semiconductor switch (S3), the fourth semiconductor switch (S4), which is operated complementary with the second semiconductor switch (S2) and at the frequency of the carrier wave (switching frequency), fifth semiconductor switch (S5) and sixth semiconductor switch (S6) and the value of common mode voltage (V_{gcm}) is derived from the $V_{cm} = \frac{(V_{dc}+0)}{2} = \frac{V_{dc}}{2}$ equation as a result of the work carried out in this way.
6. An inverter (1) according to claim 4, **characterized in that**; to obtain the freewheeling path during the positive half-cycle of the reference sinusoidal signal, the second semiconductor switch (S2), which is in the conduction position while the fourth semiconductor switch (S4) is off and thus ensures that the output voltage is zero, the fifth semiconductor switch (S5) and the sixth semiconductor switch (S6) which are off state, the seventh semiconductor switch (S7), which is clamping switch, simultaneously turned on and as a result of this work, the current $I_s(t)$ flows through the snubber circuit until the voltage

value of the snubber capacitor (Cs) reaches half of the DC line voltage (Vdc) flow and the value of the common mode voltage (Vgcm) is the value derived from the $V_{cm} = \frac{(V_{dc}/2 + V_{dc}/2)}{2} = \frac{V_{dc}}{2}$ equation.

7. An inverter (1) according to claim 4, **characterized in that**, during the negative half-cycle of the reference sinusoidal signal, it comprises second semiconductor switch (S2) which is alternately transmitted and a fourth semiconductor switch (S4) and as a result of this work, the value of the common mode voltage (Vgcm) is the value obtained from the $V_{cm} = \frac{(0 + V_{dc})}{2} = \frac{V_{dc}}{2}$ equation.

8. An inverter (1) according to claim 4, **characterized in that**; in freewheeling mode during the negative half-cycle of the reference sinusoidal signal, the value of common mode voltage (Vgcm) is the value derived from the $V_{cm} = \frac{(V_{dc}/2 + V_{dc}/2)}{2} = \frac{V_{dc}}{2}$ equation because the voltage value per-second is equal to half of the DC line voltage (Vdc), as the two snubber circuits are equivalent.

9. An inverter (1) according to claim 1, **characterized in that**, during the freewheeling periods, it comprises seventh semiconductor switch (S7) which ensures that the voltages on the snubber circuits that remain at constant common mode voltage (Vgcm) without fluctuations, are shared equally by half of the DC line voltage (Vdc) level and allows current (Is (t)) to flow through the snubber circuits and charge from the snubber capacitors (Cs).

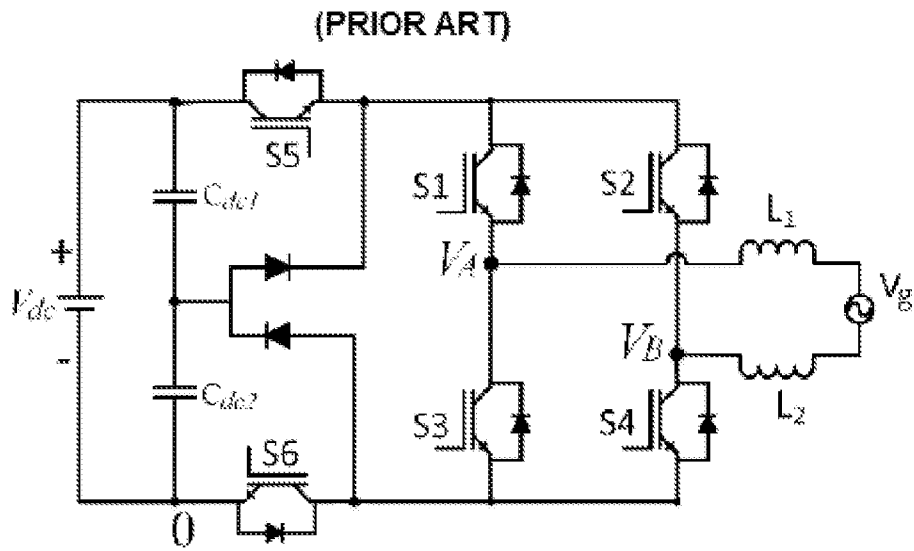


Fig.1

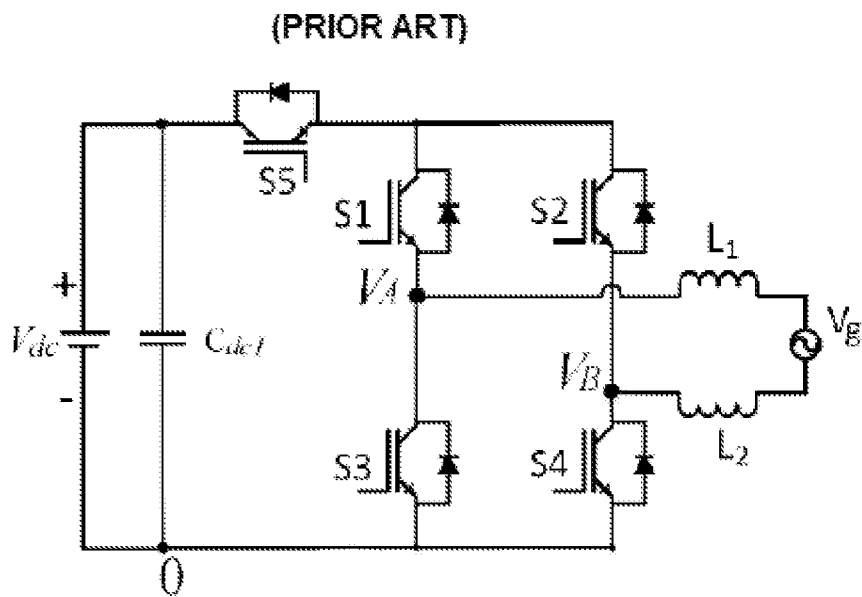


Fig. 2

(PRIOR ART)

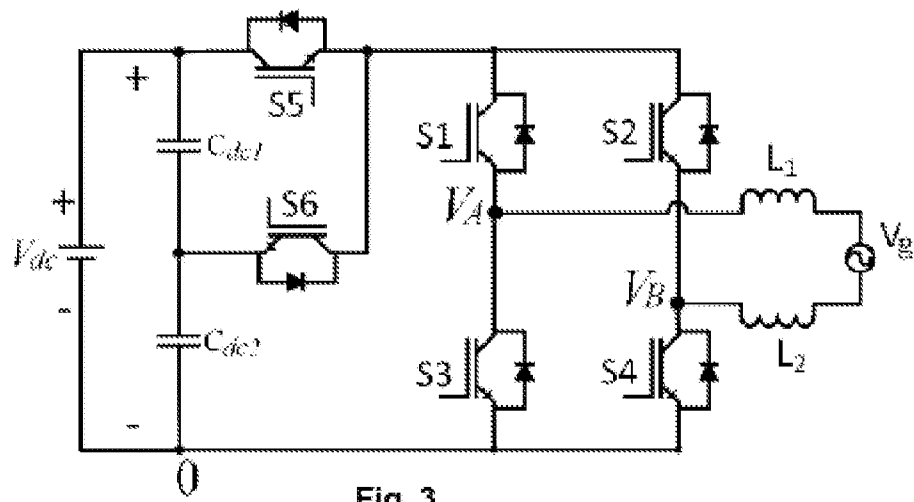


Fig. 3

(PRIOR ART)

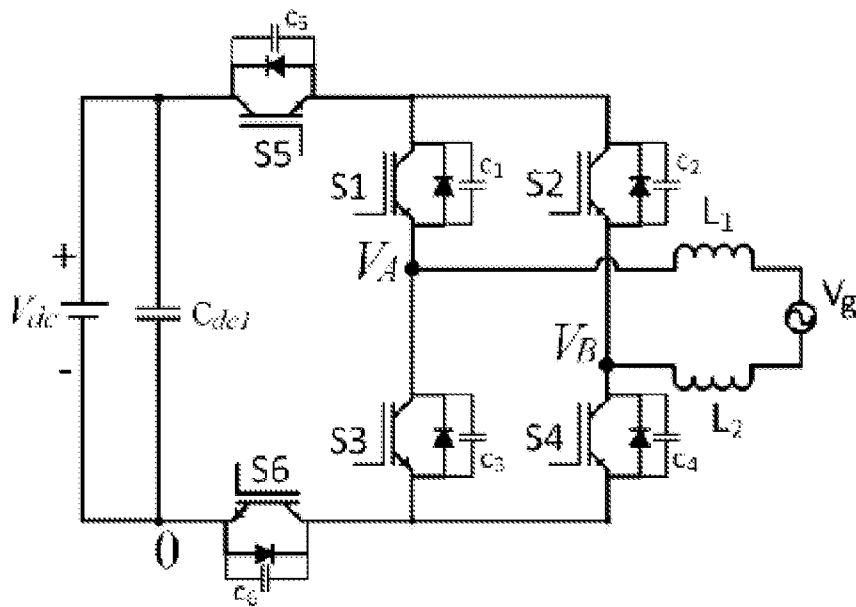


Fig. 4

(PRIOR ART)

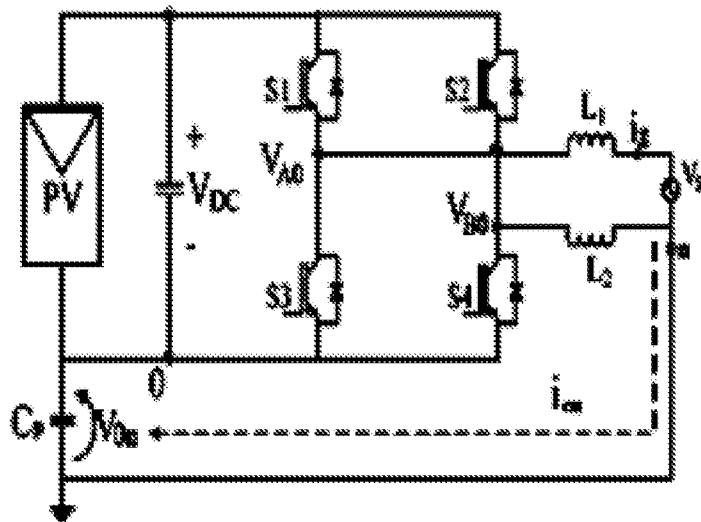


Fig. 5

(PRIOR ART)

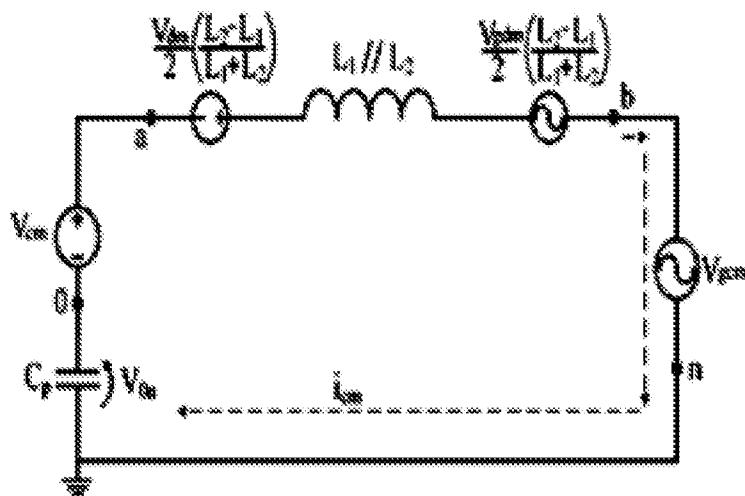


Fig. 6

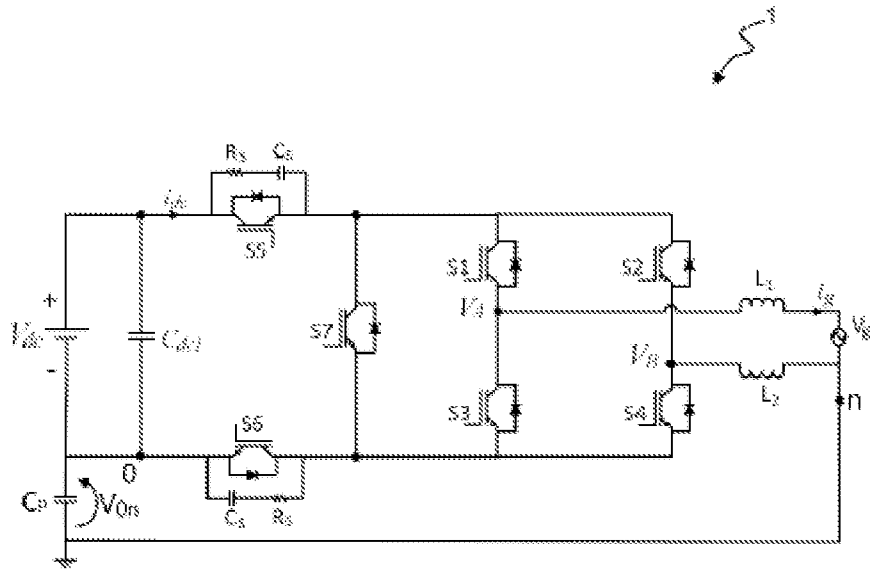


Fig. 7

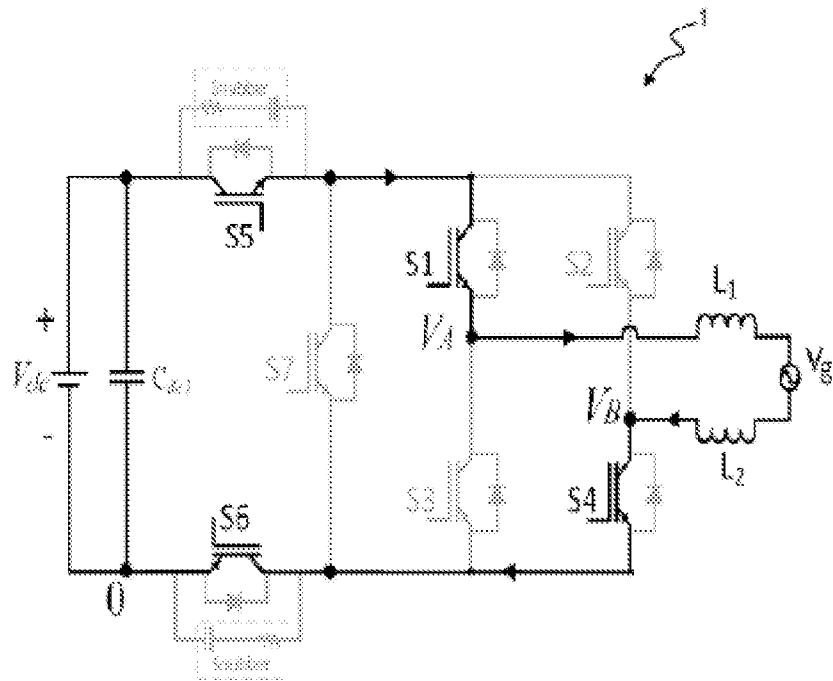


Fig. 8

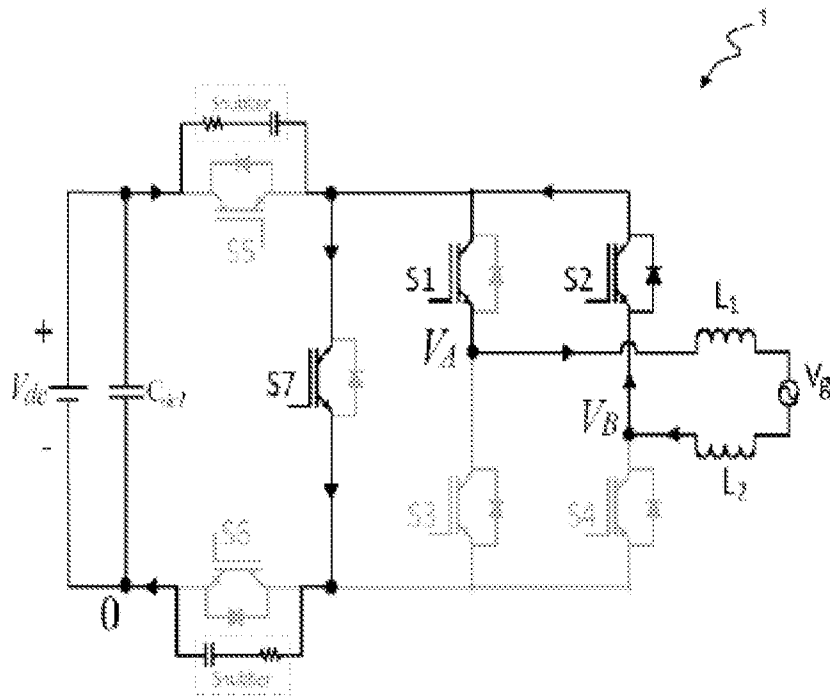


Fig. 9

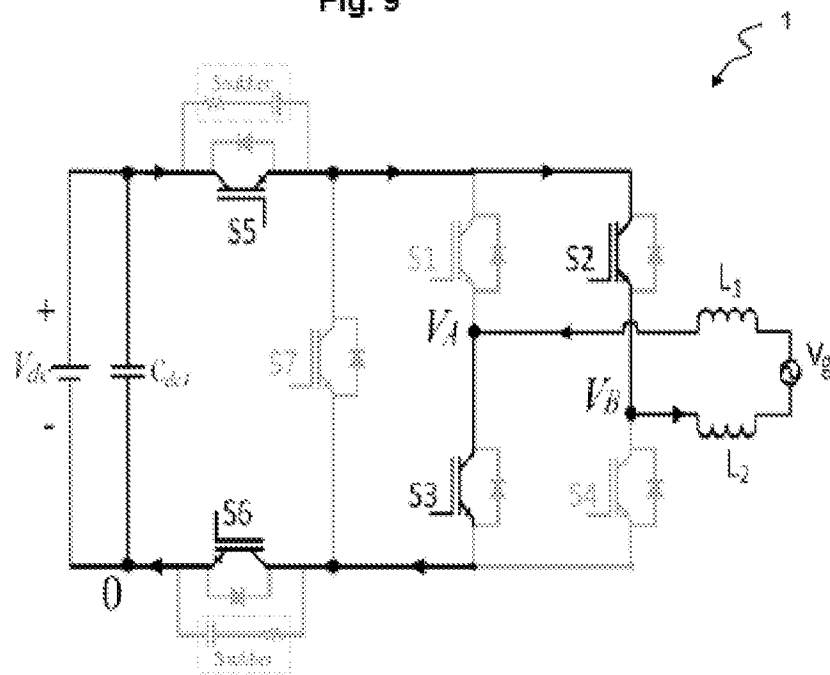


Fig. 10

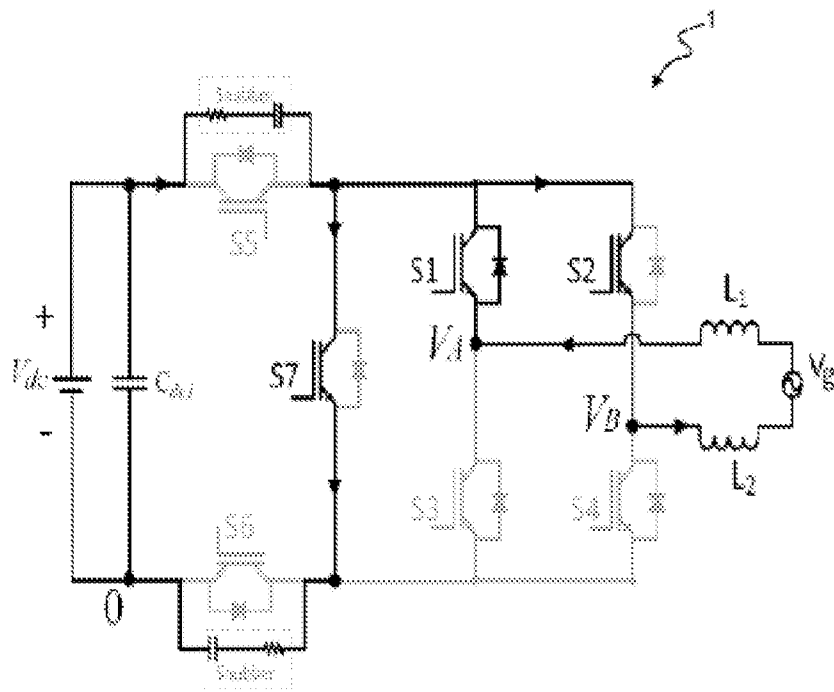


Fig. 11

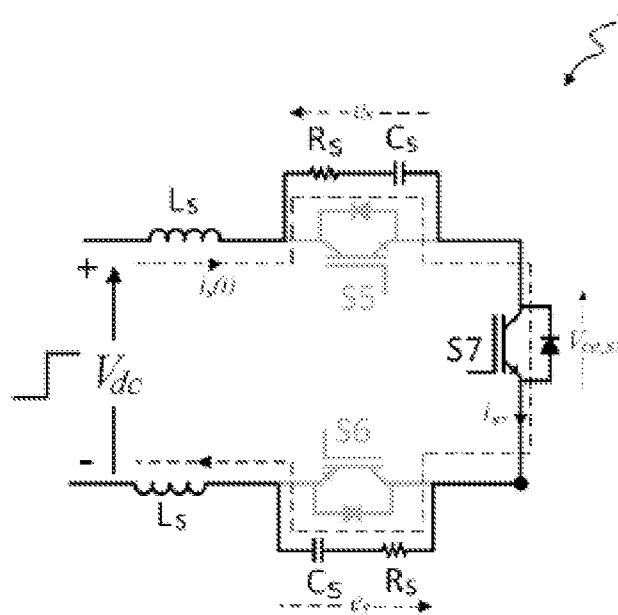


Fig. 12