PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :
H01L 21/336, 21/8238

A2

(11) International Publication Number: **WO 00/63964**

(43) International Publication Date: 26 October 2000 (26.10.00)

(21) International Application Number: PCT/SE00/00731

(22) International Filing Date: 17 April 2000 (17.04.00)

(30) Priority Data:
9901345–0 15 April 1999 (15.04.99) SE

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S–126 25 Stockholm (SE).

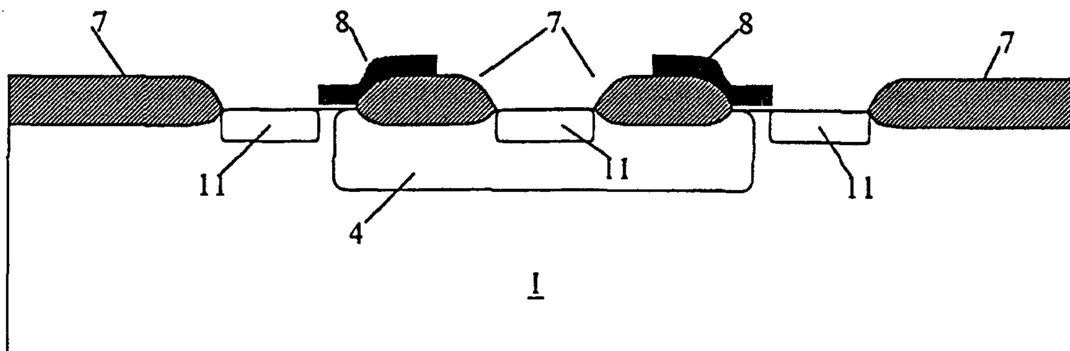
(72) Inventor: SÖDERBÄRG, Anders; Norbyvägen 129 C, S–754 65 Uppsala (SE).

(74) Agent: ERICSSON MICROELECTRONICS AB; Department for Intellectual Property Rights, S–164 81 Kista–Stockholm (SE).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: CMOS PROCESS



(57) Abstract

A high–voltage MOS transistor is produced in a low–voltage CMOS process without adding extra process steps for producing the high–voltage MOS transistor. The high–voltage MOS transistor is to be used as an analog line driver and is produced on the same silicon area as low–voltage AD/DA– converters. Hereby, the low–voltage and the high–voltage design block are directly compatible with each other, e.g. have the same threshold voltages, which simplifies the design of the total solution.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

Code	State
AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

CMOS PROCESS

TECHNICAL FIELD

The invention relates generally to a CMOS process and more specifically to a method of producing a high-voltage MOS transistor in a CMOS process.

BACKGROUND OF THE INVENTION

In ADSL (Asymmetric Digital Subscriber Line) systems, data are transferred at high speed from a central office to subscribers on existing telephone lines.

In the central office, there is a separate ADSL line card having an analog front end comprising e.g. high-speed AD/DA converters, line drivers and receivers.

To achieve required performance concerning speed and signal-to-noise ratio, the line driver has to work with a supply voltage above 10V. At the same time, modern mixed signal technologies, using submicron channel length, have to be used for the AD/DA part. Such technologies can normally not operate above 5V. Therefore, the line driver is implemented on a separate chip using bipolar technology, while the remaining part of the analog front end is implemented in an ordinary CMOS technology suited for modern AD/DA-design.

If extra process steps were added to the standard CMOS process, it would of course be possible to include the line driver on the same chip as the rest of the analog front end, but such a process would be more complicated and more expensive compared to the standard technology. It could e.g. be done using a BiCMOS process, i.e. a process including both bipolar and CMOS transistors, where the bipolar part is optimized for the line driver. However, as mentioned above, such a process is more expensive and complicated compared to a single CMOS process.

It could also be implemented using a dual gate CMOS process, which includes CMOS devices with two different gate oxides. A thicker gate oxide will then be able to handle

the higher voltage. Such a process will of course also be more complicated. Furthermore, it will be hard to obtain the necessary performances for ADSL using such types of MOS devices because a thicker gate oxide decreases the performance at high frequency.

A further way would be to add an LDMOS device to the process, where the channel length and the threshold voltage are set by adding an extra p-doped region inside the n-well. Extra process steps are then needed and the low-voltage devices and the high-voltage device will get different threshold voltages.

BRIEF DESCRIPTION OF THE INVENTION

The object of the invention is to implement all necessary functions for the analog front end on the same chip, i.e. including also the line drivers, by using an ordinary CMOS process flow suited for low voltage mixed signal design.

This is attained in that the design of the MOS transistor is modified in such a way that the process includes high-voltage MOS transistors with similar frequency performance and with the same threshold voltage as the low voltage n-channel MOS transistor. The high voltage MOS transistor is added without any extra mask steps or other steps to the process flow. Instead, the voltage is distributed inside an extended field region consisting of the same n-well dopants as is formed for the low-voltage PMOS transistor.

Hereby, in the same CMOS process, a high-voltage MOS transistor will be produced together with a low-voltage NMOS transistor and a low-voltage PMOS transistor on the same substrate. Further, the supply voltage for the low-voltage transistors can then be decreased without changing the breakdown voltage capability for the high voltage transistor.

BRIEF DESCRIPTION OF THE DRAWING

The invention will be described more in detail with reference to the appended drawing on which Figs. 1-12 illustrate different steps in a CMOS process according to the invention.

DESCRIPTION OF THE INVENTION

Fig. 1 is a cross-sectional view of a substrate 1, e.g. a p-type substrate or a p-type silicon layer on a silicon substrate differently doped, with a mask 2 of an oxide, e.g. SiO_2, with openings 3 defining where n-well regions are to be located in the substrate for a high-voltage MOS transistor (to the right in Fig. 1) and a low-voltage PMOS transistor (to the left in Fig. 1).

Fig. 2 is a top-view of the substrate with the mask 2 and the openings 3 illustrated in Fig. 1.

Fig. 3 is a cross-sectional view of the substrate 1 with the mask 2 with the openings 3 after that n-well regions 4 and 5 have been produced for the high-voltage MOS transistor and the low-voltage PMOS transistor, respectively.

The n-wells 4 and 5 are produced by doping the substrate through the openings 3 in the mask 2. The doping can e.g. be done by means of ion implantation of phosphorous.

In a CMOS process, the n-well regions are the regions where PMOS transistors are defined.

In accordance with the invention, the same implantation and masking sequences are used to create the drain region and the region that is to distribute the voltage potential for the high-voltage transistor.

In a step not illustrated, the mask 2 is removed from the substrate 1 and a protective film of e.g. silicon nitride (Si_3N_4) is deposited on the substrate.

Fig. 4 is a cross-sectional view of the substrate 1 after that portions of the protective film have been removed.

The remaining portions 6 of the protective film are located where source, gate and drain regions for both the high-voltage MOS transistor and the low-voltage NMOS and PMOS transistors are to be defined. The low-voltage NMOS transistor is to be located between the high-voltage MOS transistor and the low-voltage PMOS transistor.

Next, the substrate 1 is exposed to an oxidizing atmosphere to produce an oxide on areas not covered by the protective film 6. In Fig. 5, these oxide regions are denoted 7.

This method of creating an oxide pattern on a silicon substrate is known and called LOCOS (LOCal Oxidation of Silicon). LOCOS oxidation is described i.a. in S. Wolf, "Silicon Processing for the VLSI Era, Volume 2 - Process Integration", ISBN 0-961672-4-5, Lattice Press Carlifornia 1990, pp. 17-44. LOCOS technique is regularly used in almost all CMOS processes to laterally separate the transistors from each other. This technique is normally used to create active regions, i.e. the regions where transistors are to be located.

In accordance with the invention, this step also defines part of the voltage distributing region for the transistor. The thickness of the oxide is normally between 4000 and 15000 A.U.

Fig. 6 is a top-view of the substrate 1 after it has been oxidized, i.e. the same step as illustrated in Fig. 5. The little square 13 to the left indicates where a contact to the n-well 5 is to be defined.

Fig. 7 illustrates the step where gate-regions 8, 9 and 10 have been defined for the high-voltage MOS transistor, the low-voltage NMOS transistor and the low-voltage PMOS transistor, respectively.

To define the gate regions, the portions 6 of the protective film as illustrated in Fig. 5, have been removed, and a thin gate oxide (not shown) has been produced on the substrate 1. On the gate oxide (not shown), a layer of polycrystalline silicon (poly-Si) has been deposited and patterned to define the gate regions 8, 9 and 10.

As apparent from Fig. 7, the gate region 8 for the high-voltage MOS transistor extends partly on the oxide 7 above the n-well 4.

A normal thickness for the poly-Si layer is between 200 and 600 nm.

In accordance with the invention, the same gate structure, i.e. gate material and underlying gate oxide, that is used for the low-voltage PMOS transistor is used also for the high-voltage MOS transistor. Further, the doping concentration within the region where the channel for the high-voltage MOS transistor is to be located, looks identical to the channel region for the low-voltage NMOS transistor. Thereby, the high voltage MOS transistor will also have the same threshold voltage as the low voltage NMOS transistor.

The next step is illustrated in Fig. 8. In this step, n^+-regions 11 are defined, i.e. the regions that define the regions corresponding to drain and source for the low-voltage NMOS transistor and the contact to the n-well (not illustrated in the cross-sectional view). The same process step is also used to define source and drain for the high-voltage MOS transistor.

In the next step, illustrated in Fig. 9, p^+-regions 12 are defined. These regions define the regions that correspond to drain and source for the low-voltage PMOS transistor to be produced.

From Fig. 10, it is apparent that the cross-section of the high-voltage MOS transistor is the same as the cross-section of the low-voltage transistors. Thus, no extra masking

step or any other process step is needed to produce the high-voltage MOS transistor in the normal CMOS process. The source region for the high-voltage MOS transistor is identical to the source region for the low-voltage NMOS transistor as apparent from cuts 1' and 1" in Fig. 10. The channel region for the high-voltage MOS transistor is identical to the channel region for the low-voltage NMOS transistor as apparent from cuts 2' and 2" in Fig. 10. The first portion of the voltage distributing region for the high-voltage MOS transistor is identical to the channel region for the low-voltage PMOS transistor as apparent from cuts 3' and 3", respectively, in Fig. 10. The remaining portion of the voltage distributing region is defined in that the gate, i.e. the poly-Si, extends on top of the thicker oxide and that the n-well is defined within the whole of this region. No part of this region has to be defined by means of extra process steps or extra masks but are fully defined by the process sequences and masks that already are present in the process flow. The drain region for the high-voltage MOS transistor (cut 4' in Fig. 10) is the same as the contact region (not illustrated in Fig. 10) to the n-well for the low-voltage PMOS transistor.

Fig. 11 illustrates how the layout looks from the top excluding succeeding steps such as metallization and passivation. The high-voltage MOS transistor is preferably done symmetrical, i.e. so that it is mirrored in the middle of the drain region (at cut 4' in Fig. 10) so that all of the drain region is surrounded by the gate and source regions as illustrated in Fig. 12 which illustrate a cross-sectional view of a high-voltage MOS transistor that is symmetrical around the drain region in the middle.

CLAIMS

1. A method of producing, in a CMOS process, a high-voltage MOS transistor together with a low-voltage NMOS transistor and a low-voltage PMOS transistor on a substrate, comprising

- producing a mask on the substrate with openings defining where n-well regions are to be located in the substrate for the high-voltage MOS transistor and the low-voltage PMOS transistor,
- doping the substrate through said mask openings to produce the n-well regions for both the high-voltage MOS transistor and the low-voltage PMOS transistor in the same process step,
- removing the mask,
- depositing a protective film on the substrate,
- removing the protective film except where source, gate and drain regions for both the high-voltage MOS transistor and the low-voltage NMOS and PMOS transistors are to be located,
- exposing the substrate to an oxidizing atmosphere to produce an oxide on areas not covered by the protective film,
- removing the rest of the protective film,
- defining the gate regions for both the high-voltage MOS transistor and the low-voltage NMOS and PMOS transistors by producing a thin gate oxide on the substrate, depositing a layer of poly-Si thereon, and patterning the poly-Si layer,
- defining n^+-regions corresponding to the drain and source regions for the low-voltage NMOS transistor and for the high-voltage MOS transistor in the same process step.

2. The method as claimed in claim 1, **characterized in** that the poly-Si patterned as a gate for the high-voltage MOS transistor, extends over the oxide edge, whereby the thickness of the oxide under the gate of the high-voltage MOS transistor differs towards the source and the drain, respectively.

3. The method as claimed in claim 2, **characterized in** that the difference between the thickness of the oxide under the gate on the source side and on the drain side, is selected to be larger than a factor 10.

4. The method as claimed in claim 1, **characterized in** that the channel length of the high-voltage MOS transistor is determined by the fitting between the mask for defining the n-well regions and the gate poly-Si.

5. The method as claimed in claim 1, **characterized in** that the high-voltage MOS transistor can withstand voltages twice as high as the low-voltage transistors.

6. The method as claimed in claim 1, **characterized in** that the threshold voltage of the low-voltage NMOS transistor and the high-voltage MOS transistor is the same.

7. The method as claimed in claim 1, **characterized in** that the substrate is selected to be a p-type substrate.

8. The method as claimed in claim 1, **characterized in** that the substrate is selected to comprise is a p-type silicon layer on a differently doped substrate.

9. Use of a high-voltage MOS transistor, produced on a substrate in the same process as low-voltage CMOS transistors, as an analog line driver at the same time as the low-voltage CMOS transistors are used as AD/DA converters.

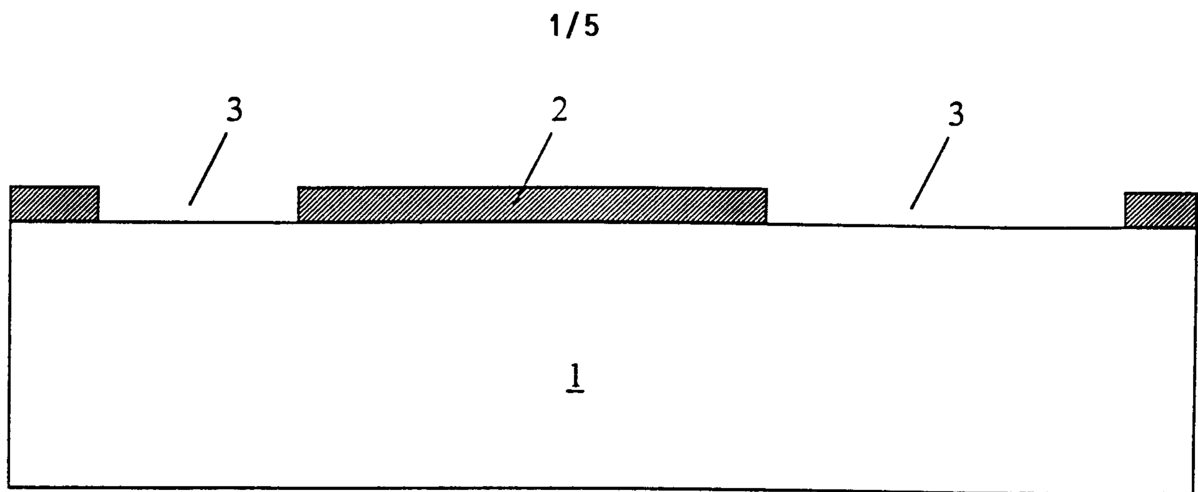


Fig.1

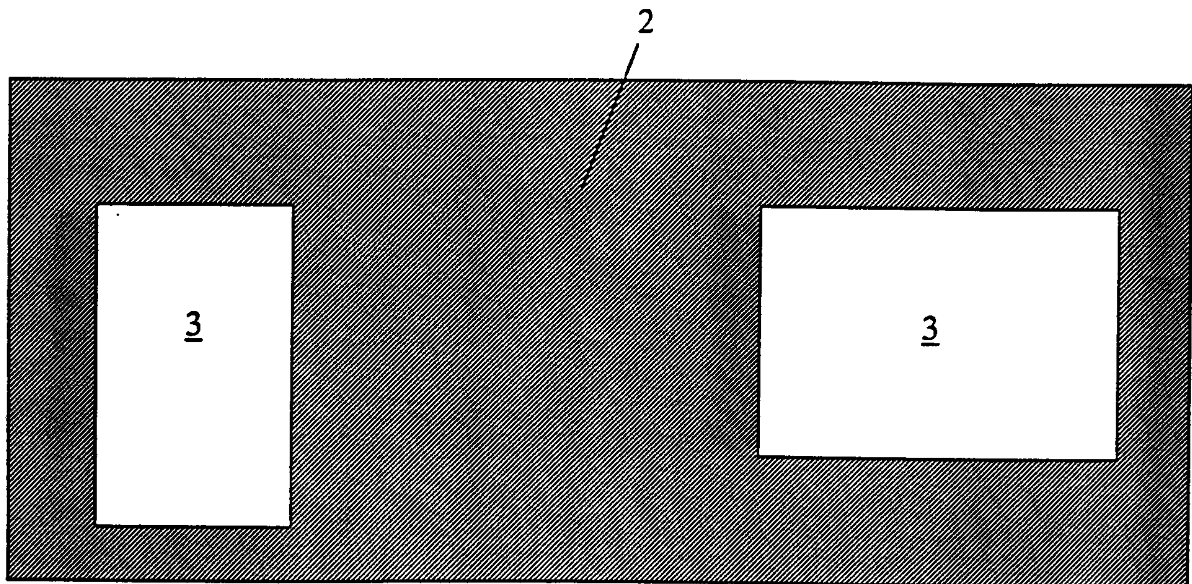


Fig. 2

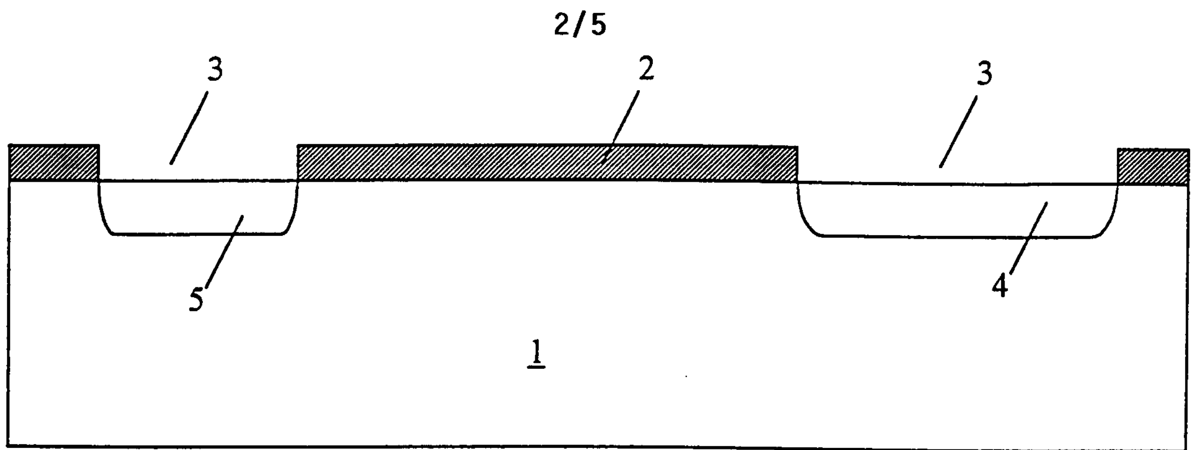


Fig.3

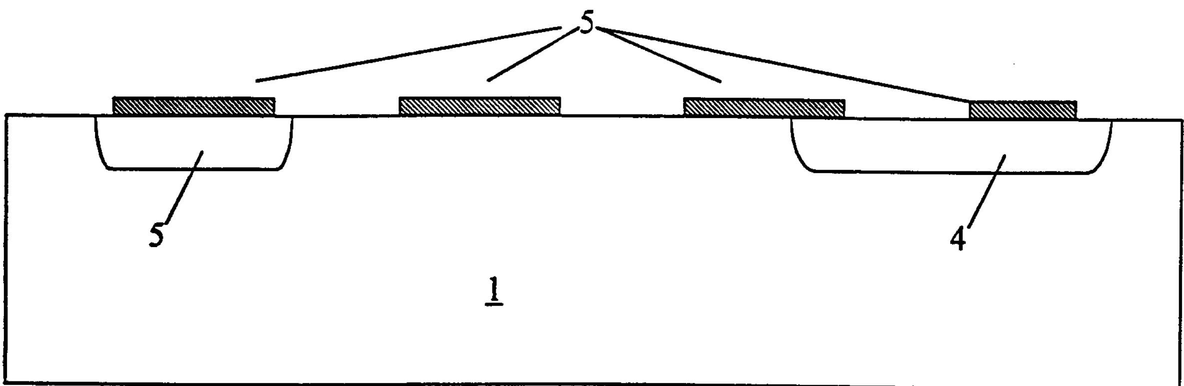


Fig. 4

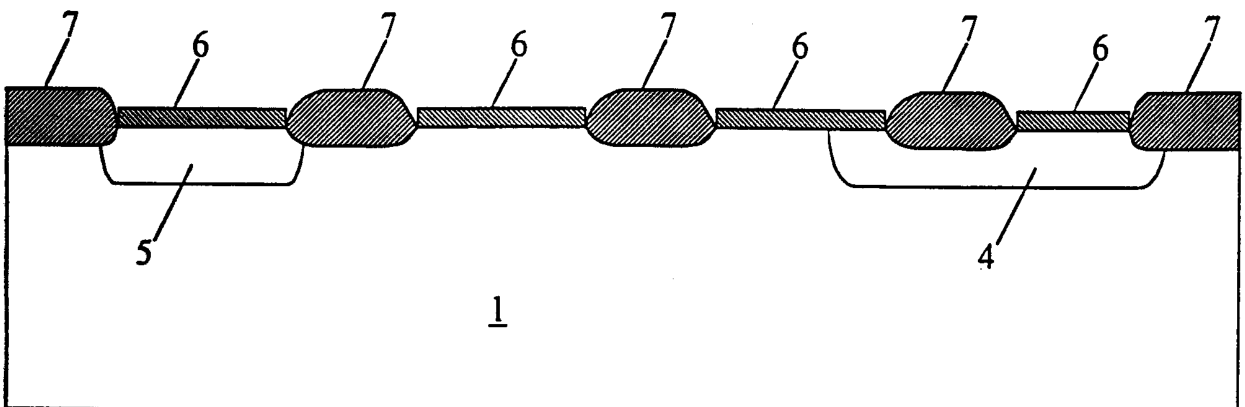


Fig. 5

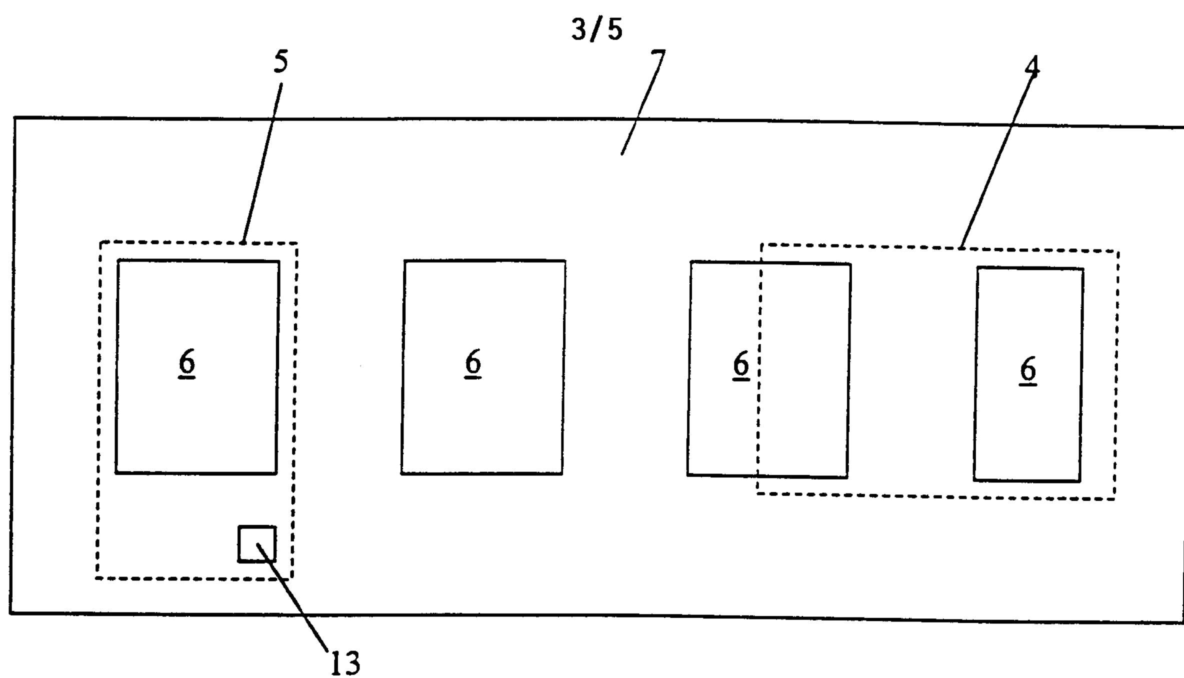


Fig. 6

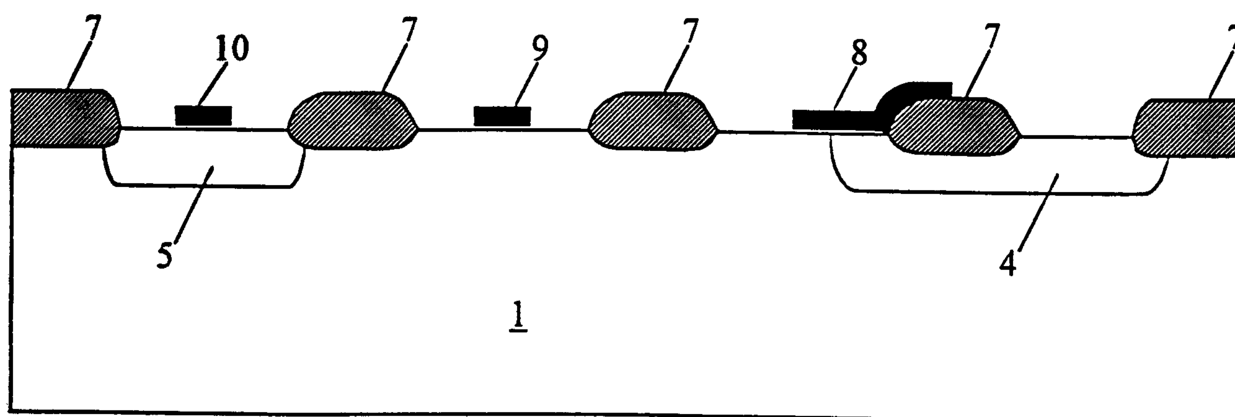


Fig. 7

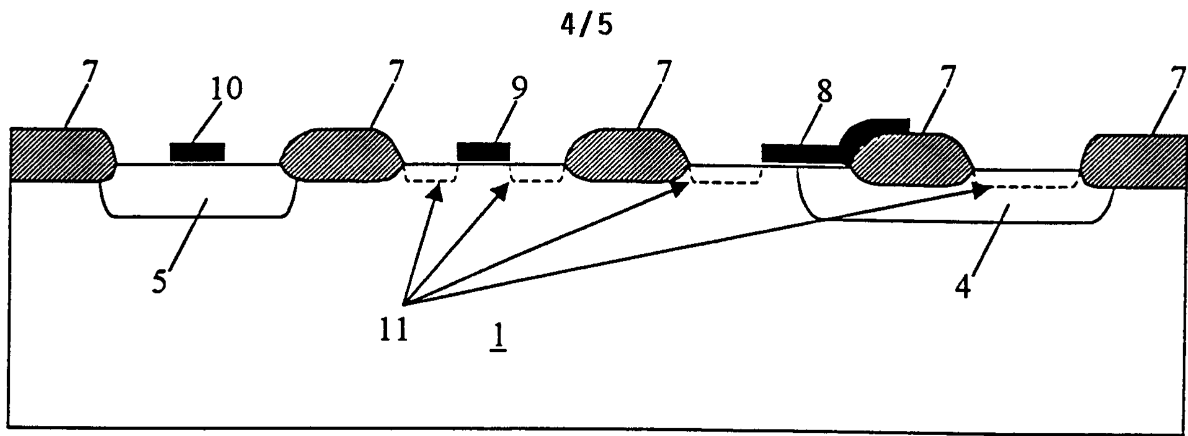


Fig. 8

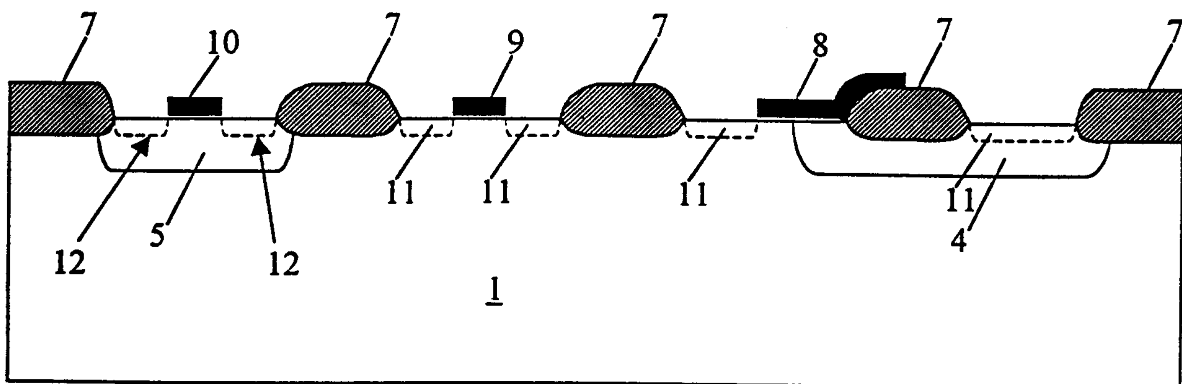


Fig. 9

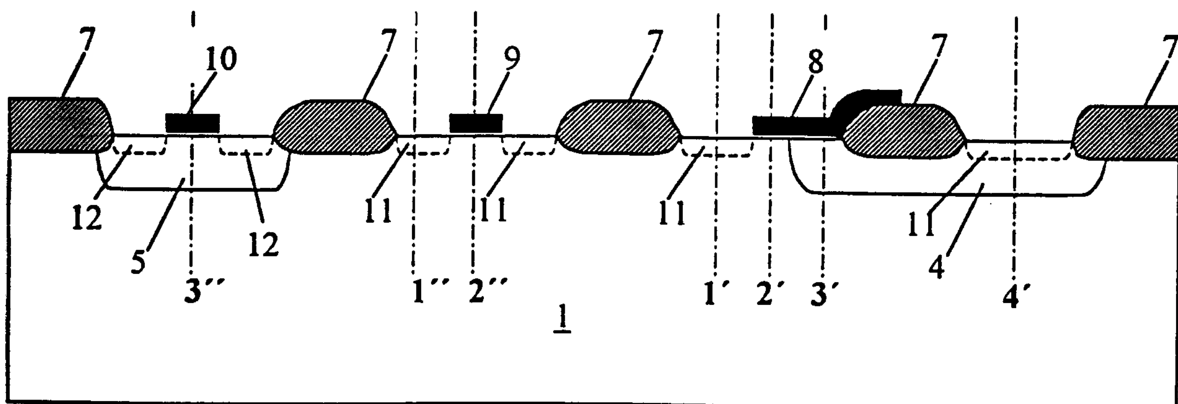


Fig. 10

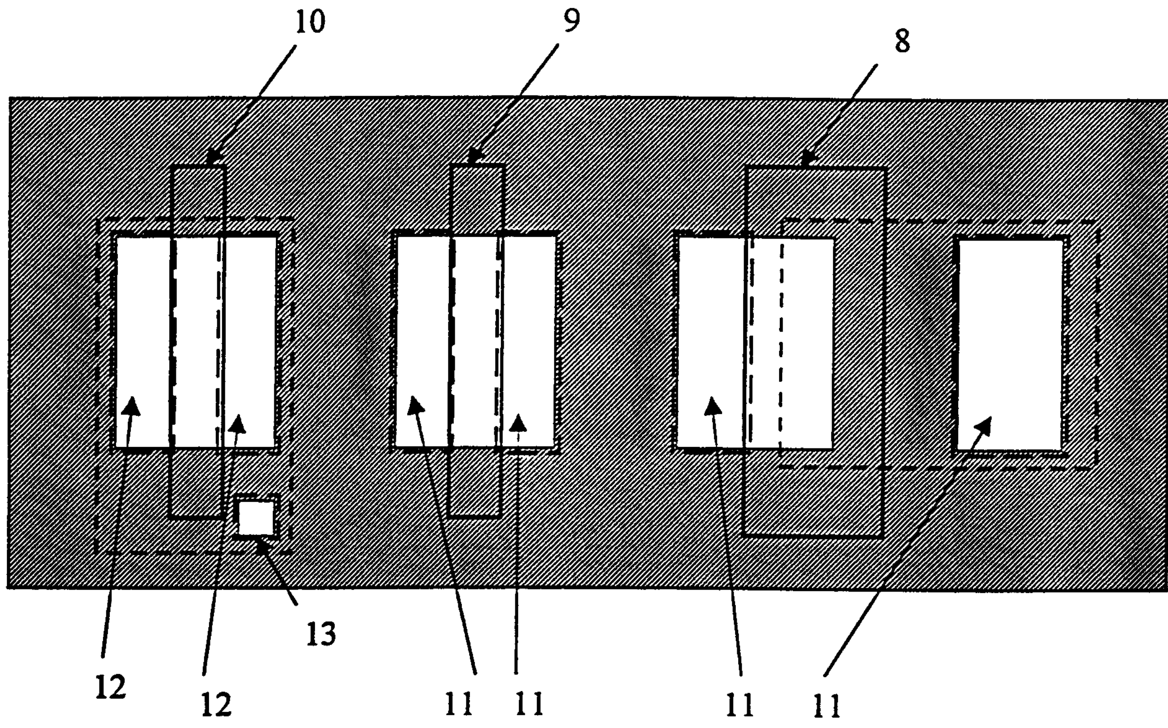


Fig. 11

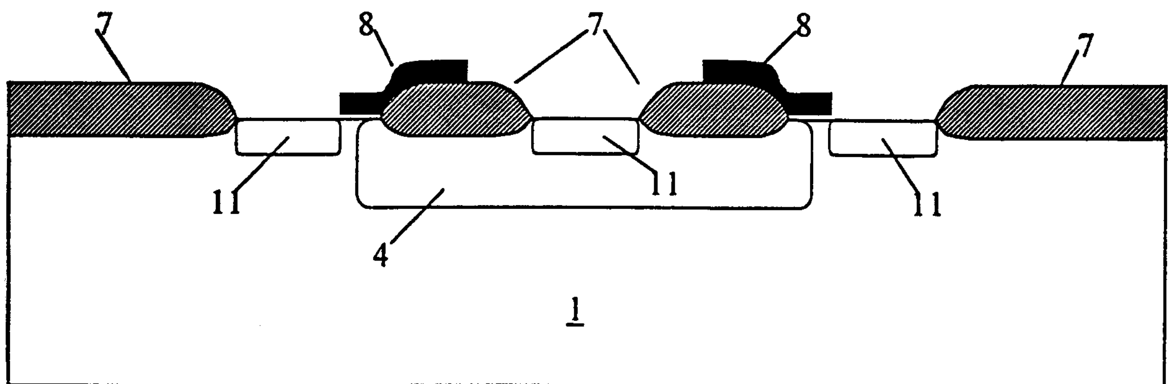


Fig. 12