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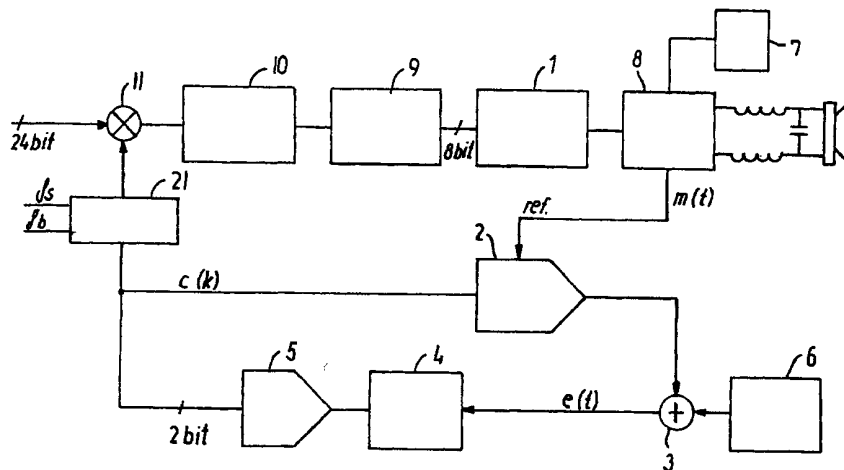
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(54) Title: A CIRCUIT FOR COMPENSATING NOISE AND ERRORS FROM AN OUTPUT STAGE OF A DIGITAL AMPLIFIER



(57) Abstract: In a digital amplifier of the PCM-UPWM type there is no negative feedback stage, which means that noise caused by the switching output stage of such an amplifier is directly affecting the audio signal. According to the invention, a regulation loop is inserted between the output and the input of the digital amplifier, said regulation loop being adapted to form a compensation signal $c(k)$ which is multiplied by the audio signal to compensate noise and errors from the switching output stage. In an embodiment, the regulation loop consists of a multiplying D/A converter (2) which is adapted to multiply the compensation signal $c(k)$ by a multiplicative error signal $m(t)$, and a summation unit (3), by summation of the output of the multiplying D/A converter (2) and a reference voltage (6), forms a second error signal $e(t)$ which is fed to a low-pass filter (4) that is fed to the input of an ADC circuit (5) to form the multiplicative error signal $c(k)$, which, optionally via a second adaptation filter (21), is fed to a multiplier (11) and the multiplying D/A converter (2). Expediently, the circuit of the invention is formed in full or in part by an integrated circuit.



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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/30

According to International Patent Classification (IPC) or to both national classification and IPC

E. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	WO 99 45641 A (TOCCATA TECHNOLOGY) 10 September 1999 (1999-09-10) page 1, line 6 - line 26 page 4, line 20 - line 29 page 8, line 12 - line 22; figure 1 abstract	1-19
A	US 4 495 470 A (BRISTOL LLOYD R) 22 January 1985 (1985-01-22) column 2, line 38 - line 62; figure 3 abstract	1-19
A	US 5 339 054 A (TAGUCHI TETSU) 16 August 1994 (1994-08-16) column 1, line 53 -column 2, line 60; figure 1 abstract	1-19
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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 396 190 A (MURATA TAKASHI) 7 March 1995 (1995-03-07) column 3, line 3 - line 68; figure 1 abstract	1-19
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