

[54] CONTROL CIRCUIT FOR VENDING AND
OTHER COIN CONTROLLED DEVICES

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[51] **Int. Cl.**..... **G07f 5/22**

[58] **Field of Search**..... 194/1 N, 1 M, 10, 9 R,
194/DIG. 3

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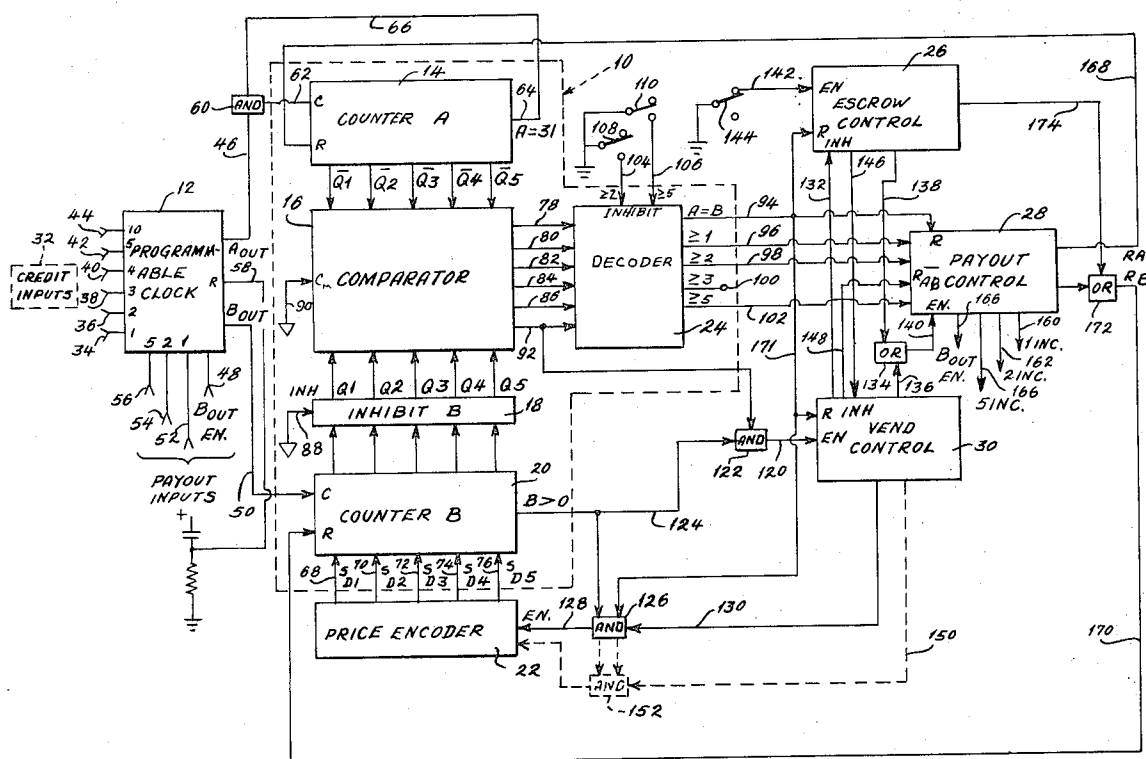
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[57] ABSTRACT

A control circuit for vending and other coin controlled devices, said circuit including separate counter means, one of which establishes a credit condition for moneys or other forms of credits deposited or otherwise entered and the other of which has the vend price as well as amounts accumulated in excess of the vend price entered in it to control refunding and escrowing. The circuit also includes means for comparing the amounts accumulated in the separate counter means for the purpose of controlling vending, payback of excessive deposits, counter reset and subsequent operations of the vending machine, and the circuit includes means which recognize, decode and make use of various relationships between the amounts accumulated in the separate counter means to control the paying out in particular coins, coin denominations and combinations thereof and in the least possible number of available coins. It is also an important feature that this present circuit makes use of integrated circuit elements which substantially reduce the number of circuit elements required and the size and space requirements for the circuit.

27 Claims, 5 Drawing Figures



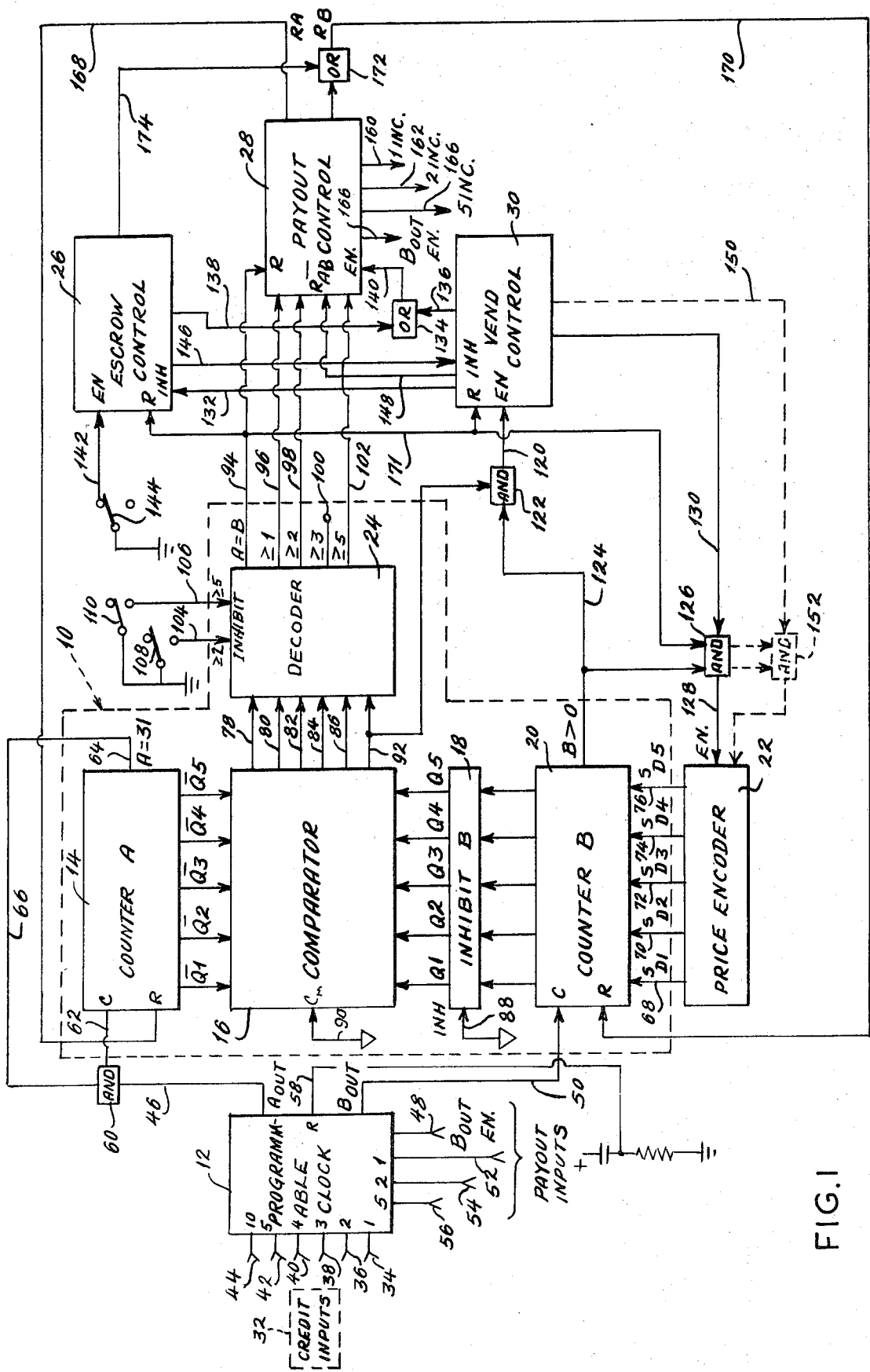


FIG. 1

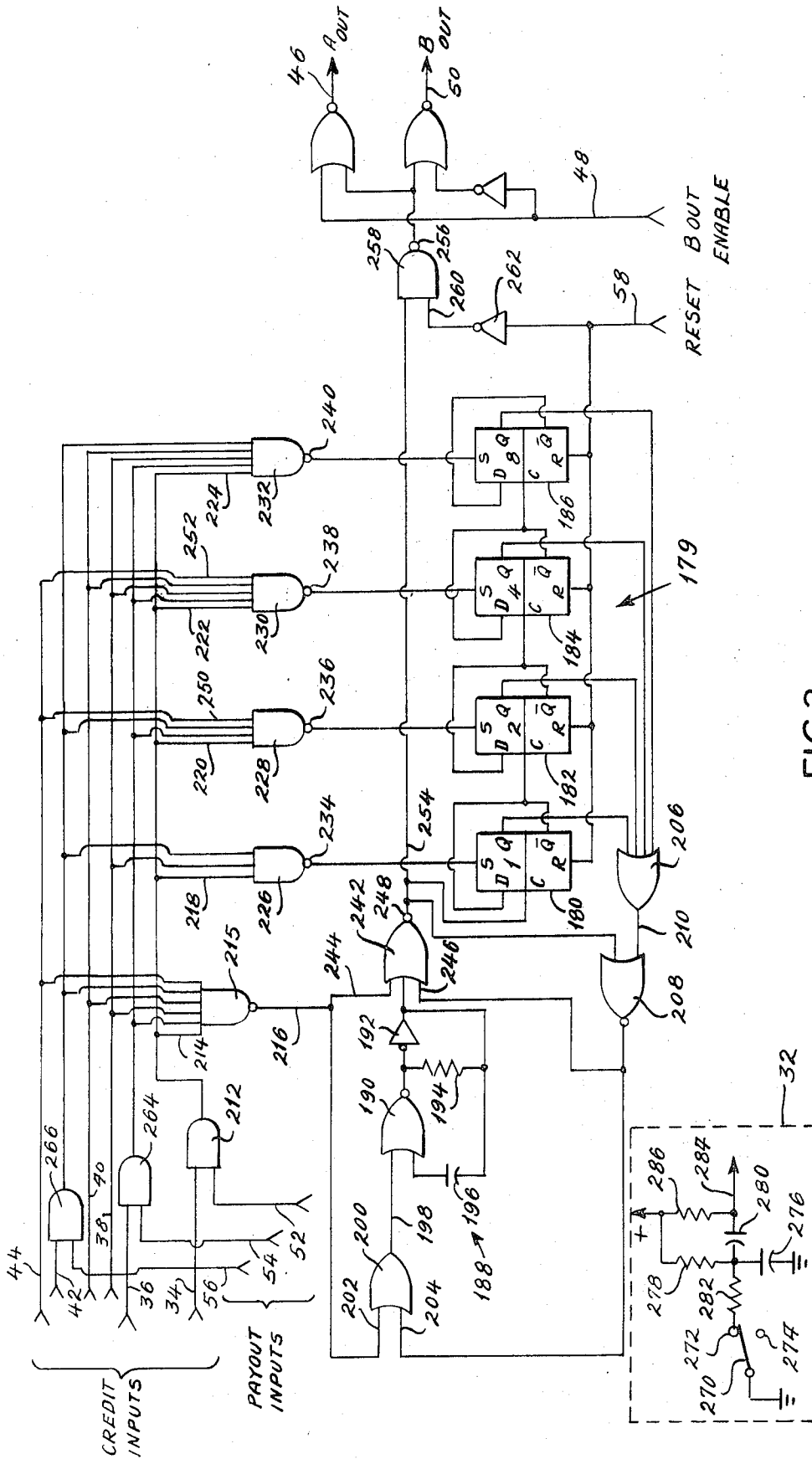
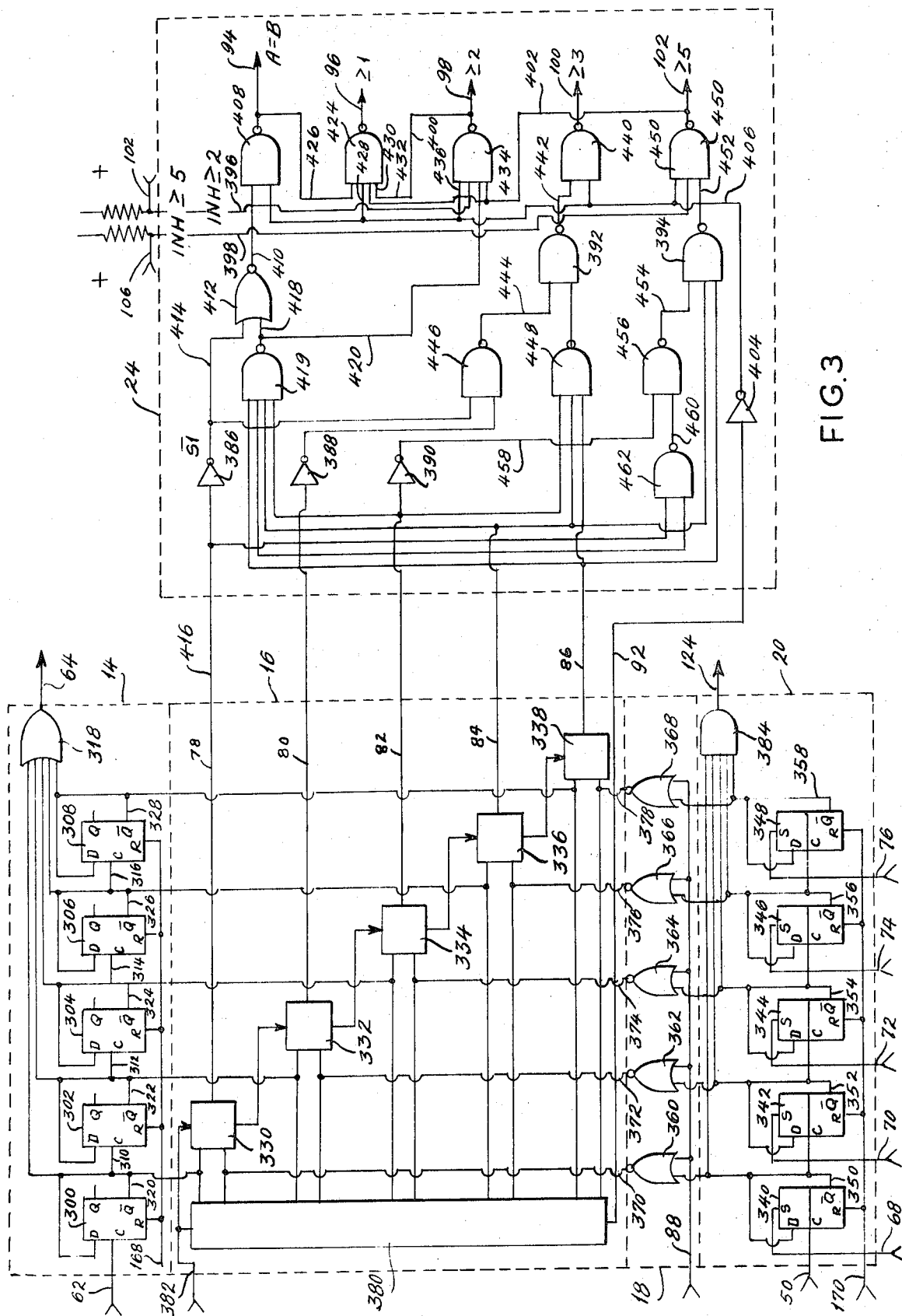


FIG. 2



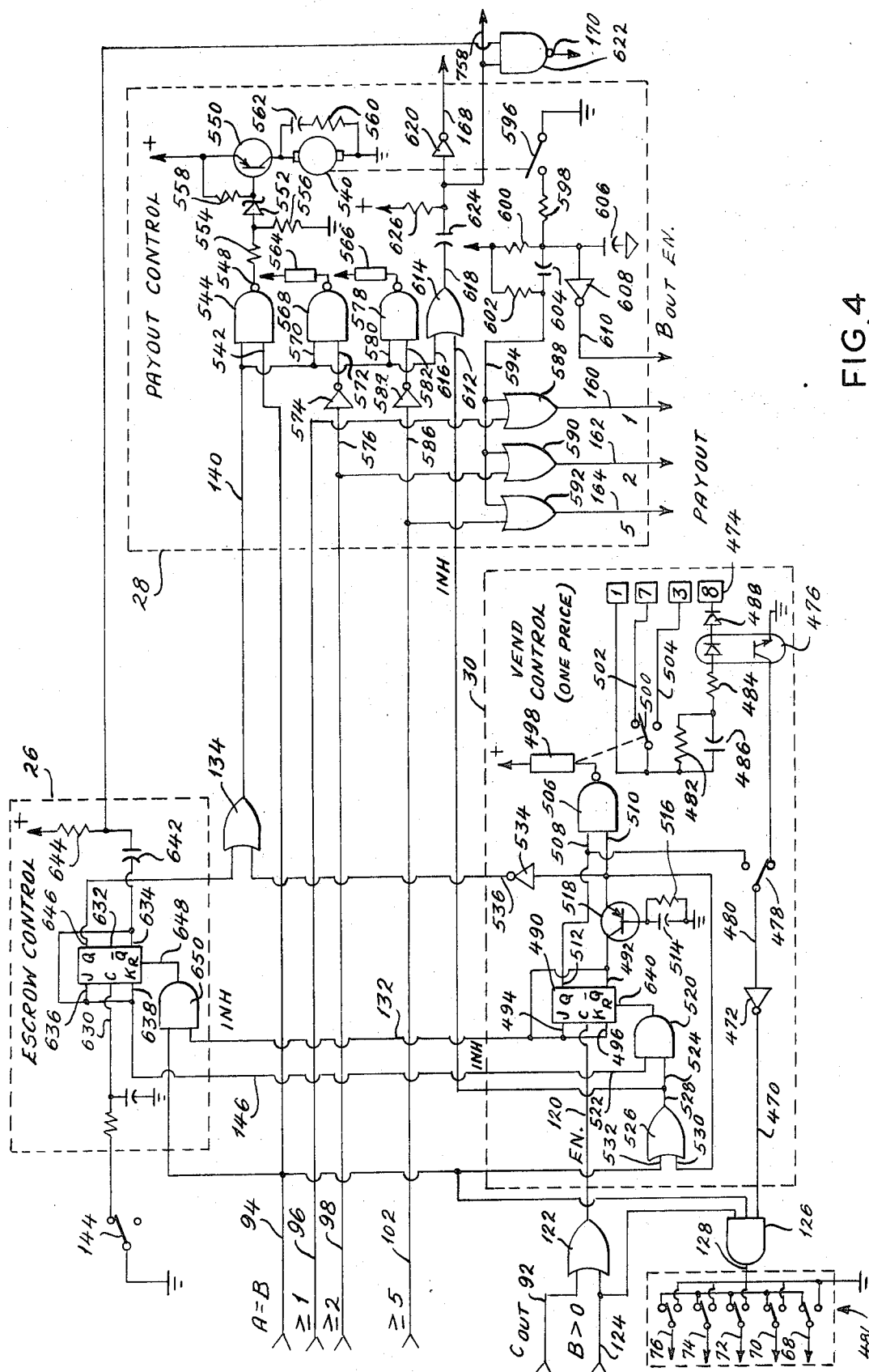


FIG. 4

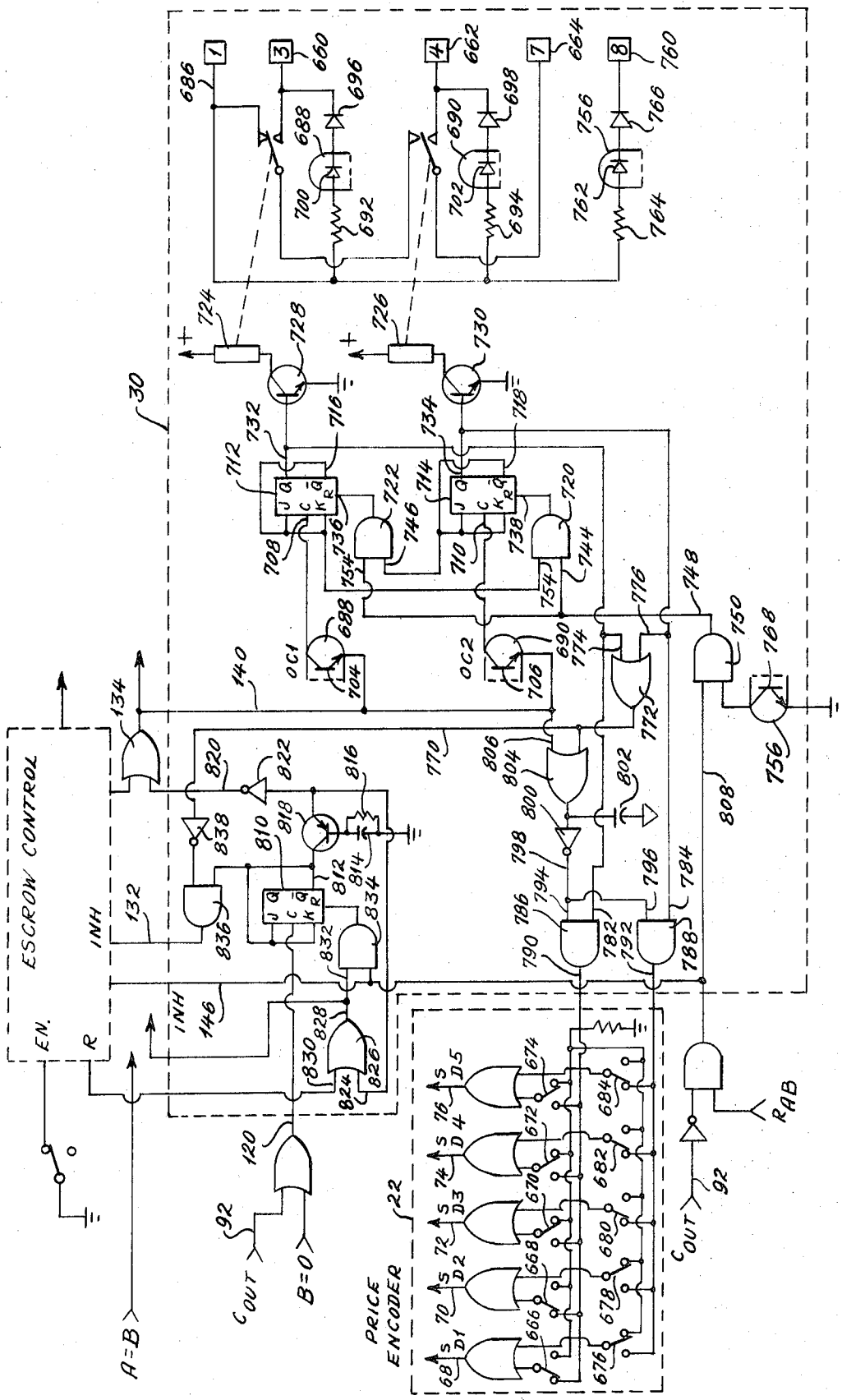


FIG. 5

CONTROL CIRCUIT FOR VENDING AND OTHER COIN CONTROLLED DEVICES

Many different electronic and mechanical control systems and circuits are in existence and have been used to control vending and other machines and particularly to control and to provide the various requirements for the vending of products and services and for the making of change and refunding. These include simple circuit means which cause vending upon accumulation of one or more coin denominations with the vending price usually not greater than the largest acceptable denomination coin. The more complex systems and devices include single sale price devices with change making capabilities wherein change is made by paying out coins of a single denomination, and devices are also known which have the capability of vending at more than one price and accepting and paying out or refunding coins of two or more denominations, and for change making and refunding or escrowing, as well as being able to perform other functions and combinations of functions.

The complexity and cost of the known circuits, devices and systems increases as they have added to them such capabilities as refunding deposits using the same or different coins sometimes called "escrowing" or until a particular product is selected for vending. An example of such a circuit is disclosed in Levasseur U.S. patent application Ser. No. 331,380. For an example of a circuit with multiple vend price selection capability, see Johnson U.S. Pat. No. 3,687,255; for a circuit with extended price and payback capability, see Douglass U.S. application Ser. No. 204,988; for a circuit control means capable of accepting and being used to accept almost any different combination of coin denominations including any of the various U.S. and foreign coin denomination systems, see Levasseur U.S. patent application Ser. No. 267,558; for systems capable of paying out change and refunds with the fewest possible number of coins and capable of switching to different coin payouts when the supply of one or more coin denominations has been depleted, see the same U.S. applications Ser. Nos. 204,988 and 267,558; and systems or circuits which have various forms of antichecking devices and features which add to their complexity are shown in many of the above and other patents and applications, all of which patents and applications as well as others, are assigned to Applicant's assignee. Other systems and circuits including those capable of accepting dollar bills and other paper money and systems capable of paying out three or more different denomination coins during refunding and escrowing are also known.

The devices disclosed in the above identified and other U.S. and foreign Letters Patent and pending applications have solved many of the problems of the vending industry and have substantially increased the flexibility and versatility of control devices and particularly control circuits for controlling vending machines and the like. However, it can be readily understood that to provide a single system or control which can accomplish all of the above mentioned requirements as well as others using conventional and existing technology would require very complex controls and circuitry and might not be advantageous from the cost standpoint particularly in relation to the less complex systems which provide a fairly broad range of capabilities with

a minimum of trouble but with some sacrifice in versatility and flexibility. By the same token there are some disadvantages particularly cost disadvantages in providing a separate system or control to satisfy each different requirement or combination of requirements. Inventory and technical requirements are both limiting factors in this regard. Furthermore, with the less versatile and less complex circuits and systems greater production volume can usually be obtained because of the reduced manufacturing costs involved and the lower selling price, and this makes them more readily available and more widely used.

The system and circuit disclosed in the present case achieves many of the desired results by using integrated circuits in a way which vastly increases the versatility and flexibility while at the same time providing a relatively simple arrangement and at a minimum cost and with a minimum of parts and equipment being required. Furthermore, the subject improved construction can be made to be extremely compact and lightweight and can be made to be relatively trouble free. To accomplish all of the above and other objectives as set forth, the present circuit provides means which reduce system costs by employing relatively large scale integrated circuit packaging which is designed to give the circuit versatility. The use of large scale integrated circuits also reduces the circuit design time, minimizes inventory requirements and reduces the number of circuit connections that must be made at the assembly site, and the subject circuit lends itself to being constructed to satisfy many different requirements and applications using the same basic building blocks and circuit connections. For example, the present circuit construction can be made to include means to accumulate the value of any combination of money deposits, it can include means to establish any desired vend price and to accumulate and control any required payouts using the same or separate accumulator means, it can be used to determine conditions of equality as well as various incremental differences between amounts stored in two or more accumulators, it can include means to control the payout of amounts deposited using the least number of coins available to achieve the payout, it can be interfaced with single as well as with multiple vend price machines, it can be used with control means capable of vending at one or more than one different vend prices, it can be used to refund accumulations until a vend selection is initiated, it can control the paying out of one, two or three different denomination coins, and can make refunds or escrows in the least number of coins, and it may include means for generating any number of pulses as required for the incremental value of credit accumulated when coins, tokens, credit cards or other means representing money are entered or deposited. The present control circuit can also be used to provide deposit refunding or escrowing, if desired, and so far as known, the present control circuit is the most versatile vending control circuit yet devised and represents a new generation of control circuit technology in the vending control field.

It is therefore a principal object of the present invention to provide improved and more versatile means for controlling the operation of vending machines and other coin and money controlled devices.

Another object is to provide an integrated circuit capable of being used to provide logic and arithmetic

functions in a vending control and refunding operation.

Another object is to provide a relatively inexpensive, compact, lightweight and trouble-free vending control circuit.

Another object is to provide means for refunding amounts accumulated in a vending machine until a product has been successfully selected at a time when the amount accumulated at least equals the cost of the selected product.

Another object is to minimize the possibilities for cheating a vending machine.

Another object is to eliminate the need for mechanical latching and lockout selection means which in the past has been required in control devices where one or more vend prices are available and selectable.

Another object is to provide improved means for accumulating and paying out or refunding amounts in various coins and coin denominations, including in any of the various coinage systems presently in existence.

Another object is to teach the construction and operation of a control circuit having integrated circuit portions which minimize the supporting circuitry required to be used in association therewith.

Another object is to simplify the circuitry and circuit design required in vending control devices and circuits.

Another object is to teach the construction and operation of a relatively versatile integrated circuit for use in vending control circuits and the like.

Another object is to teach the construction of a relatively simple component or integrated circuit chip which has both logic and accumulation capabilities.

These and other objects and advantages of the present invention will become apparent after considering the following specification which covers several preferred embodiments thereof in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic block diagram showing the more important circuit components and the connections therefor of a versatile vending control circuit constructed according to one form of the present invention;

FIG. 2 is a more detailed circuit diagram of the programmable clock portion of the circuit shown in FIG. 1;

FIG. 3 is a more detailed circuit diagram of those portions of the circuit shown in FIG. 1 that are included within the dashed line identified therein by the number 10;

FIG. 4 is a detailed circuit diagram showing more of the circuit details of the escrow control, payout control, and vend control portions of the circuit shown in FIG. 1; and,

FIG. 5 is a diagram similar to that shown in FIG. 4 but for use on a vending machine capable of vending at two or more different vend prices.

Referring to the drawings more particularly by reference numbers, number 10 in FIG. 1 identifies that portion of the subject control circuit which is totally integrated and is included in a single package or chip. The circuitry included in the outline 10 may be similar for both embodiments of the present construction that are disclosed including the embodiment which includes those portions disclosed in the one-price construction

of FIGS. 1-4 as well as in the circuit shown in FIG. 5.

The block form of the circuit shown in FIG. 1 is made up of a plurality of different circuit portions each of which will be described in detail hereinafter. The principal circuits or circuit portions include a programmable clock circuit 12, a counter or accumulator circuit 14, sometimes called the A Counter, a comparator circuit 16, an inhibit circuit 18, a second counter or accumulator circuit 20, sometimes called the B Counter, a price encoder circuit 22, an output decoder circuit 24, an escrow circuit 26, a payout control circuit 28 and a vend control circuit 30. In the circuit as shown in FIG. 1, the circuit portions 14, 16, 18, 20 and 24 are preferably all included in a single integrated circuit member or chip referred to generally by the number 10. This integrated circuit will have output connections which can be connected into the circuit in different ways to enable it to be used to perform many different functions and combinations as will be explained. This substantially reduces the size and expense of the subject circuit while at the same time making the circuit extremely flexible and versatile. In the detailed specification which follows the individual more important circuit components will be described individually in detail, and subtitles will be used for ease in referring to and finding the various descriptions.

PROGRAMMABLE CLOCK

The programmable clock 12 is constructed to provide a proper number of pulses for the credit inputs which are received from a coin unit or other similar input device including any input unit capable of receiving coins, tokens, paper money, credit cards and other similar devices. The credit input means are indicated generally by number 32 and have a plurality of output connections which are connected to corresponding inputs to the programmable clock circuit 12. In the drawings, the inputs to the clock unit are labeled 34, 36, 38, 40, 42 and 44. The actual input connections between the credit unit 32 and the programmable clock unit 12 may be made by various types of interfacing means including electric connections, magnetic connections, optical interfaces and so forth.

When an input is received at the input terminal 34, the programmable clock unit provides one output pulse which appears on output lead 46 which is the A output lead. This output can represent a penny, a nickel or any other basic unit of credit, including basic units of foreign money as well. Whenever an input is received at the input connection 36, two output pulses are produced on the clock output lead 46, representing twice the basic unit. Similarly, an input on the input lead 38 produces three outputs on clock output lead 46, an input at the input connection 40 produces four outputs on clock output lead 46, an input on the input lead 42 produces five outputs, and an input on clock input lead 44 produces ten output pulses on the output lead 46. Obviously a greater or lesser number of clock input and output pulse combinations can also be provided as desired. The clock outputs available on the lead 46 in the circuit as shown are available whenever another input to the programmable clock 12, namely, an input on lead 48 (labeled Output Enable Input) is in a particular state such as in a low voltage state. When the input at the lead 48 is at a high state or high voltage condition then the clock pulses from the programmable clock 12

will exit from another output lead 50 which is labeled the B output lead.

The programmable clock 12 has other input leads labeled payout inputs 52, 54 and 56, and these can be used for generating one, two or five pulses respectively to control the paying out of change. One, two and five in the case shown represent respectively the paying out of nickels, dimes and quarters. These inputs are connected to other locations in the circuit which will be described later. It is sufficient at this point to recognize that the programmable clock 12 is in the nature of a controllable pulse generator which receives input pulses when coins or other forms of credits are deposited or otherwise entered in the vending machine according to the amount of the deposit, and it also includes means responsive to other means which control the amount of money by coin denomination to be refunded for each amount entered that is in excess of a selected vend, or to make a total deposit refund or escrow when a customer after making a deposit decides for some reason not to carry through with a vend. This can occur because the customer changes his mind after making a partial deposit, discovers that he does not have enough money to complete a desired vend, discovers that the supply of the product he wishes to purchase is exhausted in the vending machine, or for some other reasons decides that he wants his deposit back.

In addition to the connections to the programmable clock circuit discussed above, the clock circuit has another input 58 which is its reset input. When this input is held at a high state, it stops any clock pulses from being programmed and/or from being generated. A control circuit such as a vend control circuit with a programmable clock such as the clock 12 provides an extremely versatile and flexible means to control and keep track of amounts deposited and refunded, and it does so by means that are adaptable for use with any of the known existing coinage systems in use in the world.

COUNTER AND COMPARATOR CIRCUITS

The A counter circuit 14 receives inputs as aforesaid from the programmable clock circuit 12 on lead 46. These pulses from the clock circuit are fed to one terminal of an AND gate 60 which has its output connected by lead 62 to the input or count terminal of the counter 14. The counter 14 also has an output terminal which is labeled 64 and is connected by another lead 66 to the other input of the AND gate 60. The output terminal 64 has a signal produced on it whenever the count in the counter 14 reaches some predetermined maximum count such as 31 in the case shown. A count of 31 is the maximum possible count for a five stage binary counter and is obtained by adding the possible counts for the stages of 1, 2, 4, 8 and 16. When a count of 31 is reached a signal will be produced at the output terminal 64 and on the lead 66 to prevent the AND gate 60 from enabling the outputs produced by the clock circuit 12 from being fed to the A counter 14. This prevents further accumulation beyond the binary limitation which otherwise would result in the loss of 31 counts or credit increments.

The means by which a sufficient credit accumulation for a given vend is determined is accomplished by means of the price encoder circuit 22 which is constructed and connected to directly set into or transfer into selected ones of the binary stages of the B counter

circuit 20 by way of its input leads 68, 70, 72, 74 and 76 the amount of a selected vend price. The leads 68-76 encode into the respective stages of the counter 20, one, two, four, eight and sixteen increments or any combination thereof. The counter circuit 20 also has output connections from each of the respective stages which are connected to the inhibit circuit 18, and from there to corresponding inputs of the comparator circuit 16. In addition, the counter 20 has an input which is connected to the output of the programmable clock circuit 12 on clock output lead 50.

The purpose of the comparator circuit 16 is to add the binary complement (inverted amount entered therein) from the counter circuit 14 to the binary amount in the corresponding stages present at the output connections of the counter circuit 20 to produce a resultant binary summation of these two amounts. This summation appears on output terminals 78, 80, 82, 84 and 86 of the comparator circuit 16. The output signals which appear on these leads are fed to the decoder circuit 24 and are represented therein as the incremental difference between the amounts accumulated in the counters 14 and 20.

The inhibit circuit 18 is a gate type circuit and is included to provide means to decode the amounts accumulated in the accumulator 14 irrespective of the condition of the counter circuit 20. The inhibit function occurs whenever the input to the inhibit circuit 18 is at a high voltage state. The input lead to the inhibit circuit 18 is identified as lead 88 and this is shown grounded as is another lead 90 which is connected to another control input of the comparator circuit 16. Either or both of these connections may optionally include means to make them go high under certain conditions and to satisfy other design requirements (not shown). The comparator circuit 16 also has a carry output lead 92 which is at a low state at all times except at times when the amount accumulated in the counter 20 is greater than the amount accumulated in the counter 14. In the present circuit the counters 14 and 20, the comparator circuit 16, the inhibit gate circuit 18, the decoder circuit 24, and the internal circuitry associated therewith are preferably all included in a single, relatively small and compact integrated circuit member or element. The details of these circuits are shown in the drawings and will be described more in detail in connection with FIG. 3.

DECODER

The decoder circuit 24 is in the output of the comparator circuit 16 and produces outputs which control the operation of certain other circuit portions and devices including devices on the vending machine. As explained above, the decoder circuit 24 has a plurality of input connections some of which are connected to the output leads 78-86 of the comparator circuit 16 and the decoder has an input connection to the carry output lead 92 from the comparator circuit and it has a plurality of output leads 94, 96, 98, 100 and 102. These leads go to low conditions when they are active. The output lead 94 goes to a low condition whenever the A counter 14 has an amount accumulated therein that exactly equals the amount that is accumulated in the B counter 20. This is illustrated in the drawing by the expression $A = B$ adjacent to the lead 94. In a similar manner, the voltage on the encoder output lead 96 goes low whenever the amount accumulated in the counter 14 is one

or more increments greater than the amount accumulated in the counter 20, the voltage on the output lead 98 goes low whenever the amount entered in the counter 14 is two or more increments greater than the amount in the counter 20; the voltage on the output lead 100 goes low whenever the amount entered in the counter 14 is three more increments greater than the amount in the counter 20; and the voltage on the lead 102 goes low whenever the counter 14 has in it five or more increments more than are entered in the counter 20. Only one of the encoder output leads 94, 96, 98, 100 or 102 can be at a low condition at any one time, and the highest detected incremental difference between the amounts entered in the counters will prevail. That is, if the condition exists for an output on the lead 102 to be low, this will prevail and take precedence over possible lows which may also exist on the other three output leads 96, 98 and 100, and so forth.

The encoder circuit 24 has two other inhibit input connections, one being an inhibit input described as a "two or more input" inhibit which appears on lead 104 and the other is described as a "five or more input" inhibit which appears on lead 106. When either of the leads 104 or 106 is at a low state due to closure of a respective empty coin switch 108 or 110 they operate to prevent the encoder output leads 98 and 102 from being operative, and they also enable another next highest incremental difference encoder output lead to assume control. In the circuit as shown, the encoder output lead 100, which is the three or greater encoder output lead, is shown to be independent of the other decoder output leads, and this lead is not connected in the present circuit. This is done because the circuit as shown is wired primarily to accommodate a monetary system such as that used in the United States where one increment represents a nickel, two increments represent a dime, and five increments represent a quarter. In monetary systems where different combinations of increment values are used it may be necessary to use the lead 100 and to provide another associated inhibit input connection. In such a case, it may also be necessary to provide an additional coin switch corresponding to the different value coins.

VEND CONTROL

The vend control circuit 30 is enabled by signals it receives on lead 120 which is the output lead of AND gate 122. The AND gate 122 has two input connections, one of which is connected to the carry output 92 of the comparator circuit 16 and the other to the output of the B counter 20 which receives a signal whenever the counter 20 has an amount accumulated that is greater than zero. The counter input to the AND gate 122 is on lead 124 and is an indication of the presence of an encoded price. A carry output from the comparator circuit 16 on the carry output lead 92 indicates that the A counter 14 has an amount accumulated at least equal to the amount accumulated in the counter 20. When these conditions exist at the same time, the AND gate 122 will produce an output signal which enables the vend control 30.

The vend control 30 provides output which are indications of product selection and are fed through another AND gate 126 to gate output lead 128, see FIGS. 1 and 4. The AND gate 126 has three inputs, one of which is the same as that which is connected to the input of the AND gate 122 on lead 124, the second is

on lead 130 which is an output lead of the vend control circuit 30, and the third is on the lead 94 which is the counter equality $A = B$ output lead of the decoder circuit 24. The AND gate 126 is satisfied whenever the B counter 20 has no accumulation so that there is a signal on the lead 124 and when at the same time the A counter 14 has an amount in it that is not equal to the count in the B counter 20 as indicated by the signal present on the lead 94. When the vend control circuit 30 is enabled by receiving an input at the lead 120, it initiates a vend delivery function and it also operates to inhibit the escrow control 26. Inhibiting an escrow is accomplished by producing an output signal in the vend control 30 for feeding to the escrow control 26 on lead 132. In this way also the payout control circuit 28 is enabled through a circuit which includes an OR gate 134 that has two input connections, one of which receives outputs from the vend control circuit 30 on lead 136, and the other input is from the escrow control circuit 26 on the lead 138. When either of the inputs to the OR gate 134 on leads 136 or 138 is present, the OR gate 134 will produce an output on its output lead 140 for feeding to and enabling the payout control circuit 28. The escrow control circuit 26 and the payout control circuit 28 both have reset input connections which are connected to the equality $A = B$ output lead 94 of the decoder circuit 24 for reset purposes. In addition, the escrow control circuit 26 has a switch operated enable input 142 which is connected to be operated by actuation of an escrow switch 144. The escrow control circuit 26 also has an inhibit output lead 146 which is connected to an inhibit input to the vend control circuit 30. This connection like the inhibit input provided by signals on the lead 132 prevents a vend control circuit 30 from operating and producing a vend whenever the escrow control 26 is actuated. The same is true but in reverse sense whenever the vend control circuit 30 is operated first. The details of the escrow circuit 26 are shown in FIGS. 4 and 5 and will be described later.

The payout control circuit 28 has input connections respectively connected to the output leads 96, 98 and 102 of the decoder circuit 24. In addition, another input connection is provided from the vend control circuit 30 on lead 148. This latter connection operates to reset the payout control circuit 28 whenever the vend control circuit 30 receives identical inputs from the counter circuits 14 and 20 indicating equality. This is indicated on the drawing by the legend R_{AB} . The vend control circuit 30 has a second output connection to the price encoder circuit 22. This is an optional connection and is shown as including lead 150 and AND gate 152 (FIG. 1). This connection is included whenever additional price encoding means are required as is true in systems that have the capacity for vending at more than one vend price.

PAYOUT CONTROL

The payout control circuit 28 provides means to control the paying out of coins to the customer of amounts which represent accumulations in the counter 14 in excess of the vend price as established and encoded in the number of coins that will be paid out by signals it receives on the leads 96, 98 and 102 in the output of the decoder circuit 24. For example, a signal on the lead 96 calls for a payout of one coin increment, a signal on the lead 98 calls for a payout of a coin of two increments value, and a signal on the lead 102 calls for a payout of

a coin representing five increments. As each coin is paid out the programmable clock circuit 12 is actuated to direct an appropriate number of pulses to the counter 20. The connections between the payout control 28 and the clock 12 are fed by way of leads 160, 162 and 164, which leads are connected respectively to the clock input lead 52, 54 and 56. The lead 160 is the one increment lead, the lead 162 is the two increment lead and the lead 164 is the five increment lead, one, two and five representing nickels, dimes and quarters respectively in the circuit as shown. When outputs appear on any one of these leads, the clock 12 will be energized to produce a corresponding number of outputs on the clock output lead 50 which is the connection to the counter 20. It is possible at this time to feed impulses to the counter 20 over this connection because the input lead 48, which is the B counter enable input to the clock 12, is caused to go to a high condition under control of the connection from the output enable connection 166 of the payout control circuit 28.

During payout operations, the clock pulses are directed to the B counter 20 rather than to the A counter 14, and this continues to be true until the counter 20 has an amount accumulated in it that is equal to the amount accumulated in the counter 14. Both of these amounts are represented in binary form as indicated above. When this happens an equality output appears on the decoder output lead 94 which causes the voltage on the lead 94 to go low. It is then possible to reset the payout control circuit 28. This condition also establishes circuits to reset the counters 14 and 20. The resetting of the A counter 14 takes place through lead 168 connected to an output of the payout control 28. The resetting of the B counter 20 takes place through another lead 170 which receives outputs from either the escrow circuit 26 or from the payout control circuit 28. The lead 170 is connected to the reset control input of the B counter 20. At the same time the equality decoder output lead 94 applies another reset signal to the reset input of the vend control circuit 30. This reset signal is applied by way of another lead 171 if the vend time has elapsed. When the vend control circuit 30 is reset its output lead 148 goes low, and this inhibits the resetting of the counters 14 and 20 by way of the payout control 28 until after the vend time is over. As will be explained, the reset output produced on the equality (A = B) lead 94 also operates to reset the escrow control 26.

ESCROW CONTROL

The escrow control 26 is disclosed in detail in FIG. 4 and provides the means in the subject circuit whereby a customer may obtain a complete refund of any deposit or accumulation present in the counter 14 as long as the inhibit input thereto on lead 132 from the vend control circuit 30 is not operating to prevent escrow. In order for the escrow means to be effective the equality output lead 94 of the decoder circuit 24 should not be indicating equality. If these conditions are satisfied an escrow operation can be initiated at any time by the customer activating the escrow switch 144. When the escrow switch 144 is activated the escrow control circuit 26 operates to inhibit operation of the vend control circuit 30 by a signal that is produced on the inhibit output lead 146, and at the same time the escrow control circuit produces an output on the lead 138 which is applied to one of the inputs of the OR gate 134 and

to the input of the payout control circuit 28. The energizing of the escrow control 26 also produces another output on lead 174 and this output is applied to the OR gate 172 and from there to the reset input of the counter 20 as already described. With these conditions established by operation of the escrow control 26, the payout control circuit 28 is set to control the paying out of coins until the B counter 20, which now starts in reset direction, is clocked to a count condition that is equal to that count accumulated in the counter 14. When this condition is reached, an output low condition will appear on the equality output lead 94 of the decoder circuit 24 to thereby reset the escrow control 26, the payout control 28, and in turn the counters 14 and 20 as aforesaid.

To this point, the description has given a clear but to some extent broad understanding of the structural and operational details of the subject circuit and a more detailed description follows. It should be apparent also that many of the circuits and components including the counters, the comparator, the inhibit means, and the decoder means are capable of being packaged as integrated circuits in a substantially miniaturized form and this can be done by including all of these and other of the circuit elements in the same or in several integrated circuit blocks or chips. By so doing, the same basic building block can be used to fabricate control circuits having many different capabilities and connection possibilities including circuits capable of operating at one or more vend prices, circuits capable of refunding in one or in several different coin denominations including refunding in the fewest possible coins, circuits capable of providing complete escrow capability, and circuits capable of determining the amount of overage of each deposit for payback purposes based on the price of a selected vend. So far as known, no known control circuit has these capabilities and versatilities and therefore it is believed that this circuit and its construction represents a new generation of control circuits for the purposes indicated. The following portions of the specification describe in even greater detail the circuit construction and operating characteristics of the more important components of the subject circuit. This includes a description of a single price construction (FIG. 4) and a two or multiple price construction (FIG. 5).

PROGRAMMABLE CLOCK DETAILS

The details of the programmable clock circuit 12 are shown in FIG. 2 of the drawings. The clock 12 as shown includes a four stage binary counter 179 constructed of four D-type flip-flop circuits 180, 182, 184 and 186. These flip-flops are clocked by an oscillator circuit 188 which includes a NOR gate 190, an inverter 192, a resistor 194 and a capacitor 196 connected as shown. The oscillator circuit will clock whenever the input on its input lead 198 is at a low condition. The oscillator input lead 198 is the output lead of OR gate 200, and goes low whenever the OR gate 200 has a low on either of its two inputs 202 and 204. The gate input lead 204 is high whenever the clock binary counter 179 is reset and causes a low condition on each input of OR gate 206. The inputs to the OR gate 206 are connected respectively to the Q output terminals of the binary stages 180, 182, 184 and 186. This in turn produces a low at the corresponding input to another NOR gate 208 on its input lead 210.

When a low condition is present on the clock input lead 34 it is applied as one of two inputs to an AND gate circuit 212, and the output of the gate 212 is connected to one of a plurality of inputs 214 of another AND gate 215. These conditions cause the output of the AND gate 215 on lead 216 to go high. Since the lead 216 is connected as one of the two inputs to the OR gate 200, when the signal on the lead 216 is high it will operate to inhibit operation of the clock. At the same time, and while the input on the lead 214 is low, the same low will also be applied as inputs on other gate input leads 218, 220, 222 and 224 of respective NAND gates 226, 228, 230 and 232, each of which has its output connected to a respective SET input of one of the clock flip-flops 180, 182, 184 and 186. When these conditions exist, they cause the gates 206 and 208 to apply a low condition to the NOR gate 200 on the input lead 204.

Thereafter, when the condition on the clock input lead 34, which is the clock input lead that programs one clock pulse, returns to its high state, the inputs to the gate 200 on input leads 202 and 204 will cause a low condition to occur on the input lead 198 of the gate 190 and this input condition will allow the clock 12 to oscillate. Another NOR gate 242 is connected to the oscillator circuit and has two of its three input connections 244 and 246 connected respectively to the input leads 202 and 204 of the gate 200. When these input leads are low the output gate connection 248 will clock and continue to do so until all of the inputs to the OR gate 206 go low. This will occur for the case illustrated where there has been an input on the clock input lead 34 after one clock pulse because in this condition it is the next binary state after the set condition of the binary circuit 180-186.

In similar manner, when a pulse train of ten pulses is required, a momentary low will occur at the clock input 44 instead of at the clock input 34, and this will start the clock with a preset count of 6 as set by the signals on input leads 250 and 252, respectively, of the NAND gates 228 and 230. For this condition, the oscillator circuit will be required to clock ten pulses until the output lead 204 of the gate 208 changes its state. During this clocking the first binary stage 180 of the clock counter 179 receives inputs on lead 254 which lead is connected between the output of the gate 242 and the D input of the first stage flip-flop 180. At this time, the output lead 46, which is the lead that connects the clock 12 to the counter 14 will have clock pulses on it if the input enable connection 48 from the output lead 166 of payout control circuit 28 is at a low condition. If the B output enable lead 48 is at a high condition instead of a low condition then the outputs of the clock 12 will be fed instead to the B counter 20 on the lead 50.

By setting the binary clock stages 180, 182, 184 and 186 to a count short of 16, which is the reset count, the clock will provide an output equal to the number of pulses that exists between the two states. For example, setting a count of 11 will require five clock pulses to reach the sixteenth or reset pulse state. Whenever a high is introduced at the clock reset lead 58, it will cause the four binary stages 180, 182, 184 and 186 of the clock circuit 179 to reset even if the clock has not completed its normal operation. This provision is included to prevent any output from being produced on the output connection 256 of NAND gate 258 in the

output of the clock 12 (FIG. 2). This is because the NAND gate 258 receives a low at its other input 260 which is connected to the reset circuit. This connection includes an inverter 262 which has its input side connected to the clock reset input connection 58. The clock reset lead 58 is also connected directly to all of the reset inputs of the clock binary stages 180, 182, 184 and 186. The AND gate 212 which is connected to the clock input 34, as well as other similar input AND gates 264 and 266 in the credit input circuits of the clock 12 are connected to the one, two and five increment inputs, respectively, of the clock circuit 12, and these gates are included simply to provide isolation for the respective credit inputs and also for the associated inputs to the clock from the payout circuit 28 which are received on the leads 52, 54 and 56.

A preferred form of the credit input circuit 32 is shown in FIG. 2. The credit input circuit 32 includes a coin actuated switch 270 which, when transferred from engagement with normally closed switch contact 272 to engagement with normally open contact 274, allows a capacitor 276 to charge relatively slowly through a circuit which includes resistor 278 selected because it has a relatively high resistance. The operation of the switch 270 allows another capacitor 280 to equalize its charge to the charge on the capacitor 276. Subsequently, when the switch 270 returns to its deactivated condition in engagement with the normally closed contact 272, the capacitor 276 will discharge rapidly through another relatively low resistance resistor 282 to keep the current within the limits of the coin switch 270. The rapid discharge of the capacitor 276 causes a momentary low to occur at the output connection 284. The duration of this momentary low is controlled by the resistance of another resistor 286 and also by the action of the capacitor 280. The particular form and construction of the credit input circuit 32 as disclosed in the drawing is chosen for illustrative purposes only since numerous different types of credit input circuits could be used to pulse the programmable clock 12.

COUNTERS, COMPARATOR AND DECODER DETAILS

FIG. 3 shows the circuit details of the counter 14, the comparator 16, the inhibit circuit 18, the counter 20 and the decoder circuit 24. The counter 14 is shown as being a five stage binary counter made up of five D-type flip-flops 300, 302, 304, 306 and 308. The first stage flip-flop 300 receives the inputs to the circuit 14 on lead 62, which is the output lead of the AND gate 60, and all of the flip-flops have reset inputs which are connected to the reset lead 168 from an output of the payout control circuit 28. Each of the flip-flop circuits, except for the first stage flip-flop 300, also has a respective clock input 310, 312, 314 and 316 which is connected respectively to the preceding stage of the counter. For example, the clock input to the second stage 302 is controlled by $\bar{Q}$ outputs received from the first stage 300 and so on for the other stages. This means that when inputs are received they are accumulated in the usual manner for such counters. The accumulator circuit 14 also has an output OR gate 318 which has a plurality of inputs connected respectively to each $\bar{Q}$ output of the accumulator stages 300-308, and the gate 318 has an output 64 which is in a low condition only at times when all five stages of the binary accumulator are at their maximum count conditions

which occurs only when the counter has 31 accumulated therein.

Each stage 300-308 of the accumulator 14 has a respective $\bar{Q}$ output terminal 320, 322, 324, 326 and 328, and the combined signals present on these terminals represent the binary complement of the accumulation in the counter 14. The $\bar{Q}$ outputs in addition to being connected as already described are connected to respective full adder or summing circuits 330, 332, 334, 336 and 338 which are parts of the comparator circuit 16. The following truth table illustrates how the comparator circuit 16 subtracts the binary numbers it receives from the five stages of the counter 20 from the inputs it receives from the five stages of the counter 14 by adding the complements of the counter 14 (sum of the $\bar{Q}$ outputs) to the Q outputs of the counter 20. The complement of the result $\bar{S}$ is the binary difference.

TRUTH TABLE

	1	2	4	8	16	
A	= 1	1	1	0	0	= 7
A	= 0	0	0	1	1	= 24
+B	= 0	1	0	0	0	= 2
S	= 0	1	0	1	1	= 26
$\bar{S}$	= 1	0	1	0	0	= 5

As indicated, the counter 20 is shown having five stages 340, 342, 344, 346 and 348 which is the same number of stages as in the counter 14. The individual stages of the counter 20 can be set directly by inputs received on respective input leads 68, 70, 72, 74, and 76, and these stages are clocked by inputs received on the B counter input lead 50 and reset by inputs received either from the escrow control circuit 26 or from the payout control 28. The reset inputs are fed from the OR gate 172 on its output 170. Each stage of the counter 20 also has a $\bar{Q}$ output identified respectively by numbers 350, 352, 354, 356 and 358. Signals appearing on these outputs are inverted by respective NOR gates 360, 362, 364, 366 and 368 and therefore the NOR gates provide non-inverted binary outputs from the counter 20. These outputs are applied respectively to the adder circuits 330, 332, 334, 336 and 338 in the comparator circuit 16 in a manner similar to the inputs to the adders from the A counter 14.

The inhibit input lead 88 to the inhibit circuit 18 is shown in FIG. 3 connected to a second input of each of the NOR gates 360-368. When this input has a high state it causes a low condition to be present at the respective gate outputs 370, 372, 374, 376, and 378 and in so doing causes an inhibit function to take place between the B counter 20 and the comparator circuit 16. This would prevent the comparator circuit 16 from receiving signals from the B counter 20.

The comparator circuit 16 includes a parallel carry circuit portion 380 which provides carry out control signals on the carry-out lead 92. When the signal on the carry-out lead 92 is low it means that the binary count in B counter 20 is not larger than the binary count in the A counter 14. The carry-out lead 92 will remain low as long as the counters are in an equal condition or in a condition where the A counter 14 has a larger accumulation than the B counter 20. The comparator circuit 16 also has a carry-in lead 382, and this lead is normally held low and is included to provide an additional control parameter for other future uses such as for use with other designs which allow additional operating possibilities.

Another AND gate 384 is included in the circuit of the B counter 20 and has a plurality of input terminals which are connected respectively to the $\bar{Q}$ outputs of the stages 340-348. The gate 384 has a low on its output 124 whenever there is any count present on the B counter 20. In other words, the output of the AND gate 384 provides an indication that the B counter 20 has a count greater than zero, and this output is fed to the price encoder circuit 22 and to the vend control circuit 30 as aforesaid.

The decoder circuit 24 (FIG. 3) is included to provide the complement of the sum of the outputs of the counters 14 and 20, and this is accomplished in the decoder circuit by means of inverters 386, 388 and 390 and NAND gates 392 and 394 which are connected as shown. The outputs of the decoder circuit 24 are present on the output leads 94, 96, 98, 100 and 102 and these outputs indicate the various relationships that exist between the values accumulated in the A and B counters 14 and 20. These conditions are indicated by the presence of a low on the respective output leads. For example, when the amount accumulated in the A counter 14 is equal to the amount accumulated in the B counter 20 the output on the decoder output lead 94 will be low, and the outputs on the other decoder output leads will be high. By the same token and in similar manner, when the counter 14 has accumulated in it a larger amount than is accumulated in the B counter 20, the output on the output lead 96 will be low. When the amount in the A counter 14 is larger than the amount in the B counter by two, three and four increments, then the output on output lead 98 will be low. When a coin tube switch such as the dime coin tube switch 108 is closed indicating the tube is empty and producing a low condition on the lead 104, which lead is connected to lead 396, it will operate to inhibit the output on the lead 98. When the counter 14 has three or more increments more than the counter 20, the output 100 will go low to indicate the condition. This condition, while available, is not used in the circuit as shown, but could be particularly if the circuit were adapted to other coinage systems. When the A counter 14 has five or more increments more than the B counter 20, the output on the lead 102 goes low unless at this time the quarter empty tube switch 110 is activated putting a low on connected leads 106 and 398 and on the input to the gate associated with the ≥ 5 lead 102.

The decoder circuit 24 has other connections which operate to prevent certain outputs from occurring. For example, when the output lead 98 is low it prevents the lead 96 from going low. This is accomplished in the circuit by lead 400 which couples the output of the gate associated with the lead 96 as will be explained later. In like manner, whenever the output on the lead 102 goes low it will prevent outputs on the leads 96 and 98 from going low by signals on lead 402 which is connected between the output of the gate associated with the output lead 102 and the inputs to the gates associated with the outputs 96 and 98. Consequently, if the inhibit ≥ 5 lead 398 is low, the ≥ 2 output on the lead 98 will go low for any count present in the A counter 14 that is two or more (5, 6, etc.) greater than the amount accumulated in the B counter 20. Similarly, if both the inhibit input leads 396 and 398 are low at the same time, then the ≥ 1 output lead 96 will go low for any count in the A counter 14 that is one or more greater than the amount in the B counter 20. Whenever

a five increment coin such as a quarter is not available for refund or escrow, the circuit, as shown, will indicate that a two increment coin such as a dime should be refunded instead, and if dimes are likewise not available then the circuit will indicate that refunds are to be made in one increment coins only, namely, in nickels. It should be apparent that the present circuit can also be used with any known coinage system regardless of the relative increment values of the coins involved, although some minor changes in the connections may be required.

The decoder circuit 24 has another inverter 404 which is connected between the carry-out output lead 92 of the comparator circuit 16 and the various output gates of the decoder circuit 24. For example, the inverter 404 provides a low condition on lead 406 to prevent any false outputs from being produced by the decoder 24 when the A counter 14 has an amount accumulated therein that is less than the amount accumulated in the B counter 20. The outputs on the lead 406 are applied to the inputs of a plurality of decoder output gates including NAND gate 408 which is the gate that produces the outputs on the lead 94 to indicate a condition of equality between the amounts accumulated in the counters 14 and 20. The equality condition, as aforesaid, is indicated by a low on the lead 94 and this occurs whenever the output lead 410 of NOR gate 412 goes high due to a low on its input lead 414. This happens when the inverted output S_1 on lead 416 from the first stage adder circuit 330 indicates a zero state and when the other input to the gate 412 on lead 418 is low due to the condition of the inverted outputs of the other adder circuits 332, 334, 336 and 338 which appear as inputs to another NAND gate 419. The output of the NAND gate 419 appears in the lead 418 and on connected lead 420 indicating a zero state by the condition of the NAND gate 419. Under these conditions another NAND gate 424 will indicate this condition and produce a ≥ 1 function on its output lead 96 by having it go low when the output to it on lead 426 (which is connected to the output lead 94 of the gate 408) is high indicating the absence of an equality condition, $A = B$. The lead 426 is connected between the decoder output lead 94 of the NAND gate 408 and one of the input leads to the NAND gate 424, which is the ≥ 1 gate. The conditions just described also require that another input to the gate 424 on lead 428 be at a high condition indicating that the amount in the A counter 14 is not smaller than the amount in the counter 20, that input 430 to the gate 424 be high indicating the absence of a ≥ 5 condition, and that the other input lead 432 of the gate 424 be also high indicating that the ≥ 2 condition is not present.

Another decoder circuit output NAND gate 434 is associated with the ≥ 2 output lead 98 and provides a low output condition thereat when (1) input lead 436 is high indicating that the counter 14 has an amount that is not smaller than the amount in the counter 20, (2) inhibit input on lead 396 is high so as not to inhibit the gate, (3) input lead 420 from the output of the NAND gate 419 is high, and (4) the input it receives on lead 402 (output lead 102) is also high representing the absence of the ≥ 5 condition.

Another NAND gate 440 associated with the decoder ≥ 3 output lead 100 provides a low to represent the condition of ≥ 3 . This condition, while not used in the circuit as shown, is available and occurs when the

gate input lead 406 is high at a time when there is also a high on the other gate input lead 442 which lead is connected to the output of the NAND gate 392. This lead is high when the gate input on lead 444 is low due to the operation of another NAND gate 446 producing a high output condition. The NAND gate 446 has inputs connected respectively to the outputs of the inverter circuits 386 and 388 which inverters produce inverted forms of the outputs of the adder circuits 330 and 332. The NAND gate 392 also depends on inputs it receives from the output of another NAND gate 448 especially when these inputs go low. The NAND gate 448 has direct input connections to the outputs of the adder circuits 334, 336 and 338 which are the adders associated with the third, fourth and fifth stages, respectively, of the counters 14 and 20.

Another decoder NAND gate 450 is provided in association with the ≥ 5 output lead 102. The NAND gate 450 produces an output low on the lead 102 when (1) its input on the lead 406 is high indicating that the counter 14 has an amount accumulated that is not less than the amount accumulated in the counter 20, (2) the inhibit input lead 398 is high so that it is not being inhibited, and (3) its other input lead 452 is likewise high. The lead 452 is connected to the output of the NAND gate 394 and provides a high whenever the inputs to the gate 394 from the adder circuits 336 and 338 in the comparator circuit 16 are low or its other input on lead 454 is low. The lead 454 is connected to the output of another NAND gate 456 which has two inputs one of which is connected to the output of the inverter circuit 390 on lead 458, and the other on lead 460 is connected to the output of yet another NAND gate 462. The NAND gate 456 will provide a low on the output 454 whenever the output from the adder circuit 334 as inverted by the inverter 390 on lead 458 is high and its other input on the lead 460 from the NAND gate 462 is also high. The NAND gate 462 provides a high output when either the output of the first stage adder circuit 330 or the output of the second stage adder circuit 332 is low.

The control circuits shown in FIG. 3 provide a large measure of flexibility and selectivity in their construction and operation, and, as pointed out, lend themselves to use under a variety of different operating circumstances including a variety of different vend price possibilities, coin denomination possibilities, and a variety of selectivity with respect to the outputs produced. These possibilities manifest themselves in the circuit as disclosed by providing control over the vend control means, the payout control means, the escrow control means and the other circuits and circuit elements associated therewith.

SINGLE PRICE VEND CONTROL DETAILS

FIG. 4 shows circuit details specifically designed to provide control for a single price vending machine. This is to be contrasted with the circuit shown in FIG. 5 which is a dual price control circuit and will be described later. The circuits of FIGS. 4 and 5 also contain the details of the associated escrow control and payout control means. The vend control 30 is enabled by the presence of a signal on its enable input lead 120 which is from the output of the AND gate 122. The AND gate 122, as already described, has inputs from the carry output from the comparator circuit 16 which are present on the lead 92 and is effective when the carry out-

put is low to indicate that the accumulation in the counter 14 is equal to or greater than the accumulation in the counter 20, and from the B counter 20 when the $B > 0$ lead 124, which indicates that the B counter 20 has an accumulation greater than zero, to produce a low on the lead 124.

The vend price that is entered in the B counter 20 is introduced from the price encoder circuit 22 by way of the AND gate 126, and its output connection 128 goes high whenever the accumulation in the counter 20 is greater than zero. This is the condition that exists when there is a high on the decoder output lead 94 indicating an equal condition between the accumulations in the counters 14 and 20, and where there is a high on another input lead 470 to the gate 126. The lead 470 goes high in response to a condition existing on inverter circuit 472 at the time when a selection is made in the vending machine (not shown). This change causes current to flow from an input control terminal 474 (connected to the vending machine) to activate an electro-optical device shown as optical coupler 476. The coupler 476 operates through a mode-switch 478 to cause the input lead 480 of the inverter 472 to go low at a time when the output lead 128 of the gate 126 goes high thereby establishing circuits to enter the price in the B counter 20. The actual entry occurs by causing highs to be present at certain of the leads 68-76 which are the leads connected between the price encoder circuit 22 and the stages of the B counter 20. This depends upon the setting of the plurality of switches connected to the leads 128. These switches are designated generally by the number 481 and their combined setting conditions establish the vend price.

As in copending U.S. patent application Ser. No. 331,380, the elements of the circuit associated with the optical coupler 476 include resistors 482 and 484, capacitor 486, and diode 488 connected as shown. These elements and their connections enable the coupler 476 to pulse when a selection is made in the vending machine. The mode-switch 478 is shown in the drawing in position to provide refunds of accumulation until a product is selected. When the mode-switch 478 is moved to its opposite position it causes the established vend price to be transferred into the counter 20 in the manner described as soon as j-k flip-flop circuit 490, also in the vend control circuit 30, is reset. When the j-k flip-flop 490 is clocked or caused to go to a low condition by a signal on its enable input 120 from the gate 122, its $\bar{Q}$ output terminal 492 goes low thereby causing its j input 494 and its k input 496 to also go low to prevent any possible further clocking of the flip-flop and to inhibit (hold its reset condition low) the escrow control 26 by way of a signal appearing on the escrow inhibit lead 132. Vend time, which is the time that the vend relay 498 is energized and its contacts 500 transferred from engagement with a stationary contact associated with lead 502 to engagement with a stationary contact associated with the lead 504, is controlled by input signals or responses that are fed from the j-k flip-flop circuit 490 to and through a NAND gate 506 by way of leads 508 and 510. The input lead 508 is connected to the Q output terminal 512 of the flip-flop 490 and goes high as soon as the j-k flip-flop 490 itself goes high. The $\bar{Q}$ output 492 was high until the input to the gate circuit 506 on the lead 510 became high and remained high until the low on the $\bar{Q}$ output 492 allows capacitor 514 to discharge through resistor 516, both

of which are connected in parallel and between the base element of transistor 518 and ground. The resistor 516 and the capacitor 514 are included to forward bias the transistor 518 and to cause the input to the gate circuit 506 on the lead 510 to go low.

Another AND gate 520 is provided to reset the j-k flip-flop 490 by signals received on its input terminal 522 whenever the escrow control 26 is set, or by signals received on its other input lead 524 when OR gate 526 has its output lead 528 go low. This condition occurs when the input 530 to the gate 526 is low after vend time and when its other input 532 is also low indicating that the same count exists in both of the counters 14 and 20. This occurs either when the accumulation is equal to the vend price or when the payout of change as added to the vend price entered in the B counter 20 causes the accumulation in counter 20 to equal the accumulation in the counter 14. When the accumulation in the counter 14 does not equal the accumulation in counter 20 after vend time is over as indicated at the lead 510, another inverter 534 connected to the lead 510, has its output on lead 536 go high. This high is applied as an enable input to the OR gate 134 in the enable circuit to the payout control 28 and causes a high on the lead 140 which is the enable input lead to the payout control 28.

When a payout condition is called for by a high at the enable input lead 140, a payout motor 540 will be energized. This is because there will also then be a high on the input lead 542 of another NAND gate 544 to represent the condition when the amount accumulated in the counter 14 is not equal to the amount accumulated in the counter 20. Therefore, since the NAND gate 544 at this time has highs on both of its inputs 542 and 140,, its output 548 will be at a low to cause a transistor 550 to be forward biased through zener diode 552. The zener diode 552 is connected into the base circuit of the transistor 550 in series with a current limiting resistor 554 and with other biasing resistors 556 and 558 connected as shown. The zener diode 552 provides isolation between the motor supply and logic circuitry. Another resistor 560 and capacitor 562 are connected in a circuit across the payout motor 540 to suppress motor noise. The resistor 558 assures turnoff of the transistor 550 whenever it is not forward biased by the NAND gate 544. When the payout motor 540 is energized it will operate means to payout one increment coins. However, when the motor 540 is operated in conjunction with relay 564, to be described later, it will payout two increment coins, and when the motor 540 is operated in conjunction with another relay 566 it will payout coins of five increment value. The two increment relay 564 is energized when NAND gate 568 has highs on both of its input leads 570 and 572. The input lead 572 goes high when the input to an inverter circuit 574 on lead 576 goes low. This occurs when there is a low on the ≥ 2 lead 98.

The five increment relay 566 is energized when NAND gate 578 has its inputs on leads 580 and 582 high. The input on lead 580 goes high during a payout operation due to a high being present on the payout input enable lead 140, and the input lead 582 goes high when an inverter circuit 584 has a low on its input lead 586. The lead 586 is connected to the ≥ 5 output 102 from the decoder circuit 24.

The payout control circuit 28 has output connections 160, 162 and 164 which are connected to respective

input leads 52, 54 and 56 of the clock 12 as shown in FIGS. 1 and 2. The outputs from the payout control circuit 28 provide momentary low pulses which program the clock circuit 12 so that the clock circuit will produce one, two or five clock pulses, respectively. The leads 160, 162, and 164 of the payout control circuit 28 are connected respectively as outputs of OR gates 588, 590 and 592 which provide pulses whenever the voltages on a lead 594 goes low under control of the operation of the payout motor 540 which operates a motor pulse switch 596 through a mechanical connection therewith. The momentary closing of the switch 596 operates through a pulse shaping circuit which is formed by resistors 598, 600 and 602 and capacitors 604 and 606 to produce the output pulses that occur on the lead 594. The pulse shaping circuit is similar to the pulse shaping circuit used in the credit input circuit 32 described in connection with FIG. 2. When the lead 594 is pulsed to a low condition, the one increment OR gate 588 will provide the pulsed low output on lead 160 if at the same time the ≥ 1 output lead 96 is also low. In like manner, the OR gate 590 will provide an output pulse on lead 162 when the ≥ 2 output on lead 98 is low, and when the ≥ 5 output on lead 102 is low at a time when there is a low on the lead 594 there will be a pulse on the lead 164. When the motor switch 596 closes it discharges the capacitor 606 in the pulse shaping circuit as each coin is paid out and this action will operate through an inverter circuit 608 to cause a high to be produced on output lead 610 which is the B_{out} enable lead, also labeled 48 in FIG. 1. This is the signal which causes the clock 12 to feed signals to the B counter 20 instead of to A counter 14. Hence, a signal on the lead 48 provides that the clock pulses will be directed to the counter 20 during payout operations. Thereafter, when the accumulation in the B counter 20 is reduced to the point where it equals the accumulation in the A counter 14 during payout, the lead 94 which represents this equality will go low to provide a low at the output 528 of the gate circuit 526 which is located in the vend control circuit 30. This low is connected to input 612 of another gate 614 in the payout control circuit 28. At the same time, if the other input 616 of the gate 614 goes low because of the condition on the output lead 140 of the gate 134, the output of the gate 614 on lead 618 will go low causing the counters 14 and 20 to be reset by signals present on the reset output leads 168 and 170 which are respectively under control of inverter 620 and gate circuit 622. These circuits are both momentarily pulsed by a circuit which includes capacitor 624 and resistor 626.

ESCROW CONTROL DETAILS

The details of the escrow control circuit 26 provided to return an amount deposited and accumulated under circumstances where a vend operation is not achieved are also shown in FIG. 4. Escrow operations are under control of the operator actuatable escrow switch 144 when the movable switch contact is moved from its normal to its transferred position. When the switch 144 is operated it causes an enable input signal to be applied to input lead 630 of j-k flip-flop 632 and this input goes high and then low. This causes the flip-flop circuit 632 to have a low on its $\bar{Q}$ output 634. This also holds the j and k inputs 636 and 638 low and prevents further changes in the state of the flip-flop even though additional changes should occur on the input lead 630. The

inhibit output lead 146 supplies inhibit outputs from the escrow control 26 to the vend control circuit 30 to keep the vend control circuit 30 from being activated during escrow. This is done by holding the j-k flip-flop circuit 490 in its reset state by applying the low on the lead 146 to the reset input 640. A capacitor 642 and a resistor 644 are also connected in the output circuit of the escrow flip-flop 632 to provide a low to one of the inputs of the gate circuit 622. The gate 622 was described above in connection with the payout control 28 and has its output lead 170 connected to the reset input R_b of the B counter 20. As already indicated, the payout control 28 is enabled by a high present on the enable input lead 140 which lead is connected through the gate 134 from the Q output lead 646 of the escrow flip-flop 632. When the payout control 28 causes the counter 20 to have an amount accumulated therein that is equal to the amount accumulated in the counter 14 as indicated previously, an output will be present on the lead 94 which is the $A = B$ output, and this output will be low and will cause the escrow control circuit 26 to be reset by a reset input applied to the reset input lead 648 of the flip-flop 632. This signal is applied by way of gate circuit 650 which has one input connected to the lead 94 and the other input to the lead 132. Thereafter, the inputs on the two input leads 542 and 140 of the NAND gate 544 in the payback control circuit 28 are caused to go low, and as soon as this happens the payback operation will terminate.

VEND CONTROL DETAILS (MORE THAN ONE PRICE)

FIG. 5 shows an alternate embodiment of the subject vend control circuit 30 wherein it is able to handle more than one vend price. Vend control leads 660 and 662 on the right side of FIG. 5 provide inputs to monitor a selection in the vending machine as well as to apply a control potential available on another lead 664 for two different respective vend prices. One vend price is determined and set into the machine by means of switches 666, 668, 670, 672 and 674 which are in a price encoder circuit shown in the lower lefthand corner of FIG. 5, and the other vend price is set into the circuit and determined by the setting of another set of switches 676, 678, 680, 682 and 684 also in the price encoder circuit 22. When a selection is made in the vend control circuit 30, it provides a path from either vend control lead 660 or from vend control lead 662 to cause current to flow from lead 686 through the optical coupler 688 or 690, respectively. Current flow through the associated couplers is limited by associated resistors 692 and 694 and is rectified by associated diodes 696 and 698. The current that flows through these circuits will cause the corresponding optical coupler 688 or 690, each of which includes a light emitting diode 700 or 702, respectively, to illuminate an associated photo-transistor 704 or 706. In the drawing, the light emitting diodes 700 and 702 are shown separated from the associated transistor portions 704 and 706 of the same devices. This is done for convenience in the drawing but in an actual construction each diode is positioned in the same envelope with its associated photo-transistor. When a price selection has been made and the respective phototransistors 704 (or 706) is caused to saturate (provide a good current flow path between its collector and emitter) clock pulses are applied to the clock input terminals 708 (or 710) of the respective

j-k flip-flop circuits 712 and 714. This will occur as long as the payout control lead 140 is not activated or at its low. When this happens, one of the flip-flops 712 or 714 will be operated and the other not, and which ever one has its $\bar{Q}$ output 716 or 718 go low will cause the opposite flip-flop circuit to be held in a reset condition. This is accomplished by means of a circuit which includes cross-coupled gates 720 or 722. These gates are included to make sure that only one of the vend relays 724 or 726 can be energized at any one time. Transistors 728 and 730 are provided in the respective output circuits of the j-k flip-flops 712 and 714 to provide an interface between the vend relays 724 and 726 and the associated Q terminals 732 and 734 of the flip-flops 712 and 714.

The reset inputs 736 and 738 of the flip-flops 712 and 714 are controlled by the gates 722 and 720 respectively which provide the necessary reset low conditions whenever the opposite flip-flop 714 or 712 is turned on by inputs which appear at the respective gate input terminals 744 or 746 at times when output lead 748 of another AND gate 750 is low.

The gate 750 is included in the reset circuit to provide the reset function whenever another optical coupler which is the reset optical coupler 756 is activated which occurs during product delivery when the carry output lead 92 from the decoder circuit 24 goes high. This occurs when the A counter 14 has less accumulation than the price accumulated in the counter 20 as well as when total reset occurs because of a signal on a lead such as on lead 758 of FIG. 4.

The vend control lead 760 in FIG. 5 (lower right hand corner) is connected to cause current to flow through the optical coupler 756 and through light emitting diode (LED) 762 during a product delivery operation. A resistor 764 and a diode 766 are connected in series with the light emitting diode 762 to control the amount and direction of the current flow. The light emitting diode 762 of the optical coupler 756 is in the same envelope with photo-transistor 768. Whenever selection is made of a particular product and the selection causes clocking of one of the j-k flip-flops 712 or 714, this will cause a lead 770 to go high because of the operation of an OR gate 772 which has its inputs 774 and 776 connected respectively to the Q output terminals 732 and 734 of the flip-flops 712 and 714. The same highs also occur at respective input terminals 782 and 784 of other AND gates 786 and 788 and cause a high to appear at gate output 790 or 792 of the gates 786 and 788. The other inputs on leads 794 and 796 to the same gates are also high because they are connected to output terminal 798 of inverter circuit 800. The high that appears on the lead 770 as discussed above is delayed somewhat by operation of a capacitor 802 which causes the output of the inverter circuit 800 on lead 798 to go low at a slightly later time, thus causing the high that is fed to the price encoder circuit 22 to be momentarily pulsed. The circuit just described also includes OR gate 804 which has an input 806 that goes high under control of signals received on the payout lead 140 to prevent any possible encoding from taking place during a payout operation.

When the vend price is encoded by the encoder circuit 22 due to the presence of a signal on either lead 790 or 792, an output will appear on the encoder output leads 68-76 which connect the encoder to the B counter 20. The accumulation entered in the B counter

20 is then compared in the comparator circuit 16 to the accumulation in the A counter 14, and this will result in producing a clocking output on the enable lead 120 of the vend control 30 if there is an equal or greater accumulation in the counter 14 than in the counter 20. If there is not enough credit accumulated in the counter 14 to produce a vend then the carry output on lead 92 will cause another lead 808 (FIG. 5) to go low thereby resetting whichever binary flip-flop 712 or 714 initiated the event. However, when there is sufficient credit to provide clocking of another j-k flip-flop circuit 810 in the vend control circuit 30, the low condition established at its $\bar{Q}$ output terminal 812 will cause a capacitor 814 to discharge through a resistor 816 to thereby provide a delayed conduction by an associated transistor 818. The transistor thereafter provides a high on lead 820 which is connected to the output side of an inverter 822. This condition is necessary for payout, and the low which is produced at the output side of the transistor 818 is also present on input terminal 824 of another OR gate 826. The gate 826 in the circuit of FIG. 5 is similar to and operates similar to the gate 526 in the circuit of FIG. 4. It also has similar connections. The circuits associated with the gate 826 including also the flip-flop circuit 810 and its connections and associated circuitry are similar to those described above in connection with FIG. 4.

When a low is applied to the input terminal 824 of the gate 826, a low will be produced at the gate output on lead 828. This will happen as soon as the other gate input lead 830 to the gate 826 is low indicating either that the accumulation in both counters 14 and 20 is the same or that the accumulation in the counter 14 exceeds the vend price. The low produced on output lead 828 of the gate 826 is applied to input terminal 832 of another gate 834 and is used to reset the j-k flip-flop 810. The flip-flop 810 can also be reset by a signal applied on the lead 808 when the output terminal 92 of the comparator circuit 16 goes high. The same can also occur when the escrow output lead 146 goes low.

Another gate 836 is connected in the circuit associated with the flip-flop 810 to control the inhibit operation of the escrow control circuit 26 which is applied thereto on lead 132 from the output of the gate 836. This circuit is available when the $\bar{Q}$ output lead 812 of the flip-flop 810 is low and while the lead 770 which is applied to the input of another inverter 838 is high.

To provide the capability of vending at still more vend prices simply requires adding additional price coding switches and associated isolation gating and vend control circuitry, all of which can be connected in a manner similar to that already described. Furthermore, whereas the subject invention is shown employing D-type flip-flop circuits for the counters 14 and 20, the same can be accomplished using j-k flip-flops for these elements as well as other bistable devices. The accumulation means can also include ring counters, shift registers, counters capable of counting in both directions, and other binary accumulation devices. Also, the means selected for use in the comparator and decoder circuits as disclosed can be accomplished by EXCLUSIVE OR gates, half-adders and other state-of-the-art devices and techniques. The pulse generating means can also be similar to that disclosed in copending Levasseur U.S. patent application Ser. No. 267,558, which is assigned to Applicant's assignee. Other suitable pulsing devices are also known and could be used.

It is also anticipated that the types and combinations of gates and other elements and their interconnections can be varied substantially in some cases from the particular embodiments as disclosed without departing from the basic inventive concepts and the basic functions and operations as set forth and described herein. Furthermore, certain features as disclosed can be omitted from the circuit for operational or expense reasons. For example, the escrow control, the feature of being able to payout in multiple coin denominations, and the use of photodiodes can be substituted for by other similar devices including electrical and magnetic devices capable of performing similar functions. The use of photodiodes in certain portions of the subject circuit as described is preferred because of the type of signals they produce and the type of signals that the circuit is capable of using and responding to. Such devices are also relatively small and are reliable and relatively maintenance free.

Thus there has been shown and described a novel and extremely versatile vending control circuit which fulfills all of the objects and advantages sought therefor. It is apparent, however, as indicated, that many changes, modifications, variations, and other uses and applications of the subject control are possible and will become apparent to those skilled in the art after considering this specification which describes several embodiments and the accompanying drawings. All such changes, modifications, variations and other uses and applications which do not depart from the spirit and scope of the invention are deemed to be covered by the invention which is limited only by the claims which follow.

What is claimed is:

1. A circuit for controlling a vending machine capable of vending products and of refunding amounts deposited in excess of the vend price comprising a first counter circuit having input, output and reset connections, means including a programmable clock circuit connected to the counter in and operable to introduce input pulses for feeding thereto when credit is introduced into the vending machine, said clock circuit having a credit input, a refund input, an enable input, an output and reset connection means, said clock producing output pulses at its output connection means corresponding to each credit and refund input received thereat, means connected to the credit input of the clock to energize the clock circuit according to an amount of credit to be entered into the first counter, a second counter having an input, an output and a reset terminal, price encoder means operatively connected to the input to the second counter and including means for transferring an established vend price from the price encoder means to the second counter, means for comparing amounts accumulated in the first counter circuit with the vend price entered in the second counter including means to generate an electric response to indicate which of the first and second counter circuits has the greater accumulation therein, means for enabling a vend operation to take place whenever the amount accumulated in the first counter circuit at least equals the vend price entered in the second counter circuit, payout means operatively connected to the comparing means and energizable thereby to refund amounts in the first counter circuit which exceed the vend price entered in the second counter circuit, said payout means including means to add to the vend

price entered in the second counter circuit an amount equal to the amount of each refund until the first and second counter circuits have the same amount accumulated therein, and means associated with the means for comparing that are responsive to the occurrence of equal accumulations in the first and second counter circuits to reset the said first and second counter circuits and the payout means.

2. The circuit defined in claim 1 including escrow means operatively connected to the payout means and to the vend enabling means, and means to initiate the escrow operation to refund amounts deposited, said escrow means including means which when an escrow operation is initiated inhibit operation of the vend enabling means.

3. The circuit defined in claim 1 including escrow means operatively connected to the payout means and to the vend enabling means, and means in the vend enabling means to inhibit operation of the escrow means simultaneously with the initiations of a vend operation.

4. The circuit defined in claim 1 including means to inhibit a vend price entered in the second counter circuit from being communicated to the means for comparing the vend price to the amount accumulated in the first counter circuit.

5. The circuit defined in claim 1 including means connecting the payout means to the programmable clock circuit whereby each time the payout means produces a signal it will be applied to the refund input of the programmable clock circuit to cause said clock circuit to produce an output representative of the value of the refund, and means for feeding said clock outputs to the second counter circuit.

6. The circuit of claim 1 wherein the first and second counter circuits, the means for comparing, the price encoder means and the circuit connections therefor are all included in a single integrated circuit chip.

7. The circuit of claim 1 wherein said means to generate a response to indicate which of the first and second counter circuits has the greater accumulation includes a difference decoder circuit having a first output at which signals are produced to represent equal accumulations in the first and second counter circuits, and other outputs at which signals are produced to represent the magnitude of the difference between the amounts accumulated in the first and second counter circuits.

8. A control circuit for vending and other money controlled machines comprising a first counter for accumulating credit amounts introduced into the machine, a second counter and means for entering into the second counter amounts equal to an established vend price, a comparator circuit having first input means connected to respond to amounts accumulated in the first counter and second input means connected to respond to amounts accumulated in the second counter, comparator output means including decoder circuit means responsive to a comparison between the amounts accumulated in the first and second counters, said decoder circuit means having a plurality of outputs at which signals are produced to represent respectively equality or preselected amounts of difference between the amounts accumulated in the first and second counters, a vend control circuit having an enable input operatively connected to the comparator circuit, said enable input receiving a vend control enable input signal

whenever the comparator circuit indicates that the first counter has an amount accumulated in it at least equal to the amount accumulated in the second counter, a payout control circuit having a plurality of inputs connected to the respective outputs of the decoder circuit means including the outputs at which signals are produced that represent preselected amounts of excess difference between the amounts accumulated in the first counter relative to amounts accumulated in the second counter, said payout control circuit also having a reset input connected to receive outputs of the decoder circuit means when the comparator circuit indicates that the amount accumulated in the first and second counters is the same, said payout control circuit including means to produce output signals to cause the refunding of said excess accumulations.

9. The control circuit defined in claim 8 wherein said first and second counters, said comparator circuit, and said decoder circuit are parts of a single integrated circuit chip.

10. The control circuit defined in claim 8 including controllable means connected between the outputs of the second counter and the comparator circuit to control communication therebetween.

11. The control circuit defined in claim 8 including means associated with the first counter to prevent the loss of a maximum possible accumulation therein when inputs are received at times when the first counter has its maximum capacity accumulated therein.

12. The control circuit defined in claim 8 including means to select between different vend prices for entering in the second counter.

13. The control circuit defined in claim 8 wherein the first and second counters are formed by a plurality of serially connected bi-stable flip-flop circuits.

14. The control circuit defined in claim 8 wherein the vend control circuit includes a photoelectric diode having a light emitting portion connected to be energized when a vend operation is initiated and a light sensitive portion responsive to light emitted by the light emitting portion, said light sensitive portion being connected in the circuit between the means for entering the established vend price and the second counter.

15. The control circuit defined in claim 14 wherein a similar photoelectric diode and associated circuitry are provided for each possible vend price that can be selected.

16. The control circuit defined in claim 8 including an escrow control circuit operatively connected to the payout control circuit and to the vend control circuit, said escrow control circuit including an operator actuable escrow switch, actuation of which energizes the escrow control circuit and the payout control circuit to cause refunds of the total amount of an accumulation entered in the first counter, said energized escrow control circuit including output means for simultaneously inhibiting operation of the vend control circuit.

17. The control circuit defined in claim 16 including means to inhibit operation of the escrow control circuit whenever the vend control circuit is actuated by selection of a vend at a time when the amount accumulated in the first counter at least equals the vend price.

18. A vend control circuit comprising

- a first counter for accumulating credit amounts entered in the machine,
- a second counter for entry of a vend price and amounts refunded,

a counter input circuit including a pulse generator having first and second input and output means, said first output means being operatively connected to the first counter and said second output being operatively connected to the second counter,

a source of credit input signals connected to the first input means of the pulse generator for energizing the pulse generator to produce outputs at said first output means to represent the value of each credit amount entered in the machine,

price encoder means operatively connected to the second counter having input and output means, means connecting the output means of said price encoder means to the second counter,

means to compare amounts entered in the first counter to amounts entered in the second counter including means to indicate if the amounts are equal or different and if different the amount of the difference, and

vend enabling circuit means operatively connected to the comparison means including means to initiate a vend operation in the vending machine whenever the amount accumulated in the first counter at least equals the vend price in the second counter.

19. The vend control circuit of claim 18 including: payout circuit means operable under control of the indicating means to refund amounts deposited in excess of the vend price, said payout circuit means having an output at which signals are produced to represent the amount of each refund, means connecting the output of said payout circuit to the second pulse generator input, and other means connected between the payout circuit means and the pulse generator to cause said pulse generator to feed outputs from its second output means to the second counter during payout operations until the magnitude of the amount accumulated in the second counter is equal to the magnitude of the amount accumulated in the first counter.

20. The vend control circuit of claim 19 wherein said payout circuit means includes means under control of the indicating means to payout coins of different denominations depending on the difference between the amounts entered in the first and second counters.

21. The vend control circuit of claim 18 wherein the means to indicate the difference between the amount entered in the first and second counters include means to indicate when the difference is ≥ 1 , ≥ 2 , and ≥ 5 .

22. The vend control circuit of claim 18 wherein each of said first and second counters includes a plurality of serially connected bi-stable circuit stages, and said means for comparing including a corresponding number of summer circuits each having corresponding pairs of input connections connected to the corresponding stages of the first and second counters.

23. The vend control circuit of claim 18 wherein the pulse generator includes an oscillator circuit.

24. The vend control circuit of claim 18 including means for refunding the total amount of a credit entered in the first counter, said refund means including an operator actuable refund switch, and means operatively connecting said refund means to the vend enabling circuit means, operation of said refund switch

prior to initiation of a vend operation operating to inhibit operation of the vend enabling circuit means.

25. A vend control circuit including means to control the vending of a product and the refunding of amounts deposited in excess of the vend price comprising

a first counter for accumulating credit amounts entered in a vending machine when coins are deposited therein,

a second counter including means for entering a vend price therein,

other means for entering in the second counter amounts to represent the value of each coin refunded to the customer,

counter input means including means for generating signals to represent the value of each coin deposited in the vending machine,

means for comparing amounts entered in the first and second counters, said comparing means including means to indicate if the amounts entered are equal or are different, and if different the amount of the difference, vend enabling circuit means operatively connected to the comparing means including means to initiate a vend operation in the vending machine whenever the amount accumulated in the first counter at least equals the vend price entered in the second counter,

payout means operatively connected to the comparing means including means to payout coins as refunds to represent amounts entered in the first counter in excess of the vend price entered in the second counter, said payout means including means operatively connected to the second counter to enter amounts therein to represent the value of each coin paid out and to increase the amount accumulated in said second counter, said comparing means producing an output when the amount accumulated in the second counter equals the amount accumulated in the first counter,

and means responsive to said equality output signal of the comparing means to terminate the payout operation and to reset the first and second counters.

26. The vend control circuit defined in claim 25 including means actuable by the customer to refund the total of an amount entered in the first counter prior to initiation of a vend operation, said last named means including means to substantially simultaneously inhibit operation of the vend enabling circuit means.

27. A control circuit for vending and other money controlled machines comprising a first counter for ac-

cumulating credit amounts introduced into the machine, a second counter and means for entering into the second counter amounts equal to an established vend price, a comparator circuit having first input means connected to respond to amounts accumulated in the first counter and second input means connected to respond to amounts accumulated in the second counter, comparator output means including decoder circuit means responsive to a comparison between the amounts accumulated in the first and second counters, said decoder circuit means having outputs at which signals are produced to represent respectively equality or the amount of difference between the amounts accumulated in the first and second counters, a vend control circuit having an enable input operatively connected to the comparator circuit, said enable input receiving a vend control enable input signal whenever the comparator circuit indicates that the first counter has an amount accumulated in it at least equal to the amount accumulated in the second counter, a payout control circuit having a plurality of inputs connected to the respective outputs of the decoder circuit means, said payout control circuit also having a reset input connected to receive outputs of the decoder circuit means when the comparator circuit indicates that the amount accumulated in the first and second counters is the same, the other of said plurality of inputs to the payout control circuit being connected respectively to outputs of the decoder circuit means which represent various amounts accumulated in the first accumulator in excess of the amounts accumulated in the second counter, said payout control circuit including means to produce output signals to cause the refunding of said excess accumulations, a source of clock pulses operatively connected to the inputs of the first and second counters, means to excite said clock source in response to deposit of each coin in the vending machine to cause said source to generate output clock pulses corresponding to the value of each deposited coin for entry into the first counter, other means including said payout control circuit having connections to the clock source to excite said source to produce outputs to represent the value of each refund, means for entering clock pulses produced during refund into the second counter, and means to reset the payout control circuit whenever the comparator circuit indicates that the amount accumulated in the second counter is equal to the amount accumulated in the first counter.

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