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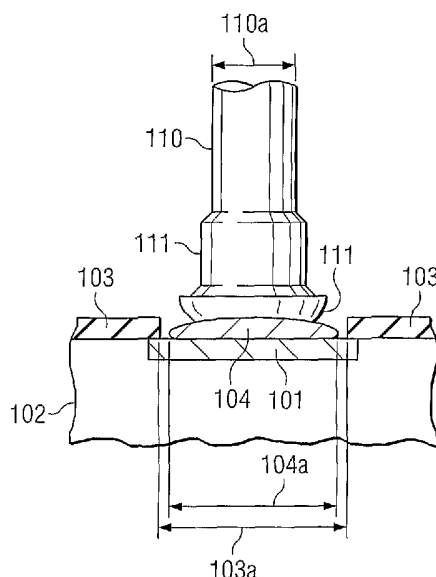
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
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[Continued on next page]

(54) Title: WIRE BONDS HAVING PRESSURE-ABSORBING BALLS



(57) Abstract: A semiconductor device with a chip having at least one metallic bond pad (101) over weak insulating material (102). In contact with this bond pad is a flattened metal ball (104) made of at least 99.999 % pure metal such as gold, copper, or silver. The diameter (104a) of the flattened ball is less than or equal to the diameter (103a) of the bond pad. A wire (110) is connected to the bond pad so that the wire has a thickened portion (111) conductively attached to the flattened metal ball. The wire is preferably made of composed metal such as gold alloy. The composition of the flattened ball is softer than the wire. This softness of the flattened ball protects the underlying insulator against damage caused by pressure or stress, when the composed ball is attached.



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WIRE BONDS HAVING PRESSURE-ABSORBING BALLS

The present invention is related in general to the field of semiconductor devices and processes and more specifically to structure and method of metal bonds to contact pads over dielectrics.

5 BACKGROUND

It is well known in semiconductor technology that bond pads on silicon integrated circuits can be damaged during conventional thermosonic wire bonding to circuit bond pad made of aluminum or copper. Mechanical loading and ultrasonic stresses applied by the tip of the bonding capillary to the bond pad are particularly suspect. When the damage is not
10 apparent during the bonding process, the defects may manifest themselves subsequently by succumbing to thermo-mechanical stresses generated during plastic encapsulation, accelerated reliability testing, temperature cycling, and device operation. The damage appears in most cases as microcracks which may progress to fatal fractures in the underlying dielectric, as chip-outs of brittle or mechanically weak dielectric films, often together with
15 pieces of metal or silicon, or as lifted ball bonds or delamination of metal layers.

Recent technological developments in the semiconductor industry tend to aggravate the problem. For instance, newer dielectric materials such as silicon-containing hydrogen silsesquioxane (HSQ) are being preferred due to their lower dielectric constant which helps to reduce the capacitance C in the RC time constant and thus allows higher circuit speed.
20 Since the density and porosity of dielectric films affect the dielectric constant through absorption or desorption of water, films with these characteristics are introduced even when they are mechanically weaker. Films made of aerogels, organic polyimides, and parylenes fall into the same category. These materials are less dense and mechanically weaker than previous standard insulators such as the plasma-enhanced chemical vapor deposited
25 dielectrics. This trend even affects stacks of dielectric layers such as alternating layers of plasma-generated tetraethylorthosilicate (TEOS) oxide and HSQ, or ozone TEOS oxide and HSQ. Since these materials are also used under the bond pad metal, they magnify the risk of device failure by cracking.

In addition, the pitch of bond pads is being progressively more reduced to save
30 valuable silicon real estate. Consequently, the bonding parameters have to become more aggressive to achieve stronger bonds in spite of smaller size. Bonding force and ultrasonic

energy during bonding are being increased. Again, the risk of yield loss and lowered reliability is enhanced.

Attempts to solve these problems by using softer wires and attachments balls have failed because these wires sag under their own weight in long-looping spans, or can be swept in the transfer molding process. In addition, these difficulties tend to get aggravated, when larger wire diameters are needed to keep the electrical resistance of long loops at an acceptable value. Furthermore, bonding balls made from these large-diameter wires would end up with ball diameters too large for the ever shrinking pad sizes.

SUMMARY

A need has therefore arisen for a low cost, reliable wire bonding method combining simultaneously small ball sizes with reliable intermetallics, low risk of damaging the dielectrics under the bond pad during the bonding process, avoiding sagging of long wire spans, and keeping the electrical resistance of these long wire spans at acceptable values. There is a technical advantage, when the method is flexible enough to be applied for different semiconductor product families and a wide spectrum of design and assembly parameters, and also achieves improvements toward the goals of improved process yield and device reliability. These are further technical advantages when these innovations are accomplished using the installed equipment base so that no investment in new manufacturing machines is needed.

One embodiment of the invention is a semiconductor device with a chip, which has at least one metallic bond pad over insulating material. In contact with this bond pad is a flattened metal ball made of at least 99.999 % pure metal such as gold, copper, or silver. The diameter of the flattened ball is less than or equal to the diameter of the bond pad. A wire is connected to the bond pad so that the wire has a thickened portion conductively attached to the flattened metal ball. The wire is preferably made of composed metal such as gold alloy, copper alloy, or copper-coated gold; the composition of the flattened ball is softer than the wire. This softness of the flattened ball protects the underlying insulator against damage caused by pressure or stress, when the composed ball is attached, even when the insulator includes mechanically weak dielectrics.

The device may also have an electrically conducting line spaced from the bond pad by a gap. The wire is spanning this gap by means of a loop of controlled shape, whereby the

bond pad is connected to the conducting line. Due to the hardness of the composed wire, the loop does not sag even for long spans. Furthermore, the wire has a diameter selected so that the electrical resistance of the loop can be kept below a pre-determined value.

Another embodiment of the invention is a method for fabricating a semiconductor device, which has a chip with at least one bond pad over insulator material. A flattened metal ball is formed in contact with the bond pad. A wire is then connected to the bond pad by forming a thickened portion of the wire and conductively attaching the thickened portion to the flattened metal ball, which has a composition softer than the wire.

Another embodiment of the invention is a method for fabricating a semiconductor device, which starts by providing a semiconductor chip with at least one metallic bond pad over insulator material. A first free air ball is formed at the tip of a first capillary, which is loaded with a wire of at least 99.999 % pure metal. The freshly formed first free air ball is then attached to the bond pad, flattened by means of the first capillary, and separated from the pure wire. A second free air ball is formed at the tip of a second capillary, which is loaded with a wire of composed metal. The freshly formed second free air ball is then attached to the flattened first ball and flattened by means of the second capillary; the composed wire is finally spanned into a controlled loop. The diameter of the composed wire is selected so that the loop has a predetermined electrical resistance.

It is a technical advantage of the invention to eliminate restrictions on the size of the dielectric pattern, thus minimizing the risks of inflicting cracking damage even to very brittle dielectrics.

It is another technical advantage of the invention to provide design concepts and process methods which are flexible so that they can be applied to several families of products, and are general, so that they can be applied to several generations of products. The invention supports the ongoing miniaturization trend in the semiconductor industry, especially the shrinking of bond pad diameters.

Another object of the invention is to use only processes already employed in the fabrication of integrated circuit devices, thus avoiding the cost of new capital investment and using the installed fabrication equipment base.

The technical advances represented by certain embodiments of the invention will become apparent from the following description of the preferred embodiments of the

invention, when considered in conjunction with the accompanying drawings and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic cross section of a contact pad on a semiconductor device with metals attached according to an embodiment of the invention.

FIG. 2 is a schematic cross section of a contact pad on a semiconductor device after the first step of a contact fabrication method according to an embodiment of the invention.

FIG. 3 is a schematic cross section of a completed bonding wire loop having a contact to a semiconductor bond pad fabricated according to the invention.

FIG. 4 is a schematic cross section of two adjacent contact pads after the first step of a contact fabrication method according to an embodiment of the invention.

FIG. 5 is a schematic cross section of two adjacent contact pads after completing the contact fabrication according to an embodiment of the invention.

FIG. 6 is a schematic cross section of two adjacent contact pads illustrating the improved process tolerance gained by the contact fabrication method of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The schematic cross section of FIG. 1 illustrates a portion on the surface of a semiconductor device, which has a protective overcoat 103, typically consisting of silicon nitride or oxynitride. A window in this overcoat exposes a metallic bond pad 101. The window has a diameter 103a. Bond pad 101 is located over insulating material 102. The bond pad metal 101 may be aluminum or copper, or stacked layers thereof. The insulator 102 may include mechanically weak dielectrics such as silicon-containing hydrogen silsesquioxane (HSQ), aerogels, organic polyimides, parlenes, or alternating layers of plasma-generated tetraethylorthosilicate (TEOS) oxide and HSQ, or ozone TEOS oxide and HSQ. The mechanical weakness of these dielectrics, generally referred to as low-k dielectrics, is prone to suffer cracks by mechanical pressure and stress created during the wire bonding operations, but their lower dielectric constant helps to reduce the capacitance C in the RC time constant of circuits and thus allows higher circuit speed.

A flattened metal ball 104 is in contact with bond pad 101. In this embodiment, the diameter 104a of ball 104 is less than or equal to diameter 103a of the overcoat window and the flattened metal ball is made of metal at least 99.999% pure, such as pure gold, copper, or

silver. These metals are commercially available by many companies, for instance, Nittetu Micro Metal, Japan, under the brand name 5N, or Degussa, Germany. At these high purity levels, these metals are very soft, especially when they are macro-crystalline (heat treated).

FIG. 1 further shows a wire 110 connected to the bond pad, wherein the wire has a diameter 110a and a thickened portion 111. Preferably, thickened portion 111 is created from a free air ball at the end of wire 110, by flattening this air ball. The thickened portion 111 is conductively attached to the flattened metal ball 104. Wire 110 is a composed metal such as gold alloy, copper alloy, or copper-coated gold, and has typically a diameter of about 20 to 25 μm . These wires are commercially available by many companies, for instance, Nittetu Micro Metal, Japan, under the brand name NT. In this composition, metal 110 is harder than the soft metal 104. These wires will, therefore, not sag even at long wire loops, and by choosing a large enough diameter, they will also have an electrical resistance lower than a predetermined value.

The cross section of FIG. 2 illustrates schematically a preferred method of fabricating a flattened ball 201 from a wire 202 of diameter 202a by employing the generally practiced wire ball bonding technology. Diameter 202a of wire 202 is preferably smaller than diameter 110a of bonding wire 110.

The preferred wire bonding process begins by positioning the semiconductor chip (only portion 200 shown in FIG. 2) on a heated pedestal to raise the temperature to between 150 and 300 $^{\circ}\text{C}$. The gold wire 202 is strung through a capillary of a diameter suitable for wire diameter 202a and a predetermined orifice. At the tip of the wire, a free air ball is created using either a flame or a spark technique. The ball has a typical diameter from about 1.2 to 1.6 wire diameters. The capillary is moved towards the chip bonding pad 210 and the ball is pressed against the metallization of the pad. Generally, a combination of compression force and ultrasonic energy create the formation of intermetallics between ball metal and pad metal and thus a strong metallurgical bond. The compression (also called Z- or mash) force is typically between about 17 and 75 g; the ultrasonic time between about 10 and 20 ms; the ultrasonic power between about 20 and 50 mW. At time of bonding, the temperature usually ranges from 150 to 270 $^{\circ}\text{C}$. For gold wire on copper pad, metal interdiffusion takes place in order to generate the strong weld. The exact outline of the flattened ball on FIG. 2 is a

function of the shape of the capillary orifice; the ball will be more flattened by the impact of the thickened wire end (ball) (111 in FIG. 1).

With the soft flattened ball 201 protecting the bond pad and its underlying dielectrics, the air ball 111 (FIG. 1) formed from wire 110 can be metallurgically attached with the required ultrasonic energy and pressure. In this action, ball 201 is flattened approximately into the shape shown for ball 104 in FIG. 1. After flattened ball 111 is attached, automated wire bonding allows tightly controlled shape of the wire loop.

As schematically illustrated in the example of FIG. 3, an electrically conducting line 301, or leadframe segment, is spaced from bond pad 101 by a gap 302. The gap 302 is bridged by wire loop 303. Moving the capillary in a predetermined and computer-controlled manner through the air will create a wire looping of exactly defined shape. For instance, with a modern wire bonder, rounded, trapezoidal, linear and customized loop paths can be formed without sagging. The electrical resistance of the whole loop 303 is kept under a predetermined value by the suitably large selected diameter 110a of wire 110. Finally, the capillary reaches its desired destination at conductive line or leadframe segment 301. The capillary is lowered to touch the line at 304; with the imprint of the capillary, a metallurgical stitch bond is formed, and the wire is broken off to release the capillary. Stitch contacts are small yet reliable; the lateral dimension of the stitch imprint is about 1.5 to 3 times the wire diameter (its exact shape depends on the shape of the capillary used, such as capillary wall thickness and capillary footprint).

FIG. 4 shows two bond pads 401 and 402 in close proximity; the ongoing trend in semiconductor technology is that the pad pitch 403 center-to-center is shrinking. It is a technical advantage of the present invention that it supports this trend towards fine pad pitch, because it provides metal stud contacts in the form of soft flattened balls 404 and 405, which may have a diameter smaller than or equal to the diameter of pads 401 and 402. The flattened balls 404 and 405 have been made from soft metal wire of small enough diameter 406.

FIGS. 5 and 6 illustrate how the present invention supports flattened contact balls with a diameter as large as, or even slightly larger than, the bond pads. In FIG. 5, two bond pads are designated 501 and 502, respectively, having a pitch center-to-center 503. The flattened, soft contact balls of small diameter, made from highly pure wire of small diameter,

are designated 504 and 505, respectively. The wire 510 of harder metal and larger diameter 510a provides flattened balls 511 and 512 having a diameter as large as, or even slightly larger than, the diameter of pads 501 and 502. The large diameter of balls 511 and 512 can be tolerated because of the height 520 of the underlying flattened soft balls 504 and 505.

5 FIG. 5 illustrates a flattened ball 511 and 512 in good alignment with contact pads 501 and 502, indicated by the dashed center lines.

In FIG. 6, however, the automated bonder of the capillary with the hard wire was misaligned relative to the pad locations, and thus produced flattened contact balls 611 and 612 having center lines systematically misaligned relative to the center lines of the pads. The
10 misalignment is designated 630. In spite of this mishapening, no electrical short between neighboring pads 601 and 602 is produced due to the height 620 of the flattened soft balls 604 and 605 under the balls 611 and 612. The invention thus supports process forgiveness in the device fabrication.

Another embodiment of the invention is the preferred method for fabricating a
15 semiconductor device, which comprises the following steps: Providing a semiconductor chip having at least one metallic bond pad over insulator material; the insulator may include mechanically weak low-k dielectrics. Next, forming a first free air ball at the tip of a first capillary loaded with an at least 99.999 % pure metal wire; examples include gold, copper, and silver wire. Next, attaching the freshly formed first free air ball to the bond pad,
20 flattening the first ball by means of the first capillary, and separating the flattened first ball from the pure wire.

The step of attaching the first free air ball may include mechanical pressure and ultrasonic energy without damaging mechanically weak low-k dielectrics under the bond pad, because of the softness of the pure metal. The step of separating the flattened ball may
25 consist of a flame-off process. It is preferred that the flattened first ball has a diameter smaller than or equal to the diameter of the bond pad.

In the next process step, a second free air ball is formed at the tip of a second capillary loaded with a composed metal wire. Examples of composed metals are alloys, such as gold alloy, coated wires, such as copper-coated gold, and process-hardened wires. The
30 freshly formed second free air ball is then attached to the flattened first ball; in this process, the second ball is flattened by means of said second capillary. The diameter of the second

flattened ball may be approximately the diameter of the bond pad. The step of attaching the second free air ball may include mechanical pressure and ultrasonic energy, but they are less likely to damage mechanically weak low-k dielectrics under the bond pad, because the flattened first ball made out of soft metal acts as a pressure-absorbing cushion.

5 Subsequently, the composed wire is spanned into a controlled loop, which bridges a gap between the bond pad and an electrically conductive line or a leadframe segment. The diameter of the composed wire is selected so that the loop has an electrical resistance equal to or below a certain predetermined value. This means, the diameter of the composed-metal wire may be larger than the diameter of the pure-metal wire.

10 While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description.

 As an example, the invention covers integrated circuits made in silicon, silicon
15 germanium, gallium arsenide, or any other semiconductor material used in integrated circuit manufacture.

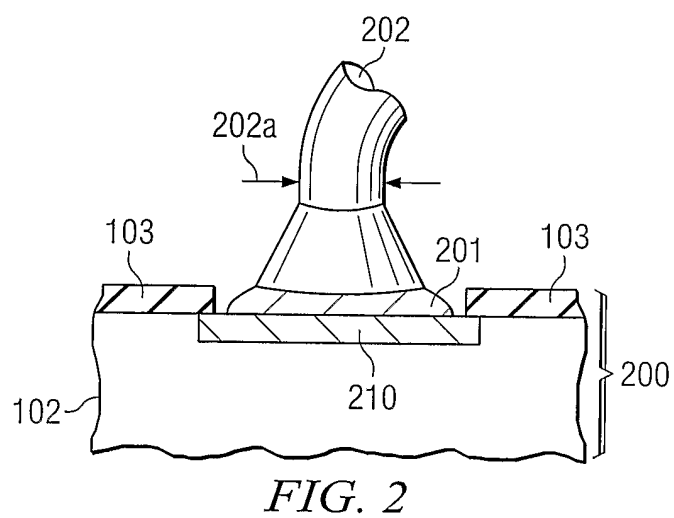
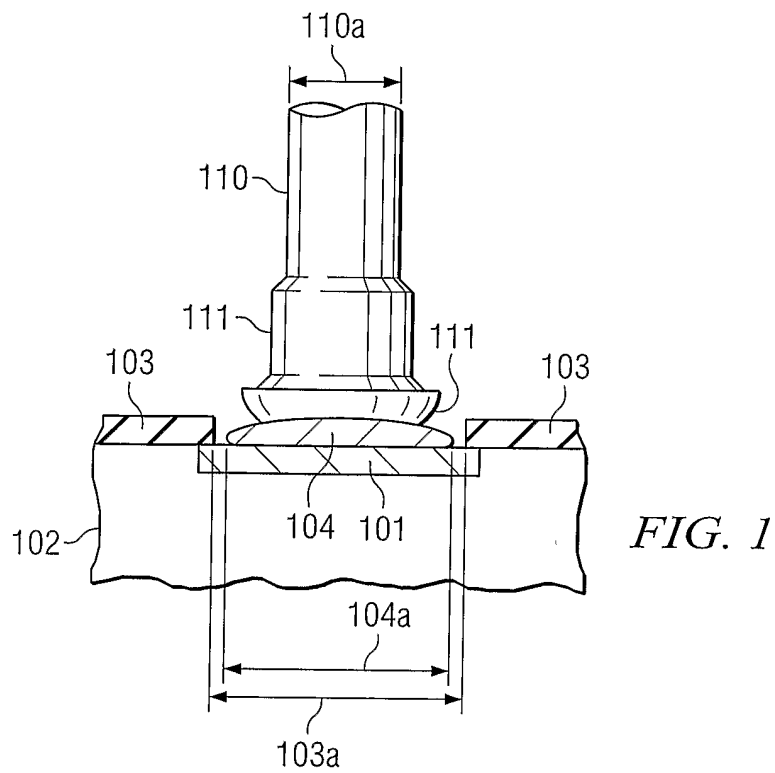
 As another example, in some devices, the dielectrics are fortified by metal-grid structures. For these strengthened insulators, a first flattened ball made of lightly less pure metal, for example, 99.99 % or 99.9 %, may be satisfactory.

20 It is therefore intended that the scope of the invention as defined by the specification and the claims encompass any such modifications or embodiments.

CLAIMS

1. A semiconductor device comprising:
a semiconductor chip having at least one metallic bond pad over insulator material;
a flattened metal ball in contact with said bond pad; and
a wire connected to said bond pad, said wire having a thickened portion conductively attached to said flattened metal ball, the composition of said ball being softer than said wire.
2. The device according to Claim 1, wherein said thickened wire portion is a flattened free air ball.
3. A method for fabricating a semiconductor device, comprising the steps of:
providing a semiconductor chip having at least one metallic bond pad over insulator material;
forming a flattened metal ball in contact with said bond pad; and
connecting a wire to said bond pad by forming a thickened portion of said wire on said flattened metal ball, the composition of said ball being softer than said wire.
4. The method according to Claim 3, wherein said forming and connecting steps further comprise:
forming a first free air ball at the tip of a first capillary of an at least 99.999 % pure metal wire;
attaching said freshly formed first free air ball to said bond pad, flattening said first ball with said first capillary, and separating said flattened first ball from said pure wire;
forming a second free air ball at the tip of a second capillary of a composed metal wire; and
attaching said freshly formed second free air ball to said flattened first ball and flattening said second ball with said second capillary.
5. The method according to Claim 4, further comprising the step of spanning said composed wire into a controlled loop to an electrically conducting line spaced from said bond pad by a gap and attaching the end of said loop to said line so that said loop bridges said gap.

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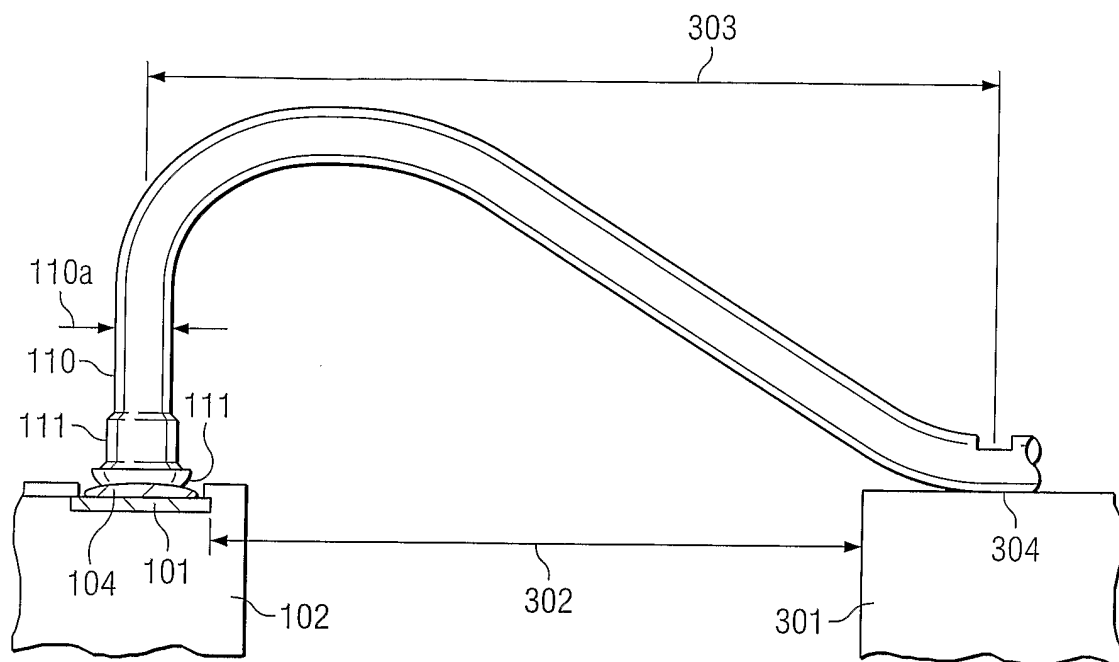


FIG. 3

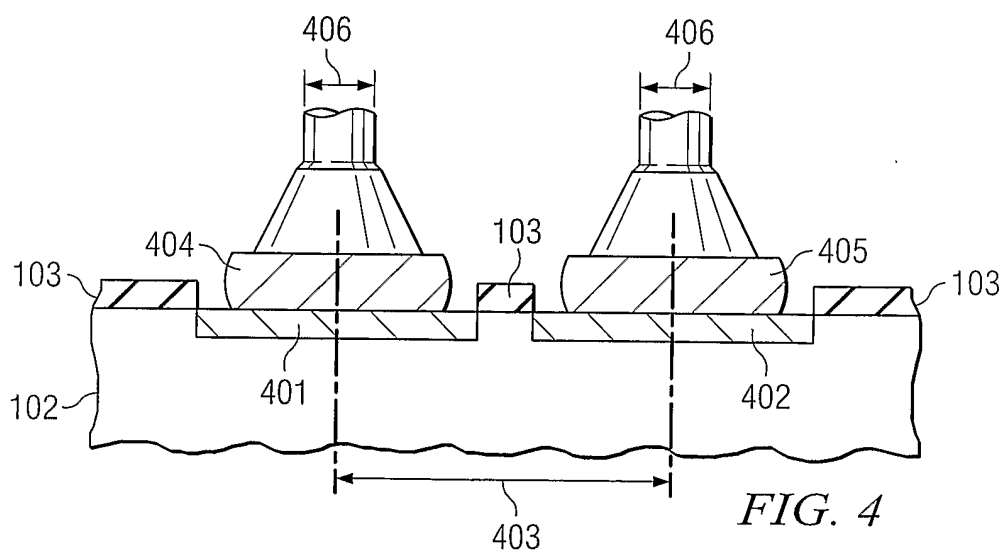
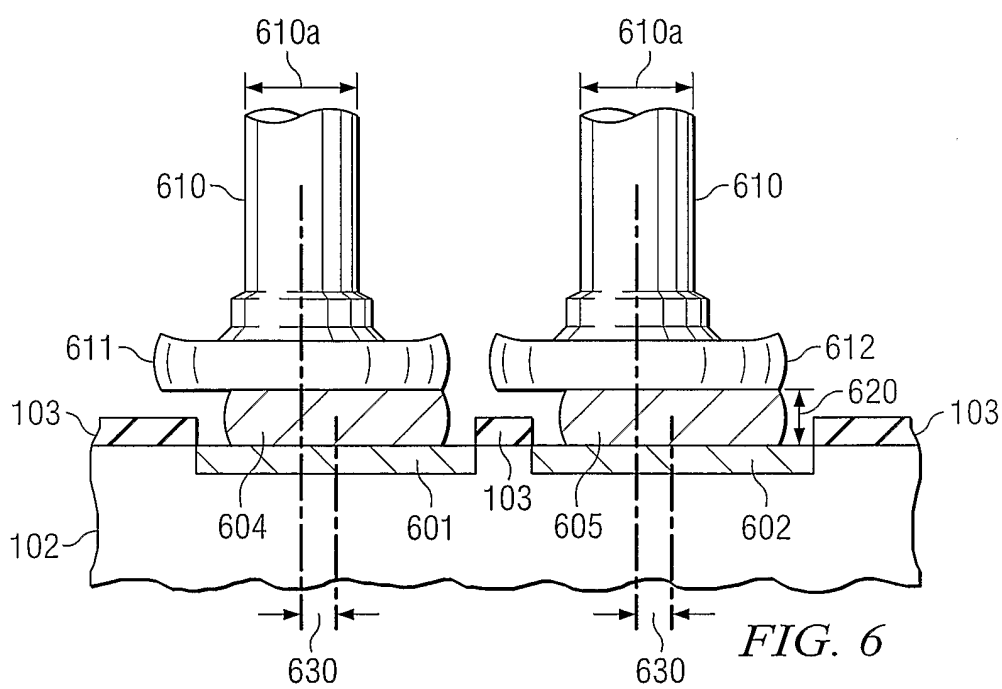
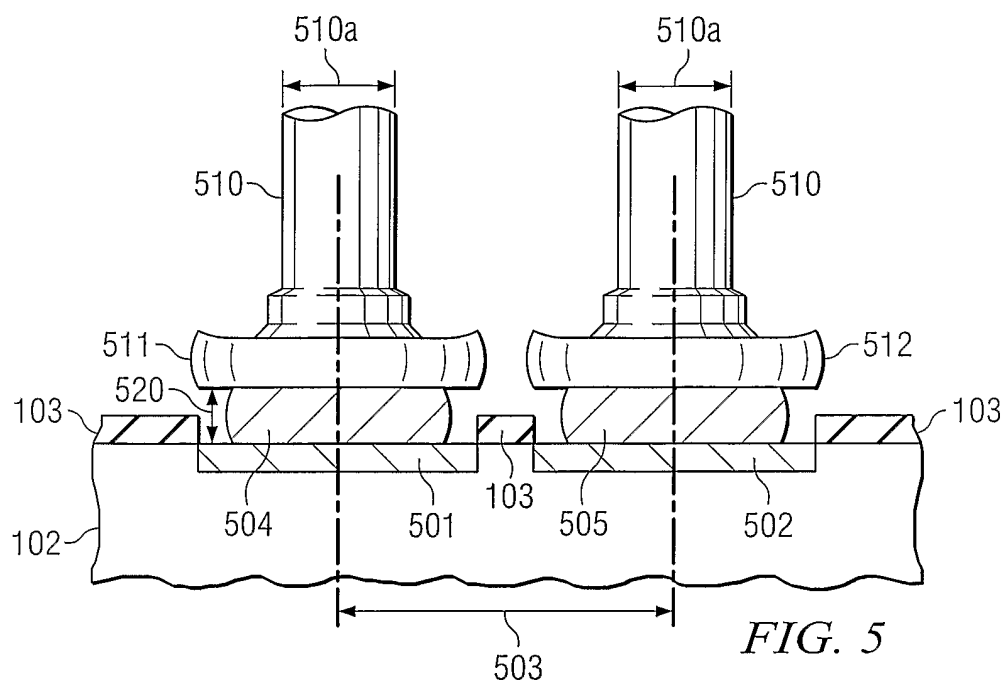


FIG. 4

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/47639

A. CLASSIFICATION OF SUBJECT MATTER

IPC: H01L 21/44(2006.01);B23K 31/00(2006.01),31/02(2006.01),37/00(2006.01)

USPC: 438/612,613,614;228/4.5,180.5

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/612,613,614; 228/4.5,180.5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6523255 B2 (SHIH et al) 25 February 2003 (25.02.2003), figure 5, and column 4 lines 40-64.	1-3
X	US 4695870 A (PATRAW) 22 September 1987 (22.09.1987), column 5 line 60 - column 6 line 23 and column 7 line 52 -column 8 line 19.	1-3
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Y	----- column 2 lines 44-62.	4,5
X	US 6334247 B1 (BEAMAN et al) 1 January 2002 (01.01.2002), figure 15, column 3 lines 40-67 and column 6 lines 18-37.	1-3
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Y	----- column 5 lines 53 - 67.	4,5
Y	US 5164336 A (OHNO et al) 17 November 1992 (17.11.1992), column 11 lines 20-29.	4,5

☐ Further documents are listed in the continuation of Box C.	☐ See patent family annex.
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