July 9, 1968 H. PATALONG 3,392,313

SEMICONDUCTOR DEVICE OF THE FOUR-LAYER TYPE

Original Filed June 17, 1963

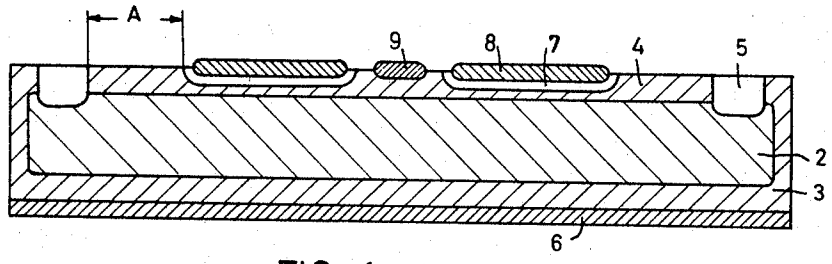

FIG. 1

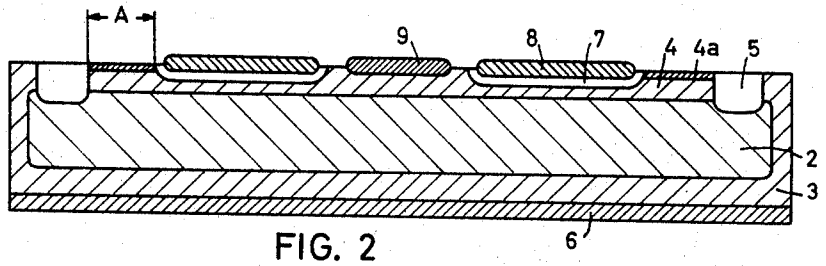

FIG. 2

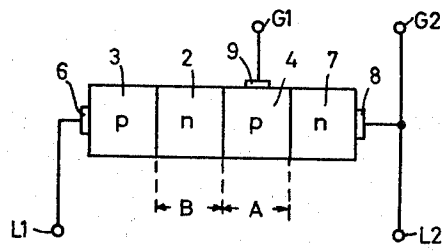

FIG. 3

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SEMICONDUCTOR DEVICE OF THE FOUR-LAYER TYPE

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Continuation of application Ser. No. 288,137, June 17, 1963. This application Dec. 12, 1966, Ser. No. 601,219
Claims priority, application Germany, June 19, 1962, S 79,974
6 Claims. (Cl. 317—235)

This application is a continuation of application S.N. 288,137 filed June 17, 1963, and now abandoned.

My invention relates to silicon controlled rectifiers, dynistors and other semiconductor devices of the four-layer type, having a substantially monocrystalline semiconductor body with four layers of alternately different types of conductance forming p-n junctions.

Such semiconductor devices afford a switching operation of thyratron character. The load current through all of the four layers may be started by means of an ignition current applied between one of the two intermediate layers and the adjacent outer layer. Switching-off is effected by the load current approaching, or passing through, zero. As a rule, the two outer layers carry respective electrodes for the load current, and one of the intermediate layers carries a base or gate contact for supplying the igniting or firing current. When the voltage applied across the two outer layers is greatly increased, the four-layer device may ignite without application of a firing current. The voltage magnitude at which this takes place is the so-called forward break-over voltage. This voltage decreases with increasing temperature so that p-n-p-n devices may lose the ability to block forward voltage. Particularly with respect to four-layer semiconductor devices that have a gate or third electrode for firing, efforts have been made to increase the break-over voltage as much as possible, because this voltage determines the rated load voltage of the device.

It is, therefore, an object of my invention to provide a p-n-p-n device of this type exhibiting a considerable increase in forward break-over voltage and load voltage by reliable means of utmost simplicity.

According to a feature of my invention, the distance or spacing between the two outer layers and the intermediate p-n junction on the surface of a p-n-p-n semiconductor body is larger by at least a factor of 20 than the diffusion length of the minority charge carriers in one surface layer of each intermediate layer. It has been found that this affords greatly increasing the break-over voltage, especially at elevated temperatures. This may be explained by the observed fact that even at room temperature the reverse current which exists while the four-layer semiconductor device is in the non-ignited state, flows mainly on the surface of the semiconductor body. Even with low voltages this surface current may reach such a high value that ignition will occur. Consequently, the ignition can be considerably retarded by a corresponding reduction of the surface current. This is particularly necessary at elevated temperatures, for instance, 100 to 150° C.

The invention will be further explained in detail by way of example with reference to the accompanying drawing in which FIGS. 1 and 2 show enlarged cross sections of two four-layer silicon-controlled rectifiers embodying features of the invention, and FIG. 3 is an explanatory diagram.

The device illustrated in FIG. 1 is produced in the following manner. A circular disc of n-type silicon has a resistivity of from 10 to 100 ohm-centimeters, a diameter of 18 mm., and a thickness of 250 microns. The disc is subjected to a diffusion process with aluminum and

is thus provided with a p-type region which completely surrounds the disc on all sides. By working an annular groove 5 into the disc, the region is subdivided into two p-type regions 4 and 3. The interior of the semiconductor body constitutes the original, unmodified n-type zone 2. The diffusion of aluminum into the body may be effected, for instance, by introducing a plurality of such semiconductor bodies and an amount of aluminum into a quartz ampoule which is then sealed off. The ampoule preferably is kept in an electric resistance furnace, at a temperature of 1200° C. for a period of approximately 60 hours. Thereafter the penetration depth of the aluminum diffused into the semiconductor body is approximately 60 to 70 microns. The aluminum concentration near the surface is approximately 3×10^{16} cm.$^{-3}$.

The groove 5 may be obtained by etching. For this purpose, the semiconductor body can be coated with Picein varnish. Then a pattern corresponding to the desired groove shape, for instance an annular trace, is scratched into this Picein layer on one of the flat faces of the round semiconductor disc. Subsequently, the entire unit is dipped into an etching solution which will now attack the semiconductor body surface only in those areas where the Picein has been removed therefrom. The depth of the groove is easily determined by correspondingly selecting the etching time. The groove must, along its entire length, penetrate at least the aluminum-doped marginal zone. Thus, in the illustrated embodiment of the present invention, the groove depth may be approximately 100 microns, its width depending on the width of the trace scratched open in the Picein coating and being, for instance, about 1 mm. For reasons of clarity the drawing illustrates the semiconductor elements on an enlarged and greatly disproportionate scale, particularly with respect to the thickness ratios thereof.

The groove 5 may also be obtained by a suitable mechanical process such as by grinding or lapping, using a tool of the hollow drill type, or by milling or cutting.

The required contacting electrodes are provided on the semiconductor body by a subsequent alloying process, with the still missing fourth zone being produced simultaneously therewith. The semi-conductor body is placed upon an aluminum foil having approximately the same diameter as the semiconductor body and having a thickness of about 60 microns. An annular foil consisting of a gold-antimony compound (approx. 0.5% Sb) and having an interior diameter of about 4 mm. and an outer diameter of about 11 mm. is superimposed upon the grooved surface of the semiconductor body. Another foil consisting of gold containing boron and having a diameter of approximately 3 mm. is placed centrally into the aperture of this annular disc. The foils may have a thickness of approximately 40 microns. The entire assembly is then heated in a furnace to a temperature of approximately 800° C., and the unit illustrated in FIG. 1 is obtained. The zone 3 receives a contact electrode 6 formed by the aluminum foil alloyed to the unit. An annular zone 7 doped with antimony and consequently exhibiting an n-type conductivity is formed on the top surface of the semiconductor element. It is contacted by an electrode 8, while the zone 4 carries a contact electrode 9.

As illustrated in FIG. 1, the semiconductor element thus comprises a four-layer structure consisting of the zones 3, 2, 4 and 7 arranged in a p-n-p-n sequence in accordance with the schematic diagram shown in FIG. 3 where the same respective reference numerals are applied as in FIG. 1. The intermediate p-n junction which will exert a blocking action as long as the semiconductor device is not ignited, is the p-n junction between zones 2 and 4. In accordance with the invention the dimensions

of the semiconductor member are such that the spacing A or B of the two outer layers 3, 7 from this p-n junction on the surface of the semiconductor body is larger by at least the factor 20 than the diffusion length of the minority charge carriers in the semiconductor material of the two intermediate layers 4 and 2 on the surface of the semiconductor body. The distance A on the surface of the semiconductor body between the layer 7 on the one hand, and the p-n junction located between the layers 2 and 4 on the other hand, is particularly of special importance. This distance was made approximately 2 mm. (this resulted from the chosen dimensions of the gold-antimony foil employed). The diffusion length L of the minority carriers in this range of the semiconductor surface is approximately 50 microns, so that the requirement

$$\frac{A}{L} \geqq 20$$

is met because

$$\frac{A}{L} = 40$$

As a result, the reverse current on the surface is considerably reduced, whereby the forward break-over voltage and its temperature stability are greatly increased.

FIG. 2 illustrates another embodiment of a four-layer semiconductor element embodying features of the present invention. The design and composition thereof is substantially the same as in FIG. 1. Identical zones and electrodes, respectively, are denoted by the same reference numerals. Also, the method of production thereof is substantially the same as described with reference to the first-mentioned embodiment. The only essential difference consists of adding a process step after the diffusion step producing the p-type marginal zones 4 and 3, and before the alloying process, so as to reduce considerably the diffusion length of the minority carriers within the surface area of zone 4. For this purpose the surface area denoted by 4*a* in FIG. 2, is flooded with impurities which are diffused therein. This may be effected by first coating the entire surface area of the semiconductor disc with an oxide layer, for instance by way of oxidation in steam at higher temperatures. Then an annular zone of this oxide layer is removed from the surface of the semiconductor body, for example by mechanical removal of the oxide with the aid of a tool of the hollow drill type. This annular zone may have an interior diameter of about 15 mm. and an outer diameter of about 17 mm. Then boron is diffused in a manner similar to the diffusion of aluminum forming the p-type marginal zone. This diffusion of boron, however, merely produces a high marginal concentration in the order of approximately 10^{18} to 10^{20} cm.$^{-3}$. Heating to a temperature of approximately 1280° C. for a duration of approximately one hour will be sufficient. The penetration depth of boron is only slight (about 5 to 10 microns) and will have the desired effect on the surface only. The diffusion length of the minority carriers within this zone 4*a* is reduced to approximately $L=10$ microns and the distance A may consequently also be reduced accordingly. This reduction allows for a larger n-type zone 7 and a larger contact electrode 8 superimposed thereon, thereby imparting an increased current-carrying capacity to the four-layer semiconductor device.

The same results can be obtained by increasing the annular width of the groove 5 and/or reducing the diffusion length of the minority carriers within the surface area at the bottom of groove 5. This is effective when the n-conductive zone 2 is contacted by an electrode at the bottom of groove 5 or at a similarly exposed area and is used as the gate. More particularly, according to the invention, when the zone 2 is the gate, separation between p-conducting zones 3 and 4 is not accomplished by etching but rather by completely cutting off the periphery of the disc. This is done by directing a sand blast at the location of the groove 5 and turning the disc through its vertical axis. The sand stream is then continued until it passes through the zone 2 and the entire thickness of the disc from top to bottom. In this case it is the dimension B, constituted by the thickness of zone 2, which is critical.

While embodiments of the invention have been described in detail, it will be obvious to those skilled in the art that the invention may be otherwise embodied.

I claim:

1. A semiconductor element comprising a substantially monocrystalline semiconductor body having a surface and a plurality of zones of alternating conductivity type forming three spaced intermediate p-n junctions one of which is formed between two others and emerges at the surface of said semiconductor body, said one of said p-n junctions being spaced from another of said p-n junctions by a distance along the surface of said semiconductor body larger than the diffusion length of the minority carriers on the surface of said semiconductor body between said p-n junctions by at least a factor of 20.

2. A semiconductor element as claimed in claim 1, further comprising a contact electrode on one of said zones at the surface of said semiconductor body between said p-n junctions.

3. A semiconductor element as claimed in claim 1, wherein the surface layer of said semiconductor body between said p-n junctions is provided with more dopant impurity atoms than the remainder of said semiconductor body.

4. A semiconductor element as claimed in claim 1, wherein said semiconductor body has four zones of alternating conductivity type consisting of two outer zones and two inner zones, said zones forming said three spaced intermediate p-n junctions one of which is formed between the two inner zones and emerges at the surface of said semiconductor body and is central to the other two and each of the others of which is formed between a corresponding one of said outer zones and a corresponding one of said inner zones, one of the p-n junctions formed between one of said outer zones and a corresponding one of said inner zones being spaced from the central p-n junction by a distance along the surface of the semiconductor body larger than the diffusion length of the minority carriers on said one of said inner zones of the semiconductor body on the surface of said semiconductor body between said two p-n junctions by at least the factor 20.

5. A semiconductor element as claimed in claim 4, further comprising a contact electrode on said one of said inner zones at the surface of said semiconductor body between said p-n junctions.

6. A semiconductor element as claimed in claim 4, wherein the surface layer of said semiconductor body between said p-n junctions is provided with more dopant impurity atoms than the remainder of said semiconductor body.

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