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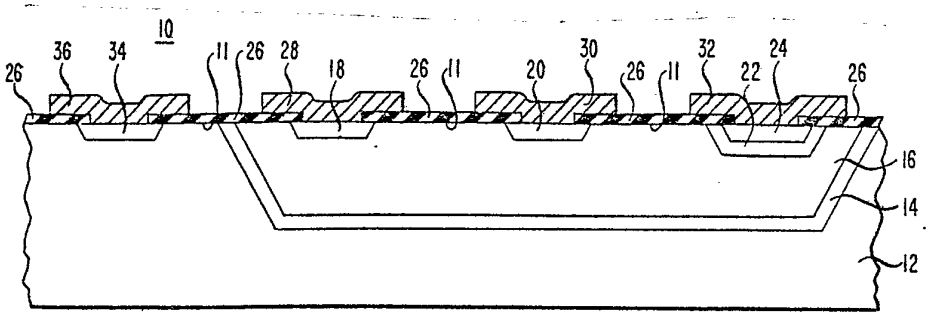

(57) Abstract

A high voltage solide-state switch, which allows alternating current or direct current operation and provides bidirectional blocking, consists of a first p-type semiconductor body (16) separated from a semiconductor substrate (12) by a dielectric layer (14) with a p+ type anode region (18), an n+ type cathode region (24) and an n+ type gate region (20) located on a common major surface of the semiconductor body. A second *p* type region (22) of higher impurity concentration than the semiconductor body encircles the cathode region. Separate low resistance electrical contacts are made to the anode, cathode, and gate regions.

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HIGH VOLTAGE DIELECTRICALLY ISOLATED SOLID-STATE SWITCH

Technical Field

This invention relates to solid-state structures and, in particular, to high voltage solid-state structures useful in telephone switching systems and many other applications.

Background of the Invention

In an article entitled "A Field Terminated Diode" by Douglas E. Houston et al, published in IEEE Transactions on Electron Devices, Vol. ED-23, No. 8, August 1976, there is described a discrete solid-state high voltage switch that has a vertical geometry and which includes a region which can be pinched off to provide an "OFF" state or which can be made highly conductive with dual carrier injection to provide an "ON" state. One problem with this switch is that it is not easily integrated, i.e., manufactured with other like switching devices on a common substrate. Another problem is that the spacing between the grids and the cathode should be small to limit the magnitude of the control grid voltage; however, this limits the useful voltage range because it decreases grid-to-cathode breakdown voltage. This limitation effectively limits to relatively low voltages the use of two of the devices connected in antiparallel, i.e., with the cathode of each coupled to the anode of the other. Such a dual device structure would be useful as a high voltage bidirectional solid-state switch. An additional problem is that the base region should ideally be highly doped to avoid punch-through from the anode to the grid; however, this leads to a low voltage breakdown between anode and cathode. Widening of the base region limits the punch-through effect; however, it also increases the resistance of the devices in the "ON" state.

It is desirable to have a solid-state switch which is easily integratable such that two or more switches

can be simultaneously fabricated on a common substrate and wherein each switch is capable of bilateral blocking of relatively high voltages.

Summary of the Invention

One embodiment of the present invention is a structure comprising a semiconductor body whose bulk is of one conductivity type and which has a major surface within which semiconductor body is a localized anode region which is of the one conductivity type, and localized gate and cathode regions which are both of the opposite conductivity type. The anode gate and cathode regions are spaced apart from each other, have separate electrode connections thereto, and are of relatively low resistivity compared to the bulk of the semiconductor body. The structure is so adapted that during operation there is dual carrier injection and is further characterized in that each of the three regions has a portion which forms part of the major surface of the semiconductor body.

In a preferred embodiment the semiconductor body is isolated from a semiconductor support by a dielectric layer and a plurality of said bodies are formed in said support and are separated from each other by at least a dielectric layer.

The structure of the present invention, when suitably designed, can be operated as a switch that is characterized by a low impedance path between anode and cathode when in the ON (conducting) state and a high impedance path between anode and cathode when in the OFF (blocking) state. The potential applied to the gate region determines the state of the switch. During the ON state there is dual carrier injection that results in the resistance between anode and cathode being relatively low.

This structure, which is to be denoted as a gated diode switch (GDS), when suitably designed, is capable in the OFF state of blocking relatively large potential differences between anode and cathode regions, independent of polarity, and is capable in the ON state of conducting relatively large amounts of current with a relatively low

voltage drop between anode and cathode.

Arrays of these GDSs can be fabricated on a single integrated circuit chip together with other high voltage circuit components. The bilateral blocking characteristic of the structure facilitates its use in a bidirectional switch formed by two of the structures of the present invention with the cathode of each coupled to the anode of the other and the gates being coupled together.

These and other novel features and advantages of the present invention are better understood from consideration of the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 illustrates a structure in accordance with one embodiment of the invention;

FIG. 2 illustrates a proposed electrical circuit symbol for the structure of FIG. 1;

FIG. 3 illustrates a bidirectional switch circuit in accordance with another embodiment of the invention;

FIG. 4 illustrates a structure in accordance with another embodiment of the invention;

FIG. 5 illustrates a structure in accordance with still another embodiment of the invention; and

FIG. 6 illustrates a structure in acccordance with still another embodiment of the invention;

FIG. 7 illustrates a structure in accordance with another embodiment of the invention;

FIG. 8 is a top view of the structure of FIG. 6.

Detailed Description

Referring now to FIG. 1, there is illustrated a structure 10 comprising a support member 12 of n- conductivity type having a major surface 11 and a monocrystalline semiconductor body 16 whose bulk is of p- conductivity type and which is separated from support member 12 by a dielectric layer 14.

A localized anode region 18, which is of p+ type conductivity, is included in body 16 and has a

portion thereof that extends to surface 11. A localized gate region 20, which is of n+ conductivity, also is included in body 16 and has a portion thereof which extends to surface 11. A localized cathode region 24, which is of n+ type conductivity, is included in body 16 and has a portion which extends to surface 11. A region 22, which is of p+ type conductivity and has a portion which extends to surface 11, encircles region 24 and acts as a depletion layer punch-through shield. In addition it acts to inhibit inversion of the portions of body 16 at or near surface 11 between regions 20 and 24. Gate region 20 exists between anode region 18 and region 22 and is separated from both by bulk portions of body 16. The resistivities of regions 18, 20, and 24 are low compared to that of the bulk portions of body 16. The resistivity of region 22 is intermediate that of cathode region 24 and the bulk portion of body 16.

Electrodes 28, 30, and 32 are conductors which make low resistance contact to the surface portions of regions 18, 20, and 24, respectively. A dielectric layer 26 covers major surface 11 so as to isolate electrodes 28, 30 and 32 from all regions other than those intended to be electrically contacted. An electrode 36 provides a low resistance contact to support 12 by way of a highly doped region 34 which is of the same conductivity type as support 12.

Advantageously, the support 12 and the body 16 are each of silicon and the support 12 may be either of n or p type conductivity. Each of electrodes 28, 30 and 32 advantageously overlaps the semiconductor region to which they make low resistance contact. Electrode 32 also overlaps region 22. This overlapping, which is known as field plating, facilitates high voltage operation because it increases the voltage at which breakdown occurs. Dielectric layer 14 is silicon dioxide and electrodes 28, 30, 32, and 36 are all aluminum. Conductivities complementary to those described may be used.

A plurality of separate bodies 16 can be formed in a common support 12 to provide a plurality of switches. Significantly, planar processing techniques can be used to fabricate many devices as an integrated circuit on a common surface.

Structure 10 is typically operated as a switch which is characterized by a low impedance path between anode region 18 and cathode region 24 when in the ON (conducting) state and as a high impedance between said two regions when in the OFF (blocking) state. The potential applied to gate region 20 determines the state of the switch. Conduction between anode region 18 and cathode region 24 occurs if the potential of gate region 20 is below that of the potential of anode region 18 and cathode region 24. During the ON state holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons can be in sufficient numbers to form a plasma which conductivity modulates body 16. This reduces the resistance of body 16 such that the resistance between anode region 18 and cathode region 24 is low when structure 10 is operating in the ON state. This type of operation is denoted as dual carrier injection. The type of structure described herein is denoted as a gated diode switch (GDS).

Region 22 helps limit the punch-through of a depletion layer formed during operation between gate region 20 and cathode region 24 and helps inhibit formation of a surface inversion layer between these two regions. This permits closer spacing of gate region 20 and cathode region 24 and results in a relatively low resistance between anode region 18 and cathode region 22 during the ON state.

Substrate 12 is typically held at the most positive potential level available. Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of gate region 20 is sufficiently more positive than that of anode region

18 and cathode region 24. The amount of excess positive potential needed to inhibit or cut off conduction is a function of the geometry and impurity concentration (doping) levels of structure 10. This positive gate potential causes the portion of body 16 between gate region 20 and dielectric layer 14 to be depleted of current carrier such that the potential of this portion of body 16 is more positive than that of anode region 18 and cathode region 24. This positive potential barrier inhibits the conduction of holes from anode region 18 to cathode region 24. It essentially pinches off body 16 against dielectric layer 14 in the bulk portion between gate region 20 and dielectric layer 14. It also serves to collect electrons emitted at cathode region 24 before they can reach anode region 18.

During the ON state of structure 10, the junction diode comprising body 16 and region 20 becomes forward-biased. Current limiting means (not illustrated) are preferably included to limit the conduction through the forward-biased diode.

A proposed electrical symbol adopted for this type of switch is illustrated in FIG. 2. The anode, gate, and cathode electrodes of the GDS are denoted as terminals 28, 30, and 32, respectively.

One embodiment of structure 10 has been fabricated with the following design. Support member 12 is an n type silicon substrate, 0.457 to 0.559 mm. thick, with an impurity concentration of approximately 2 x 10^{13} impurities/cm^3, and has a resistivity greater than 100 ohm-centimeters. Dielectric layer 14 is a silicon dioxide layer 14 that is 2 to 4 microns thick. Body 16 is typically 30 to 50 microns thick, approximately 430 microns long, 300 microns wide, and is of p type conductivity with an impurity concentration in the range of approximately 5- 9 x 10^{13} impurities/cm^3. Anode region 18 is of p+ type conductivity, is typically 2 to 4 microns thick, 44 microns wide, 52 microns long, and has an impurity

concentration of approximately 10^{19} impurities/cm^3. Electrode 28 is typically aluminum, with a thickness of $1\frac{1}{2}$ microns, a width of 84 microns, and a length of 105 microns. Region 20 is of n+ type conductivity and is typically 2 to 4 microns thick, 15 microns wide, 300 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm^3. Electrode 30 is aluminum, $1\frac{1}{2}$ microns thick, 50 microns wide, and 210 microns long. The spacing between adjacent edges of electrodes 28 and 30 and between adjacent edges of electrodes 30 and 32 is typically 40 microns in both cases. Region 22 is p type conductivity and is typically 3-6 microns thick, 64 microns wide, 60 microns long, and has an impurity concentration of approximately 10^{17} to 10^{18} impurities/cm^3. Cathode region 24 is n+ type conductivity and is typically 2 microns thick, 48 microns wide, 44 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm^3. Electrode 32 is aluminum, $1\frac{1}{2}$ microns thick, 104 microns wide, and 104 microns long. The spacing between the ends of regions 18 and 22 and the respective ends of region 16 is typically 55 microns. Region 34 is n+ type conductivity and is typically 2 microns thick, 26 microns wide, 26 microns long, and has an impurity concentration of 10^{19} impurities/cm^3. Electrode 36 is aluminum which is $1\frac{1}{2}$ microns thick, 26 microns wide, and 26 microns long.

Structure 10, using the parameters denoted above, has been operated as a gated diode switch (GDS) with 500 volts between anode and cathode. A layer of silicon nitride (not illustrated) was deposited by chemical vapor deposition on top of silicon dioxide layer 26 to provide a sodium barrier. Electrodes 28, 30, 32, and 36 were then formed and thereafter a coating of radio frequency plasma deposited silicon nitride (not illustrated) was applied to the entire surface of structure 10 except where electrical contact is made. The layers of silicon nitride serve to help prevent high

voltage breakdown in the air between adjacent electrodes.

Typically the anode had +250 volts applied thereto, the cathode had -250 volts applied thereto, and substrate 12 had +280 volts applied thereto. The -250 volts can also be applied to the anode and the +250 volts applied to the cathode. Thus, structure 10 bilaterally blocks voltage between anode and cathode. A potential of +280 volts applied to gate conductor 30 interrupted (broke) 350 mA of current flow between anode region 15 and cathode region 24. The ON resistance of the GDS with 100 mA flowing between anode and cathode is approximately 15 ohms and the voltage drop between anode and cathode is typically 2.2 volts.

Referring now to FIG. 3, there is illustrated a bidirectional switch combination comprising two GDSs (GDS and GDSa) in accordance with the present invention with electrode 28 (the anode electrode of GDS) electrically connected to electrode 32a (the cathode electrode of GDSa), and electrode 32 (the cathode electrode of GDS) electrically connected to electrode 28a (the anode electrode of GDSa). This switch combination is capable of conducting signals from electrodes 28 and 32a to electrodes 28a and 32 or vice versa. The bilateral blocking characteristic of structure 10 facilitates this bilateral switch combination. Two separate bodies 16 can be formed in a common support 12 and the appropriate electrical connections can be made to form the above-described bidirectional switch. A plurality of separate bodies 16 can be formed in a common support 12 to form an array of switches.

Referring now to FIG. 4, there is illustrated a structure 410 which is very similar to structure 10 with all components essentially identical or very similar to those of structure 10 being denoted by the same reference number with the addition of a "4" at the beginning. The basic difference between structures 410 and 10 is the elimination from structure 410 of

semiconductor region 22 of FIG. 1. Appropriately increasing the spacing of region 424 from region 420 provides sufficient protection against depletion layer punch-through to region 424 and permits the use of structure 410 as a high voltage switch.

Referring now to FIG. 5, there is illustrated a structure 510 which is very similar to structure 10 and all components of which are essentially the same or very similar are denoted by the same reference number with the addition of a "5" at the beginning. The main difference between structure 510 and structure 10 is the use of a semiconductor guard ring region 540 which encircles cathode region 524. The dashed line portion of guard ring 540 illustrates that it can be extended so as to contact cathode region 524. The combination of region 522 and guard ring 540 provides protection against inversion of portions of region 516 at or near surface 511 particularly between gate region 520 and cathode region 524 and provides protection against depletion layer punch-through to cathode region 524. Guard ring 540 is of the same conductivity as region 522, but is of lower resistivity. This type of dual protection structure encircling cathode region 524 is the preferred protection structure.

The embodiments described herein are intended to be illustrative of the general principles of the invention. Various modifications are possible consistent with the spirit of the invention. For example, for the designs described, support members 12, 412 and 512 can alternatively be p-type conductivity silicon, gallium arsenide, sapphire, a conductor, or an electrically inactive material. If regions 12, 412 and 512 are electrically inactive materials then dielectric layers 14, 414 and 514 can be eliminated. Still further, bodies 16, 416 and 516 can be fabricated as air insulated type structures. This allows for the elimination of support members 12, 412 and 512 and dielectric layers 14, 414 and 514. The electrodes can be

doped polysilicon, gold, titanium, or other types of conductors. Further, the impurity concentration levels, spacings between different regions, and other dimensions of the regions can be adjusted to allow significantly different operating voltages and currents than are described. Other types of dielectric materials, such as silicon nitride, can be substituted for silicon dioxide. The conductivity type of all regions within the dielectric layer can be reversed provided the voltage polarities are appropriately changed in the manner well known in the art. It is to be appreciated that the structure of the present invention permits alternating or direct current operation.

Referring to FIG. 6 there is shown another embodiment with reference numbers in the 600 series corresponding to FIG. 1, in which the semiconductor body 616 is isolated from the dielectric layer 614 by an intervening semiconductor layer 638 having a conductivity type opposite that of semiconductor body 616. Electrodes 628, 630, and 632 are conductors which make low resistance contact to the surface portions of regions 618, 620, and 624, respectively. A dielectric layer 26 covers major surface 611 so as to isolate electrodes 628, 630, and 632 from all regions other than those intended to be electrically contacted. Electrode 630 makes electrical contact to region 638 at surface 611 in the rear or front of body 616 (not illustrated).

Layer 638 can be modified such that it exists only on the lower portion of body 16 as shown by region 638a. With such modification an appropriate diffused or ion implanted region(s) (not illustrated) is formed between surface 611 and modified layer 638a. Electrode 630 would extend to make electrical contact to this region at surface 611.

Layer 638 serves to isolate body 616 from the properties of dielectric layer 614 and thus aids the fabrication process in that the tolerances in the formation of the dielectric layer 14 can be relaxed

somewhat. This increases fabrication yields and reduces costs. In addition layer 638 serves as a lower gate region which aids in reducing the magnitude of the gate potential needed to inhibit or cut off conduction between the anode 618 and cathode 624 regions. The use of only portion 638a of layer 638 serves to isolate body 616 from region 614 in the portion of body 616 which is under region 620. This particular portion of body 616 is the most critical portion since body 616 is essentially "pinched off" in this portion when structure 610 is operated in the OFF state.

Layer 638a does not provide complete isolation from dielectric layer 14, but it reduces the gate potential needed for turn-off while essentially not affecting the breakdown voltage of the structure. Layer 638 provides complete isolation from dielectric layer 614 but does reduce the breakdown voltage of the structure somewhat. If layer 638 is used, then generally body 616 is increased in thickness to maintain breakdown voltages at preselected levels.

Layer 638 need not necessarily be directly connected to electrode 630. Because positive charge resides in layer 626, a surface inversion layer will form near the surface 611 of body 616 between layer 638 and gate region 620 which may electrically couple the two. Even without said positive charge it is believed that, due to punch-through, electrode 630 and layer 638 may be electrically coupled.

Referring to FIGS. 7 and 8, there is shown still another embodiment, having reference numbers in the 700 series corresponding to FIG. 1, in which the gate region 720 is not located between the anode region 718 and the cathode region 724. Structure 710 is designed such that anode region 18 and cathode region 724 can be spaced relatively closely to each other in order to reduce the resistance between the two during the ON (conducting) state. A conductor 738, which is optional, is located on top of layer 726 between electrodes 728 and

732. Conductor 738 is electrically coupled to electrode 730, and it helps reduce the magnitude of the gate voltage necessary in the operation of structure 710, but is not essential for operation.

One embodiment of structure 710 has been fabricated with the following design. Semiconductor wafer (substrate,) 712 is an n-type silicon substrate, 457 to 559 microns thick, with an impurity concentration of approximately 5 x 10^{13} impurities/cm^3, and is 100 ohm-centimeter type material. Dielectric layer 714 is silicon dioxide that is typically 2 to 4 microns thick. Body 716 is typically 30 to 40 microns thick, approximately 430 microns long, 170 microns wide, and is of p- type conductivity with an impurity concentration of approximtely 5- 9 x 10^{13} impurities/cm^3. Anode region 718 is of p+ type conductivity, is typically 2 to 4 microns thick, 28 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm^3. Electrode 728 is aluminum, with a thickness of $1\frac{1}{2}$ microns, a width of 55 microns, and a length of 95 microns. Gate region 720 is of n+ type conductivity, is typically 2 to 4 microns thick, 38 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm^3. Electrode 730 is aluminum with a thickness of $1\frac{1}{2}$ microns, a width of 76 microns, and a length of 95 microns. The spacing between adjacent edges of electrodes 728 and 732 is typically 40 microns (with no conductor 738) and the spacing between adjacent edges of electrodes 728 and 730 is typically 40 microns. Region 722 is of p type conductivity and is typically 3.5 microns thick, 44 microns wide, 44 microns long, and has a surface impurity concentration of approximately 10^{18} impurities/cm^3. Cathode region 724 is of n+ type conductivity and is typically 2 microns thick, 30 microns wide, 30 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm^3. Electrode 32 is aluminum, $1\frac{1}{2}$ microns thick, 82 microns wide, and 82

microns long. The spacing between the ends of electrodes 728 and 732 and the respective ends of p- type body 716 is 50 microns. Conductor region 738, which is aluminum, is spaced 30 microns apart from electrodes 728 and 732 and is 10 microns wide, $1\frac{1}{2}$ microns thick, and 75 microns long. Conductor region 738 makes electrical contact to electrode 730 in the front or rear of region 16. It can be appreciated that with this configuration the cathode to anode spacing is significantly reduced.

Structure 710, using the parameters denoted above, has been operated as a gated diode switch with 400 volts between anode and cathode. The anode had +200 volts applied thereto and the cathode had -200 volts applied thereto. As before, the -200 volts can also be applied to the anode and the +200 volts can be applied to the cathode to permit bilateral voltage blocking. With conductor region 738 being present, a potential of +210 volts was found sufficient to break 1 mA of current flow between anode and cathode. It is estimated that this voltage would need to be 20 volts higher if conductor 738 were eliminated. The ON resistance of the gated diode switch with 100 mA flowing between anode and cathode was approximately 10-12 ohms and the voltage drop between anode and cathode is typically 2.2 volts. A layer of silicon nitride (not illustrated) was deposited by chemical vapor deposition on top of silicon dioxide layer 26 to act as a sodium barrier. Electrodes 728, 730, 732, and 736 were then formed and a coating of radio frequency plasma deposited silicon nitride (not illustrated) was applied to the entire surface of structure 710 to help prevent high voltage breakdown in the air between adjacent electrodes.

As in FIG. 5, a guard ring either surrounding or enclosing and contacting the cathode region 724 can be used, or, as in FIG. 4, region 722 can be eliminated if the anode cathode spacing is sufficient. Gate region 20 can be located to the right of cathode region 724, as indicated by the dashed lines of FIG. 7,

or to the front or rear of semiconductor body 716 as indicated by the dashed line of FIG. 2. Gate region 720 can be separated from the dielectric layer 714 or, as illustrated by the dashed lines of FIG. 7, or extend so as to contact dielectric layer 714. Other modifications as mentioned before may be used.

Claims

1. A solid-state switching device comprising a semiconductor body (16) a bulk portion of which is of a first conductivity type, a first region (18) of the first conductivity type, a second region (24) of a second conductivity type opposite that of the first conductivity type, a gate region (20) of the second conductivity type, the first, second, and gate regions being mutually separated by portions of the bulk portion, the resistivities of the first, second and gate regions being lower than the resistivity of the bulk portion, the parameters of the device being such that, with a first voltage applied to the gate region, a depletion region is formed in the semiconductor body which substantially prevents current flow between the first and second regions, and that, with a second voltage applied to the gate region and with appropriate voltages applied to the first and second regions, a relatively low resistance current path is established between the first and second regions by dual carrier injection,

CHARACTERIZED IN THAT

the first and second regions and the gate region each have a surface contained on a first major surface of the semiconductor body (16).

2. A switching device in accordance with claim 1

CHARACTERIZED IN THAT

the gate region (20) is located between the first (18) and second (24) regions.

3. A switching device in accordance with claim 1

CHARACTERIZED IN THAT

the second region (24) is surrounded by a third region (22) of the first conductivity type but of a lower resistivity than the bulk portion (16).

4. A plurality of switching devices each in accordance with claim 1

CHARACTERIZED IN THAT

each is included in a semiconductor support (12)

and is dielectrically (14) isolated from one another.

5. A pair of switching devices each in accordance with claim 1

CHARACTERIZED IN THAT

the gate electrodes of the pair are connected to one another and the first region of each is connected to the second region of the other to provide a bilateral switch (FIG. 3).

6. The switching device of claim 1

CHARACTERIZED IN THAT

a plurality of semiconductor bodies (16) are separated by a dielectric layer (16) and are supported by a support member (12), the support member and semiconductor bodies are of silicon, and a contact region (34) is included in the support member.

7. The switching device of claim 6

CHARACTERIZED IN THAT

the gate regions of first and second semiconductor bodies are interconnected, the first region of the first body is connected to the second region of the second body and the first region of the second body is connected to the second region of the first body (FIG. 3).

8. The switching device of claim 1

CHARACTERIZED IN THAT

the semiconductor body (16) is located within a support member (12) and is separated from the support member by a dielectric layer (14).

9. The switching device of claim 8

CHARACTERIZED IN THAT

the semiconductor body includes a fourth region (638) of the second conductivity type contained between the bulk portion (616) and the dielectric layer (614).

10. The switching device of claim 9

CHARACTERIZED IN THAT

the fourth region (638) is connected to the gate region (620).

11. The switching device of claim 10 CHARACTERIZED IN THAT the second region (624) is surrounded by a third region (622) of the first conductivity type but of a lower resistivity than the bulk portion (616).

12. The switching device of claim 9 CHARACTERIZED IN THAT the fourth region (638a) is located only in the area of the semiconductor body (616) which is between the gate region (620) and the dielectric layer (614).

13. The switching device of claim 9 CHARACTERIZED IN THAT the fourth region (638) is located along substantially the entire area of the semiconductor body (616) bounded by the dielectric layer (614).

14. The switching device of claim 1 CHARACTERIZED IN THAT the first (718) and second (724) regions are separated by part of the bulk portion (716) and the gate region (720) is located on part of the major surface other than the part that separates the first and second regions.

15. The switching device of claim 14 CHARACTERIZED IN THAT a conductor (738) electrically coupled to the gate region (720) is located between the first (718) and second (724) regions.

16. The switching device of claim 14 CHARACTERIZED IN THAT the bulk portion (716) is separated from a semiconductor support member by a dielectric layer.

17. The switching device of claim 16 CHARACTERIZED IN THAT the semiconductor support member has a separate electrode contacted thereto which is adapted to be biased at the most positive voltage of the

switching device.

18. The switching device of claim 3 CHARACTERIZED IN THAT the conductivity of the semiconductor body bulk portion (16), the first region (18), the second region (24), the third region (22) and the gate region (20) are of p-, p+, n+, p, and n+ conductivity type, respectively.

19. The switching device of claim 3 CHARACTERIZED IN THAT the third region surrounds but does not contact the second region.

20. The switching device of claim 3 CHARACTERIZED IN THAT the second region contacts, and is contained within, the third region.

FIG. 1

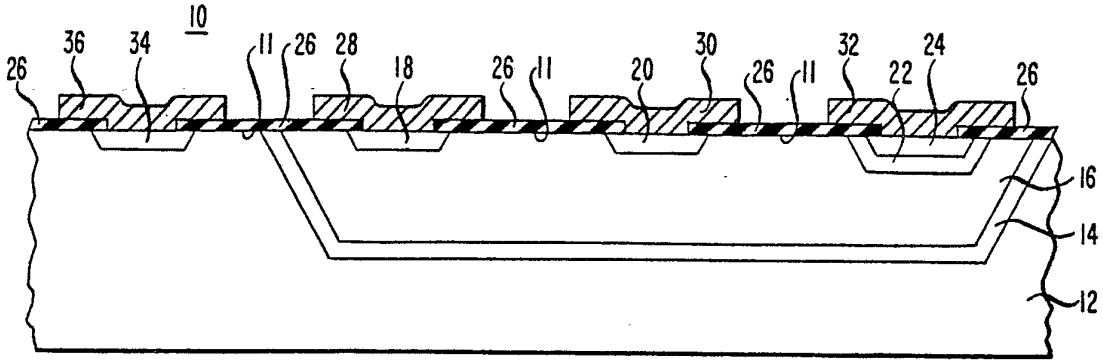


FIG. 2

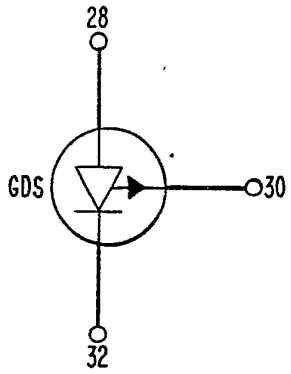


FIG. 3

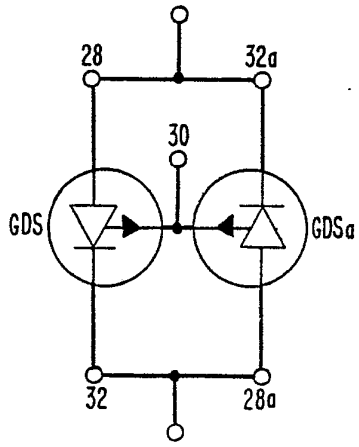


FIG. 4

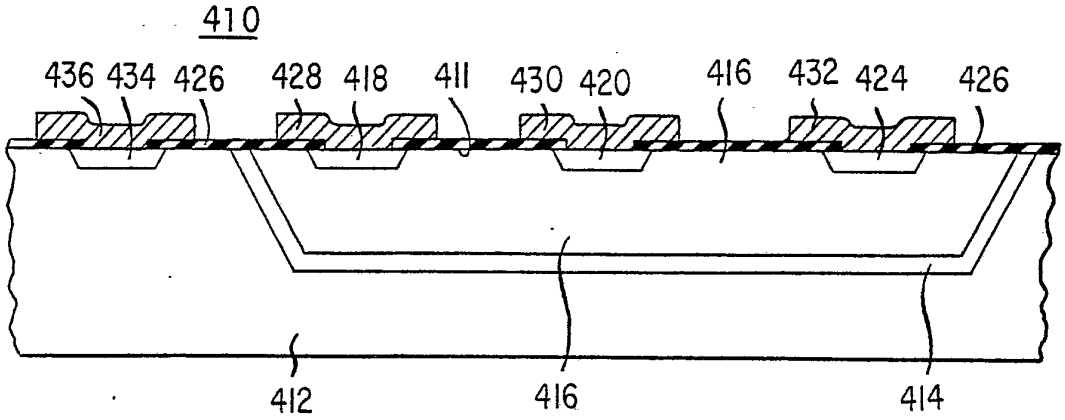


FIG. 5

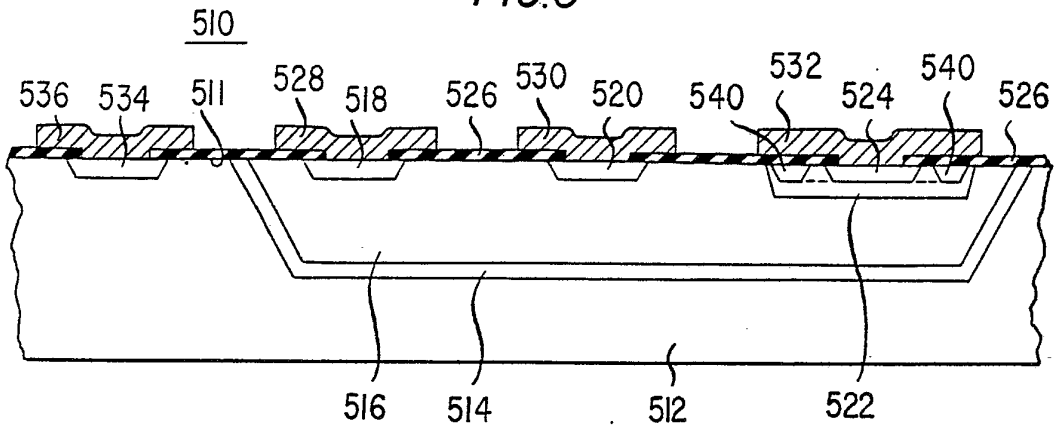


FIG. 6

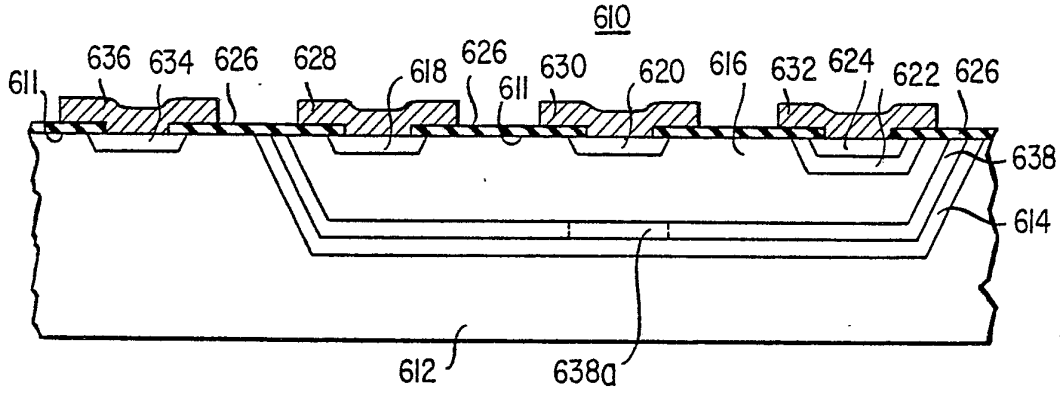


FIG. 7

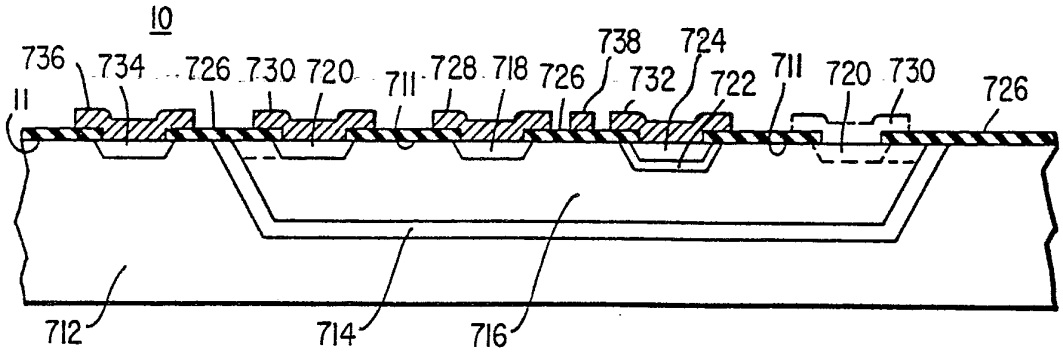
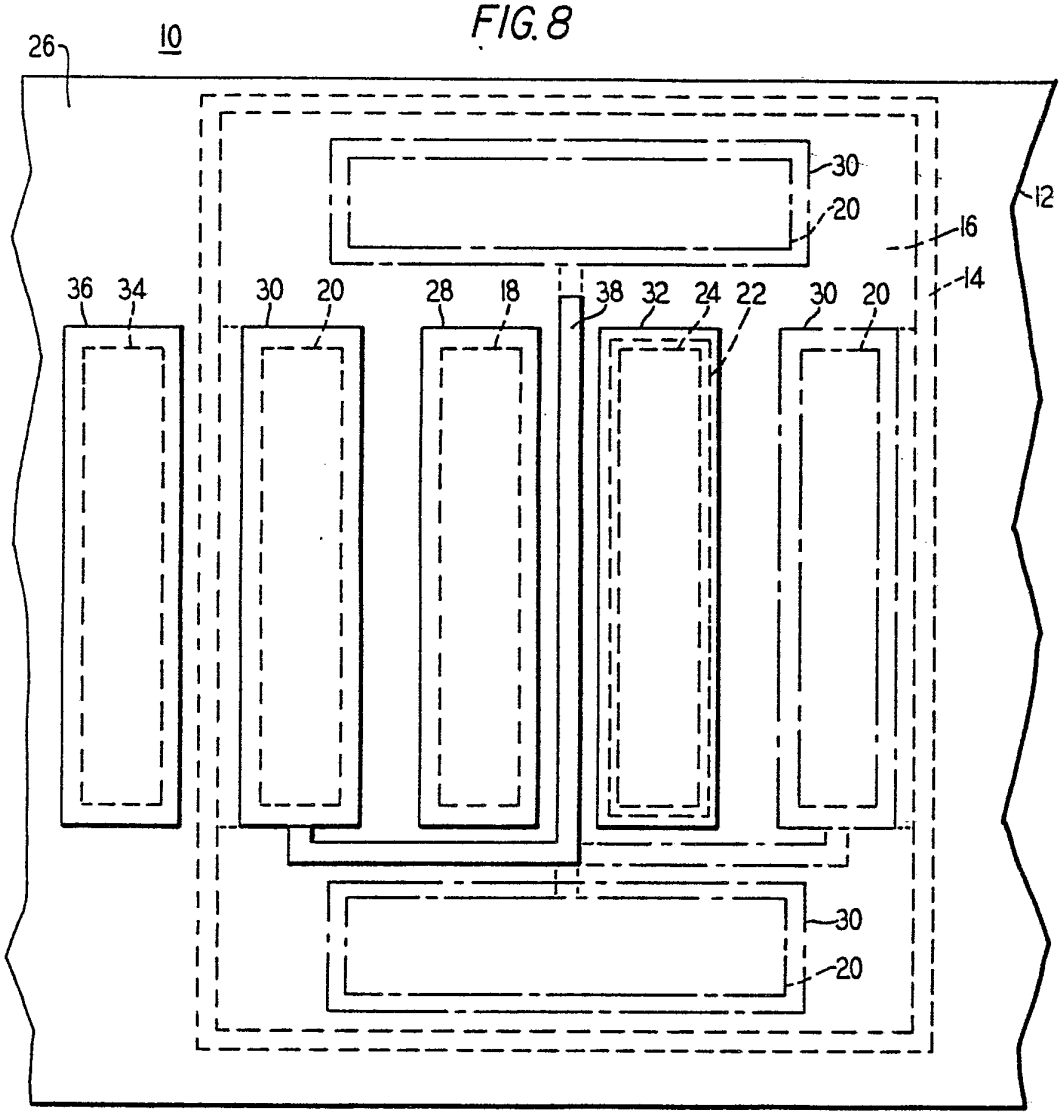


FIG. 8



INTERNATIONAL SEARCH REPORT

International Application No PCT/US79/01043

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

US CL 357/21, 22, 38, 39, 41, 45, 48 WO 80/01337

INT CL[3] H01L 29/74, 29/80, 29/747, 27/02, 27/10, 27/04

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	357/21, 22, 38, 39, 41, 45, 48

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3,657,616, Published 18 APRIL 1972, Mizushima et al	1-20
X P	US, A, 4,146,905, Published 27 MARCH 1979, Appels et al	1-20
X	US, A, 3,911,463, Published 7 OCTOBER 1975, Hull et al	1-20
X	US, A, 3,722,079, Published 27 MARCH 1973, Beasom	1-20
X	N, IEEE INTERNATIONAL SOLID STATE CIRCUITS CONF., Issued 17 FEBRUARY 1978, Scharf et al, A MOS-CONTROLLED TRIAC DEVICE	1-20
X	N, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-23, No. 3 Issued AUGUST 1976, Houston et al, A FIELD TERMINATED DIODE	1-20
X	N, INTERNATIONAL SWITCHING SYMPOSIUM, Issued 25 OCTOBER 1976, Kyoto, Japan, Tokunaga et al, DEVELOPMENT OF INTEGRATED SEMICONDUCTOR CROSSPOINT SWITCHES AND A FULLY ELECTRONIC SWITCHING SYSTEM	1-20

* Special categories of cited documents: [15]

"A" document defining the general state of the art

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"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
9 APRIL 1980	23 APR 1980
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	E. Wojciechowicz

Form PCT/ISA/210 (second sheet) (October 1977)