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GB 2061665 A
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GB 1251767
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(54) **Digitized video data recording and reproducing apparatus**

(57) A signal processing circuit divides a digitized video signal of each horizontal scan interval into a plurality of data blocks D_1 to D_8, and a signal distributing circuit distributes the data blocks D_1 to D_8 within each horizontal scan interval between rotary magnetic heads in a helical scan VTR. For each horizontal interval, heads GA, GB, GC, GD (Figure 8 not shown) simultaneously record blocks D_1, D_3, D_2, D_4 respectively then blocks D_5, D_7, D_6, D_8 respectively. The heads are stacked, together with an audio head AH, with a slight circumferential stagger and delay circuits may be used so that the ends of the tracks are effectively aligned in the track width direction or staggered in the track length direction each field being recorded as a set of four digital, video tracks and one digital audio track (Figures 9, 11, not shown). Each data block D_1 to D_8 includes a sync signal, track identification and address signals and block parity data (Figure 4H).

In the video recording circuits, Figure 2 (not shown), an interface (11) halves the data rate and multiplexes the data blocked to an AB channel and a CD channel. Each such channel has a time base compression circuit (12), to make room for error codes, an error correcting encoder (13), and a recording processor (14) which converts from 8 to 10 - bits per sample and feeds record amplifiers for two heads (GA and GB, or GC and GD).

In the audio recording circuits, (Figure 6 not shown), 16 analog signals are converted to digital form then multiplexed onto one audio recording channel which includes a time compressor (75), and an error correcting encoder (76).

On reproduction, an analyzer ANA indicates the number of data blocks having errors on a monitor 6, (Figures 1, 10 not shown).

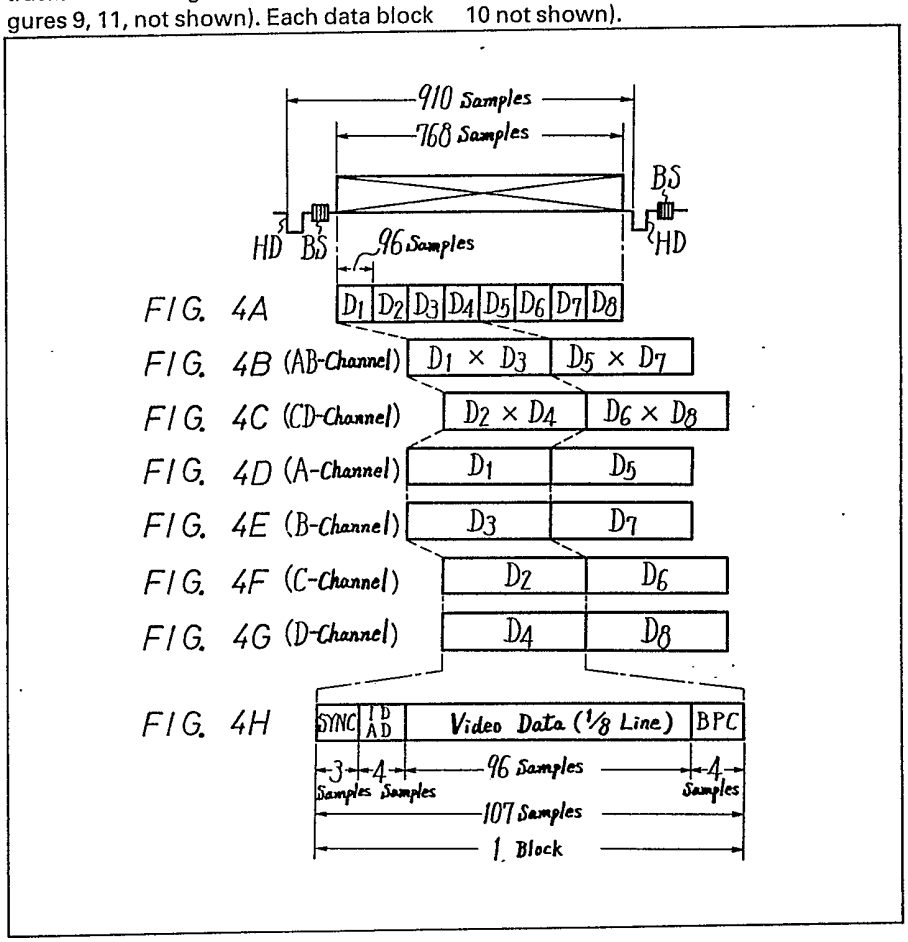

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FIG. 1

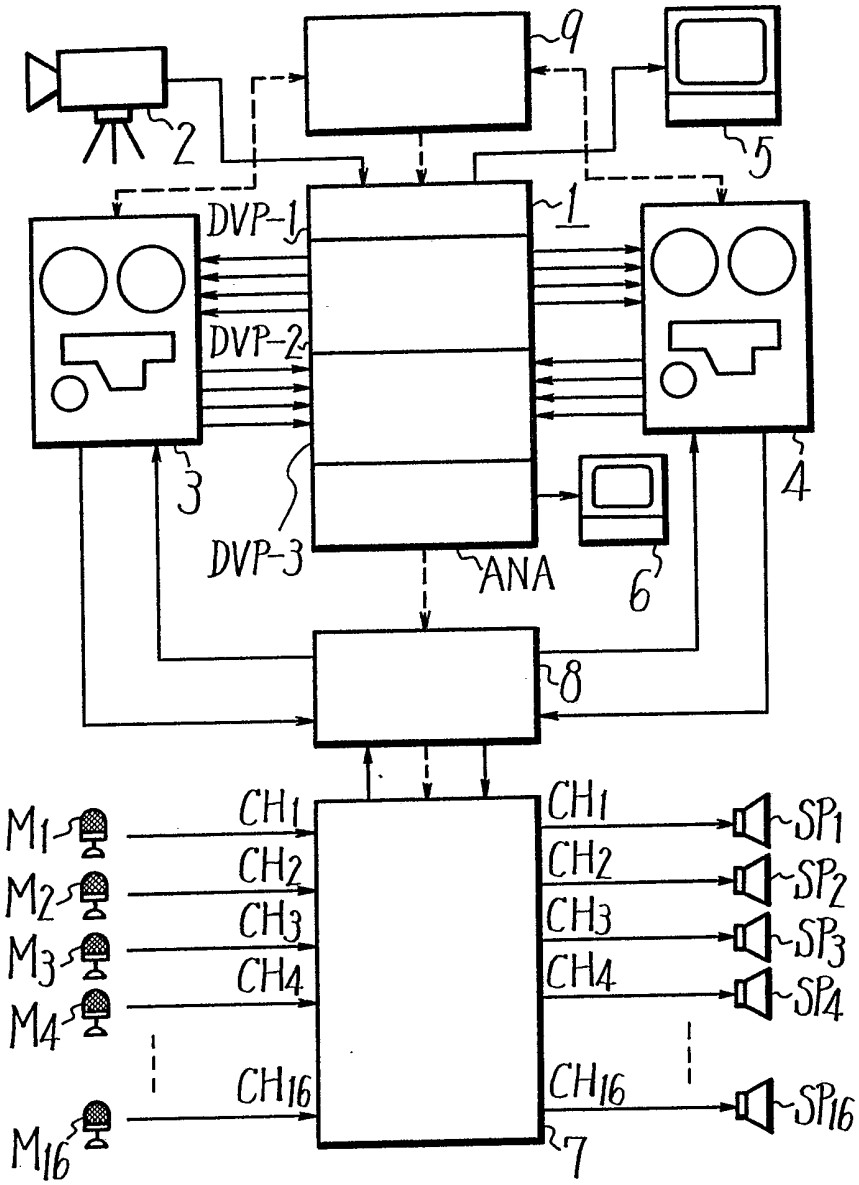

9
2
5
1
DVP-1
DVP-2
3
4
DVP-3
ANA
6
8
M1
M2
M3
M4
M16
CH1
CH2
CH3
CH4
CH16
CH1
CH2
CH3
CH4
CH16
SP1
SP2
SP3
SP4
SP16
7

FIG. 2

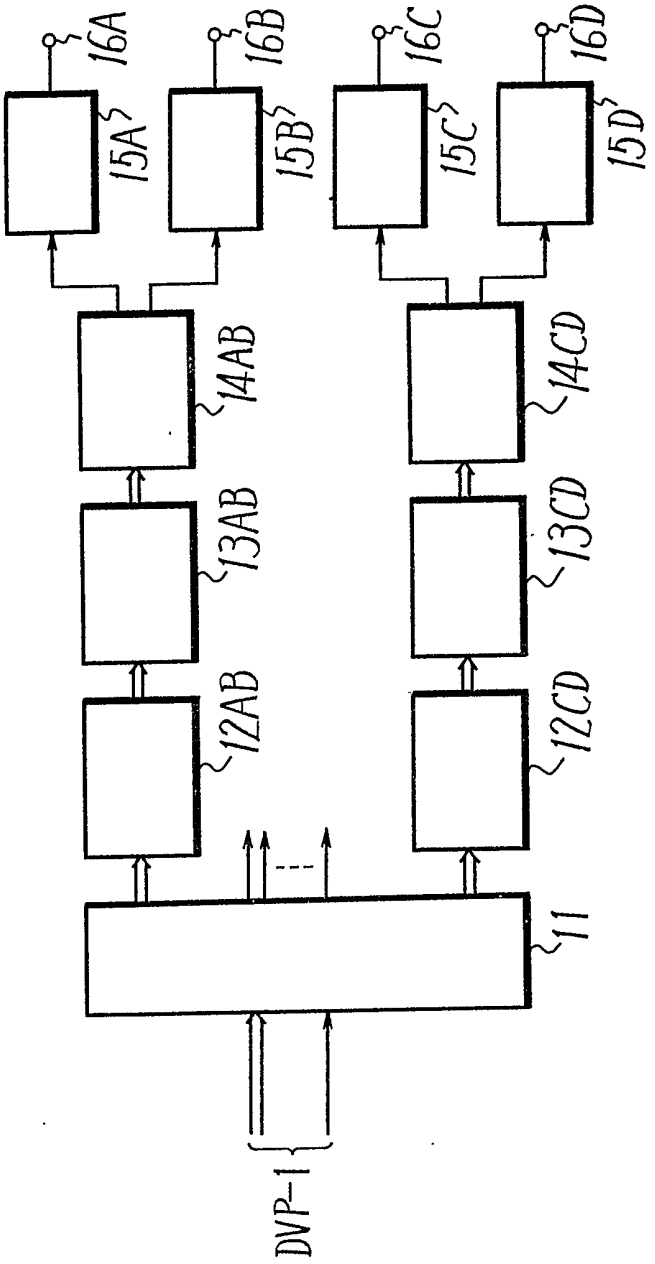
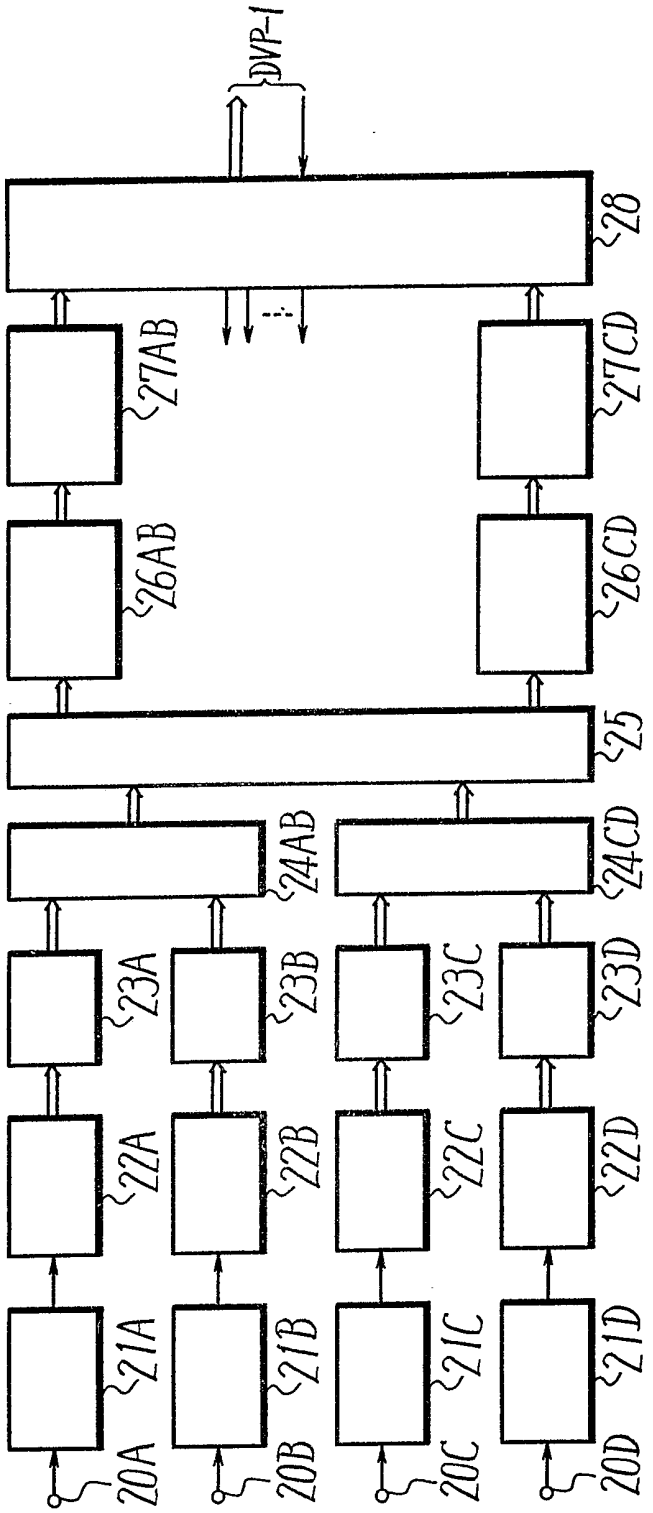

16A
16B
16C
16D
15A
15B
15C
15D
14AB
14CD
13AB
13CD
12AB
12CD
11
DVP-1

FIG. 3


DVP-1
28
27AB
27CD
26AB
26CD
25
24AB
24CD
23A
23B
23C
23D
22A
22B
22C
22D
21A
21B
21C
21D
20A
20B
20C
20D

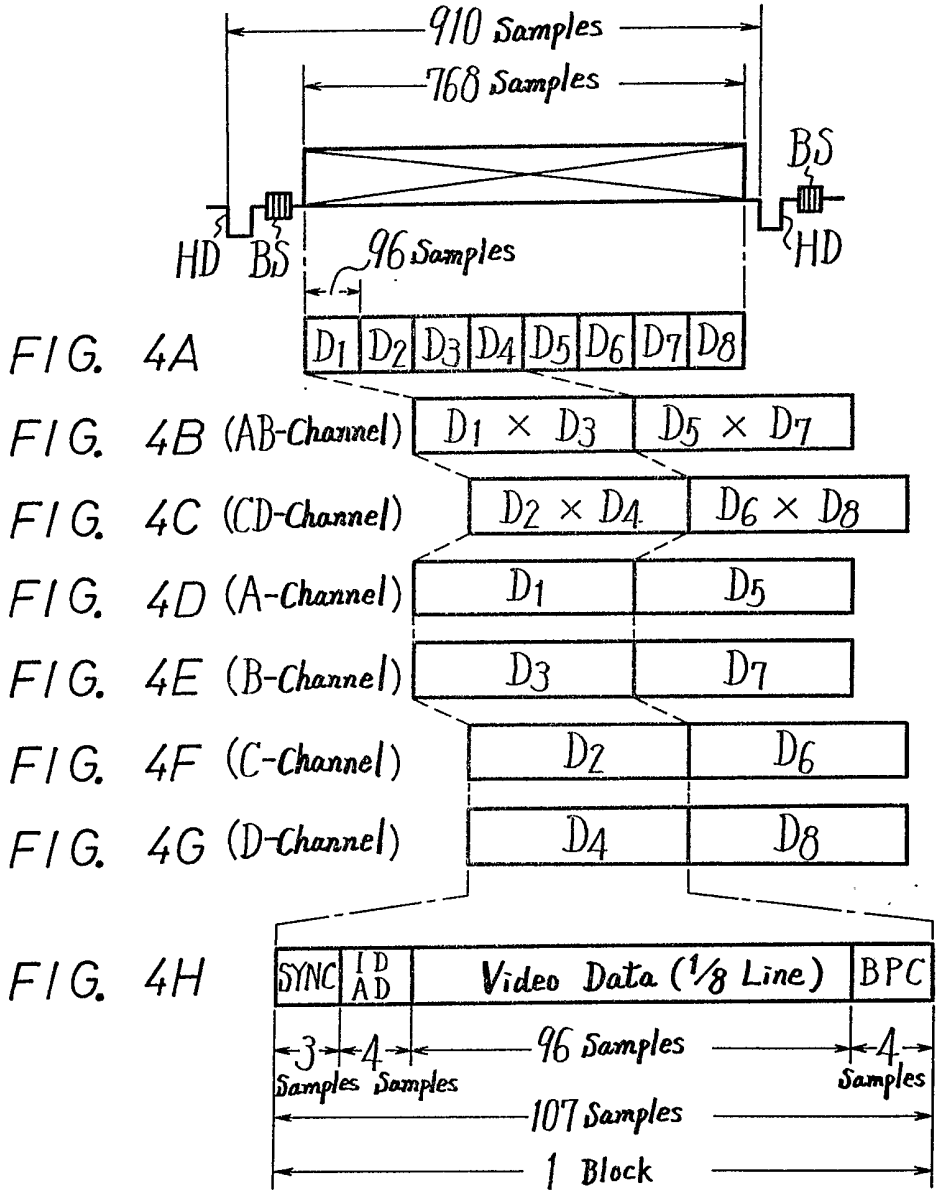


FIG. 4A

FIG. 4B (AB-Channel)

FIG. 4C (CD-Channel)

FIG. 4D (A-Channel)

FIG. 4E (B-Channel)

FIG. 4F (C-Channel)

FIG. 4G (D-Channel)

FIG. 4H

FIG. 5

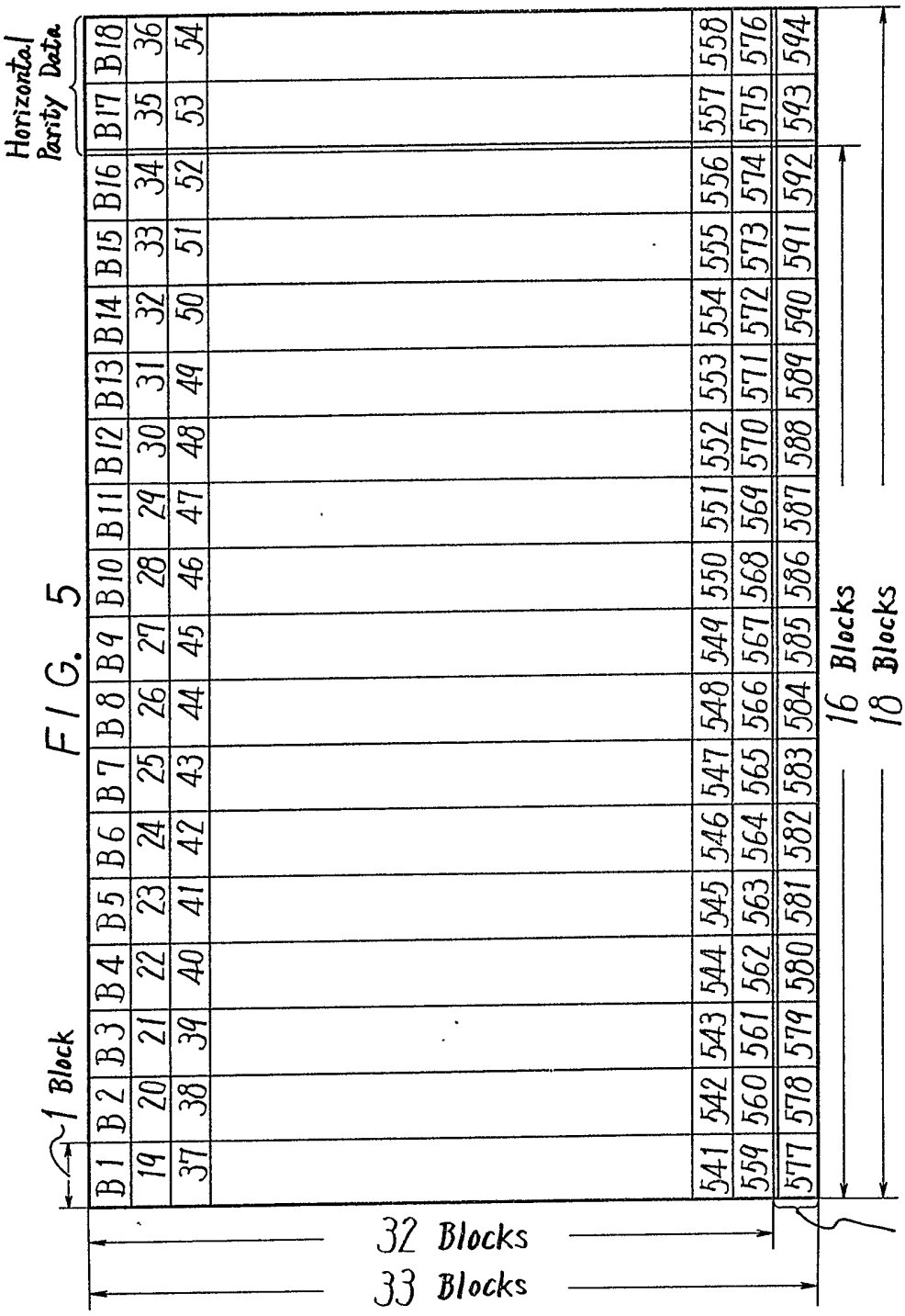

Horizontal Parity Data
1 Block
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18
19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54
541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558
559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576
577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594
32 Blocks
33 Blocks
16 Blocks
18 Blocks
Vertical Parity Data

FIG. 6

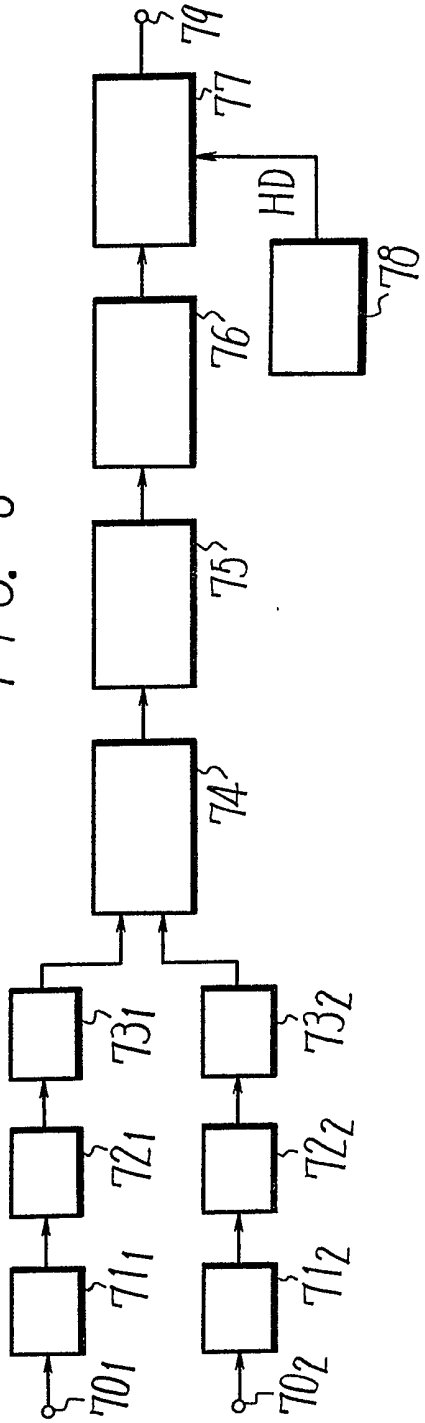

701
702
711
712
721
722
731
732
74
75
76
77
78
79
HD

FIG. 7

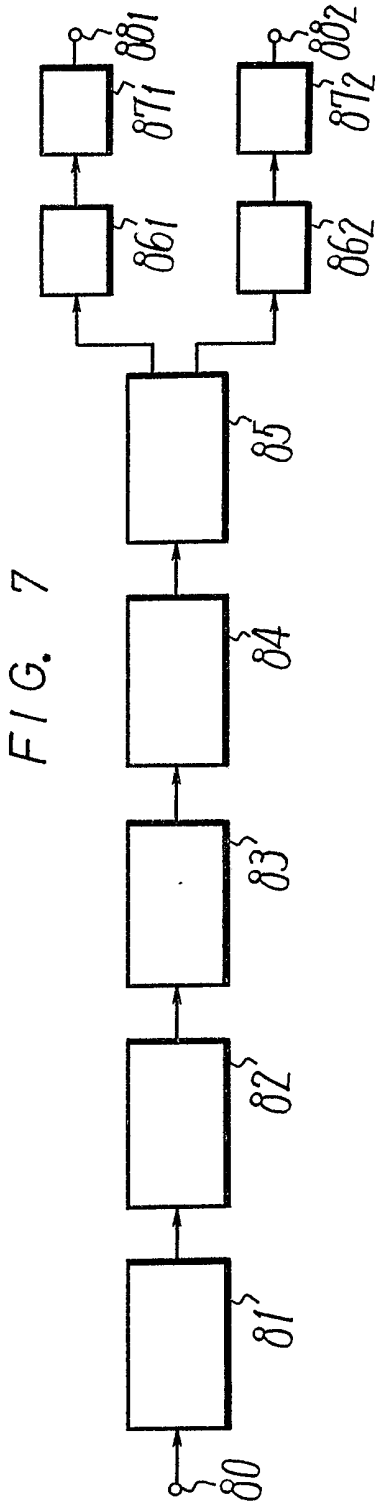

80
81
82
83
84
85
861
862
871
872
881
882

FIG. 8A

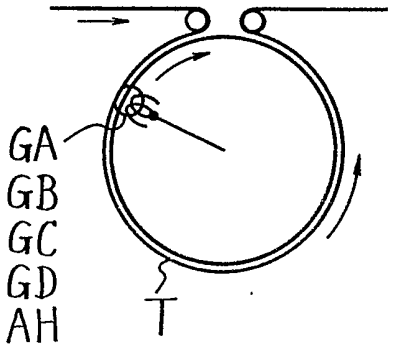


FIG. 8B

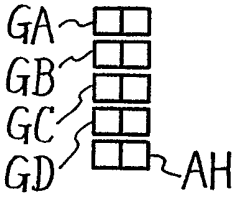


FIG. 9

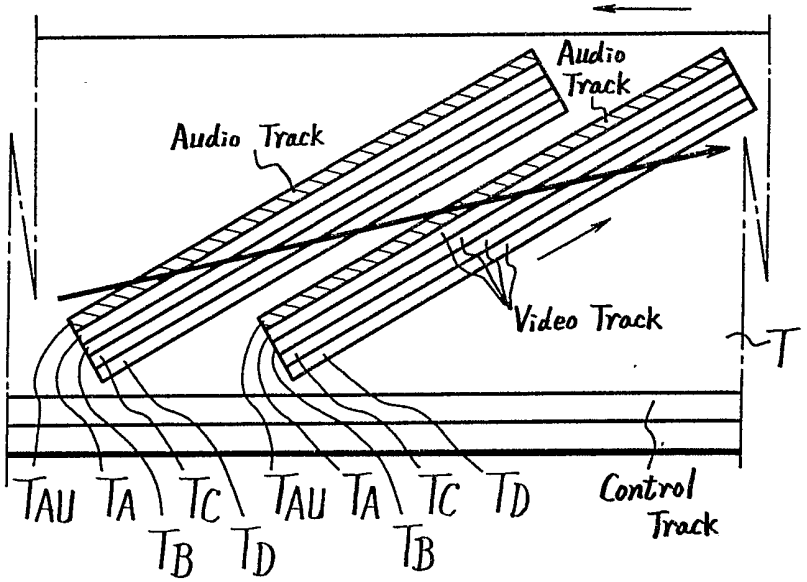


FIG. 10

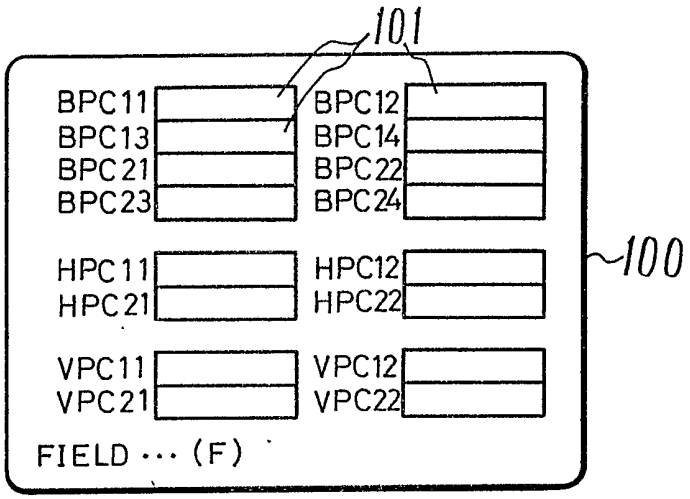
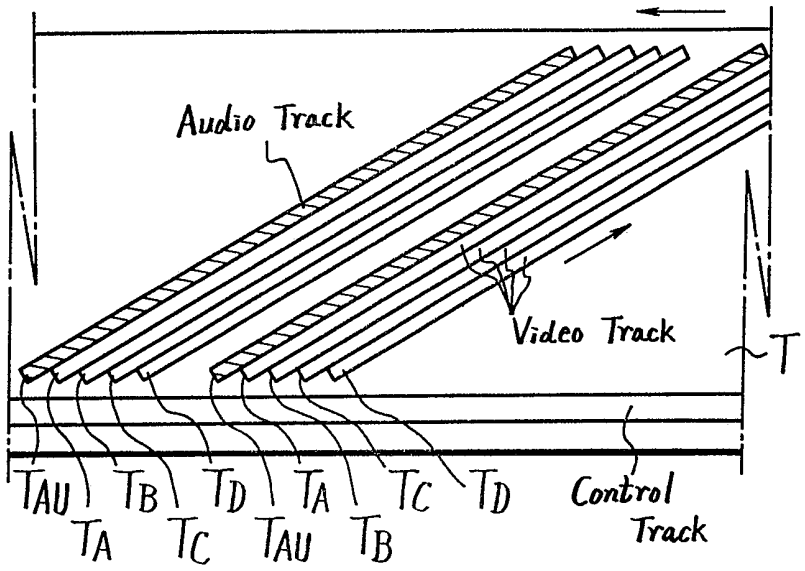

101
BPC11
BPC12
BPC13
BPC14
BPC21
BPC22
BPC23
BPC24
HPC11
HPC12
HPC21
HPC22
VPC11
VPC12
VPC21
VPC22
FIELD ··· (F)
100

FIG. 11


Audio Track
Video Track
T
TAU
TB
TD
TA
TC
TD
Control Track
TA
TC
TAU
TB

SPECIFICATION

Digitized video data recording and/or reproducing apparatuses

This invention relates to digitized video data recording and/or reproducing apparatuses.

A video signal has usually been frequency-modulated for recording on a video tape. More recently, digital video processing has become popular for studio equipment, such as video tape recorders (VTRs). When recording digital data for a video signal, digital data are divided into a plurality of data blocks each having a sync word, identification data, address data, and cyclic redundancy check (CRC) data in association with the video data.

Although the selection of the number of blocks, and the number of rotary magnetic heads employed for recording these blocks are very important to improve the recording-reproducing quality, and also to simplify the total system, these considerations have not up to now been well developed.

According to the present invention there is provided digitized video data recording and/or reproducing apparatus comprising:

a plurality of rotary magnetic heads provided in association with a tape guide drum on a periphery of which a magnetic tape is helically transported at a predetermined wrap angle;

signal processing means for dividing a digitized video signal of one horizontal scan interval into a plurality of data blocks; and

signal distributing means for assigning every even number of said data blocks within one horizontal scan interval to each of said rotary magnetic heads for recording.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a block diagram showing an embodiment of apparatus according to the invention;

Figure 2 is a block diagram showing an example of a digital processing circuit at the recording side of a digital video processor;

Figure 3 is a block diagram showing an example of a digital processing circuit at the reproducing side of a digital video processor;

Figures 4 and *5* are diagrams used to explain the signal format when a colour video signal is digitally recorded;

Figure 6 is a block diagram showing an example of a digital processing circuit at the recording side of a digital video processor;

Figure 7 is a block diagram showing an example of a digital processing circuit at the reproducing side of a digital video processor;

Figure 8 is a diagram used to explain an example of the rotary magnetic head assembly of a VTR;

Figure 9 is a format showing one example of a recording track pattern;

Figure 10 is a diagram showing an example of an error display; and

Figure 11 is a format showing another example of the recording track pattern.

Figure 1 is a block diagram of an embodiment of digitized video and audio data recording and/or reproducing apparatus, in which an editing function is also taken into consideration.

A digital video processor 1 comprises a first processor DVP-1 including an analog-to-digital (A-D) converter, a digital-to-analog (D-A) converter and a signal generator for generating various kinds of clock and timing signals, a second processor DVP-2 for processing a digitized video signal for recording, a third processor DVP-3 for processing reproduced digital video signals, and a data analizer ANA having an error display function.

Figure 1 also shows a television camera 2 and VTRs 3 and 4 which are somewhat different from an ordinary VTR in their head mechanism and the associated circuit portions thereof.

A monitor 5 displays the reproduced video signal, and a monitor 6 displays error conditions by way of the data analizer ANA. A digital audio processor 7 is made of a slightly modified pulse code modulation (PCM) processor in which an audio signal is converted to a PCM signal and then recorded and/or reproduced by a VTR.

An audio switcher 8 is used to couple the digital audio processor 7 to the VTRs 3 and 4. In this case, the number of channels of the audio signals is selected as 16 channels CH_1 to CH_{16} and pairs of microphones M_1 to M_{16} and loudspeakers SP_1 to SP_{16} at maximum are respectively able to be connected. Upon recording, the digital audio signal from the digital audio processor 7 is selectively supplied to the VTRs 3 and 4, while upon reproducing, the reproduced signal from the VTR 3 or 4 is supplied to the digital audio processor 7 through the audio switcher 8.

A remote control apparatus 9 produces remote control signals which can be utilized to control the digital video processor 1, the VTRs 3 and 4, and the digital audio processor 7 from a remote location.

Now, the recording and/or reproducing of the colour video signal and audio signal will be described in detail.

When the television camera 2 views an object (not shown), the colour video signal derived from the television camera 2 is supplied to the first video processor DVP-1 of the digital video processor 1, then sampled and digitized. In this case, one television line of the colour video signal, excluding the horizontal sync (synchronizing) pulse HD and burst signal BS portions is sampled as the effective region. The vertical

sync pulse and the equalizing pulse portions in the colour video signal of one field are not taken as an effective data, and the signal in that period is not recorded. However, since a test signal such as VIR, VIT or the like is inserted in the vertical fly-back period, the number of the total effective video lines is determined including the above lines. For example, in the case of the NTSC colour video signal, the number of the effective video lines in one television field period is selected as 256 lines starting from the 10th line in each field.

Further, in the embodiment of the invention, a sampling frequency f_{VS} of the colour video signal is 4 times the colour sub-carrier frequency f_{SC}. To this end, the horizontal sync signal HD and the burst signal BS extracted from the input colour video signal are fed to a signal generator which produces a clock pulse signal which is synchronized to the burst signal BS and has the frequency of $4f_{SC}$. A sampling pulse is generated based on this clock pulse signal.

The above effective portion of the colour video signal is sampled based on the above sampling pulse and A-D converted to be, for example, a parallel 8-bit digital signal.

In this case, the sampling frequency f_{VS} is $4f_{SC}$ and the colour sub-carrier frequency f_{SC} in the case of the NTSC colour video signal is expressed as follows:

$$f_{SC} = \frac{455}{2} f_H$$

where f_H is the horizontal frequency. Therefore, the number of samples included in one horizontal period is 910 samples. However, since it is not necessary to sample the signal in the horizontal blanking period as set forth above, the number of the effective video samples in one line becomes less than 910 samples and, for example, 768 samples.

The digital video signal thus provided is fed to the second video processor DVP-2 together with the clock pulse signal.

The second video processor DVP-2 is basically constructed, for example, as shown in Figure 2. In this example, the digital video signal and clock pulse signal from the processor DVP-1 is fed to a video interface (multiplexer) 11, where the digital video signal is processed in time-sharing manner as described later. Identification signals relating to the line, field, frame and track and various timing signals generated in the processor DVP-1 are supplied to predetermined circuits of the processor DVP-2 respectively.

As described above, the digital video signal is distributed to a plurality of channels and then recorded. In this embodiment, *n* rotary magnetic heads are provided in the VTRs 3 and 4 for the video signal, and when the digital video signal is distributed to *n* channels, the video signal data of one horizontal line are separated to $2n$ blocks and 2 blocks thereof are distributed to each channel in the case of this example. Further in this example, *n* is selected as 4. Thus, as shown in Figure 4A, the data of one television line are separated to the data of a former 1/2 line and the data of a latter 1/2 line and the data of the former 1/2 line and the data of the latter 1/2 line are respectively divided by 4 to provide 8 data groups, i.e. data groups D_1, D_2, ... D_8 each having 96 samples. Then, the former 4 data groups D_1, D_2, D_3, D_4 are distributed to the tracks of respective channels A, B, C, D and recorded, while the latter 4 data groups D_5, D_6, D_7, D_8 are distributed to the tracks of the respective channels A, B, C, D and recorded. That is, in this case, the data groups D_1 and D_5 are recorded on a track T_A of the channel A, and similarly the data groups D_3, D_7; D_2, D_6 and D_4, D_8 are respectively recorded on tracks T_B, T_C and T_D of the channels B, C, and D.

If the data which are divided into 4 channels are processed separately at respective channels, 4 signal processing systems are required, which makes the construction complicated and also the cost thereof high. Therefore, the A channel and the B channel, and the C channel and the D channel are respectively combined as two systems of AB channel and CD channel and then processed.

To this end, in the video interface 11 the data rate is halved and also at the AB channel side as shown in Figure 4B, the data groups D_1 and D_3 are so multiplexed and processed in time-sharing manner that the sample from the data group D_1 and the sample from the data group D_3 are combined alternatively and then the data groups D_5 and D_7 are so multiplexed and processed in time-sharing manner that the sample from the data group D_5 and the sample from the data group D_7 are combined alternatively. At the CD channel side, as shown in Figure 4C, the data groups D_2 and D_4 are multiplexed and processed in time-sharing manner and then the data groups D_6 and D_8 are multiplexed and processed in time-sharing manner.

The digital signal of the AB channel thus derived from the video interface 11 is fed to a time-base compressing circuit 12AB and the digital signal of the CD channel is fed to a time-base compressing circuit 12CD. Then, they are time-base-compressed at a predetermined ratio for making room for error correcting codes, and data format conversion for recording.

The time-compressed digital data of the video signals of both the AB and CD channels from the time-base compressing circuits 12AB and 12CD are respectively fed to error correcting encoders 13AB and 13CD and then to recording processors 14AB and 14CD. In the error correcting encoders 13AB and 13CD and the recording processors 14AB and 14CD, the video signal data which are multiplexed at every sample are respectively processed at every sample in time-sharing manner. In other words, the samples of the same data groups in the respective data groups D_1, D_2, ... D_8 are signal-processed within that sample unit and also the data rate thereof is again halved (rate down to $\frac{1}{4}$ of the original sample data). Namely, in view of the

signal process as shown in Figures 4D, 4E, 4F and 4G, the signal process is carried out with the respective channels A, B, C and D separately.

As described above, the video signal data are processed in time-sharing manner in the error correcting encoders 13AB and 13CD and the recording processors 14AB and 14CD and converted into signals with the formats shown in Figures 4H and Figure 5.

That is, in the above example, one block B is assigned to every data group D_1, D_2, .. D_8 (each has data of 96 samples) of $\frac{1}{8}$ line of the video signal. As shown in Figure 4H, this block B further includes a block sync signal SYNC of 3 samples (24 bits) and an identification signal ID and address signal AD of 4 samples (32 bits) and also a block parity data BPC of 4 samples (32 bits). In this case, the sync signal SYNC is used to extract the signals ID and AD, and the data and block parity data BPC upon reproduction.

The identification signal ID shows classifications of the channels A, B, C and D and the frame and field, and the address of the block B. The block parity data BPC is used to detect an error in the data upon reproduction and also to correct the error of the data within one block B.

Further, as to one field of every channel, the data are processed to have the following structure. That is, Figure 5 shows the data structure of one channel of the video signal data in one field, in which two of one block B are data from one line of the video signal ($\frac{1}{4}$ line). In this case, the numerals marked on the respective blocks B correspond to the above-mentioned address AD.

In case of the NTSC system colour video signal, if the number of the effective video lines is selected as 256 as set forth above, the number of blocks of one field in each channel is 512. Since, however, 16 blocks in the horizontal direction and 32 blocks in the vertical direction are arranged in a matrix with a block unit as shown in Figure 5, parity data in the horizontal (row) direction are added to the matrix of 16 × 32 at 17th and 18th columns, and parity data in the vertical (column) direction are added to the matrix at a 33rd row, so that there are in total 18 × 33 blocks.

Further, in this case, if it is assumed that the blocks B are from B_1 to B_{594} sequentially and with respect to the first row, the following modulo-2 additions are performed with the block unit at every other one block in the horizontal direction thereby to provide horizontal parity data B_{17} and B_{18} of the first row:

$$B_1 \oplus B_3 \oplus B_5 \oplus \ldots \oplus B_{15} = B_{17}$$

$$B_2 \oplus B_4 \oplus B_6 \oplus \ldots \oplus B_{16} = B_{18}$$

Similarly, horizontal parity data on the 2nd to 33rd rows are provided.

For the first column, the following modulo-2 additions are carried out with the block unit in the vertical direction to provide vertical parity data B_{577} of the first column:

$$B_1 \oplus B_{19} \oplus B_{37} \oplus \ldots \oplus B_{559} = B_{577}$$

Similarly, vertical parity data on the 2nd to 16th columns are provided.

These horizontal and vertical parity data and block parity data are used to enhance the data error correcting ability upon reproduction.

The signal processing to provide the above horizontal and vertical parity data and add them to the data is performed in the error correcting encoders 13AB and 13CD, while the signal processing to provide the sync signal SYNC, identification signal ID and address AD and add them to the data is performed in the recording processors 14AB and 14CD.

In the processors 14AB and 14CD, is carried out a block-encoding such that the number of bits per sample is converted from 8 bits to 10 bits. This block-encoding is a conversion such that 2^8 codes in 10 bits (2^{10}) are selected whose digital sum variation (DSV) is 0 or nearly 0 and the original code of 8 bits is corresponded to the selected code at 1:1 to provide the code of 10 bits. In other words, a conversion is carried out such that the DSV of the recording signal becomes 0 as nearly as possible and accordingly "0"s and "1"s appear substantially equally. Such block-encoding is carried out because *dc* components cannot be recovered upon reproduction by an ordinary magnetic head.

Thus block encoded digital signals of 10-bit words are further converted in the processors 14AB and 14CD from parallel signals to serial signals in sequence from the block B_1 to the block B_{594}. At the beginning and end of the digital signal of one field period of each channel, a pre-amble signal and a post-amble signal are added, respectively.

The serial digital signals are separated for each channel, supplied from the processors 14AB and 14CD and supplied through recording amplifiers 15A, 15B, 15C and 15D to output terminals 16A, 16B, 16C and 16D, respectively.

Analog audio signals collected by the microphones M_1 to M_{16} are fed to the digital audio processor 7. The recording-processing circuit of the digital audio processor 7 is shown in Figure 6. That is, if the audio signals of 2 channels are taken into consideration, the signals of the respective channels are supplied through input

terminals 70_1, 70_2 and low-pass filters 71_1, 71_2 to sampling hold circuits 72_1, 72_2, respectively. In this case, a sampling frequency f_{AS} of the audio signal is selected as 50.4/1.001 KHz. In the case of the NTSC colour video signal, in order to avoid the beat between the audio sub-carrier and colour sub-carrier, the frame frequency is selected higher than 30 Hz by 1/1000 Hz, and further when the audio signal is time-base compressed, the compressing ratio has to be determined to make the frequency of the sampling frequency, which is compressed, an integee times the horizontal frequency f_H. Therefore, the sampling frequency f_{AS} for the audio signal is selected as the compressing ratio becomes as noted above.

Now, the relation between the sampling frequency f_{VS} of the video signal and the sampling frequency f_{AS} of the audio signal will be explained.

$$f_{AS} = \frac{8}{7} \cdot \frac{14}{5} \cdot f_H$$

$$= \frac{8}{7} \cdot \frac{14}{5} \cdot \frac{2}{455} \cdot f_{SC}$$

$$= \frac{32}{2275} \cdot f_{SC} \quad \ldots\ldots\ldots (1)$$

$$f_{VS} = 4 \cdot f_{SC} \quad \ldots\ldots\ldots (2)$$

$$\therefore f_{AS} = \frac{8}{2275} \cdot f_{VS} \quad \ldots\ldots\ldots (3)$$

The data thus sampled are fed to A-D converters 73_1 and 73_2 respectively for converting into digital signals of 16 bits per one sample.

The serial digital signals from the A-D converters 73_1 and 73_2 are both fed to a multiplexer 74 and time-sharing-processed such that the data of the first channel and the data of the second channel appear alternatively at every one sample. The output data from the multiplexer 74 are then fed to a time compressing circuit 75 which includes a random access memory (RAM). The output data are therein interleaved data block by data block, and time-compressed for making room for error detection and error correction codes at a predetermined time compressing ratio and then fed to an error correcting encoder 76 for adding error detecting codes and error correcting codes to the time-compressed data stream.

The digital audio signal from the error correcting encoder 76 is fed to a video amplifier 77. A sync signal generating circuit 78 is provided, and the television sync signal and data sync signal therefrom are also fed to the video amplifier 77 in which the above sync signals are added to the audio data and then they are supplied to an output terminal 79.

The above description is given in the case of 2 channels, but in the case of 16 channels it is enough that the digital data of 16 channels of the audio signal are time-sharing-processed in the multiplexer 74.

If the digital signals of 4 channels are supplied to the VTRs 3 and 4 and the digital signals from the digital audio processor 7 are supplied through the audio switcher 8 to the VTR 3 or 4.

Each of the VTRs 3 and 4 has 4 rotary magnetic heads GA, GB, GC and GD and one rotary magnetic head AH as shown in Figures 8A and 8B. These 5 heads GA, GB, GC, GD and AH are located closely and sequentially displaced along the rotary axis approximately in line. They are rotated at the field frequency of 60 Hz in synchronism with the colour video signal. A magnetic tape T is helically wrapped around the rotary surface of the heads GA, GB, GC and GD in Ω-shape and also transported at a constant speed.

When, for example, the VTR 3 is in a recording mode, the digital video signals of the A , B , C and D channels are respectively recorded in the VTR 3 by the heads GA, GB, GC and GD on the tape T as 4 slant tracks T_A, T_B, T_C and T_D per every one field as shown in Figure 9. Also the digital audio signal is recorded on the tape T as a slant track T_{AU} by the head AH.

In this example, the track widths of the heads GA, GB, GC, GD and AH and the distance between adjacent ones thereof are so selected that a set of the tracks T_A, T_B, T_C, T_D and T_{AU} correspond to one video track with the SMPTE "C" format.

Now, it is taken into consideration that if the data rate of the audio signal is R_A, how many samples can be included in one field with 8-bit unit when it is converted into the digital data sample of the video signal.

At first, the data rate R_A of the audio signal is calculated.

One sample of the audio signal is 16 bits and the audio channels are 16 channels. Thus, if the redundancy of the error correcting code, sync signal etc. is taken as 100 %, the total data rate R_A is expressed as follows:

$$R_A = (16 \times 2) \times 16 \times f_{AS}$$
$$= \frac{4096}{2275} \cdot f_{VS}$$
$$= 25.779 \text{ M bit/s} \quad \ldots\ldots\ldots (4)$$

Accordingly, a sample number N_A of the digital audio signal inserted per one field becomes as follows:

$$N_A = R_A \times \frac{1}{8} \times \frac{1.001}{60}$$
$$= \frac{4096}{2275} \times 4 \times f_{SC} \times \frac{1}{8} \times \frac{1.001}{60}$$
$$= 53760 \quad \ldots\ldots\ldots (5)$$

Since the number of video samples in one line is 910 as set forth previously, when the audio data rate is converted into the data rate of the digital video signal, the number of audio samples to be interposed in one television field is expressed as follows:

$$\frac{53760}{910} = 59.0769 \text{ (lines)} \quad \ldots\ldots\ldots (6)$$

That is, about 60 lines are necessary.

Accordingly, since the number of effective video lines is 256, the audio signal data is about 1/4 of the video signal data. Hence, the occupying ratio of the audio signal data in the total data of the video and audio signals is about 20 %.

Accordingly, one audio track is sufficient for four video tracks per one field.

In practice, it is difficult to arrange 5 heads to be precisely in in-line relation and the effect of leakage fluxes from adjacent heads cannot be negligible, so that the 5 heads GA, GB, GC, GD and AH are sequentially off-set in the rotary direction. In this case, the record starting positions of the respective tracks T_A, T_B, T_C, T_D and T_{AU} are not theoretically aligned as shown in Figure 9. However, if the digital signals of 4 channels or A to D channels and the digital audio signal are respectively given with relative delays and then they are supplied to the heads GA, GB, GC, GD and AH upon recording, the track pattern on the tape T can be formed similar to those formed by the 5 heads arranged in-line shown in Figure 9.

As described above, the digitized colour video signal and associated digitized audio signal can be recorded in digital form.

Now, the reproduction of the digital signal recorded as above will be explained.

When the VTR 3 is changed to a reproducing mode, the digital data of the respective channels are reproduced substantially at the same time by the heads GA, GB, GC and GD from the tracks T_A, T_B, T_C and T_D and substantially at the same time the digital audio signal is also reproduced by the head AH from the track T_{AU}. In this case, if the heads GA, GB, GC, GD and AH are sequentially off-set in the rotating direction as set forth above, the digital signals of the respective track are reproduced in sequentially delayed state. But these delays can easily be corrected by using, for example, a buffer memory.

The reproduced digital video signal is fed to the processor DVP-3 of the digital video processor 1 and the reproduced digital audio signal is fed through the audio switcher 8 to the digital audio processor 7.

At first, the reproduction of the digital video signal will be described. The video processor DVP-3 is constructed as shown in Figure 3. That is, the digital signals of 4 channels are respectively supplied to its input terminals 20A, 20B, 20C and 20D and then supplied through reproducing amplifiers 21A, 21B, 21C and 21D to reproducing processors 22A, 22B, 22C and 22D in which they are respectively converted from serial to parallel signals and also block-decoded from the 10-bit code to the original 8-bit code. Also, a clock signal is generated by a phase locked loop (PLL) based on the reproduced digital signal.

The parallel 8-bit digital signals are respectively fed to time-base correctors (TBCs) 23A, 23B, 23C and 23D for removing their time-base fluctuation components. As well known, the TBCs 23A, 23B, 23C and 23D each include a digital memory, and the block sync signal SYNC is used to detect the start of the following data signal, the writing operation to the memory is carried out based on the clock from the processors 22A, 22B, 22C and 22D. The reading operation from the digital memory is performed by the clock provided based on the reference sync, whereby the time-base fluctuation component is removed.

The signals from the TBCs 23A and 23B are both fed to a multiplexer 24AB, and the signals from the TBCs

23C and 23D are both fed to a multiplexer 24CD. Then, in the multiplexer 24AB, digital signals of the A channel and the B channel are processed in time-sharing manner to alternate sample by sample and, in the multiplexer 24CD, digital signals of the C channel and the D channel are also processed in time-sharing manner to alternate sample by sample.

The digital data from the multiplexers 24AB and 24CD are each supplied through an interchanger 25 to error correcting decoders 26AB and 26CD. In this interchanger 25, the respective channels are identified by the track identification signals among the identification signals added to the respective blocks, and the block data are distributed to the corresponding channels. In this interchanger 25, the process is of course carried out in time-sharing manner.

The interchanger 25 operates effectively, especially in a special reproducing mode. That is, upon a normal reproducing mode where the position of the record track on the magnetic tape and the running trace of the rotary head thereon are coincident, the 4 rotary heads reproduce the recorded signals only from the corresponding tracks. While, in a special reproducing mode such as a high speed reproducing mode where the running speed of the magnetic tape is selected as several tens of times that of the normal reproducing speed, the rotary heads scan across a plurality of the tracks as shown in Figure 9 by an arrow. Therefore, the respective heads GA, GB, GC and GD each reproduce a signal in which the signals from the A , B , C and D channels are mixed.

In the above case, the interchanger 25 discriminates the channel identification based upon the track identification signal and the reproduced signals from the tracks T_A and T_B are both fed to the decoder 26AB and the AB channel and the reproduced signals from the tracks T_C and T_D are both fed to the decoder 26CD for the CD channel.

The decoders 26AB and 26CD each include a field memory having a capacity to memorize the data of one channel of one field. Thus, the data of the A and B channels and the data of the C and D channels are respectively processed in the decoders 26AB and 26CD in time-sharing manner as follows. That is, the data are written in the field memory at every block B in response to the address signal AD and simultaneously the error of the data is corrected by the block parity data and horizontal and vertical parity data. As to the error correction, the error within the block unit is first corrected by the block parity data, then the error correction by the horizontal parity data is achieved, and finally the error correction by the vertical parity data is achieved.

Thus error corrected data are respectively supplied to time-base expanding circuits 27AB and 27CD, in which the data are respectively time-expanded at every channel and recovered to be the original signal format.

The video signal data from the time-base expanding circuits 27AB and 27CD are both fed to a video interface 28, and converted into the original single channel digital data. The data are then fed to the first processor DVP-1. In the video processor DVP-1, the digital signal is D-A converted, and further added with the sync pulse and colour burst signal to be the original colour video signal, and then fed to, for example, the monitor television receiver 5. In this case, the various timing pulses generated based upon the reference clock pulse derived from the signal generator in the processor DVP-1 are also respectively supplied through the video interface 28 to respective circuits of the reproducing processor circuits.

In the above reproducing system, the data process from the heads GA, GB, GC and GD to the write-in side of the TBCs 23A, 23B, 23C and 23D uses the clock pulse extracted from the reproduced data, but the data process from the read-out side of the TBCs 23A, 23B, 23C and 23D to the output terminals uses the clock pulse derived from the signal generator in the processor DVP-1.

The reproduced digital audio signal, supplied to the digital audio processor 7 by way of the audio switcher 8 is reproduced as follows. That is, the reproducing processor circuit of the digital audio processor 7 is constructed, for example, as shown in Figure 7. The reproduced signal fed through an input terminal 80 is supplied to a data extracting circuit 81 in which the television sync and data sync signals and the data are extracted based on the clock signal generated therein.

The data thus extracted are fed to a time-base expanding circuit 82, where the audio data are de-interleaved to be of the original code arrangement having the original time-base. The digital signal thus processed is then fed to an error correcting decoder 83, where the errors thereof are corrected based on the error detecting code and the error correcting code.

When the error of the data cannot be corrected at the error correcting decoder 83, the digital data signal is fed to an error concealing circuit 84 of the next stage in which the remaining error is concealed by mean value interpolation using the mean value of the words before and after the erroneous word, or pre-value hold interpolation.

The error corrected and concealed digital signal is fed to a de-multiplexer 85 in which the signal is distributed to the original first and second channel signals. The first channel signal is fed to a D-A converter 86_1 and converted into the analog signal which is supplied through a low-pass filter 87_1 to an output terminal 88_1, while the second channel signal is fed to a D-A converter 86_2, converted into an analog signal and supplied through a low-pass filter 87_2 to an output terminal 88_2.

The above description is given for the case of 2 channels, but the above reproducing system can be applied to the case of 16 channels with the same processing except that the digital signal is distributed to the signals of 16 channels by the de-multiplexer 85.

The analog audio signals of the respective channels thus obtained from the digital audio processor 7 are

respectively supplied to the loudspeakers SP_1, SP_2 ... SP_{16}. In the above manner, the digital video and audio signals can be reproduced.

Upon the reproduction, the number of blocks having errors is indicated on the monitor 6 by the analyzer ANA in the digital video processor 1.

Figure 10 illustrates the display format of the monitor receiver 6 on which, by way of example, the number of blocks having errors is indicated. In the figure, reference numeral 100 designate a picture screen of the monitor receiver 6 and within each of the frames 101 each surrounded by a square, for example, 10 figures in decimal number can be displayed to display the number of erroneous blocks. The letters marked at the left side of each of the square frames 101 are indices which show the display status. That is, the followings are respectively displayed in the frames.

(i) The letters BPC 11, BPC12, BPC21 and BPC22 represent the numbers of erroneous blocks which will appear in from the first channel to the fourth channel.

(ii) The letters BPC13, BPC14, BPC23 and BPC24 represent the numbers of erroneous blocks of the respective channel which cannot be corrected by the block parity data.

(iii) The letters HPC11, HPC12, HPC21 and HPC22 represent the numbers of erroneous blocks after the error is corrected by the horizontal parity data.

(iv) The letters VPC11, VPC12, VPC21 and VPC22 represent the numbers of erroneous blocks after the error is corrected by the vertical parity data.

In Figure 10, the letters FIELD ... (F) appeared on the lower portion of the picture screen 100 represent that the displayed number of erroneous blocks is obtained over F fields. For example, if "FIELD ... (60)" is displayed, it represents that the number of blocks displayed is obtained from data of 60 fields.

When the editing operation is required between the VTRs 3 and 4, the reproduced digital from the VTR 3 through the reproducing processor DVP-3 of the digital video processor 1 are fed directly to the recording processor DVP-2 and the output signal therefrom is fed, for example, to the VTR 4 and recorded therein.

In the digital audio processor 7, the output from the error concealing circuit 84 of the reproducing system is fed to the time-base compressing circuit 75 of the recording system, and the output derived at the output terminal 79 is supplied to the VTR 4.

A tracking servo for an ordinary VTR is sufficient for the VTRs 3 and 4 when they are in the recording and reproducing modes.

As described above, the video signal data of one television line are divided into a plurality of blocks whose number is twice the number of rotary magnetic heads for recording the video signal, and two blocks of the plurality of video signal data blocks are distributed to the respective heads, i.e. channels, and recorded thereby. Therefore, the following effect can be achieved. That is, if the dividing number of the data of one line is selected the same as the number of rotary magnetic heads for the video signal, the unit block for error correcting becomes too large for error correction and hence the error correction becomes poor. While, if the above dividing number is selected more than three times the number of rotary magnetic heads, the redundancy becomes too much.

Contrary to the above, with the embodiment, the above-mentioned defects are avoided, and good error correction and acceptable redundancy are achieved.

Moreover, with the embodiment, when the video signal data are distributed to the channels, the data of one line are roughly divided into two blocks, each of the divided (1/2) data is divided into blocks whose number corresponds to a plurality of channels and thus divided blocks are respectively distributed to the channels in sequence. Therefore, when the data of one field are distributed to the channels and processed, a delaying buffer memory of a small capacity which is used to make the data of the respective channels in time is sufficient.

Further, in the embodiment, since two channels in four channels are signal-processed in time-sharing manner by the digital processors DVP-2 and DVP-3 recording and/or reproducing the video signal, the circuit construction can be much simplified and made compact in size and inexpensive.

A separate track is formed for the audio signal so that upon editing it is easy for the video signal and the audio signal to be recorded and inserted independently.

In the illustrated embodiment, although the signals fed to five rotary heads are given with relative delays to form the track pattern similar to that formed by the rotary heads located in-line, it is possible for the relative delays to the signals to be varied to form a track pattern which effectively utilizes the width direction of the tape T as shown in Figure 11.

CLAIMS

1. Digitized video data recording and/or reproducing apparatus comprising:

a plurality of rotary magnetic heads provided in association with a tape guide drum on a periphery of which a magnetic tape is helically transported at a predetermined wrap angle;

signal processing means for dividing a digitized video signal of one horizontal scan interval into a plurality of data blocks; and

signal distributing means for assigning every even number of said data blocks within one horizontal scan interval to each of said rotary magnetic heads for recording.

2. Apparatus according to claim 1 wherein said each block has identification data and parity data for

recovering the original sequence and condition of said digitized video signal.

3. Apparatus according to claim 2 further comprising at least one rotary magnetic head for recording a digitized audio data associated with said digitized video data on a track parallel to a group of tracks for said digitized video data.

4. Apparatus according to claim 1 wherein said plurality of rotary magnetic heads are positioned close together.

5. Apparatus according to claim 1 wherein said digitized video signal is a digitized composite colour video signal quantized by a clock signal having a frequency of four times the colour sub-carrier.

6. Digitized video data recording and/or reproducing apparatus substantially as hereinbefore described with reference to the accompanying drawings.

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