An apparatus for processing a transport stream is provided. The apparatus includes a detector which detects data bits in a stream, an encoder which encodes the data bits detected by the detector and generates two encoding values for each data bit, and a stream constructor which constructs a transport stream using the encoding values generated by the encoder. Accordingly, it is possible to encode the data bits into a transport stream having a coding rate of \( \frac{1}{3} \).

**Diagram**: Start -> Receive Stream Coded at Coding Rate of 1/3 -> Detect Data Bits and Encoding Values -> Perform Decoding -> End
[Fig. 7]

710 RECEIVER → 720 DETECTOR → 730 DECODER

[Fig. 8]

START

S810 RECEIVE STREAM CODED AT CODING RATE OF 1/3

S820 DETECT DATA BITS AND ENCODING VALUES

S830 PERFORM DECODING

END
TRANSMISSION AND RECEPTION STREAM PROCESSING DEVICES FOR PROCESSING STREAM CODED WITH CODING RATE OF 1/3, AND METHODS THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a National Stage of International Application No. PCT/KR2007/002952 filed Jun. 18, 2007 and claims benefit of U.S. Provisional Application No. 60/814,070 filed on Jun. 16, 2006, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention
[0003] Devices and methods consistent with the present invention relate to processing transmitted and received streams, and more particularly, to processing transmission and reception streams, in which streams coded at a coding rate of 1/3 are transmitted or received and the transmitted or received streams are processed.

[0004] 2. Description of the Related Art
[0005] With the development of electronic and communication technologies, digital technologies have been introduced into the field of broadcasting system, and diverse standards for digital broadcasting have been published. Specifically, examples of such standards are U.S.-oriented Advanced Television Systems Committee (ATSC) Vertical Side Band (VSB) standard, and European-oriented Digital Video Broadcasting for Terrestrial Television (DVB-T) system. These two standards vary from each other in many ways, such as ways of audio compression, channel bands, number of carrier waves, etc.

[0006] The U.S.-oriented digital broadcasting (8-VSB) system defines that a VSB data frame includes two fields, and one field includes one field sync segment, which is the first segment, and 312 other data segments. Also, one segment in the VSB data frame corresponds to one MPEG-2 packet, and is composed of a segment sync signal of four symbols and 828 data symbols.

[0007] The U.S.-oriented digital broadcasting system conforms to the ATSC DTV standard. Recently, attempts have been made to generate and transmit/receive a multi-stream by adding robust-processed turbo coding data to normal data of the conventional ATSC VSB system.

[0008] In this situation, the turbo coding data transmitted together with the normal data may be data, which is coded at a coding rate different from the normal data to have robustness different from the normal data. Accordingly, various types of data may be transmitted together in a single frame, and thus broadcasts may be appropriately provided to various types of digital broadcasting apparatuses.

[0009] In order to generate such various types of data, various coding rates need to be applied. However, since there is no configuration to code and transmit a stream at a coding rate of 1/2 in the conventional art, it is difficult to generate various types of data.

SUMMARY OF THE INVENTION

[0010] An aspect of the present invention is to provide transmission/reception processing devices and methods thereof which can process various types of data by transmitting or receiving a stream coded at a coding rate of 1/3.

[0011] According to an aspect of the present invention, there is provided a transmission stream processing device comprising a detector to detect data bits from a stream; an encoder to encode the detected data bits and generate two encoding values for each data bit; and a stream constructor to construct a transmission stream with a coding rate of 1/3 using the generated encoding values.

[0012] The encoder may comprise first, second and third shift registers which are connected in series to perform shifting operations complementary to each other; a bit output line to output a data bit value without alteration if the data bit in the stream is input; a first adder to sum the data bit value output from the bit output line, a value prestored in the first shift register and a value prestored in the third shift register, and to output the sum of the values to the third shift register; a second adder to sum the data bit value output from the bit output line, a value prestored in the second shift register and a value prestored in the third shift register, and to output the sum of the values as a first encoding value for the data bit value; and a third adder to sum the data bit value output from the bit output line and the value prestored in the second shift register, and to output the sum of the values as a second encoding value for the data bit value.

[0013] Accordingly, the stream constructor may sequentially arrange the data bit value, first encoding value and second encoding value which are output from the encoder, to construct the transmission stream.

[0014] The device may further comprise a duplicator to receive the stream and generate place-holders at one side of each of the data bits in the stream.

[0015] In this situation, the encoder may comprise first, second and third shift registers which are connected in series to perform shifting operations complementary to each other; a first adder to sum the data bit value, a value prestored in the first shift register and a value prestored in the third shift register, and to output the sum of the values to the third shift register if the data bit in the stream is input; a second adder to sum the data bit value, a value prestored in the second shift register and a value prestored in the third shift register, and to output the sum of the values as a first encoding value for the data bit value; and a third adder to sum the data bit value and the value prestored in the second shift register, and to output the sum of the values as a second encoding value for the data bit value.

[0016] The stream constructor may construct the transmission stream by inserting the first and second encoding values output for each data bit in the place-holders.

[0017] According to an aspect of the present invention, there is provided a transmission stream processing method comprising detecting data bits from a stream; encoding the detected data bits to generate two encoding values for each data bit; and constructing a transmission stream with a coding rate of 1/3 using the encoding values.

[0018] The encoding may comprise encoding each of the data bits using an encoder comprising first, second and third shift registers, which are connected in series to perform shifting operations complementary to each other, and a plurality of adders, and outputting data bit values and the two encoding values for each data bit.

[0019] The constructing may comprise sequentially arranging the data bit value, first encoding value and second encoding value which are output from the encoder, to construct the transmission stream.
The method may further comprise receiving the stream and generating placeholders on one side of each of the data bits in the stream. The detecting may comprise detecting the data bits from the stream having the place-holders.

The encoding may comprise encoding each of the data bits using an encoder comprising first, second and third shift registers, which are connected in series to perform shifting operations complementary to each other, and a plurality of adders, and outputs two encoding values for each data bit.

The constructing may comprise constructing the transmission stream by inserting the two encoding values output from the encoder into the place-holders.

According to an aspect of the present invention, there is provided a reception stream processing device comprising a receiver to receive a stream coded at a coding rate of 1/2; a detector to detect data bits and encoding values in the stream; and a decoder to perform decoding using the detected data bits and encoding values to retrieve data from the stream.

According to another aspect of the present invention, there is provided a reception stream processing method comprising receiving a stream coded at a coding rate of 1/2; detecting data bits and encoding values in the stream; and performing decoding using the detected data bits and encoding values to retrieve data from the stream.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and/or other aspects of the invention will become and more readily appreciated as the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a block diagram showing a configuration of a transmission stream processing device according to an exemplary embodiment of the present invention;

FIG. 2 is a circuit diagram showing a configuration of an encoder which is applied to the transmission stream processing device of FIG. 1 according to an exemplary embodiment of the present invention;

FIG. 3 is an exemplary diagram explaining a stream processing method in the transmission stream processing device of FIG. 1 according to an exemplary embodiment of the present invention;

FIG. 4 is a block diagram showing a configuration of a transmission stream processing device according to another exemplary embodiment of the present invention;

FIG. 5 is a circuit diagram showing a configuration of an encoder which is applied to the transmission stream processing device of FIG. 4 according to an exemplary embodiment of the present invention;

FIG. 6 is an exemplary view explaining a stream processing method in the transmission stream processing device of FIG. 4 according to an exemplary embodiment of the present invention;

FIG. 7 is a block diagram showing a configuration of a reception stream processing device according to an exemplary embodiment of the present invention; and

FIG. 8 is a flowchart explaining a reception stream processing method according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Reference will now be made in detail to the exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The exemplary embodiments are described below in order to explain the present invention by referring to the figures.

FIG. 1 is a block diagram showing a configuration of a transmission stream processing device according to an exemplary embodiment of the present invention. The transmission stream processing device of FIG. 1 comprises a detector 110, an encoder 120 and a stream constructor 130.

The detector 110 detects data bits from a stream to be transmitted, and outputs the detected data bits to the encoder 120. The detector 110 may detect data bits from the stream in reverse order, and output the detected data bits to the encoder 120. For example, if data bits D0, D1, D2, D3, D4, D5, D6 and D7 of the stream are sequentially input in the stream, the detector 110 may detect the data bits from the stream in the order of D7, D6, D5, D4, D3, D2, D1 and D0 and output the detected data bits to the encoder 120 in the order detected.

The encoder 120 encodes the detected data bits and generates two encoding values for each data bit. The encoder may output each data bit together with the encoding values.

The stream constructor 130 constructs a stream using the generated encoding values output by the encoder 120. As a result, a stream coded with a coding rate of 1/2 may be generated. In other words, single byte data is coded to obtain a stream of three bytes.

FIG. 2 is a circuit diagram showing a detailed configuration of the encoder 120 which is applied to the transmission stream processing device of FIG. 1 according to an exemplary embodiment of the present invention. In FIG. 2, the encoder 120 comprises a bit output line 121, a plurality of shift registers S0, S1 and S2, and a plurality of adders 122, 123 and 124.

The bit output line 121 is a line which sequentially receives the data bits detected by the detector 110 and outputs the received data bits without alteration. The bit output line 121 is connected to the adders 122, 123 and 124, so that the received data bits can be sent by the bit output line 121 to the adders 122, 123 and 124.

The plurality of shift registers S0, S1 and S2 are connected in series to perform shifting operations complementary to each other. Specifically, if data is input to the third shift register S2, a value prestored in the third shift register S2 may be shifted to the second shift register S1 and stored therein, and a value prestored in the second shift register S1 may be shifted to the first shift register S0 and stored therein complementarily to the above shifting operation.

The first adder 122 sums the data bit value output from the bit output line 121, the value prestored in the first shift register S0 and the value prestored in the third shift register S2, and outputs the sum of the values to the third shift register S2.

The second adder 123 sums the data bit value output from the bit output line 121, the value prestored in the second shift register S1 and the value prestored in the third shift register S2, and outputs the sum of the values as a first encoding value Z for data bit value D.

The third adder 124 sums the data bit value output from the bit output line 121 and the value prestored in the second shift register S1, and outputs the sum of the values as a second encoding value Z' for data bit value D.

Accordingly, if a single data bit value D is input, the values D, Z and Z' may be simultaneously output by the shift operations of the shift registers S0, S1 and S2. The stream
constructor 130 constructs a stream by sequentially arranging the output values D, Z₁' and Z₂'.

[0046] FIG. 3 is an exemplary diagram explaining a transmission stream processing method in the transmission stream processing device of FIG. 1 according to an exemplary embodiment of the present invention. In FIG. 3, if a single byte comprising data bits D0 to D7 (D7 being the most significant bit (MSB) and DO being the least significant bit (LSB)) is input, the data bits may be detected sequentially from the MSB to the LSB, and the detected bits may be output to the encoder 120 (S310).

[0047] The encoder 120 outputs the data bit values, first encoding value and second encoding value, in response to the input data bit values (S320).

[0048] The stream constructor 130 sequentially arranges the output data bit values, first encoding value and second encoding value, and constructs a stream comprising three bytes (S330). Specifically, the stream constructor 130 sequentially arranges initial output data D7, Z₁' and Z₂', from the MSB of the first byte of the stream, and then arranges next output data D6, Z₆' and Z₅' sequentially. Subsequently, the stream constructor 130 sequentially arranges D5 and Z₄' among next output data D₄, Z₃' and Z₂', and then arranges Z₁' in the MSB of the second byte of the stream. Accordingly, a single data bit D and two corresponding encoding values Z₁' and Z₂' may be sequentially arranged, and as a result, coding may be performed at a coding rate of ½.

[0049] FIG. 4 is a block diagram showing a configuration of a transmission stream processing device according to another exemplary embodiment of the present invention. In FIG. 4, the transmission stream processing device according to the other exemplary embodiment of the present invention comprises a duplicator 210, a detector 220, an encoder 230 and a stream constructor 240.

[0050] The duplicator 210 receives a stream, and generates place-holders in a portion of each data bit of the stream. The place-holders are regions into which the encoding values are inserted. The duplicator 210 may generate two consecutive place-holders for each data bit so that the stream can be coded at a coding rate of ½.

[0051] Specifically, the duplicator 210 divides each byte of the input stream into three sections. Some of the bit values and null data (for example, 0) for a single byte may be placed in each of the divided bytes. A region in which the null data is placed becomes a place-holder.

[0052] For example, if a single byte of the stream comprises data bits D7, D6, D5, D4, D3, D2, D1 and DO from the MSB, the duplicator 210 may generate two consecutive place-holders for each data bit. In other words, the duplicator 210 may output a first byte comprising D7, 0, 0, D6, 0, 0, D5 and 0, a second byte comprising 0, D4, 0, 0, D3, 0, 0 and D2, and a third comprising 0, D1, 0, 0, DO, 0 and 0.

[0053] The detector 220 detects only the data bits from the bytes output from the duplicator 210, and outputs the detected data bits to the encoder 230.

[0054] The encoder 230 encodes the detected data bits and outputs two encoding values for each data bit.

[0055] The stream constructor 240 constructs a stream in such a manner that the encoding values output from the encoder 230 are inserted into the place-holders generated by the duplicator 210. Consequently, two encoding values are added to a single data bit, and thus it is possible to perform coding of the stream at a coding rate of ¼.

[0056] FIG. 5 is a circuit diagram showing a configuration of the encoder 230 which is applied to the transmission stream processing device of FIG. 4 according to an exemplary embodiment of the present invention. The encoder 230 of FIG. 5 comprises a plurality of shift registers SO, S1 and S2, and a plurality of adders 231, 232 and 233.

[0057] The configuration and connection relationships of the plurality of shift registers SO, S1 and S2 and plurality of adders 231, 232 and 233 are the same as those of the plurality of shift registers SO, S1 and S2 and plurality of adders 122, 123 and 124 shown in FIG. 3, so repeated description thereof is omitted. The encoder 230 does not include a bit output line which outputs input data bits without alteration in the encoder 230 of FIG. 5, and thus the encoder 230 may output only encoding values Z₁' and Z₂', even if data bit D is input.

[0058] FIG. 6 is an exemplary view explaining a transmission stream processing method in the transmission stream processing device of FIG. 4. In FIG. 6, if the data bits are detected from the stream comprising three bytes output from the duplicator 210 (S610), the detected data bits may be input to the encoder 230. Accordingly, the encoder 230 may output the first encoding value and second encoding value corresponding to each data bit simultaneously (S620).

[0059] The stream constructor 240 may construct a stream by inserting the output first and second encoding values into the place-holders generated in one side of each corresponding data bit (S630). Specifically, the stream constructor 240 may sequentially arrange encoding values Z₁' and Z₂', for data bit D7 next to data bit D7 placed in the MSB of the first byte. In the same manner, encoding values Z₆', Z₅', Z₄', Z₃', Z₂', Z₁', Z₀', and Z₃' may be inserted into the place-holders, and thus a stream of three bytes may be formed.

[0060] The encoded stream may be transmitted to a digital broadcasting receiving apparatus through various subsequent processes in the same manner as described above. Specifically, processing such as randomization, interleaving, multiplexing of a sync signal, trellis encoding, VSB modulating, upconverting or the like may be performed.

[0061] The transmission stream processing devices shown in FIGS. 1 and 4 are applicable to normal data or turbo coding data. In other words, if a multi-data stream comprising normal data and turbo coding data is generated, the generated multi-data stream may be randomized and a parity area may be generated, and then interleaving may be performed. After demultiplexing and detecting only the turbo coding data from the multi-data stream, encoding may be performed in the same manner as described above. Accordingly, the turbo coding data may be processed more robustly. Subsequently, the encoded turbo coding data may be interleaved, and then be multiplexed into the multi-data stream again. Therefore, processing such as data deinterleaving, Reed-Solomon encoding, data interleaving, trellis encoding, multiplexing of a sync signal, modulating, or the like may be performed on the reconstructed multi-data stream, and the processed multi-data stream may be output through a wireless channel. The above transmission stream processing processes are known to those of ordinary skill in the art, so detailed description thereof is omitted.

[0062] FIG. 7 is a block diagram showing a configuration of a reception stream processing device which is applicable to a digital broadcasting receiving apparatus and which receives the stream encoded by the transmission stream processing devices of FIGS. 1 and 4.
In FIG. 7, the reception stream processing device comprises a receiver 710, a detector 720 and a decoder 730.

The receiver 710 receives a stream coded at a coding rate of $\frac{3}{4}$. The receiver 710 may comprise a demodulator (not shown) and an equalizer (not shown). The demodulator receives a stream transmitted from the digital broadcasting receiving apparatus via an antenna and demodulates the received stream. The equalizer equalizes the demodulated stream. Accordingly, the receiver 710 may generate a stream having the same configuration as the final streams as shown in FIG. 3 or FIG. 6, and may transfer the generated stream to the detector 720.

The detector 720 detects data bits and encoding values from the stream received by the receiver 710. In other words, the detector 720 may sequentially detect values $D$, $Z'$ and $Z''$ from among the received byte streams, and may send the detected values to the decoder 730. In this situation, the detector 720 may correctly detect the encoding values using sync signals output from the digital broadcasting receiving apparatus and position information of the predefined encoding values. The received bytes are respectively divided into every three bytes. For example, every three bits from the MSB of the first byte may be divided, and may be output to the decoder 730. In this situation, the remaining bits of the first byte are connected to the MSB of the second byte, and then the stream of the connected bits may be output to the decoder 730. Accordingly, the data bits and encoding values may be appropriately provided to the decoder 730.

The decoder 730 performs decoding using the detected data bits and encoding values, to restore data in the stream. Accordingly, the data stream comprising the data bits D0 to D7 can be retrieved.

FIG. 8 is a flowchart explaining a reception stream processing method according to another exemplary embodiment of the present invention. In FIG. 8, if the stream coded at a coding rate of $\frac{3}{4}$ is received (S810), the data bits and encoding values contained in the received stream may be detected from the stream (S820). In this situation, two encoding values may be detected for each data bit.

Next, decoding may be performed using the detected encoding values and data bits to restore data (S830). Therefore, it is possible to receive and process a stream coded at an unusual coding rate, for example a coding rate of $\frac{3}{4}$.

As described above, according to the exemplary embodiments of the present invention, a stream may be coded and transmitted at a coding rate of $\frac{3}{4}$, and the stream may be received and data may be retrieved from the received stream. Accordingly, when a multi-transmission stream is generated, the type of data may be varied, and thus it is possible to efficiently use the multi-transmission stream.

Although a few exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.

1. A transmission stream processing device comprising:
   - a detector which detects data bits in a stream;
   - an encoder which encodes the data bits detected by the detector and generates two encoding values for each data bit; and
   - a stream constructor which constructs a transmission stream with a coding rate of $\frac{3}{4}$ using the encoding values generated by the encoder.

2. The transmission stream processing device of claim 1, wherein the encoder comprises:
   - first, second and third shift registers which are connected in series and perform shifting operations complementary to each other;
   - a bit output line which sequentially receives the data bits detected by the detector and outputs a data bit value of each data bit without alteration;
   - a first adder which sums the data bit value output from the bit output line, a value prestored in the first shift register and a value prestored in the third shift register, and outputs the sum to the third shift register;
   - a second adder which sums the data bit value output from the bit output line, a value prestored in the second shift register and a value prestored in the third shift register, and outputs the sum as a first encoding value for the data bit value; and
   - a third adder which sums the data bit value output from the bit output line and the value prestored in the second shift register, and outputs the sum as a second encoding value for the data bit value.

3. The transmission stream processing device of claim 2, wherein the stream constructor constructs the transmission stream by sequentially arranging the data bit value, first encoding value and second encoding value which are output from the encoder.

4. The transmission stream processing device of claim 1, further comprising a duplicator which receives the stream and generates place-holders at one side of each of the data bits in the stream.

5. The transmission stream processing device of claim 4, wherein the encoder comprises:
   - first, second and third shift registers which are connected in series and perform shifting operations complementary to each other;
   - a first adder which sums a data bit value of a data bit detected by the detector, a value prestored in the first shift register and a value prestored in the third shift register, and outputs the sum to the third shift register;
   - a second adder which sums the data bit value, a value prestored in the second shift register and a value prestored in the third shift register, and outputs the sum as a first encoding value for the data bit value; and
   - a third adder which sums the data bit value and the value prestored in the second shift register, and outputs the sum as a second encoding value for the data bit value.

6. The transmission stream processing device of claim 5, wherein the stream constructor constructs the transmission stream by inserting the first and second encoding values output for each data bit in the place-holders.

7. A transmission stream processing method comprising:
   - detecting data bits in a stream;
   - encoding the detected data bits to generate two encoding values for each data bit; and
   - constructing a transmission stream with a coding rate of $\frac{3}{4}$ using the encoding values.

8. The transmission stream processing method of claim 7, wherein the encoding comprises encoding each of the data bits using an encoder which comprises first, second and third shift registers, which are connected in series and perform shifting operations complementary to each other, and a plurality of adders, and outputs data bit values and the two encoding values for each data bit.
9. The transmission stream processing method of claim 8, wherein the constructing comprises sequentially arranging the data bit value, a first encoding value and a second encoding value which are output from the encoder, to construct the transmission stream.

10. The transmission stream processing method of claim 7, further comprising receiving the stream and generating placeholders on one side of each of the data bits in the stream, wherein the detecting comprises detecting the data bits in the stream having the placeholders.

11. The transmission stream processing method of claim 10, wherein the encoding comprises encoding each of the data bits using an encoder which comprises first, second and third shift registers, which are connected in series and perform shifting operations complementary to each other, and a plurality of adders, and outputs the two encoding values for each data bit.

12. The transmission stream processing method of claim 11, wherein the constructing comprises constructing the transmission stream by inserting the two encoding values output from the encoder into the placeholders.

13. A reception stream processing device comprising:
   a receiver which receives a stream coded at a coding rate of \(1/3\);
   a detector which detects data bits and encoding values in the stream; and
   a decoder which performs decoding using the data bits and the encoding values, which are detected by the detector, to retrieve data in the stream.

14. A reception stream processing method comprising:
   receiving a stream coded at a coding rate of \(1/3\);
   detecting data bits and encoding values in the stream; and
   performing decoding using the data bits and the encoding values, which are detected, to retrieve data in the stream.

15. The reception stream processing apparatus of claim 13, wherein the detector detects two encoding values for each data bit.

16. The reception stream processing method claim 14, wherein the detecting comprises detecting two encoding values for each data bit.