(54) **APPARATUSES FOR CONTROLLING PHASE DIFFERENCE IN PLASMA PROCESSING SYSTEMS**

VORRICHTUNGEN ZUR PHASENDIFFERENZSTEUERUNG IN EINEM PLASMABEHANDLUNGSSYSTEM

DISPOSITIFS DE COMMANDE DE LA DIFFERENCE DE PHASE DANS LES SYSTEMES DE TRAITEMENT DE PLASMA

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Description

Background of the Invention

[0001]   The present invention relates to apparatuses for inducing plasma in plasma enhanced processing systems, which are typically used in semiconductor fabrication. More specifically, the invention relates to apparatuses for controlling the phase shift between generators in plasma processing systems to achieve desired process results.

[0002]   Plasma-enhanced semiconductor processes for etching, oxidation, anodization, chemical vapor deposition (CVD), or the like are known. For illustration purposes, Fig. 1 shows a chemical etch reactor 100, representing a plasma generating system which utilizes an inductive coil for plasma generation. Reactor 100 includes coil system 102 and chamber 124. Coil system 102 includes a coil element 106, which is excited by a radio frequency generator 110. Coil element 106 is coupled to a matching circuit 108 for matching the impedance of coil element 106 to that of radio frequency generator 110. The matching of the impedances permits radio frequency generator 110 to efficiently deliver power to coil element 106. To provide a path to ground, the chamber wall of chamber 124 is typically grounded. Alternatively, the ground path may be provided through the lower electrode, e.g., a chuck 128 of Fig. 1, when the plasma is confined.

[0003]   Within chamber 124, there typically exists a shower head 126. Shower head 126 is shown disposed above a chuck 128 and wafer 134, which is supported by chuck 128. Chuck 128 acts as a second electrode and is preferably biased by its independent radio frequency circuit 120 via a matching network 122. It should be borne in mind that the components of Fig. 1, as well as of other figures herein, are shown only representatively for ease of illustration and to facilitate discussion. In actuality, coil element 106 and match 108 are typically disposed proximate to chamber 124 while RF generator 110 may be placed in any reasonable location.

[0004]   Shower head 126 represents the apparatus for dispensing etchant or deposition materials onto wafer 134. Shower head 126 preferably includes a plurality of holes for releasing gaseous source materials (typically around the periphery edge of shower head 126) into the RF-induced plasma region between itself and wafer 134 during operation. In one embodiment, shower head 126 is made of quartz although it may also be made of other suitable materials and may be left either electrically floating or grounded.

[0005]   To provide power to the plasma etch system 100, generators 110 and 120 are typically driven at a given RF frequency. To ensure that both generators deliver power at the same frequency, they may be frequency-locked in a master-and-slave configuration. For example, lower (bias) generator 120 may be designated the master, and the frequency of the upper (coil) generator 110 may slaved to that of master generator 120 (or vice versa). Frequency locking may be achieved by any conventional technique, including, e.g., disabling the frequency-generating crystal in the slave generator and employing the frequency-generating crystal in the master generator to drive both the master and slave generators.

[0006]   While the configuration of the two generators in a master-and-slave configuration enables both generators to deliver power at the same RF frequency, such a configuration does not guarantee that power will be delivered by the two generators at the same phase. A phase difference may arise due to factors internal to the generators themselves or due to system parameters such as the difference in the lengths of the cables that couple the generators to their respective electrodes. It is discovered that the phase difference may give rise to undesirable or unexpected process and electrical characteristics, which may lead to uncertain consequences on the process results.

[0007]   In view of the foregoing, what is desired is apparatuses for controlling the phase difference between master-and-slave configured RF generators that are employed to deliver power to plasma processing systems.

[0008]   US-5,116482 describes a film forming system using capacitive plasma generation for sputtering thin films. The system includes a first master RF power supply connected to a top capacitive electrode by a matching box. A second slave RF power supply is connected to a bottom capacitive electrode by a second matching box. A first monitor sensor detects the voltage of the top electrode and a second monitor sensor detects the voltage of the bottom electrode. The outputs of the monitor sensors are passed to a phase adjusting device which is also supplied with an externally set signal. The phase adjusting device generates a phase shifting signal to controls the slave RF power supply to have a phase difference with respect to the master power supply corresponding to the phase difference set by the externally set signal.

[0009]   According to the present invention there is provided a plasma processing system for generating plasma for use in semiconductor fabrication, said plasma processing system having a first radio frequency (RF) power source for outputting a first RF signal to a first electrode and a second RF power source for outputting a second RF signal to a second electrode, said second RF power source being coupled to said first RF power source as a slave RF power source in a master-and-slave configuration, said plasma processing system comprising a control circuit, including: a first sensor circuit coupled to said first electrode for detecting a phase of said first RF signal; a first matching circuit connected between the first RF power source and the first electrode; a second sensor circuit coupled to said second electrode for detecting a phase of said second RF signal; a second matching circuit connected between the second

RF power source and the second electrode; a mixer circuit coupled to said first sensor circuit and said second sensor circuit for detecting a phase difference between said first RF signal and said second RF signal and for outputting a first signal representing said phase difference; a phase servo circuit coupled to said second RF power source and said mixer circuit, said phase servo circuit outputting, responsive to said first signal and a phase control set point signal, a control signal to said second RF power source for modifying a phase of said second RF signal, thereby causing said phase difference to approximate a phase difference value represented by said phase control set point signal; and characterised in that: the first sensor circuit is connected between the first matching circuit and first electrode; the second sensor circuit (414) is connected between the second matching circuit and second electrode; and wherein the first or second electrode represents an upper electrode of said plasma processing system for inductive plasma generation in a plasma processing chamber.

[0010]   These and other advantages of the present invention will become apparent upon reading the following detailed descriptions and studying the various figures of the drawings.

Brief Description of the Drawings

[0011]

Fig. 1 shows a typical plasma generating system.

Fig. 2A is a schematic illustrating, in one embodiment of the present invention, the overall control circuit for controlling the phase difference between two frequency-locked RF generators of a plasma processing system.

Fig. 2B shows an implementation of the upper TCP match circuit of the control circuit of Fig. 2A.

Fig. 2C illustrates an implementation of the lower TCP match circuit of the control circuit of Fig. 2A.

Fig. 2D illustrates an implementation of the d.c. bias measurement circuit of the control circuit of Fig. 2A.

Fig. 3 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the optical amplitude of the 261 nm plasma emission, which is employed to determine the endpoint for the aluminum etch.

Fig. 4 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the lower (bias) electrode RF peak-to-peak voltage.

Fig. 5 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the wafer d.c. bias voltage.

Fig. 6A is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the oxide etch rate.

Fig. 6B is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the remaining oxide thickness.

Fig. 7 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the aluminum-to-oxide selectivity.

Fig. 8 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the photoresist etch rate.

Fig. 9 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the aluminum-to-photoresist selectivity.

Figs. 10 and 11 are graphs illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the remaining photoresist thickness at the center of the wafer (Fig. 10), and at the edge of the wafer (Fig. 11).

Figs. 12 and 13 are graphs illustrating, in accordance with one aspect of the present invention, the effect of the

phase shift on the critical dimension (CD) at the center of the wafer and the edge of the wafer respectively.

Fig. 14 shows the steps involved in an etch process in which the phase difference between the RF power supplies are controlled, either actively or passively, to achieve the desired process results.

Detailed Description of the Preferred Embodiments

[0012]   An invention is described for improving process results by controlling the phase difference of the phases of the RF signals supplied by the RF power supplies of a plasma processing system. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order not to unnecessarily obscure the present invention.

[0013]   Fig. 2A is a schematic illustrating, according to the present invention, the overall control circuit for controlling the phase difference between two frequency-locked generators of a plasma processing system. In Fig. 2A, RF generators 402 and 404 are arranged in a master-and-slave configuration with RF generator 402 acting as the reference generator. Power to the plasma in a plasma processing chamber 406 are delivered by these two RF generators 402 and 404 through match circuits 408 and 410, respectively. It should be noted that although the chuck RF generator, e. g., RF generator 402, is designated the master generator in Fig. 2A, the invention applies equally well when the RF generator associated with the upper electrode, e.g., RF generator 404, is designated the master. Further, although the upper electrode 412 is shown having an Archimedes spiral coil in Fig. 2A, other suitable electrodes may well be employed to generate plasma within the plasma processing chamber. One end of the coil may be isolated from ground, e.g., through a transformer, or grounded.

[0014]   To ascertain the phase of the RF signal supplied to coil 412, a sensor 414 is coupled to one end of coil 412. Sensor 414 is disposed between coil 412 and match network 410 to avoid the effects of the tuning networks that are used for impedance matching. Likewise, a sensor 416 is coupled between chuck electrode 418 and match circuit 408 to ascertain the phase of the RF signal supplied to chuck electrode 418.

[0015]   The outputs of sensors 414 and 416 are input into a mixer circuit 420, which may be implemented by any one of the conventional mixer circuit designs. The output of mixer circuit 420, representing the feedback signal that is proportional to the phase difference between the phases of the RF signals detected by sensors 414 and 416, is then input into a phase servo circuit 422. When the Phase/Bias select control signal 423 is set to phase control, phase servo circuit 422, which may be implemented by an error amplifier or any number of known phase servo circuit designs, compares the feedback signal from mixer circuit 420 with a phase control set point signal 424 to output a control signal 430 to the slave generator, e.g., RF generator 404 in Fig. 2A. Responsive to control signal 430, the slave generator then modifies its phase, thereby causing the phase difference between the phases of the RF signals detected by sensors 414 and 416 to substantially match the value specified by phase control set point signal 424.

[0016]   In one embodiment, phase control set point value 424 may represent a predefined value to facilitate system matching, i.e., to ensure that the difference between the phases of the RF signals supplied to the upper electrode and lower electrode is substantially the same from machine to machine. The inventive technique of feedback control to ensure that the phase difference conforms to a predefined value is referred to herein as passive control of the phase difference. When the phase difference is passively controlled, it is possible to ensure that the phase difference between the phases of the RF signals will stay substantially constant across different systems irrespective of system parameters, e.g., the placement of the RF generators relative to the plasma processing chamber.

[0017]   In another embodiment, phase control set point value 424 may represent a user-variable value for actively controlling the phase difference between the phases of the RF signals to achieve desired process results. The inventive technique of actively modifying the phase difference to achieve specific desired process results is referred to herein as active control of the phase difference. By way of example, a user may specify that the RF signal supplied to the upper electrode lead the RF signal supplied to the lower electrode by 180 to maximize aluminum-to-photoresist selectivity during an aluminum etch step (the effect of the phase difference on the aluminum-to-photoresist selectivity is illustrated in a subsequent Fig. 9 herein). As a further example, the user may specify that the RF power supplies deliver their power in phase to maximize the etch rate during an oxide etch step (Fig. 6A). Other examples are readily apparent to those skilled in the art upon reviewing the figures and the disclosure herein.

[0018]   In another embodiment, either the chuck's RF peak-to-peak a.c. voltage or the wafer's d.c. voltage may be used as a feedback signal to facilitate control of either of those two values by changing the phase difference. With reference to Fig. 2A, an a.c./d.c. bias measurement circuit 440 represents, for ease of illustration, the circuit for measuring either the chuck's RF peak-to-peak a.c. voltage or the wafer's d.c. voltage (depending on the embodiment). By way of example, if the chuck employs mechanical clamping, a.c./d.c. bias measurement circuit 440 may represent a d.c. bias measurement circuit. On the other hand, if the chuck is an electrostatic chuck, a.c./d.c. bias measurement

circuit 440 may represent either a d.c. bias measurement circuit or one that measures the chuck's RF peak-to-peak a.c. voltage.

[0019]   The chuck's RF peak-to-peak a.c. voltage may be measured using a voltage probe or any other conventional technique. The wafer's d.c. voltage may be sensed by, for example, employing a probe inside chamber 406 to sense the state of the plasma within chamber 406, or by inferring it from the chuck's RF peak-to-peak a.c. voltage itself. For further information regarding a method of inferring the wafer's d.c. bias from the chuck's RF peak-to-peak a.c. voltage, reference may be made to the commonly-assigned, co-pending patent applications entitled "Dynamic Feedback Electrostatic Chuck," (U.S. patent no. 5,812,361) and "Voltage Controller for Electrostatic Chuck of Vacuum Plasma Processors" by Neil Benjamin, Seyed Jafar Jafarian-Tehrani, and Max Artussi (U.S. patent no. 5,708,250), both filed on even date.

[0020]   The signal output by a.c./d.c. bias measurement circuit 440 is then input into a peak bias control circuit 442. Peak bias control circuit 442 represents the circuit for comparing the signal output by a.c./d.c. bias measurement circuit 440 with a user-input bias set point signal 444 and for outputting an error signal 446. Responsive to this error signal, phase servo circuit 422 then modifies control signal 430, thereby modifying the phase difference between the RF signals supplied by the two RF generators and indirectly modifying either chuck's RF peak-to-peak a.c. voltage or the wafer's d.c. bias voltage (depending on the implementation of ac/dc bias measurement circuit 440) until it matches the bias set point signal 444.

[0021]   It is contemplated that the signal output by a.c./d.c. bias measurement circuit 440 may be monitored by an appropriate logic circuit to allow the user to, for example, determine the phase difference that results in a specific value of chuck's RF peak-to-peak a.c. voltage (or wafer's d.c. bias voltage). By way of example, the phase of the slave generator may be modified while monitoring the value output by a.c./d.c. bias measurement circuit 440 to ascertain the phase difference value that results in, e.g., the highest or lowest chuck's RF peak-to-peak a.c. voltage (or wafer's d.c. bias voltage). Since these specific values of the chuck's RF peak-to-peak a.c. voltage (or the wafer's d.c. bias voltage) are directly related to specific process characteristics, the user may then employ the ascertained phase difference as an input into phase servo circuit 422 to ensure that the desired process results can be obtained more reliably and consistently.

[0022]   It will be apparent to those skilled in the art that the inventive control circuit does not have to include all the components shown in Fig. 2A. It includes essentially of sensors 414 and 416, mixer circuit 420, two electrodes 412, 418, matching circuits 408, 410, and phase servo circuit 422. With these circuit blocks, the detection of the phase difference between the RF signals supplied by the RF power supplies and the modification of that phase difference are facilitated. If it is desired to also modify the phase difference to achieve a specific RF peak-to-peak a.c. voltage set point or a specific wafer d.c. voltage set point, the control circuit may include a.c./d.c. bias measurement circuit 440 and peak bias control circuit 442 of Fig. 2A. Match circuits 408 and 410 may be implemented by any number of conventional match circuits. Fig. 2B shows an implementation of upper TCP match circuit 410 that has been found to be suitable. In Fig. 2B, capacitor Cs resonates the inductance of the TCP coil. Capacitor C_P transforms the load impedance to match the source impedance of the RF power source, which is typically about 50 Ω. Inductors L_P and L_S are primary and secondary inductances of the match transformer. The values of these inductances L_P and L_S depend on the coil size and the coupling factor between the coil and the plasma. One version of match circuit 410, known by its part number 853-031685-001, is available from the aforementioned Lam Research Corp.

[0023]   Fig. 2C illustrates an implementation of lower TCP match circuit 408. In Fig. 2C, variable inductor Ls' is employed to resonate the load. Variable coupling factor K transforms the load to the proper impedance to maximize power delivery by the RF generator. One version of match circuit 408, known by its part number 853-015130-002, is available from the aforementioned Lam Research Corp.

[0024]   Fig. 2D illustrates a d.c. bias measurement circuit that is suitable for implementing a.c./d.c. bias measurement circuit 440. In Fig. 2D, the chuck's RF signal is sensed through a plurality of resistors 460, which provides a high impedance to ground to limit amount of RF current drawn. In one embodiment, there are five resistors 460 in series to reduce the capacitive division effect of the d.c. bias measurement circuit. Resistors 470 and 472 form a resistor network for scaling down the signal received through the plurality of resistors 460. Capacitor 474 is coupled in parallel with resistors 470 and 472 to supply a d.c. signal on conductor 476, which is coupled to the peak bias control circuit, e.g., peak bias control circuit 442 of Fig. 2. One version of the d.c. bias measurement circuit, known by its part number 810-017029-001, is available from the aforementioned Lam Research Corp.

[0025]   In accordance with one aspect of the present invention, the effects of the phase shift on process characteristics are investigated to determine whether changes to the phase shift impact certain critical process parameters such as the RF peak-to-peak voltage on the lower electrode, the wafer d.c. bias, etch rates, aluminum-to-photoresist selectivity, and others. As shown in the graphs of Figs. 3 to 13 below, it is determined that changes in the phase shift between the RF signals supplied by the RF generators do indeed impact certain critical process parameters. These discoveries buttress the conclusion that the ability to achieve reliable, consistent process results can be enhanced when the phase shift is controlled either passively or actively.

[0026] In the disclosure that follows, it should be borne in mind that the disclosed invention may be practiced in any plasma etch systems to etch, among others, the metallization layer, the oxide layer, or the polysilicon layer. The invention may also be practiced, as can be appreciated by those skilled in the art, in plasma CVD systems to control film characteristics such as density and/or stress, or in any plasma processing systems, which may be employed for anodization, oxidation, or the like. To better illustrate the invention and to provide one specific example, however, details pertaining to specific systems and materials are disclosed. To achieve the results illustrated in subsequent Figs. 3-13, two frequency-locked Advanced Energy 1,250 Watt 13.56 MHz RF generators are configured in a master-and-slave configuration to provide power to a TCP 9600™ etching system, which is available from Lam Research Corporation of Fremont, California. In this configuration, the lower (bias) generator is employed as the master to the upper (TCP) slave generator (although the invention applies equally well when the upper generator serves as the master).

[0027] To generate the requisite phase shift for the experiments pertaining to Figs. 3-13, an ENI VL400 phase shift controller by ENI, which is a division of Astec America Inc. of Rochester, New York, was coupled to both generators to keep the lower (bias) generator fixed and to phase shift the upper (TCP) generator relative to the lower generator. To determine etch rates and selectivities, a patterned wafer from SEMATECH of Austin, Texas, was exposed to a partial etch. This SEMATECH wafer comprises the following layers: photoresist layer, TiN arc (anti-reflective) layer, metallization layer comprising aluminum-silicon-copper, barrier layer comprising titanium, and oxide layer. To determine the oxide etch rates, a wafer having thereon patterned thermal oxide is employed.

[0028] In the TCP 9600™ plasma processing system, the process settings for the experiments related to Figs. 3-13 are approximately as follows:

TABLE 1

Power to top electrode (watts)	400
Power to bottom electrode (watts)	100
Reactor chamber pressure (Pa)	0.67 (5 m Torr)
Cl_2 flow rate (m^3s^{-1})	1×10^{-6} (62 sccm)
BCl_3 flow rate (m^3s^{-1})	3×10^{-7} (18 sccm)
Wafer Temperature (°C)	50
Helium cooling gas (Pa)	1,600 (12 Torr)

[0029] To determine the impact of the phase shift between the RF signals supplied by the master-and-slave configured RF generators, four different phase shift settings were employed: - 90° (i.e., the top generator lags the bottom generator by 90°), 0° (i.e., they are in phase), 90° (i.e., the top generator leads the bottom generator by 90°), and 180° (i.e., they are opposite in phase).

[0030] Fig. 3 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the optical amplitude of the 261 nm plasma emission, which is employed to determine the endpoint for the aluminum etch. Through appropriate optical filters, the mean value of the 261 nm signal when the generators are running in phase was observed to be low relative to the mean value of the same signal when the generators were running at - 90°, 90°, and 180° out of phase respectively. The lower mean value of the optical signal suggests that relatively less intense plasma is present when the power is delivered by the two generators in phase.

[0031] Fig. 4 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the lower (bias) electrode RF peak-to-peak voltage. Fig. 3 indicates that changes in phase shift indeed result in changes in the lower electrode RF peak-to-peak voltage in the range from about 34 to 41 volts, with the lower electrode RF peak-to-peak voltage attaining its maximum when the generators are in phase, as shown in Fig. 4. By controlling the phase shift, e.g., using the circuit of Fig. 2A or another suitable control circuit, the lower electrode RF peak-to-peak voltage may be controlled, leading to improved process results.

[0032] The d.c. bias of Fig. 5 tracked the lower electrode peak-to-peak voltage and varies from about - 39 volts to - 26 volts as the phase difference was shifted from 0° to 180°, as shown in Fig. 5. The changes in the d.c. bias voltage indicates that the plasma characteristics are significantly impacted by the phase shift. The d.c. bias voltage is directly linked to the process occurring on the wafer since when the d.c. bias is higher, the etching ions will likely impact the wafer with a higher energy to result in a higher etch rate and a more anisotropic etch. Since etching for semiconductor devices is a precise balancing of chemical and physical processes, and physical etching is tied directly to the difference between the plasma potential and the d.c. potential on the wafer, the bias needs to be under tight control, not only to ensure that repeatable process results can be achieved, but also to harness the phase shift to enhance process results, e.g., maximize or minimize the etch rates or the anisotropic etch quality. Again, the etch results suggest that desirable

process characteristics may be achieved by controlling, either passively or actively, the phase difference between the RF signals supplied by the RF power supplies.

[0033] Further, since there is a correspondence between the wafer d.c. bias or the lower electrode RF peak-to-peak voltage and the phase shift, it is possible, as mentioned earlier in connection with Fig. 2A, to employ either the wafer d.c. bias or the lower electrode peak-to-peak voltage as a feedback signal to a phase control circuit in order to passively or actively control the phase difference, i.e., to either maintain a desired phase difference value across different plasma processing systems or to actively control the phase difference to enhance process results.

[0034] Fig. 6A is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the oxide etch rate. As shown in Fig. 6A, when the RF power supply to the top TCP coil lags the RF power supply to the bottom electrode by 90° (- 90° in Fig. 6A), the oxide etch rate is approximately 1,600 angstroms per minute. In contrast, when these two RF power supplies are in phase, the oxide etch rate is up to about 1,750 angstroms per minute. The oxide etch rate when the top power supply leads the bottom power supply by 90° and 180° is significantly lower, at about 1,400 and 1,500 angstroms (10^{-10} m) per minute respectively. As seen, significant changes in the oxide etch rates may be obtained by changing the phase shift. With reference to Fig. 6A, for example, an etch rate difference of up to about 300 angstroms per minute may be obtained when the phase shift changes from 0° to 90°.

[0035] Fig. 6B is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the remaining oxide thickness. The oxide thickness is at its lowest when the phase difference is about 90° and is high when the phase difference is either 0° or 180°. Consequently, changes to the phase difference do indeed impact the remaining oxide thickness, and further point to the advantages that may be achieved when the phase difference is controlled.

[0036] Fig. 7 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the aluminum-to-oxide selectivity. As shown in Fig. 7, the selectivity varies significantly responsive to the phase shift, having values of about 5.6, 5.0, 6.5, and 6.0 for a phase shift value of about - 90°, 0°, 90°, and 180°, respectively. Further, there appears to be a correlating trend between a high wafer d.c. bias (as seen in Fig. 5) and low selectivity. For example, when the power supplies are in phase, the wafer d.c. bias is at its highest (in Fig. 5) while the aluminum-to-oxide selectivity is at its lowest (in Fig. 7). One possible explanation is that when the power supplies are delivering power to the plasma in phase, a high d.c. bias may increase the energy of the impacting ions, thereby decreasing the aluminum-to-oxide selectivity.

[0037] Fig. 8 is a graph illustrating, in accordance with one aspect of the present invention, the effect of the phase shift on the photoresist etch rate. Again, changes in the phase shift appear to significantly impact the etch rate of the photoresist with an etch rate of as high as over about 3,000 angstroms per minute when the power supplies are in phase, and about 2,600 angstroms per minute when the power supplies are about 180° out of phase.

[0038] In Fig. 9, the effect of the phase shift on the aluminum-to-photoresist selectivity is shown. Fig. 9 illustrates, in accordance with one aspect of the present invention, that changing the phase shift also significantly impacts the aluminum-to-photoresist selectivity. For example, the lowest aluminum-to-photoresist selectivity is obtained when the power supplies are delivering power to the plasma in phase (0° phase shift). The maximum selectivity, as illustrated in Fig. 9, is achieved when the power supplies are delivering power at about 180° out of phase. This has several important implications. As manufacturers move toward smaller devices, a high aluminum-to-photoresist selectivity is valuable. This is because as the lines become thinner, the photoresist layer must be thinner. A thinner photoresist layer requires a higher aluminum-to-photoresist selectivity so that the protective photoresist layer does not get inadvertently etched away, resulting in damage to the underlying features. Fig. 9 suggests that increased aluminum-to-photoresist selectivity can be achieved by changing the phase shift between the RF power supplies.

[0039] Further, as the trend of Figs. 6A, 7, and 8 suggests, the highest etch rate and lowest selectivities are obtained when the power supplies are in phase. It appears that the aluminum-to-photoresist selectivity can be improved when the power supplies are delivering power to the plasma out of phase. For example, the highest aluminum-to-oxide selectivity occurs when the power supplies are about 90° out of phase (Fig. 7), and the highest aluminum-to-photoresist selectivity occurs when the power supplies are about 180° out of phase (Fig. 9).

[0040] Figs. 8 and 9 also suggest that the slowest photoresist etch rate and the highest aluminum-to-photoresist selectivity are obtained when the power supplies are delivering power to the plasma at about 180° out of phase. At about 180°, it can be expected that more of the photoresist will remain, i.e., less of the photoresist layer will get etched away, resulting in better protection of the underlying features. The ability to adjust the hardware to improve the ability of a given photoresist layer to protect the underlying features is particularly valuable as devices are scaled smaller and smaller.

[0041] In Figs. 10 and 11, remaining photoresist on 0.8 μm feature is measured, after etching with a recipe commonly used to etch through the aluminum layer in semiconductor manufacturing, at the center of the wafer (Fig. 10), and at the edge of the wafer (Fig. 11). As shown in Figs. 10 and 11, maximum remaining photoresist thickness measurements occur when the power supplies deliver their power at about 180° phase shift. Note that the remaining photoresist thickness measurements are maximized and minimized at the same phase shifts, i.e., at 180° phase shift and about

90° phase shift respectively, in both Fig. 10 and Fig. 11. Consequently, it appears that the changes in the phase shift result in bulk plasma effects, i.e., not localized either at the wafer edge or the wafer center. It is therefore expected, in accordance with one aspect of the present invention, that changes to the phase difference affect the protective quality of the photoresist layer across the entire wafer.

[0042]   Figs. 12 and 13 illustrate the effect of the phase shift on the critical dimension (CD) at the center of the wafer and the edge of the wafer respectively. The critical dimension (CD) represents the post-etch measurement of the line width. Maximum critical dimension measurements were obtained when the generators were in the high bias, in-phase condition, when photoresist erosion was at a maximum. A high amount of photoresist erosion passivates the sidewall to a greater degree to protect the aluminum against erosion, resulting in more protection for the lines and a greater CD measurement. Minimum critical dimension measurements occur at both the wafer center and the wafer edge when the generators were running at a phase shift of about 180° and, as shown in Fig. 8, the photoresist etch rate is at its minimum. Since there is less photoresist erosion, less passivation of the sidewall occurs. As shown in Figs. 12 and 13, changes in the phase shift between the generators result in changes in the critical dimension. These figures suggest that undercutting of the aluminum sidewall can be minimized, in accordance with one aspect of the present invention, simply by changing the phase shift between the generators.

[0043]   Fig. 14 shows, the steps involved in an etch method, in which the phase difference between the RF signals supplied by the RF power supplies are controlled, either actively or passively, to achieve the desired process results. In step 500, the wafer is prepared for etching in a conventional pre-etch step. The pre-etch steps may include, for example, conventional photolithography steps, clamping the wafer on the chuck, stabilizing the pressure within the plasma processing chamber, and introducing helium cooling gas to the wafer backside to facilitate heat transfer between the wafer and the chuck, among others.

[0044]   In step 502, the phase difference between the RF signals provided by the RF power supplies is controlled, e.g., using the circuit of Fig. 2A. As mentioned earlier, the control may be passive (i.e., to ensure that the phase difference does not vary from a predefined value), or active (i.e., actively control the phase difference to match a user-specified phase difference value). In step 504, at least a portion of one layer of the wafer layer stack is etched while controlling the phase difference. Note that although this step 504 occurs after step 502, control of the phase difference preferably continues during etching. Further, step 504 may be initiated either before, contemporaneous with, or after the initiation of step 502.

[0045]   In step 506, the wafer may undergo additional processing steps to fabricate the desired components as well as post-etch processing steps that are conventional in nature. Thereafter, the finished wafer may be cut into dies, which may then be made into IC chips. The resulting IC chip, e.g., IC chips 140 of Fig. 1, may then be incorporated in an electronic device, e.g., any of the of well known commercial or consumer electronic devices, including digital computers.

Claims

1. A plasma processing system for generating plasma for use in semiconductor fabrication, said plasma processing system having a first radio frequency (RF) power source (404) for outputting a first RF signal to a first electrode (412) and a second RF power source (402) for outputting a second RF signal to a second electrode (418), said second RF power source being coupled to said first RF power source as a slave RF power source in a master-and-slave configuration, said plasma processing system comprising a control circuit, including:

a first sensor circuit (414) coupled to said first electrode for detecting a phase of said first RF signal;
a first matching circuit (410) connected between the first RF power source and the first electrode;
a second sensor circuit (416) coupled to said second electrode for detecting a phase of said second RF signal;
a second matching circuit (408) connected between the second RF power source and the second electrode;
a mixer circuit (420) coupled to said first sensor circuit and said second sensor circuit for detecting a phase difference between said first RF signal and said second RF signal and for outputting a first signal representing said phase difference;
a phase servo circuit (422) coupled to said second RF power source and said mixer circuit, said phase servo circuit outputting, responsive to said first signal and a phase control set point signal (424), a control signal to said second RF power source for modifying a phase of said second RF signal, thereby causing said phase difference to approximate a phase difference value represented by said phase control set point signal;

and **characterised in that**:

the first sensor circuit (414) is connected between the first matching circuit (410) and the first electrode (412);
the second sensor circuit (414) is connected between the second matching circuit (408) and the second elec-

trode (418);
and wherein the first or second electrode represents an upper electrode of said plasma processing system for inductive plasma generation in a plasma processing chamber (406).

2. The plasma processing system of claim 1 wherein said phase control set point signal is a predefined signal.

3. The plasma processing system of claim 1 wherein said phase control set point signal is a user-variable signal to actively control said phase difference.

4. The plasma processing system of any preceding claim wherein said control circuit further comprising:

a bias measurement circuit (440) for measuring a chuck RF peak-to-peak a.c. voltage;
a peak bias control circuit (442) coupled to said bias measurement circuit and a bias set point signal, said peak bias control circuit outputting an error signal to said phase servo circuit for causing said second RF power source, responsive to said control signal from said phase servo circuit, to modify said phase of said second RF signal, thereby causing said chuck RF peak-to-peak a.c., voltage to approximate an RF peak-to-peak voltage represented by said bias set point signal.

5. The plasma processing system of any claims 1 to 3 wherein said control circuit further comprising:

a bias measurement circuit (440) for measuring a d.c. voltage on a wafer being processed in said plasma processing system;
a peak bias control circuit (442) coupled to said bias measurement circuit and a bias set point signal, said peak bias control circuit outputting an error signal to said phase servo circuit for causing said second RF power source, responsive to said control signal form said phase servo circuit, to modify said phase of said second RF signal, thereby causing said d.c. voltage on said wafer to approximate a user input d.c. voltage represented by said bias set point signal.

Patentansprüche

1. Plasmabearbeitungssystem zum Erzeugen von Plasma zur Verwendung bei der Halbleiterherstellung, wobei das Plasmabearbeitungssystem eine erste Hochfrequenz-(RF)-Leistungsquelle (404) zum Ausgeben eines ersten RF-Signals an eine erste Elektrode (412) und eine zweite RF-Leistungsquelle (402) zum Ausgeben eines zweiten RF-Signals an eine zweite Elektrode (418) aufweist, wobei die zweite RF-Leistungsquelle mit der ersten RF-Leistungsquelle als untergeordnete RF-Leistungsquelle in einer Master-Slave-Konfiguration verbunden ist, wobei das Plasmabearbeitungssystem einen Steuerschaltkreis umfasst, der aufweist:

einen ersten Sensorschaltkreis (414), der mit der ersten Elektrode verbunden ist, um eine Phase des ersten RF-Signals zu detektieren;
einen ersten Anpassungsschaltkreis (410), der zwischen der ersten RF-Leistungsquelle und der ersten Elektrode angeschlossen ist;
einen zweiten Sensorschaltkreis (416), der mit der zweiten Elektrode verbunden ist, um eine Phase des zweiten RF-Signals zu detektieren;
einen zweiten Anpassungsschaltkreis (408), der zwischen der zweiten RF-Leistungsquelle und der zweiten Elektrode angeschlossen ist;
einen Mischerschaltkreis (420), der mit dem ersten Sensorschaltkreis und dem zweiten Sensorschaltkreis verbunden ist, um einen Phasenunterschied zwischen dem ersten RF-Signal und dem zweiten RF-Signal zu detektieren und ein erstes Signal auszugeben, das den Phasenunterschied angibt;
einen Phasenstellschaltkreis (422), der mit der zweiten RF-Leistungsquelle und dem Mischerschaltkreis verbunden ist, wobei der Phasenstellschaltkreis in Antwort auf das erste Signal und ein Phasensteuersollwertsignal (424) ein Steuersignal an die zweite RF-Leistungsquelle ausgibt, um eine Phase des zweiten RF-Signals zu modifizieren, wobei **dadurch** bewirkt wird, dass sich die Phasendifferenz an einen Phasendifferenzwert annähert, der durch das Phasensteuersollwertsignal angegeben ist;

und **dadurch gekennzeichnet, dass**
der erste Sensorschaltkreis (414) zwischen dem ersten Anpassungsschaltkreis (410) und der ersten Elektrode (412) angeschlossen ist;

der zweite Sensorschaltkreis (414) zwischen dem zweiten Anpassungsschaltkreis (408) und der zweiten Elektrode (418) angeschlossen ist;

und wobei die erste oder zweite Elektrode eine obere Elektrode des Plasmabearbeitungssystems zur induktiven Plasmaerzeugung in einer Plasmabearbeitungskammer (406) darstellt.

2. Plasmabearbeitungssystem nach Anspruch 1, bei dem das Phasensteuersollwertsignal ein vordefiniertes Signal ist.

3. Plasmabearbeitungssystem nach Anspruch 1, bei dem das Phasensteuersollwertsignal ein benutzervariables Signal ist, um die Phasendifferenz aktiv zu steuern.

4. Plasmabearbeitungssystem nach einem der vorherigen Ansprüche, bei dem der Steuerschaltkreis ferner umfasst:

einen Vorspannungsmessschaltkreis (440), um eine Abgriffs-RF-Spitze-Spitze-Wechselspannung zu messen; ein Spitzenvorspannungssteuerschaltkreis (442), der mit dem Vorspannungsmessschaltkreis und einem Vorspannungssollwertsignal verbunden ist, wobei der Spitzenvorspannungssteuerschaltkreis ein Fehlersignal an den Phasenstellschaltkreis ausgibt, um zu bewirken, dass die zweite RF-Leistungsquelle in Antwort auf das Steuersignal von dem Phasenstellschaltkreis die Phase des zweiten RF-Signals modifiziert, um **dadurch** zu bewirken, dass sich die Abgriffs-RF-Spitze-Spitze-Wechseispannung einer RF-Spitze-Spitze-Spannung annähert, die durch das Vorspannungssollwertsignal angegeben ist.

5. Plasmabearbeitungssystem nach einem der Ansprüche 1 bis 3, bei dem der Steuerschaltkreis ferner umfasst:

einen Vorspannungsmessschaltkreis (440), um eine Gleichspannung auf einem Wafer zu messen, der in dem Plasmabearbeitungssystem bearbeitet wird; ein Spitzenvorspannungssteuerschaltkreis (242), der mit dem Vorspannungsmessschaltkreis und einem Vorspannungssollwertsignal verbunden ist, wobei der Spitzenvorspannungssteuerschaltkreis ein Fehlersignal an den Phasenstellkreis ausgibt, um zu bewirken, dass die zweite RF-Leistungsquelle in Antwort auf das Steuersignal von dem Phasenstellschaltkreis die Phase des zweiten RF-Signals modifiziert, um **dadurch** zu bewirken, dass sich die Gleichspannung auf dem Wafer einer durch einen Benutzer eingegebenen Gleichspannung annähert, die durch das Vorspannungssollwertsignal angegeben ist.

Revendications

1. Système de traitement de plasma pour générer du plasma pour l'utilisation dans la fabrication de semiconducteurs, ledit système de traitement de plasma ayant une première source d'énergie radiofréquence (RF) (404) délivrant un premier signal RF à une première électrode (412) et une deuxième source d'énergie radiofréquence (402) délivrant un deuxième signal RF à une deuxième électrode (418), ladite deuxième source d'énergie radiofréquence étant couplée à ladite première source d'énergie radiofréquence comme une source d'énergie radiofréquence esclave dans une configuration maître-esclave, ledit système de traitement de plasma comprenant un circuit de commande, comprenant :

un premier circuit de détection (414) couplé à ladite première électrode pour détecter une phase dudit premier signal RF ;
un premier circuit d'adaptation (410) connecté entre la première source d'énergie RF et la première électrode ;
un deuxième circuit de détection (416) couplé à ladite deuxième électrode pour détecter une phase dudit deuxième signal RF ;
un deuxième circuit d'adaptation (408) connecté entre la deuxième source d'énergie RF et la deuxième électrode ;
un circuit mélangeur (420) couplé au dit premier circuit de détection et au dit deuxième circuit de détection pour détecter une différence de phase entre ledit premier signal RF et ledit deuxième signal RF et pour délivrer un premier signal représentant ladite différence de phase ;
un circuit d'asservissement de phase (422) couplé à ladite deuxième source d'énergie RF et au dit circuit mélangeur, ledit circuit d'asservissement de phase délivrant, en réponse au dit premier signal et à un signal de valeur de consigne de commande de phase (424), un signal de commande à ladite deuxième source d'énergie RF pour modifier une phase dudit deuxième signal RF, en forçant ainsi ladite différence de phase à approcher une valeur de différence de phase représentée par ledit signal de valeur de consigne de com-

mande de phase ;

et **caractérisé en ce que** :

le premier circuit de détection (414) est connecté entre le premier circuit d'adaptation (410) et la première électrode (412) ;
le deuxième circuit de détection (414) est connecté entre le deuxième circuit d'adaptation (408) et la deuxième électrode (418) ;
et dans lequel la première ou deuxième électrode représente une électrode supérieure dudit système de traitement de plasma pour la génération de plasma par induction dans une chambre de traitement de plasma (406).

2. Système de traitement de plasma selon la revendication 1, dans lequel ledit signal de valeur de consigne de commande de phase est un signal prédéfini.

3. Système de traitement de plasma selon la revendication 1, dans lequel ledit signal de valeur de consigne de commande de phase est un signal variable d'utilisateur pour commander activement ladite différence de phase.

4. Système de traitement de plasma selon l'une quelconque des revendications précédentes, dans lequel ledit circuit de commande comprend en outre :

un circuit de mesure de polarisation (440) pour mesurer une tension alternative crête à crête RF de mandrin (« chuck voltage » en anglais) ;
un circuit de commande de polarisation de crête (442) couplé au dit circuit de mesure de polarisation et à un signal de valeur de consigne de polarisation, ledit circuit de commande de polarisation de crête délivrant en sortie un signal d'erreur au dit circuit d'asservissement de phase pour forcer ladite deuxième source d'énergie RF, en réponse au dit signal de commande provenant dudit circuit d'asservissement de phase, à modifier ladite phase dudit deuxième signal RF, en forçant ainsi ladite tension alternative crête à crête RF de mandrin à approcher une tension RF crête à crête représentée par ledit signal de valeur de consigne de polarisation.

5. Système de traitement de plasma selon l'une quelconque des revendications 1 à 3, dans lequel ledit circuit de commande comprend en outre :

un circuit de mesure de polarisation (440) pour mesurer une tension continue sur une galette qui est traitée dans ledit système de traitement de plasma ;
un circuit de commande de polarisation de crête (442) couplé au dit circuit de mesure de polarisation et un signal de valeur de consigne de polarisation, ledit circuit de commande de polarisation de crête délivrant en sortie un signal d'erreur au dit circuit d'asservissement de phase pour forcer ladite deuxième source d'énergie RF, en réponse au dit signal de commande provenant dudit circuit d'asservissement de phase, à modifier ladite phase dudit deuxième signal RF, en forçant ainsi la tension continue sur ladite galette à approcher une tension continue entrée par l'utilisateur représentée par ledit signal de valeur de consigne de polarisation.
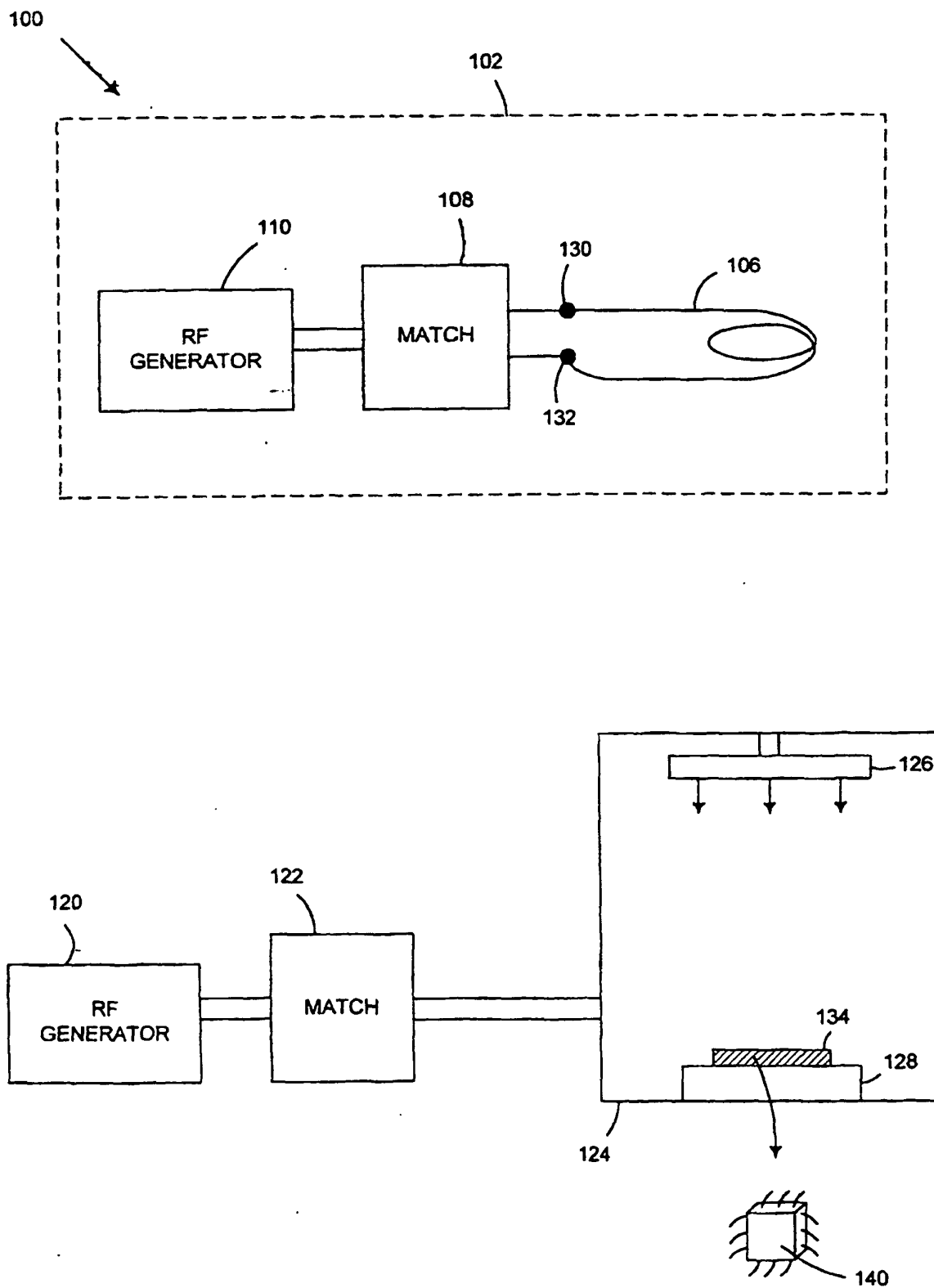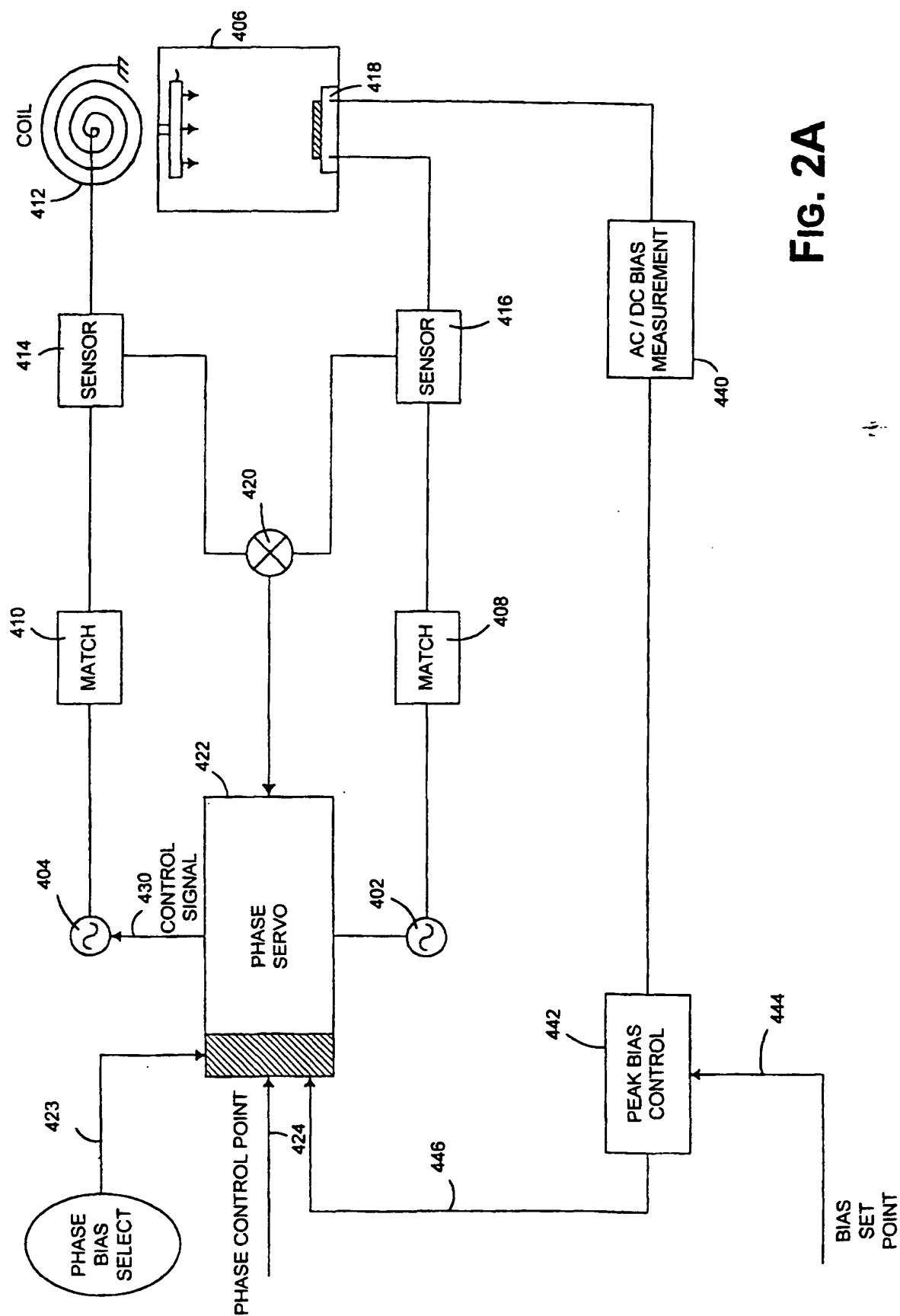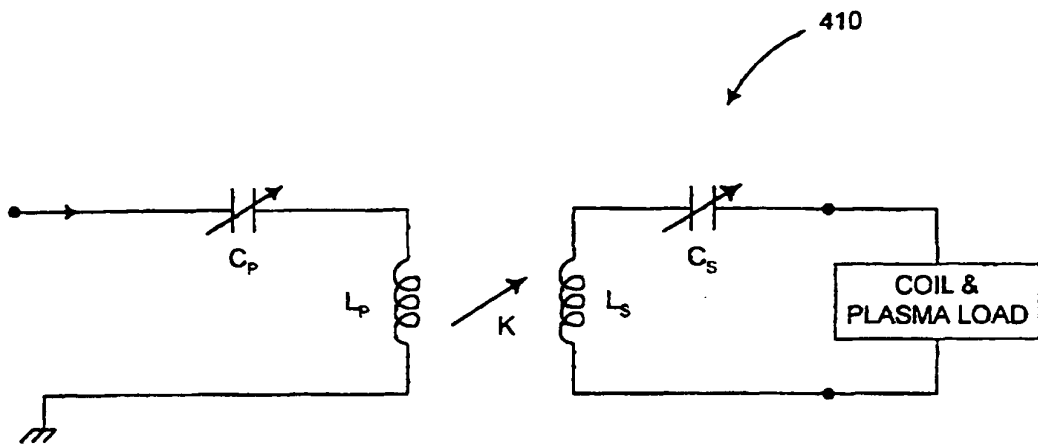
100

102

110
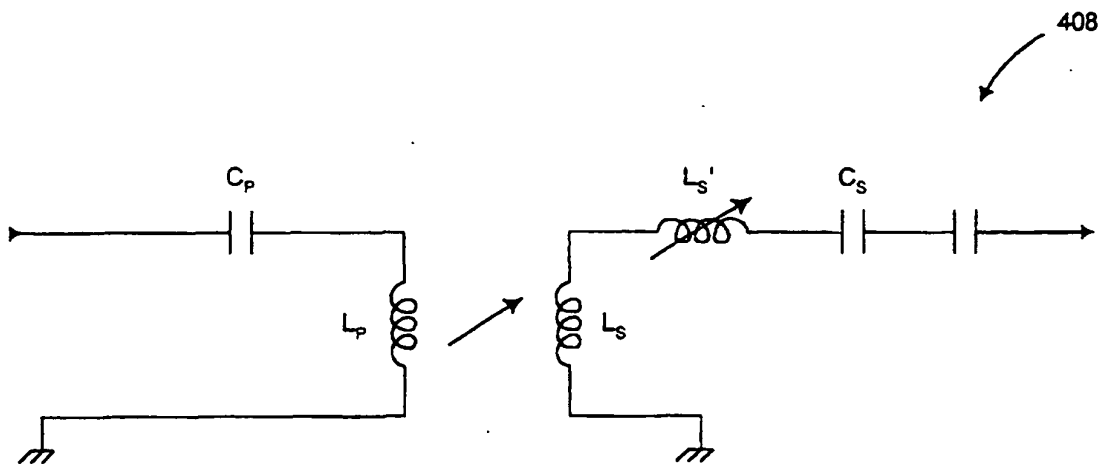
108

130

106

RF
GENERATOR

MATCH

132

120

122

126

RF
GENERATOR

MATCH

134

128

124

140

FIG. 1

FIG. 2A

410

C_P

L_P

K

C_S

L_S

COIL & PLASMA LOAD

FIG. 2B

408

C_P

L_P

L_S'

C_S

L_S

FIG. 2C

460

462

476

470

474

472

FIG. 2D

OPTICAL AMPLITUDE VS. PHASE SHIFT

FIG. 3

ELECTRODE P-P VOLTAGE VS. PHASE SHIFT

FIG. 4

FIG. 5

FIG. 6B

OXIDE ETCH RATE VS. PHASE SHIFT

FIG. 6A

ALUMINUM/OXIDE SELECTIVITY VS. PHASE SHIFT
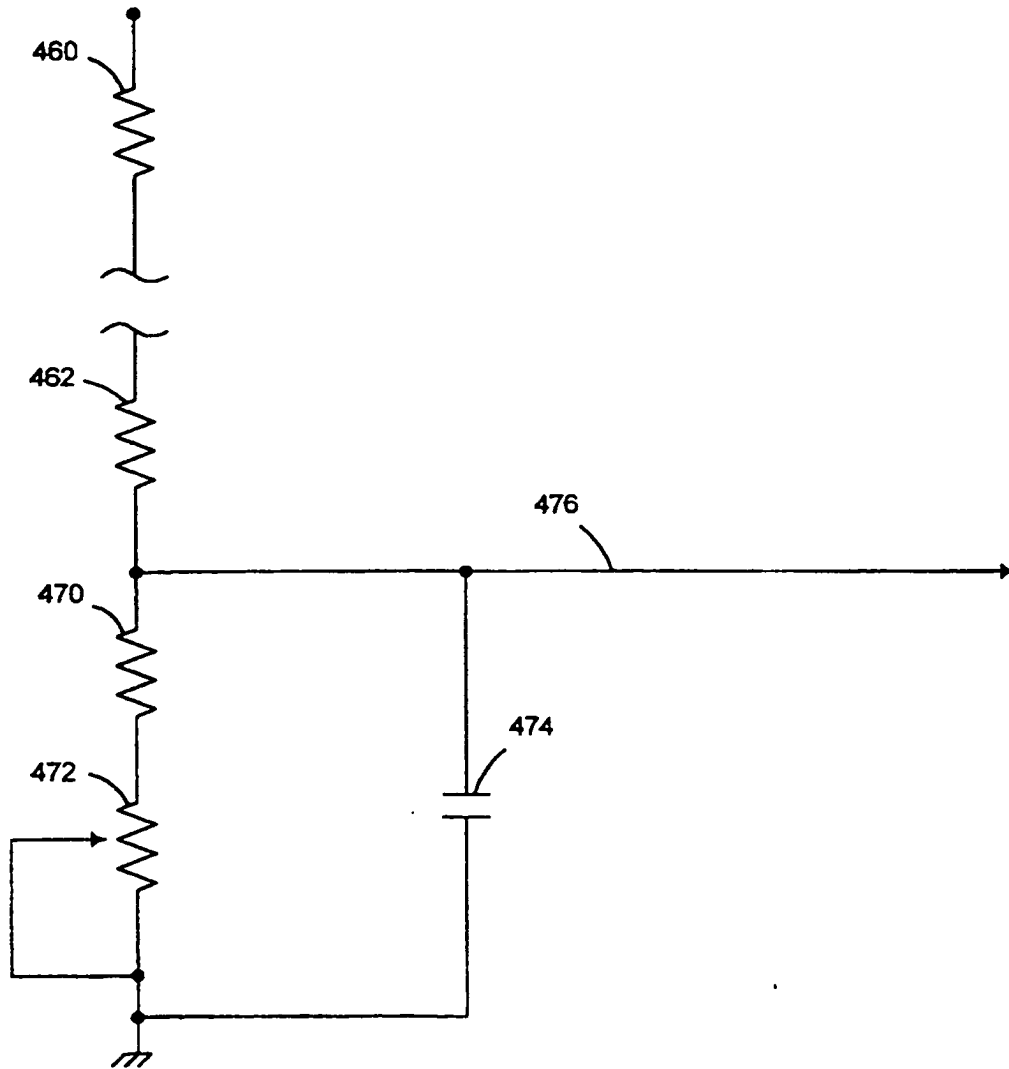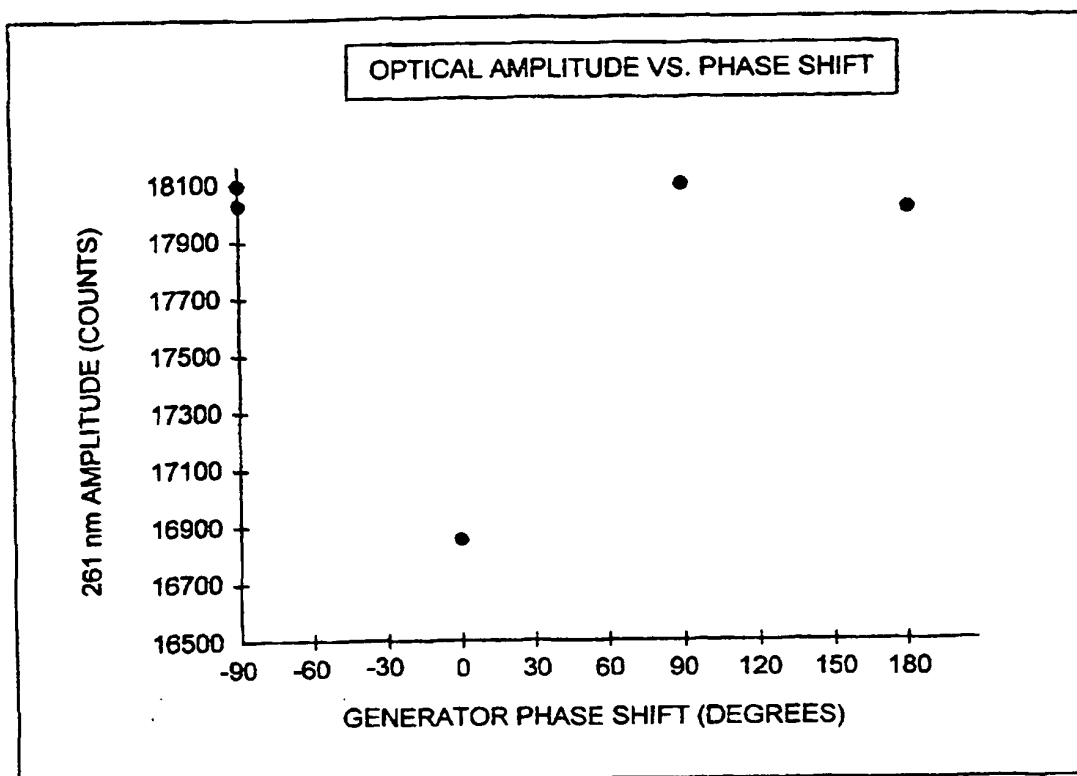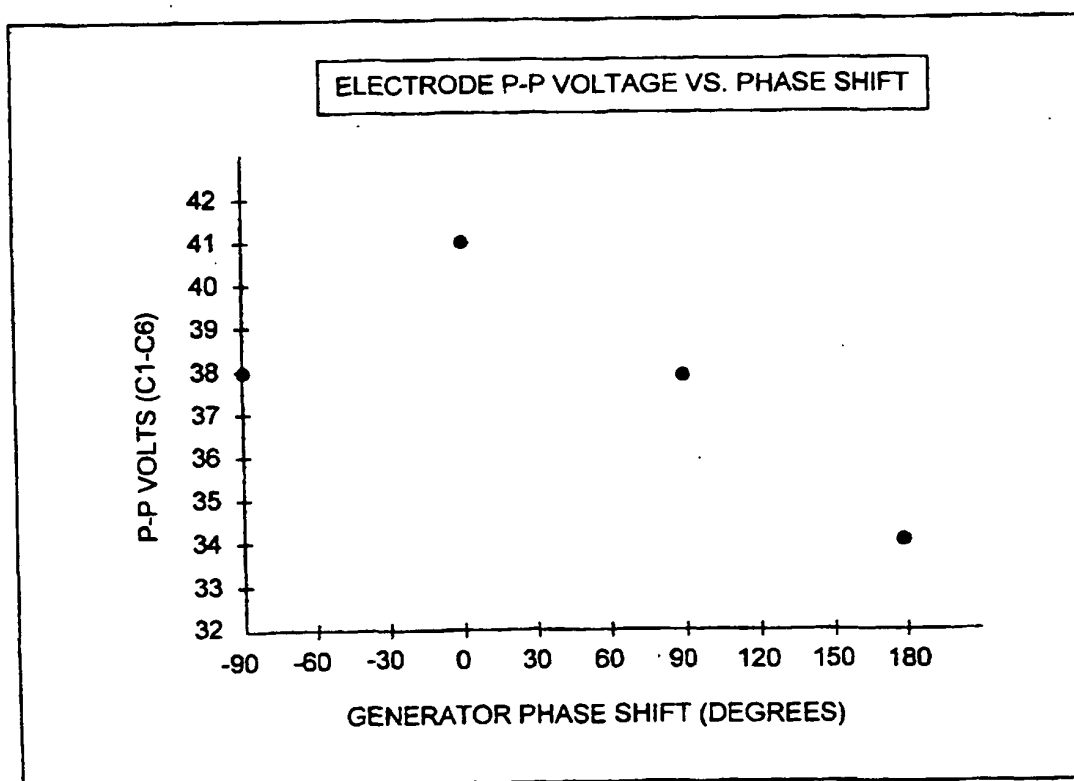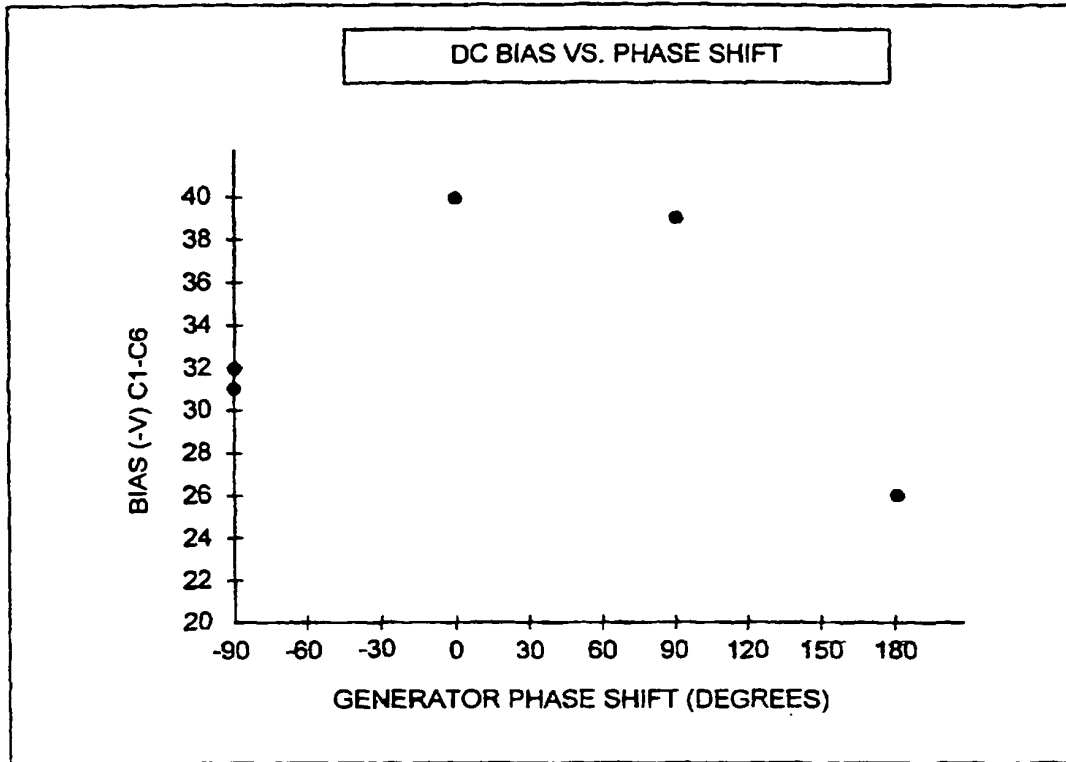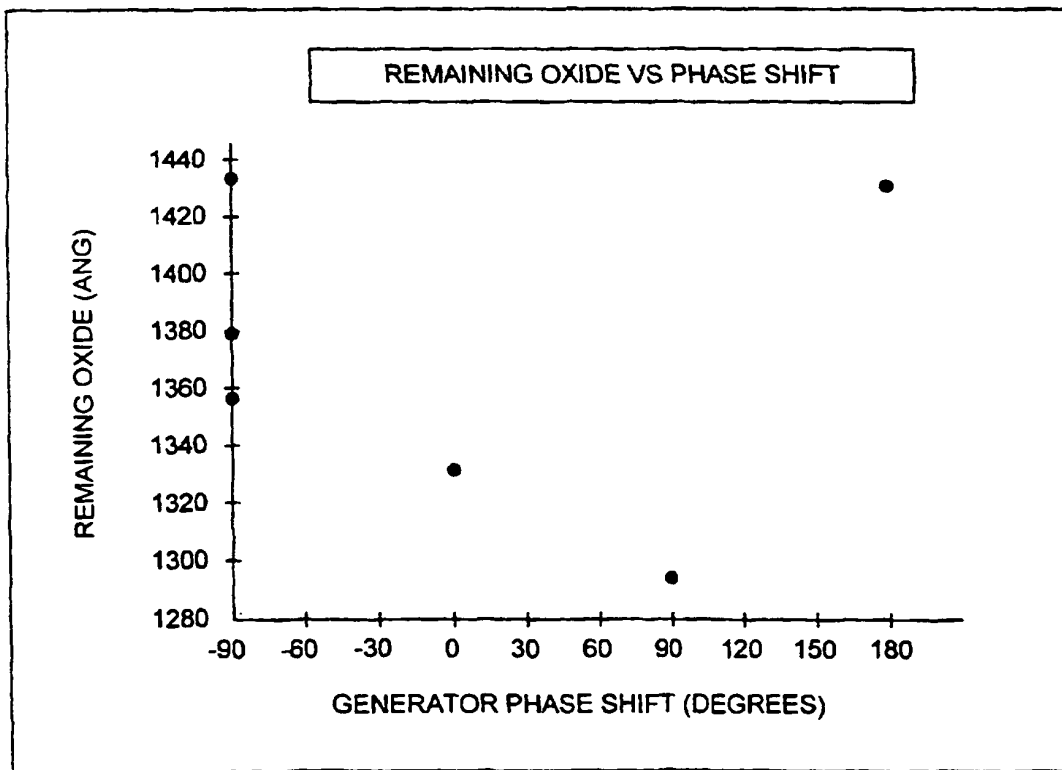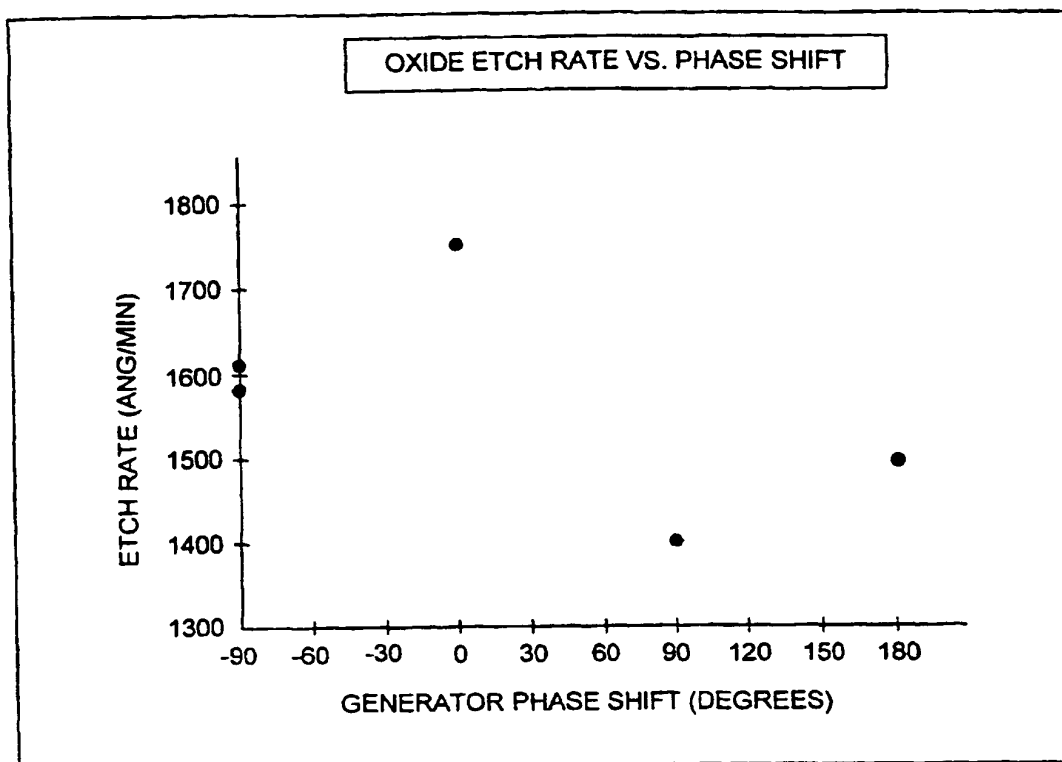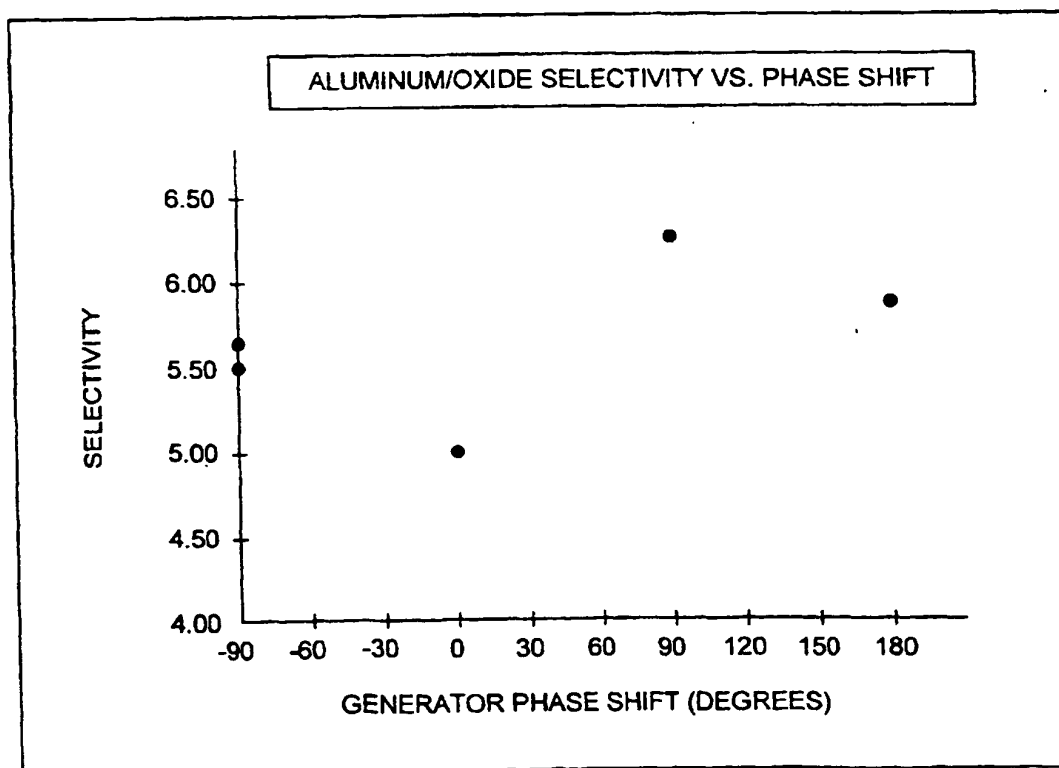
FIG. 7

FIG. 8

FIG. 9

FIG. 10

FIG. 11

CD (CENTER) VS. PHASE SHIFT

FIG. 12

CD (EDGE) VS. PHASE SHIFT

FIG. 13

500 — PRE-ETCH PROCESSING

502 — CONTROLLING PHASE DIFFERENCE BETWEEN PHASES OF RF SIGNALS PROVIDED BY RF POWER SUPPLIES

504 — ETCH AT LEAST A PORTION OF LAYER STACK

506 — POST-ETCH PROCESSING

FIG. 14