

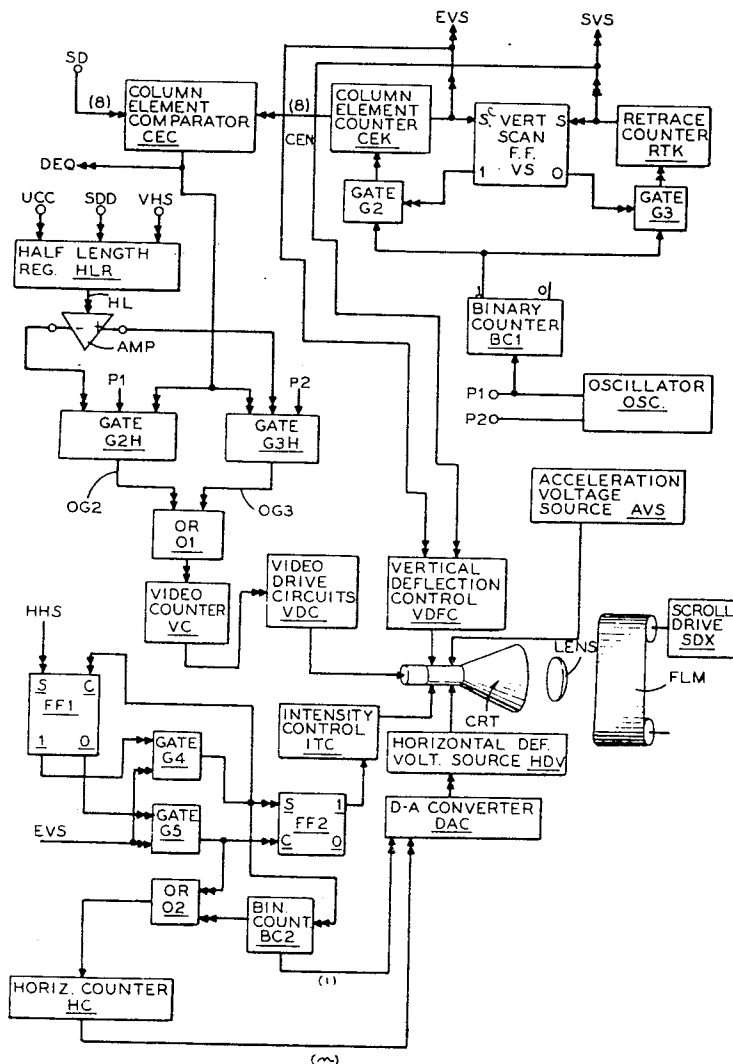
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Sands Point, N.Y.
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[45] Patented Sept. 28, 1971
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[56] References Cited
UNITED STATES PATENTS
3,422,420 1/1969 Clark..... 315/22 X
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[54] **DUAL RESOLUTION GRAPHIC SYMBOL GENERATOR**
15 Claims, 4 Drawing Figs.

[52] U.S. Cl..... 315/18,
315/22, 340/324 A
[51] Int. Cl..... H01j 29/70
[50] Field of Search..... 340/324.1;
315/18, 22, 31

ABSTRACT: A graphic symbol generator includes a cathode-ray tube assemblage disposed opposite a photosensitive film. The electron beam of the cathode-ray tube assembly while being driven in a raster scan mode, is intensity modulated in accordance with stored coded combinations of binary signals which represent the graphic symbol. Provisions are made to control the line density or resolution of the scan in two dimensions during the generation of the graphic symbol as an array of parallel line segments.



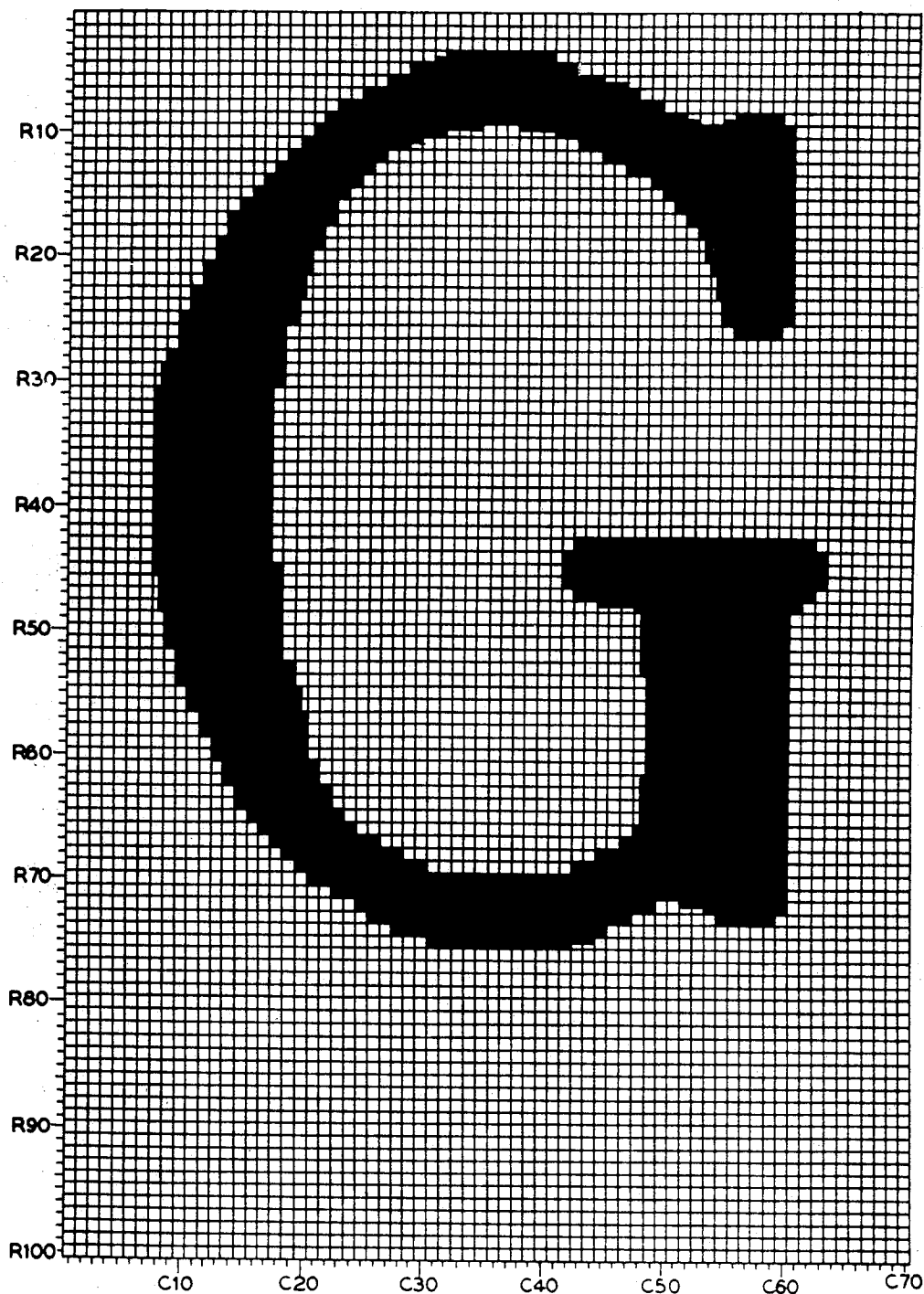


FIG. 1

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BY

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FIG. 2A

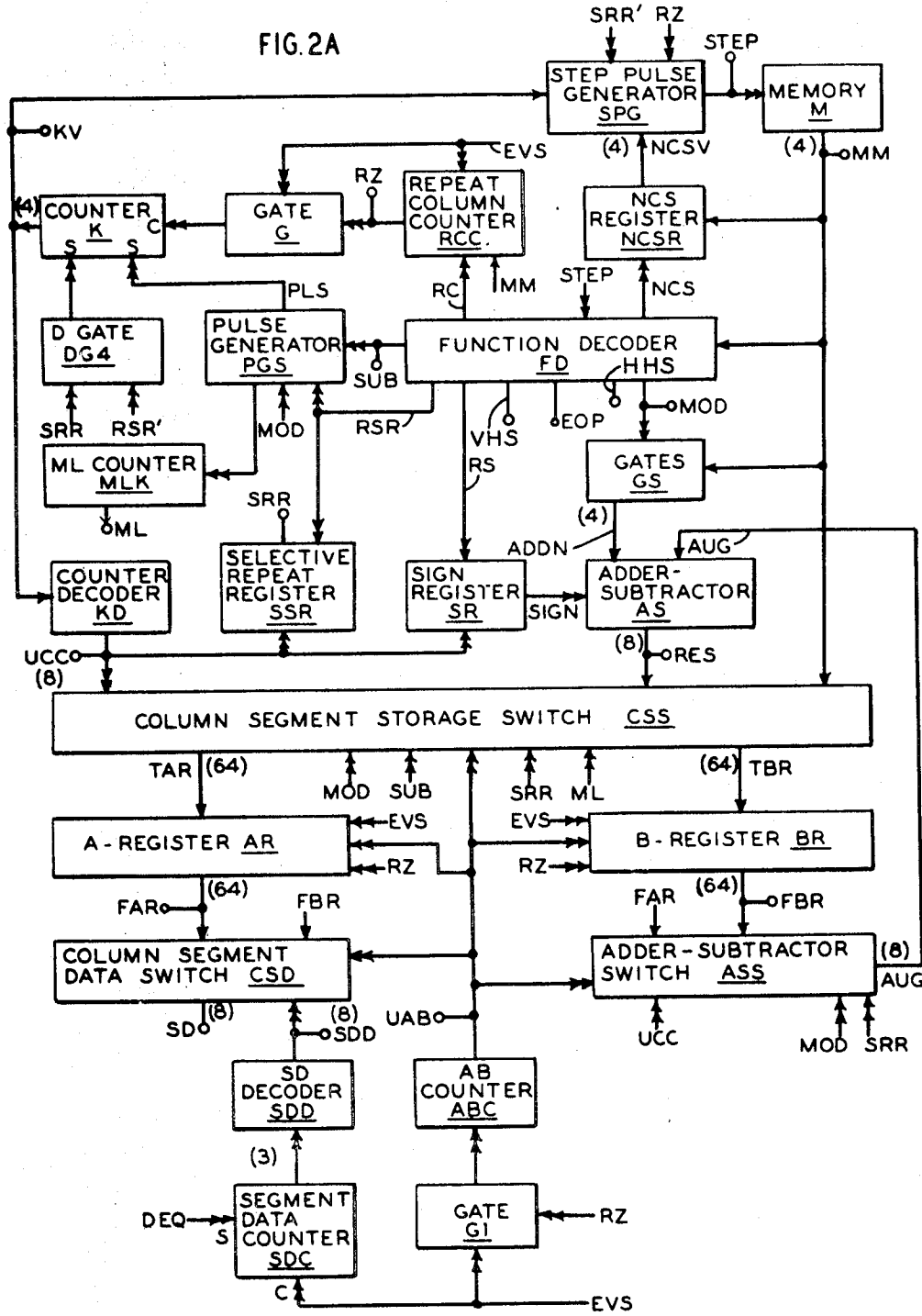
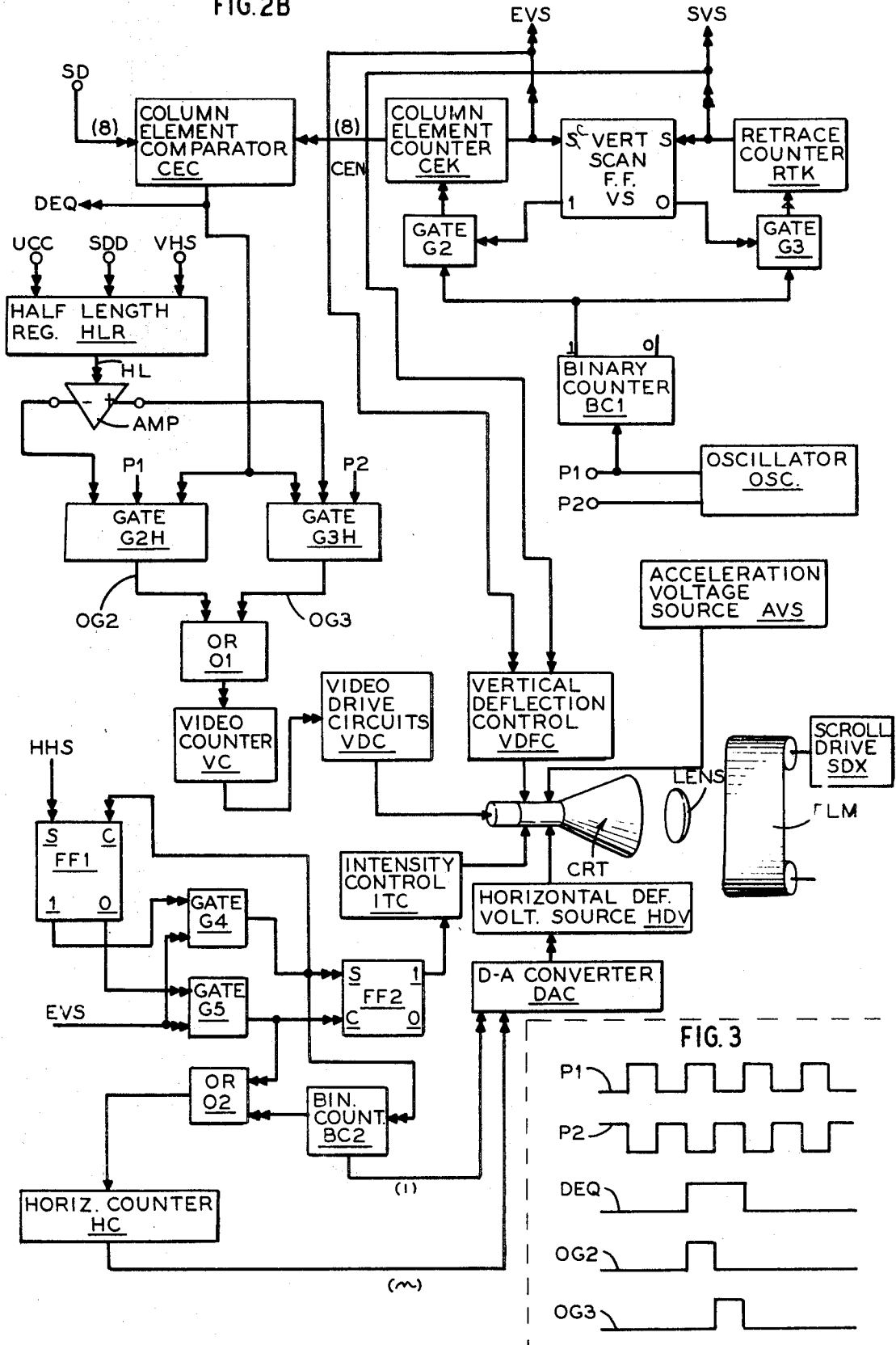


FIG. 2B



DUAL RESOLUTION GRAPHIC SYMBOL GENERATOR

This invention is related to graphic symbol generators and more particularly to the generation at a very high speed of high-quality graphic symbols such as characters, numbers ideograms or other symbols which convey information for recording on a record medium.

Graphic symbol or pattern generators have many applications such as display devices, computer output devices, etc. Of these applications the ones which produce the greatest amount of end result output are character generators used in the graphic arts and printing fields. Although these fields are very old the best automated line casting machines available today are electromechanical devices which can produce 15 to 20 characters per second.

In order to increase the rate of generating characters, there have been attempts to utilize light beams and photosensitive films. Some early approaches were to use the controlled trace of a cathode-ray tube which was driven by figure eight bar generators which produced intelligible symbols by appropriate combinations of barlike or even curved elements. However, such characters in no way approached the quality of the characters produced by conventional metal-type slugs. Vector generators were also employed to drive the cathode-ray tube beams with a slight improvement in quality.

About fifteen years ago a cathode-ray tube was introduced which included a stencil of a plurality of characters equivalent to a degenerate-type font. The electron beam was first aimed on the region of the stencil having the outline of the character selected for output and further deflection circuits deflected the beam to the desired position on the face of the tube. Although the quality of the output characters greatly improved, only one type font was available per tube. In addition, the circuits and the stencils are relatively expensive. Other cathode-ray tube devices used the stencils but external optical systems deflected the selected character to the desired place on the record medium.

Other approaches included a multicharacter stencil having controllably ignitable light sources behind each character outline with optical focusing to direct the image to a particular portion of the output media. However, the proposal suffered from all the defects of the cathode-ray tube stencil systems and was even more expensive.

A further approach included the video scanning of a stencil and using the video signal to intensity modulate the beam of a cathode-ray tube. Such a system demanded very precisely engraved stencils which are prohibitively expensive to initially fabricate and to reproduce.

The field has tried dispensing with mechanical stencils and has tried using prewired control circuits and magnetic core matrices, one per character, to generate patterns of signals to intensity modulate a cathode-ray tube beam. However, the prewired control circuits and core matrices are exorbitantly expensive when high-quality characters are required.

An improvement on these systems is disclosed in U.S. Pat. No. 3,165,045, for a Data Processing System wherein each character is represented by a plurality two-valued (black or white) elements in a matrix array. A storage means stores the representations of the characters as bits, with one bit per element. The bits are fed serially to a light source which scans a photographic medium. The bits intensity modulate the light source. Since the bits are stored on an addressable magnetic drum, the disadvantages of the prewired matrix are not present. However, this system is merely an electromagnet version of a conventional dot printer. Such printers are notorious for their inability to produce graphic arts quality characters. Such quality requires a very finely divided matrix array, for example, an array of 70 columns and 100 rows, or 7,000 elements per character. Therefore, it is necessary to store 7,000 bits per character.

In order to minimize the number of stored bits per character, there is disclosed in U.S. Pat. No. 3,305,841, for a Pattern Generator, a system utilizing coded combinations of indicia or bits. In particular, it discloses a system wherein each

character is divided into linear regions. Within each region is a line segment. The stored indicia (bits) are in groups of coded combinations of indicia which indicate the starting and ending points or addresses of the line segments in each linear region. With such a system, in the worst case, the number of bits required to represent a character is compressed, vis-a-vis the system of U.S. Pat. No. 3,165,045, by a factor of 3, and in the average case the compression is fivefold. While such a compression is extremely valuable, it has created a demand for even greater compressions.

Greater compressions are disclosed in application Ser. No. 572,609, filed Aug. 15, 1966, for a Pattern Generator, and assigned to the same assignee. In that application it is only necessary to state in full the starting and ending "addresses" of the line segment of a first linear region since the starting and ending addresses of the line segments of subsequent linear regions are obtained by incrementing the addresses of the line segment of the first linear region. Since the increments are small numbers, they can be represented by smaller coded groups of indicia than those representing the full addresses.

Since the goal of the Pattern Generator patent and the application is to produce Graphic Art's quality output it is necessary to have a resolution in excess of 500 lines (columns and rows) to the inch. Assume, that 800 lines per inch provides in most cases the desired esthetic appeal. However, it has been found that when the slope of the tangent to the peripheral edge of a graphic symbol either approaches zero or infinity, greater resolution is desired. The immediate answer is to increase the resolution to, say, 1,600 lines per inch. Such an approach would provide a graphic symbol having the desired visual esthetic but would quadruple the amount of information required to define the graphic symbols.

It is an important object of the invention to provide apparatus which generates high-quality graphic symbols having esthetically pleasing contours from a minimum amount of information.

It is another object of the invention to provide a graphic symbol generator wherein the symbols are built up from an array of adjacent lines wherein the line resolution is controllably changeable during the generation of each symbol.

Briefly the invention contemplates a system for presenting a graphic symbol (alphabetic or numeric character, ideogram or other symbol used to convey information) to a record medium. The graphic symbol includes an area divisible into linear regions. Each linear region has a given width dimension and is also divisible into a plurality of length elements, each having a given length dimension. In each linear region there is at least one contiguous array of length elements having a first visual state and the remaining length elements having a second visual state. In the system there is a storing means for storing a symbol block which is a representation of the graphic symbol. The symbol block includes a plurality of blockettes, each associated with one of the linear regions of the graphic symbol. Each blockette includes at least one coded group of indicia for indicating the position and extent of the contiguous array of length elements in the linear region. There is also stored at least one dimension control indicium associated with at least one particular linear region to control at least one of the dimensions of that region. Scanning means are provided for scanning the record medium in a linear manner wherein each scan is associated with a linear region of the graphic symbol. First, control means direct the scanning means to move transversely to the direction of the scans, before the start of a scan, by a distance related to at least the given width dimension of one linear region. Second, control means, which is responsive during each linear scan to the coded group of indicia of the associated blockette selectively energizes the scanning means during the scan for a period of time related to the contiguous array of length elements so that the portion of the record medium then being scanned manifests a representation of the first visual state whereby a line having a length related to the number of length elements of the contiguous array is traced on the record medium. Means responsive to the dimension con-

trol indicium cause one of the control means to change the dimensions of the trace of the record medium associated with the particular linear region.

These features and other objects and the advantages of the invention will be apparent from the following detailed description when read with the accompanying drawings which show, by way of example and not limitation, representative apparatus for realizing the concepts of the invention.

In the drawings:

FIG. 1 shows in detail a character superimposed on a coordinate system for explaining the invention;

FIGS. 2a and 2b show a block diagram representation of a system for generating patterns or graphic symbol on an electromagnetic radiation sensitive medium; and

FIG. 3 shows waveforms of signals generated by certain of the elements of the system.

In general, the system can generate a line of graphic symbols at a time wherein the symbols are serially generated along the line. When one line is completely generated, the system can start generating the next line of symbols. The lines of symbols will, in being generated, energize a source of electromagnetic radiation such as light source which creates visual representations of the symbols for exposure onto an electromagnetic radiation or light-sensitive medium such as a photographic film. The film thereafter can be used as a negative for creating printing plates. Therefore, each symbol will be recorded on an area of one visual state such as one color (for example, white) hereinafter called a second visual state, and the symbol, per se, will comprise line portions in another visual state such as a contrasting color (for example, black).

Not only can the symbols be generated serially along a line, but each of the actual symbols is generated by a plurality of serially generated lines, such as columns of contiguous line elements, hereinafter, called column elements.

FIG. 1 shows by way of example a greatly enlarged version of a 12 point upper case G, a typical graphic symbol. This character will now be analyzed. It is seen that it occupies the region between columns C8 and C63, and between rows R4 and R75. However, it should be noted that columns C5, C6 and C7 are blank. Similarly, columns C64, C65 and C66 are blank. These columns are space columns to the left and right of the pattern columns C8 to C63 inclusive. Each column can be called a linear region and has the same width. A pattern column is a column of the character slug which includes at least one "black" element. Accordingly, the columns defining the 12-point G include three blank columns followed by 56 pattern columns followed by three blank columns.

Now consider some typical pattern columns. Column C10 scanned from top to bottom comprises an area of "white" extending from row R1 to row R24, an area of "black" extending from row R25 to row R54, and an area of "white" from row R55 to row R100. It can also be said that column C10 includes a contiguous array of column elements; i.e., 30 column elements, wherein each column element has a length equal to the distance between two rows. Column C35 comprises a first area of white extending from row R1 to row R3, a first area of black extending from row R4 to row R9, a second area of white extending from row R10 to row R69, a second area of black extending from row R70 to row R75, and a third area of white extending from row R76 to row R100. Column C44 has three areas of black interspersed between four areas of white. If any area of black within a pattern column is defined as a column segment, (a contiguous array of column elements) it is seen that each pattern column includes at least one column segment. In fact, it has been found that the majority of available type font styles have characters which comprise no more than four column segments, or contiguous arrays column elements.

It is also possible to analyze the character by means of rows. In such a case each pattern row will have at least one row segment. The invention contemplates both types of analysis and the claims employ the generic word "line" to mean either "row" or "column."

From the above analysis of the columns it is possible to establish a method of defining the pattern within the column. In particular, it is only necessary to indicate the starting row of an area of black or column segment and to indicate the ending row of the column segment. Alternatively, it can be said that it is only necessary to indicate the position of the column elements at the start and end of the column elements. Accordingly, the pattern in column C8 can be defined as a column segment starting at row R31 and ending at row R45. The column segment of the next column, column C9, starts at row R28 and ends at row R51. Similarly, the pattern of column C35 can be defined as: a first column segment starting at row R4 and ending at row R9, and a second column segment starting at row R70 and ending at row R75. The pattern of column C44 would be similarly defined. Therefore, any pattern column can be defined with four groups of two sets of information, wherein the first set indicates a starting element address (the row address of the column element at the start of the contiguous array of column elements) and an ending element address (the row address of the column element at the end of the contiguous array).

It is also possible to define the pattern within a column by a starting element address along with a quantity indicating the number of column elements in the contiguous array. It should be noted that this quantity indirectly defines an ending element address. While the invention contemplates either method, the starting and ending address method will be used as an example.

Returning now to the starting and ending address method, it is also possible to define the starting and ending element addresses of the column segment of column C11 by incrementally modifying the starting and ending element addresses of the column segment of column C10. In particular, the starting element address R25 of column C10 can be changed by an incremental value of -2 to obtain R23, the starting element address of column C11. Similarly, the ending element address R55 of column C10 can be changed by the incremental value +2 to obtain the ending element address R56 of column C11. Thus, the incremental values indirectly define the starting and ending element address of column C11. The system will be described using the incrementally modifying of address technique. However, the invention is equally applicable to the technique of specifying full starting and ending addresses.

A study of FIG. 1 reveals several interesting phenomena. There is one column segment for columns C8 through C17, two column segments for columns C18 through C41, and three column segments for columns C42 through C48, two column segments for columns C49 through C60 and one column segment for columns C61 through C63. In addition, the columns with the same number of column segments are generally in adjacent groups of columns. Therefore, the system will be described with the coded combination of indicia associated with a column preceded by a coded combination of indicia representing the number of column segments in the column.

In FIG. 1 it can also be seen that there are a large number of incremental changes between adjacent column segments, but there are only about eleven changes in sign or the direction of the incremental change. See, for example, the transitions between columns C40 and C41, between columns C55 and C56, and between columns C60 and C61. Hence, if each coded group of indicia representing an increment has associated with it a sign indication, more information is required to represent the character. However, to achieve further compression, each coded group of indicia representing an increment actually represents the magnitude of the increment, and, wherever appropriate, coded indicia is imbedded in the flow of coded combinations of indicia from the storing means to indicate a change in the direction (sign) of the increment.

There are adjacent columns having column segments with the same starting and ending element addresses, such as columns C34 or C37. In other words, these column segments have no increments. If these zero increments are represented

by coded groups of indicia, more information than necessary is required to represent the character. In order to minimize the amount of information after the transfer from the storing means of the coded combination of indicia associated with a column which precedes a group of columns having zero increments, there is transferred a coded combination of indicia indicating that the last starting and ending element addresses are to be repeated a given number of columns.

All of these code compression concepts were disclosed and fully described in above cited application, Ser. No. 572,609 and are presented here by way of background and to facilitate the description of the operation of the system.

The present invention is concerned with the smoothness of the peripheral edges of the generated symbols. In order to point up the improvement in the esthetics, only certain portions of the generated character of FIG. 1 are modified according to the invention while the remainder of the character is left unchanged over the same character as generated according to the techniques of U.S. Pat. No. 3,305,841 and of U.S. application, Ser. No. 572,609.

Normally, the column segment of column C8 starts at row R31 while the column segment of column C9 starts at row R28. The slope of the tangent to the peripheral edge of the character in this region approaches infinity. It had been found that an unpleasing edge was recorded at this point until a modification according to the invention had been introduced. Note the region around column C19 and row R26 which has not been modified according to the concepts of the invention still shows the pronounced step. However, according to the invention column C8 is split into two half columns. The first (left) half has starting and ending addresses of R31 and R45, respectively, and the second (right) half has starting and ending address of R29 and R48, respectively. As can be seen, the curve is much smoother. The same technique is also used for columns C20, 48, 53 and 54. The technique should also be used for columns C18 and C19 but it has not been used to point up the differences in the visual esthetics.

Now consider region around row R70 between columns C31 and C42; here the tangent to the peripheral edge of the character has a slope approaching zero and the edge itself is flat over a considerable range. Such a condition is esthetically unappealing. However, now consider the region around row R10 between columns C32 and C40. Before modification, this region was the same as the region around R70. This region was modified as follows: for columns C32, C33, C34, C38, C39 and C40, modified column elements associated with row address R10 were added. These modified column elements instead of having the usual length dimension, is the distance between two rows, have half the usual length dimension. The same technique has been employed at column C29, row R11; column C31, row R4; columns C32, C33, C34, C38, C39 and C40 at row R10, column C43, row R75; column C44, row R75; column C45, row R6; column C46, row R6; column C45, row R48, column C46, row R48; column C47, row R48; column C52, row R9; column C52, row R72; column C53, row R72; and column C55, row R9.

While such a technique requires more information to define the character, it only occurs at a minority of the points and achieves the same esthetic appeal as doubling the row and column resolution without the penalty of quadrupling the amount of information to be stored. In fact, the resolution is only doubled when required.

Referring to FIG. 2, there will now be described a system for executing the above-described inventive concepts.

The system generates patterns by modulating the intensity of an electron beam as it sweeps across the inside of the face of a cathode-ray tube to excite the phosphor thereon. The electron beam is driven to scan in a rasterlike manner; i.e., there are sequential vertical (column) scans which are incrementally displaced from each other in a horizontal direction. Of course, the horizontal and vertical directions can be interchanged. However, columnar (vertical) scans are more desirable when the patterns are actually a line of characters.

In particular the electron beam is controllably turned on and off during each column scan, when the beam is on the region of the phosphor is excited to emit light.

As has been discussed above, each pattern column has a plurality of equal line or column elements and has at least one distinct line segment of contiguous column element. The line segments have start and end point or column elements. The electron beam, during each scan, is turned on at a time related to the start point and off at the end point of each line segment in each column of the pattern.

In order to determine the electron beam turn-on and turnoff times each column scan is divided into a plurality of equal time increments. Since the column scan is a linear function of time, each time increment is equal to an element in the column on the face of the cathode-ray tube. Therefore, by equating the elements on the face of the cathode-ray tube with the column elements in the pattern, the elements of the pattern are mapped onto the face of the cathode-ray tube. Now, by storing in registers the "addresses" of the start and end elements; i.e., the number of column elements from a base point of each line segment of a column of the pattern or graphic symbol and by counting the number of time increments (elements) elapsing in a column scan from the start of the column sweep by the cathode-ray tube the desired result is obtained. For example, when the number of counted time increments equals the stored address of the start element (start element address) of the first line segment in the column, the electron beam is turned on and when the time increment count equals the address of the end element (end element address) of the first line segment, the electron beam is turned off. If there is a second line segment in the column, the electron beam is turned on and off in a similar manner for the second line segment. After the column has been scanned, the registers are updated for the next column by any combination of the following methods:

1. The start and end element addresses in registers can be replaced by new start and end element addresses received from a memory; or
2. The start and end element addresses in the registers can be modified by combining them algebraically with incremental data obtained from a memory;
3. The start and end element addresses in registers can be explicitly repeated without modification. Either all element addresses can be repeated or only selected addresses repeated while the others are replaced or modified.

Several system parameters are worth noting before describing the system. All words, whether data or code (control), are transferred from the memory as 4-bit bytes (words) in parallel. Every starting and ending element address is an 8-bit byte. Therefore two words are required to transfer an address from the memory. Every increment is a 4-bit byte with the most significant bit always being zero. Therefore, the incrementing can only extend to eight column elements. There is also assumed to be a maximum of four line segments per column (or four pairs of start and end element addresses).

The following table indicates the types of words transferred from the memory.

Decimal Value	Binary Code	Mnemonic	Comments
0	0000		Data
1	0001		Data
2	0010		Data
3	0011		Data
4	0100		Data
5	0101		Data
6	0110		Data
7	0111		Data
8	1000	HHS	Half Increment a column
9	1001	VHS	Half Increment a column element
10	1010	SUB	Substitute New Value

Table - Continued

			Load Column Segment Counter
11	1011	NCS	Register
12	1100	RC	Load Repeat Counter
13	1101	RS	Reverse Increment Sign
14	1110	RSR	Reverse Selective Repeat
15	1111	EOP	End of Pattern

Only memory data words assume values from zero to seven. The operation codes or code words have values between eight and 15. The operation codes have the following meanings.

The HHS code indicates the next column has only one-half the width of a normal column. The VHS code indicates that a column element has only one half the length of the usual column element. The SUB code indicates that the next two words from memory are data words which are to be combined to form a new start or end element address for a line segment. The NCS code indicates that the next word from memory represents twice the number of line segments in a column. The RC code indicates that the next word from memory represents the number of pattern columns which are to be generated by repeating the last previous values entered prior to this operation. The RS code indicates that the direction of incrementing for one of the start or end element addresses of one of the line segments is to be changed. The RSR code controls the repeating of a selected start or end element address. The EOP code indicates the end of the data for the pattern.

The data has one of the following meanings:

DS = Start address increment
DE = End address increment
SM = Most significant half of a start

address SL = Least significant half of a start

address EM = Most significant half of an end

address EL = Least significant half of an end

address RCV = Repeat value
NCSV = Number of column segments value

The various units of the system will now be described with reference to FIG. 2.

It should be noted that signal names and the lines carrying the signal have the same reference designation. For example, the MOD signal is transmitted on the MOD signal line. Generally, the "positive" or "high" signals are shown or mentioned. However, most of the signals also have a complementary signal. For example, the AB flip-flop transmits, form its two outputs, two signals, respectively, in parallel, the UAB and UAB' signals. When the UAB signal is "high" the UAB' signal is low, and vice versa. When specifically required, both the signal and its complement are shown and mentioned. In addition, many of the lines which carry data are shown as a single line, for example, the TAR signal line. This line is actually a cable of 64 lines, TAR1 to TAR64. For simplicity, only the single line cable is shown. However, when required the cable is fanned out and the specific lines therein are given their appropriate suffix numbers. Numerals shown in parentheses adjacent to lines indicate the actual number of lines in the cable.

The memory M can be a magnetic core memory with suitable address selection and control circuits. The memory delivers 4-bit parallel words to four output lines MM1 to MM4 (shown as line or cable MM) in response to step pulses received from the step pulse generator SPG. Each step pulse causes the memory to output one word.

There is a control unit comprising a decoder FD, pulse generator PGS, and an update control counter. The decoder FD is used to generate control signals in response to code words received from memory M. The decoder FD can comprise four paraphase amplifiers having inputs connected to the

four MM signal lines, respectively. The outputs of the amplifiers are connected to inputs of a binary-to-hexadecimal decoder. The outputs of this decoder are connected via gating logic, to the set inputs of flip-flops which generate the control signals, RC, NCS, RSR, RS, SUB, VHS, HHS and EOP. The positive output of the paraphase amplifier connected to the most significant bit line MM4 drives a flip-flop for the MOD signal. However, provision is made to insure that the MOD signal does not occur for the data word following the code words RC and NCS and the two data words following the SUB code word. This can be done by feeding the MOD signal to an input of a gate having other inhibiting inputs connected to the RC, NCS and SUB signals.

The flip-flops are cleared by using a circuit employing gating logic, a counter and a delay device which responds to the pulses on line STEP. Each of the flip-flops, except the one generating the SUB signal, is cleared after the next step pulse. That flip-flop is cleared after the second next step pulse.

The pulse generator PGS which is used to step the counter K is basically two channels of one-shot multivibrators. In the first channel, the MOD and RSR signal lines are connected to the input of a first one-shot multivibrator which delivers a pulse from its output a given period of time after it receives a signal at its input. This output PLS is connected to the step input S of counter K. The SUB signal line is connected to the input of a second one-shot multivibrator which delivers a pulse from its output the given period of time after it receives a signal at its input. The output of the second multivibrator is connected to the input of a similar third one-shot multivibrator. The outputs of the second and third one-shot multivibrators are connected via another OR circuit to the input of a most-least counter MLK. This counter is a one-stage binary counter having an initial clear input (not shown) for setting it to a zero state at the start of operation. The counter delivers an output to the ML signal line. The counter is used to keep track of the most and least significant halves of start and end addresses during the SUB operations. The output of the third one-shot multivibrator is also connected to the step input of counter K. Whenever the MOD signal is present the pulse generator PGS delivers a pulse on the PLS signal line after the given period of time from the start of the MOD signal. Whenever the SUB signal is present the pulse generator delivers a first pulse to the counter MLK (which changes state) after the given period of time and a second pulse to that counter MLK. The second pulse is also transmitted via the PLS signal line to step counter K the given period of time after the first pulse. The time delay is required to insure that all required memory transfers are completed before indexing the counter K since this counter is to control the suspension of memory transfers.

The update control counter basically keeps track of the start or end element address being considered at any one time. For example, when the counter has a count of zero it indicates the start element address of the first line segment in a column, a count of one indicates the end element address of the first line segment, etc. The update control counter comprises the counter K, gate G (gate G and all other gates can be AND circuits) and the counter decoder KD. The counter K can be a four-stage binary counter which counts to 16. The counter K has a count (or step) input S, connected to the PLS signal line, and also to the D-gate DG4. The count input steps the counter for each pulse received. The counter K has a clear input C, connected to the output of gate G, which clears the counter to zero in response to a signal received from gate G, and has an initial clear input (not shown) to clear the counter at the start of operation. The gate G can be an AND circuit having two inputs connected to the EVS and RZ signal lines, respectively. The EVS signal line transmits a pulse from the cathode-ray tube circuits (FIG. 2B) at the end of each column scan of the electron beam. The RZ signal line will have an allow signal only at those times when the repeat column counter RCC contains zero indicating no column repeat. When columns are to be repeated, it is necessary to interrupt the flow of information from the memory. This is accomplished by preventing the

clearing of counter K as will become apparent during the description of the step pulse generator SPG.

The counter decoder KD is a standard "binary-to-octal" decoder which receives the outputs of the three least significant binary counter stages of counter K via paraphase amplifiers and transmits a signal on one of eight output signal lines UCC (UCC1 to UCC8) in accordance with the count accumulated by counter K. Hence each line is associated with one of the start or end addresses of one of the four possible line segments.

The step pulse generator SPG generates the stop pulses which are transmitted via the STEP signal line to direct the memory M to transfer the next word. The step pulse generator SPG can include a free-running pulse generator having an output connected to one input of an AND gate. The output of the AND gate is connected to the STEP signal. One control input of the AND gate is connected to the output of an equality comparator. The comparator compares the contents of the counter K with the signals on NCSV lines from number of column segments register NSR. This register stores an indication of the number of line segments in the column being updated. When the comparator senses equality it transmits a signal which blocks the AND gate. Then pulses will not pass through the gate until the counter K is cleared. Another control input receives the RZ signal.

The adder-subtractor AS which is used to modify by incrementing start and end element addresses, can be an eight binary position parallel adder-subtractor. The adder-subtractor has eight augend inputs connected to the eight lines AUG1 to AUG8, respectively, and has eight addend inputs. The four least significant addend inputs are connected via the four ADDN1 to ADDN4 and gates GS to the four lines MM1 to MM4, respectively. The four most significant addend inputs are wired to permanently represent zeros. (The gates GS can be four AND circuits having control inputs connected to the MOD signal line.) An adder-subtractor control is connected via the SIGN signal line to the sign register SR. When the signal on the SIGN signal line represents zero the adder-subtractor AS operates as an adder and when the signal represents one it operates as a subtractor. The eight result terminals of the adder-subtractor are connected via the eight RES signal lines to the column segment storage switch CSS.

The sign register SR stores sign indications for incrementing. Since there can be up to four line segments per column and each line segment has a start and an end element address, there are eight possible addends per column scan. Accordingly, the sign register SR includes eight one-stage binary counters, each associated with one of the possible addresses. The input of each one-stage binary counter is connected to the output of an input AND circuit. One input of the input AND circuit is connected to the RS signal line. The other input of the AND circuit is connected to one of the UCC signal lines. The output of each one-stage binary counter is connected to one input of an output AND circuit. The other input is connected to the same one of the UCC signal lines. The outputs of all of the output AND circuits are connected via an OR circuit to the SIGN signal line.

The selective repeat register SRR is identical to the sign register SR except that the one input of the input AND circuit is connected to the RSR signal line, and the associated OR circuit is connected to the SRR signal line. The register SRR controls selective repeating of starting and ending addresses of selected line segments in the column.

The register NCSR which stores a representation of the number of required line segments in a column can be a four-stage flip-flop register. The set input to each flip-flop is connected to the output of an AND circuit. One input to each of the AND circuits is connected to the NCS signal line. The other input of each of the AND circuits is connected to one of four MM signal lines. The clear inputs of the flip-flops is differentiator coupled to the NCS signal line to clear the flip-flops before they receive a new number. The output terminals of flip-flops are connected via the four NCSV signal lines,

respectively, to the step pulse generator SPG. The register has means (not shown, responding to an initial clear signal) for initially clearing it to the representation of the number two at the start of operation.

The repeat column counter RCC stores a number indicating the number of column scans which use the same start and end addresses unmodified. The number is decremented by one for each succeeding column scan. The counter can be a four-stage binary counter of the count down type. The step input is connected via an AND circuit to the EVS signal line. Upon reaching zero the counter emits a signal on the RZ signal line to the gate G. The control input of the AND circuit receives the RZ signal. Each of the stages has a presetting input connected to the output of an AND circuit. One input of each AND circuit is connected to the RC signal line. The other input of the AND circuit is connected to one of the MM signal lines to allow loading of the counter.

The column segment storage switch CSS is basically a logic network that switches information from either the memory M, via the four MM signal lines, or the result from the adder-subtractor AS, via the eight RES signal lines, to either the A-register AR, via the 64 TAR signal lines, or to the B-register BR, via the 64 TBR signal lines. Typical Boolean equations for the logic network are as follows:

$$\text{TAR1} = \text{UAB} \cdot \text{UCC1} \cdot (\text{MM1} + \text{RES1}) \cdot \{(\text{SUB} \cdot \text{ML}) + \text{MOD} + \text{SRR}\}$$

$$\text{TAR4} = \text{UAB} \cdot \text{UCC1} \cdot (\text{MM4} + \text{RES4}) \cdot \{(\text{SUB} \cdot \text{ML}) + \text{MOD} + \text{SRR}\}$$

$$\text{TAR5} = \text{UCC1} \cdot (\text{MM1} + \text{RES5}) \cdot \{(\text{SUB} \cdot \text{ML}') + \text{MOD} + \text{SRR}\}$$

$$\text{TAR9} = \text{UAB} \cdot \text{UCC2} \cdot (\text{MM1} + \text{RES1}) \cdot \{(\text{SUB} \cdot \text{ML}) + \text{MOD} + \text{SRR}\}$$

$$\text{TAR64} = \text{UAB} \cdot \text{UCC8} \cdot (\text{MM4} + \text{RES8}) \cdot \{(\text{SUB} \cdot \text{ML}') + \text{MOD} + \text{SRR}\}$$

$$\text{TBR1} = \text{UAB}' \cdot \text{UCC1} \cdot \text{CMM1} + \text{RES1} \cdot \{(\text{SUB} \cdot \text{ML}) + \text{MOD} + \text{SRR}\}$$

The integer following a letter combination indicates the specific signal line. The (+) indicates an OR operation, the (·) an AND operation, and a (') the complement of a signal.

The A-register AR is a sixty-four stage flip-flop register arrayed into eight groups of eight flip-flops. Each group is associated with a start or end element address of one of the four possible column segments. The set input of each flip-flop is connected to one of the TAR signal lines from the switch CSS. The clear input of each of the flip-flops is connected to the output of one and the same AND circuit. A first input of the AND circuit is connected to the UAB' signal line. A second input is connected to the EVS signal line and a third input is connected to the RZ signal line. Thus the A-register is cleared just prior to its updating provided a repeat scan is not called for. The output of each of the flip-flops is connected to one of the sixty-four FAR signal lines.

The B-register BR is a 64 stage flip-flop register similar to the A-register AR. The set input of each of the flip-flops is connected to one of the TBR signal lines. The clear input of each of the flip-flops is connected to the output of one and the same AND circuit. A first input of the AND circuit is connected to the UAB signal line. A second input is connected to the EVS signal line and a third input is connected to the RZ signal line. The output of each of the flip-flops is connected to one of the 64 FBR signal lines.

The column segment data switch CSD is basically a logic network which switches selected outputs of either the A-register AR, via the FAR signal lines, or the B-register BR, via the FBR signal lines, to the column element comparator CEC, via the eight SD signal lines.

A typical Boolean equation of the logic network for the least-significant bit is:

$$\text{SD1} = \left\{ \text{UAB}' \cdot \sum_{N=0}^{N=7} [\text{FAR}(1+N8) \cdot \text{SDD}(1+N)] \right\} + \left\{ \text{UAB} \cdot \sum_{N=0}^{N=7} [\text{FBR}(1+N8) \cdot \text{SSD}(1+N)] \right\}$$

where (1+N8) and (1+N) are suffix numbers for the FAR, FBR and SDD signal lines.

The adder-subtractor switch ASS is also a logic network which switches selected outputs of the A-register AR via the FAR signal lines, or the B-register BR, via the FBR signal lines, to the augend inputs of the adder-subtractor AS, via the eight AUG signal lines.

A typical Boolean equation for the least significant bit is shown on the following page.

$$AUG1 = (SRR + MOD) \cdot UAB \cdot \sum_{N=0}^{N=7} [FAR(1+N8) \cdot UCC(1+N)] + UAB' \cdot \sum_{N=0}^{N=7} [FBR(1+N8) \cdot UCC(1+N)]$$

where (1+N8 and (1+N) are suffix numbers for the FAR, FBR and UCC signal lines.

The segment data counter SDC which selects the start and end element addresses for transfer to the column element comparator CEC (FIG. 2B) can be a three-stage binary counter. The step or count input S of counter is connected to the DEQ signal line which is pulsed each time the electron beam is switched between on and off indicating a new address is required. The clear input C of the counter is connected to the EVS signal line which emits a pulse at the end of each column scan of the electron beam. At that time, the counter is cleared to zero. The counter has an initial clear input (not shown). The outputs of the counter are connected to inputs of the SD decoder SDD. The decoder can be a "binary-to-octal" decoder whose inputs are the outputs of the binary counters of the counter SDK and whose outputs are connected via the SDD via signal lines to the column segment data switch CSD.

The A-B counter ABC is a one-stage binary counter having its step input connected via the gate G1 to the EVS signal line, and an initial clear input (not shown). Signal RZ controls operation of gate G1. The counter ABC has a "1" and a "0" output connected to the UAB and UAB' signal lines (shown only as one line UAB). After the initial clear, counter ABC transmits a "positive" or "high" signal on line UAB and a "negative" or "low" signal on line UAB'. As the counter is stepped the states of the signals alternate.

In FIG. 2B there is shown the cathode ray tube control circuits. The column element counter CEK counts the time increments and therefore the elements in a column during a column scan by the electron beam. In other words, each unit count of the counter CEK represents one full column element. The column element counter CEK can be an eight-stage binary counter. The outputs of the stages are connected via the CEN signal lines to column element comparator CEC. When the counter is indexed beyond its capacity, it clears to zero and emits an overflow signal on the EVS signal line. The counter CEK has an initial clear input (not shown) which clears it to zero. The step or count input is connected to the output of gate G2. The retrace counter RTK establishes the retrace time period for the electron beam by counting time increments. The counter RTK can be a five-stage binary counter. When it reaches its capacity it resets to zero and emits an overflow pulse on the SVS signal line. The step or count input is connected to the output of gate G3. The counter RTK has an initial clear input (not shown) which sets the counter to a count of zero.

The EVS signal line is connected to the clear input of vertical scan flip-flop VS while the SVS signal line is connected to the set input of flip-flop VS. The outputs of the flip-flop are connected to the gating inputs of AND gates G2 and G3. The other input of each of the gates is connected to the "1" output of binary counter BC1 (a one-stage binary counter) whose input is driven by the output P1 of a free-running oscillator

OSC. The signals generated by oscillator OSC are shown in FIG. 3.

The EVS and SVS signal lines are connected to the vertical deflection control VDFC which drives the vertical deflection of the cathode-ray tube CRT. Control VDFC can be a gates sawtooth generator that is gated on by an SVS signal and gated off by an EVS signal.

When counter CEK is cleared to zero the EVS signal turns off the sawtooth generator and sets the flip-flop VS to the clear state opening gate G3 and closing gate G2. Pulses from the binary counter BC1 start stepping the counter RTK. When the counter RTK exceeds its capacity (overflows) the SVS pulse is emitted turning on the sawtooth generator and setting the flip-flop VS. Gate G2 opens and gate G3 closes. Pulses from binary counter BC1 are now fed to the count input of counter CEK. When the counter CEK overflows it emits an EVS pulse, and the cycle repeats. While counter CEK is counting it transfers signals (representing the instantaneous element count), via the CEN lines, to the column element comparator CEC. The other side of the comparator, which is a conventional equality comparator, is receiving a start or end address for a line segment via the lines SD. When equality is reached the comparator CEC emits a pulse on the DEQ signal line. The comparator has paraphrase amplifiers at its inputs. The occurrence of the DEQ signal indicates either the start column element or end column element of a column segment. In order to obtain half length column elements, the circuitry driving video counter VC is employed. In particular, half length register HLR stores "flag" bits to indicate which start or end column elements of a column are to have half the normal length. Since there can be up to four line segments per column and each line segment has a start and an end column element, there are eight possible half length column elements per column. Accordingly, the half length register HLR includes eight one-stage binary counters. The input of each counter is connected to the output of a two-input AND circuit, respectively. One input of each of these AND circuits is connected to the VHS signal line. The other input of each of the AND circuits is connected to one of the UCC signal lines. The output of each binary counter is connected to one input of another two-input AND circuit, respectively. The other input of each of these other two-input AND circuits is connected to one of the SDD signal lines. The outputs of these eight other AND circuits are connected to eight inputs of an OR circuit whose output is connected via line HL to the input of paraphrase amplifier AMP.

The direct output of amplifier AMP is connected to one input of gate G3, and the inverted output of amplifier AMP is connected to one input of gate G2. A second input of each of the gates receives the DEQ signal. The third input of gate G2 receives the P1 clock pulse signals from oscillator OSC, while the third input of gate G3 receives the P2 clock pulse signals from oscillator OSC. The output of gate G2 is connected via the OG2 signal line to one input of OR circuit O1; the output of gate G3 is connected via the OG3 signal line to the other input of OR circuit O1. These will now be described how half length column elements are obtained.

Binary counter BC1 generates a train of pulses having half the frequency and twice the period of the P1 clock pulses. This train of pulses drives column element counter CEK whose outputs are connected to column element comparator CEC. It can therefore be assumed that the DEQ signal has its positive-going leading edge in phase with the positive-going leading edge of the P1 clock pulses (see FIG. 3). Now the DEQ signal is fed to an input of each of the gates G2 and G3. Another input of gate G2 receives the P1 clock pulses while another input of gate G3 receives the P2 clock pulses. Now, at the start and at the end of each column segment of a column one and only one of the gates G2H and G3H is opened as determined by the contents of half length register HLR and by the presence of the SDD signals. If gate G2H is open it will transmit one P1 clock pulse on the OG2 signal line; if gate G3H is open it will transmit one P2 clock pulse on the OG3

signal line. It is seen from FIG. 3 the OG3 pulse occurs one clock pulse period (one-half the period of the normal column element periods, the period of the pulses from binary counter BC1) after the OG2 pulse. The OG2 or OG3 pulse is fed from the output of OR circuit O1.

The output of OR circuit O1 is connected to the step input of the video counter VC (a one-stage binary counter). The counter has an initial clear input (not shown) to set it to a state that turns off the electron beam. Video counter VC drives the video drive circuits VDC (the usual Z-axis circuits) of the cathode ray tube CRT.

The cathode ray tube CRT has horizontal deflection circuits which drives the horizontal deflection system. The horizontal deflection is incremented whenever an end of vertical scan EVS occurs. The horizontal deflection circuits include means for selectively incrementing either the width of column or half the width of a column. More particularly, the state of flip-flop FF1 determines whether the next column scan is full or half width. The set terminal of the flip-flop FF1 receives the HHS signal from function decoder FD whenever a "half step" is to occur. (Flip-flop FF1 has an initial clear input, not shown). The "1" output of flip-flop FF1 is fed to one input of gate G4; and the "0" output of flip-flop FF2 is fed to one input of gate G5. The second input of each gate receives the EVS signal. Thus, if the flip-flop FF1 is set, the EVS pulse passes through gate G4; and, if it is cleared, the EVS pulse passes through gate G5. The output of gate G4 is returned to the clear input of flip-flop FF1 to issue that after a half step is performed as directed the system is restored to the normal "full step" mode.

Now, the instantaneous count in horizontal counter HC represents the number of full columns the scan of the cathode-ray beam is deflected at that time. Counter HC which can be a plurality of cascaded binary counters has a step input connected to the output of OR circuit O2. One input of OR circuit O2 is connected to the output of gate G5. Therefore, whenever gate G5 passes on EVS pulse signal horizontal counter HC is incremented and the beam will be deflected a full column width as desired. The second input of OR circuit O2 is fed from the output of binary counter BC2 (a one-stage binary counter), which emits one pulse for every second pulse it receives. The input of binary counter BC2 is the output of gate G4. Thus, when gate G4 is open the EVS pulse steps binary counter BC2 which records a half step increment. Taken together the combination of the outputs of horizontal counter HC and binary counter BC2 represent the total horizontal deflection (the number of full columns plus a possible half column). The outputs of counter HC and counter BC2 are fed to inputs of digital-to-analog converter DAC of conventional design which generates an analog signal. The signal is amplified by horizontal deflection voltage source HDV which drives the horizontal deflection circuits of the cathode-ray tube CRT to deflect the electron beam by the desired position.

Now, because half a column width displacement would ordinarily increase the energy density of its associated scan and might cause nonuniformities in the recording, provision is made to decrease the electron beam intensity during the half column scans flip-flop FF2 controls the intensity control circuits ITC of the cathode-ray tube CRT. When flip-flop FF2 is set, the signal from its "1" output causes intensity control ITC to decrease the electron beam intensity. The set input of flip-flop FF2 is connected to the output of the gate G4 while the clear input is connected to the output of gate G5. Thus, whenever an EVS pulse passes through gate G4 indicating a half step, the flip-flop FF2 is set, and whenever an EVS pulse passes through gate G5 indicating a full step, the flip-flop FF2 is cleared.

The cathode-ray tube also receives electron beam accelerating voltages from source AVS.

The face of the cathode ray tube is focused by the lens LENS onto a moving film FLM. The film is driven by scroll drive SDX past lens LENS. Thus images generated on the face of the cathode-ray tube resulting from the excitation of the phosphor by the electron beam are recorded on film FLM.

The system will now be cycled through the "writing" of several typical columns of the pattern of FIG. 1. It is assumed that all register, flip-flops and binary counters have been cleared to their initial states.

Columns C8 and C9 will first be written. It should be noted that column C8 will be written at double resolution (a left half and a right half) and column C9 will be written with normal resolution. Since the number of column segments register NCSR is initially cleared to two and the counter K is cleared to zero, the comparator in the step pulse generator detects an inequality. Generally, as long as the inequality exists, step pulse generator SPG transmits pulses via the line STEP to the memory M. The first such pulse causes memory M to transmit the first memory word (1011) to the lines MM. The word is the NCS code word implying that the next word from the memory M will indicate twice the number of column segments in the column C8 and all succeeding columns until it is changed by a new NCS code word. The decoder FD transmits a signal on the NCS signal line to open the input gates of the register NCSR. The step pulse generator SPG emits the next pulse and the memory M emits the data word (0010), indicating one line segment per column, to the MM signal lines. The word enters the NCSR register. The next step pulse from step pulse generator SPG causes the memory to emit the next word, a code word (1010). Decoder FD decodes this as the SUB code word meaning that the next two words are the least and most significant halves of a start element address, and transmits a signal on the SUB signal line. The next word (1111) emitted by memory M is a data word. This word is an SL data word, the least significant half of a start address. At this time, counter K holds a count of zero causing decoder KD to emit a signal on the UCC1 signal line, the ML counter MLK is cleared and emitting the ML signal, the A-B counter ABC is cleared, by the EVS signal via gate G1, and emitting the UAB signal. These signals cooperate in the column segment storage switch CSS to cause the data word (1111) to pass from the signal lines MM via the switch CSS and the TAR1 to TAR4 signal lines to the four least significant bit flip-flops of the first group of eight flip-flops in the A-register AR. The first group stores the start address of the first line segment of a column. The SUB signal causes the pulse generator PGS to emit a first pulse. The pulse switches the ML counter MLK which thereafter emits a signal on the ML' signal line. The next word from the memory M is a word (0001); an SM (most significant half of a start address) data word. Because the ML' signal instead of the ML signal is now present, and since the remaining control signals to the column segment storage switch CSS have not changed the data word (0001) is fed via the MM signal lines, the switch CSS and the TAR5 to TAR8 signal lines to the four most significant bit flip-flops of the first group of eight flip-flops in the A-register AR. This group of eight flip-flops now contains the binary number 00011111 (decimal 31), the start element address of the line segment of the left half of column C8.

The pulse generator PGS emits the second pulse in response to the SUB signal. This second pulse clears the ML counter MLK which now generates the ML signal, and also steps via the PLS line the counter K causing counter decoder KD to emit the UCC2 signal. Step pulse generator SPG still detects an inequality between the contents of the register NCSR represented by the signals on the NCSV signal lines, and the count K, represented by the signals on the KV signal lines. The pulse generator SPG continues emitting step pulses.

The next word from the memory M is a code word (1010) representing a SUB operation code indicating the next two words are data words which, in fact, represent the least and most significant halves of the end element address of the first line segment. These next two words have the binary values (1110) and (0010). The operation on these two words is the same as that following the first SUB code word except that the UCC2 signal instead of the UCC1 signal is now present. The words pass sequentially through column segment storage switch CSS and the TAR9 to TAR12, and TAR13 to TAR16

signal lines to the second group of eight flip-flops (the storage register for the end element address of the first line segment) in the A-register AR. This group now stores the binary number 00101110 (decimal 46).

The ML counter MLK is restored by the second pulse resulting from this SUB signal. This second pulse is also fed to the step input of counter K and decoder KD emits a signal on the UCC3 signal line. Now the step pulse generator SPG detects equality between the count of counter K and the contents of the register NCSR, and suspends emitting step pulses to memory M.

The A-register AR now contains all of the information for the "writing" of the left half of column C8; i.e., the start element address (00011111), decimal 31) and the end element address (00101110, decimal 46) of a single column segment. The remainder of the A-register AR is zero.

All of this loading occurs before the first column scan by the electron beam has occurred. When the column element counter CEK next overflows, it emits an EVS pulse signal. The EVS signal switches the A-B counter ABC which then generates the UAB' signal, it clears the segment data counter SDC (redundant at this time), it clears the B-register BR (redundant at this time) and more particularly it clears the counter K via gate G. Counter decoder KD emits a signal on the UCC1 signal line. Step pulse generator SPG again detects an inequality between the count in counter K and the number stored in the number of column segment register NCSR so it again emits step pulses to the memory M.

The memory M emits the word (1000), a half increment a column code word. Decoder FD decodes the word to an HHS signal which sets flip-flop FF1 to indicate the next column scan will be the right half of column C8 instead of column C9.

The memory M emits the word (1101), a reverse sign code word. Decoder FD decodes the word to the RS signal which is transmitted to the sign register SR where it cooperates with the UCC1 signal to reverse the state of the one-stage binary counter associated with the start address of the first line segment (indicated by the UCC1 signal). Since all of the counters in the sign register SR were initially cleared to the zero state indicating (+), the reversal of this counter, switching it to the one state indicating (-), changes the sign associated with any incrementing of the start address of the first line segment to a decrement.

The next memory word (0010) is a data word (decimal 2) indicating an incremental change. Since the most significant bit is a "0", the decoder FD senses it and generates the MOD signal. Recalling that UCC1 signal is present, the MOD signal cooperates with the UCC1 signal in the sign register SR to gate out the contents of the first counter (just set to one). Since this counter is set to one a signal is fed to the adder-subtractor AS switching it to a subtractor. The MOD signal opens gates GS connecting the MM signal lines to the ADDN signal lines so that this data word (decimal 2) provides a subtrahend for the adder-subtractor AS. The MOD signal cooperates with the UAB' signal and the UCC1 signal in adder-subtractor switch ASS to nondestructively read out the contents (decimal 31) of the first group of eight flip-flops of the A-register AR via the FAR1 to FAR8 signal lines, the switch ASS, the AUG1 to AUG8 signal lines, to the adder-subtractor AS to provide a minuend. The MOD signal cooperates with the UCC1 signal and the UAB' signal switch CSS to transfer the difference (decimal 29) to the first group of eight flip-flops (storage register of the start address of the first line segment) in the B-register BR. This is done by connecting the RES1 to RES8 signal lines to the TBR1 to TBR8 signal lines.

The pulse generated by the pulse generator PGS in response to the MOD signal is transmitted via the PLS signal line to the step input of counter K which steps. Decoder KD starts transmitting a signal on line UCC2.

The next memory word (0011) is a date word (decimal 3). Decoder FD senses the zero in the most significant bit position and generates another MOD signal. This MOD signal cooperates with the UCC2 signal in the sign register SR to gate

out the contents of the second counter. Since this counter is still cleared the signal on the SIGN line makes the adder-subtractor AS an adder. The MOD signal at gates GS connect the MM signal lines to the ADDN signals to provide the data word (decimal 3) as an addend. The MOD signal cooperates with UCC2 signal and the UAB' signal in switch ASS to connect the FAR9 to FAR16 lines to the AUG1 to AUG8 lines. The contents of the second group of eight flip-flops (storing the end address of the first line segment) of the A-register AR are fed to the augend inputs of the adder-subtractor AS to provide an augend (decimal 46). The MOD signal cooperates with the UCC2 signal and the UAB' signal in switch CSS to connect the RES1 to RES9 signal lines to the TBR9 to TBR16 signal lines. The sum (decimal 49) is loaded into the second group of eight flip-flops (those storing the end address of the first line segment) of the B-register BR.

The pulse generator PGS in response to the MOD signal then transmits a pulse via the PLS signal line to the step input of counter K. Decoder KD then transmits a UCC3 signal (extraneous at this time). Step pulse generator SPG detects equality between the count of counter K and the contents of number of column segment register NCSR and stop emitting stepping pulses. Transfers from memory M are suspended. The B-register BR now stores all the information required to "write" the right half of column C9 (S=29; E=49).

Just after the start of the updating of the B-register BR (following the EVS pulse), the contents of the A-register AR start being transferred to cathode-ray tube circuits for the writing of the left half of column C8. In particular, the EVS signal that initiated the updating of the B-register BR cleared the segment data counter SDC causing the generation of the SDD1 signal by decoder SDD.

The SDD1 signal cooperating with the UAB' signal in the column data switch CSD connects the FAR1 to FAR8 signal lines to the SD1 to SD8 signal lines. The contents (00011111, representing decimal 31) of first group of eight flip-flops of the A-register AR are transferred to one set of inputs of the column element comparator CEC. The outputs of the column element counter CEK (the instantaneous addresses during the column scan) are fed to the other set of inputs of the comparator CEC. When an equality is sensed the comparator CEC emits a DEQ pulse signal which gates a P1 clock pulse through gate G2 (the binary counter in the half length register HLR is in the cleared state indicating no vertical half increment at this time and no HL signal is fed to amplifier AMP). The clock pulse passes through OR circuit 01 and triggers counter VC to the on state. Counter VC energizes the video drive circuits VDC which turn on the electron beam.

The DEQ signal also steps the counter SDC which is decoded to generate the SDD2 signal. The SDD2 signal cooperates with UAB' signal in switch CSD to connect the FAR9 to FAR16 signal lines to the SD1 to SD8 signal lines. The contents (00101110, representing decimal 46) of the second group of eight flip-flops are transferred to the first set of inputs of the column element comparator CEC. Another comparison operation is performed with the element count of counter CEK. Upon equality another DEQ pulse signal is generated. This second DEQ pulse signal gates another P1 clock pulse signal through gate G2 and OR circuit 01 which restores the counter VC deenergizing the video drive circuits VDC turning off the electron beam. This second DEQ pulse signal steps the counter SDK which causes the generation of the SDD3 signal. The contents of the third group of eight flip-flops are fed to comparator CEC. However, since the contents are 00000000 no equality can be detected before the end of the column scan. At the end of the scan the left half of column C8 has been written and the EVS signal is generated. The EVS signal cooperates with the UAB' signal in the A-register AR to clear all the flip-flops therein so it can receive the information for column C9. The EVS signal clears the counter SDC which starts generating the SDD1 signal. The EVS signal switches the counter ABC which starts generating the UAB signal. And the EVS signal passes through gate G (the RZ signal is present

all this time) to clear the counter K causing the decoder KD to generate the UCC1 signal. When the counter K is cleared, step pulse generator SPG notes the inequality between the count in counter K and the number stored in the register NCSR, and starts emitting stepping pulses to direct the memory to resume transmitting information. This information will be used to update the A-register AR for the writing of column C9.

It should be noted that the flip-flop FF1 was set prior to this EVS signal and after the previous EVS signal. This EVS signal passes through gate G4 to set flip-flop FF2 and reset flip-flop FF1. The output of flip-flop FF2 is fed to intensity control ITC which cuts down the intensity of the electron beam. The EVS signal passing through gate G4 also steps binary counter BC2. The combination of signals transmitted by counters HC and BC2 now represent the previous increment count plus a half increment. These signals are fed to digital to analog converter DAC which causes the horizontal deflection voltage source HDV to horizontally deflect the electron beam half a column width. Shortly thereafter, the contents of the B-register BR are transferred to the video circuits of the cathode-ray tube system for the writing of right half column C8.

In particular, the UAB signal cooperates with the SDD1 signal in switch CSD to connect the FBR1 to FBR8 signal lines to the SD1 to SD8 signal lines. The contents (00011101, decimal 29) of the first group of eight flip-flops (the storage register of the start address of the first line segment) of the B-register BR are fed to one set of inputs of the column element comparator CEC. The outputs of the column element counter CEK are fed to the other set of inputs of the comparator CEC. When equality is detected the DEQ pulse signal is generated. The DEQ signal gates a P1 clock pulse signal through gate G2 to switch the video counter VC to "one" which turns on the electron beam through the agency of the video drive circuits VDC.

The DEQ signal also steps the counter SDC which causes the decoder SDD to generate the SDD2 signal. The SDD2 signal cooperates with the UAB signal in the switch CSD to connect the FBR9 to FBR16 signal lines to the SD1 to SD8 signal lines. The contents (00110001, decimal 49) of the second group of eight flip-flops (the storage register for the end address of the first line segment) of the B-register BR are fed to one set of inputs of the comparator CEC. When the count of the counter CEK (represented by signals on the CEN signal lines) equals the address represented by the signals on the SD signal lines, comparator CEC emits another DEQ pulse signal. This second DEQ pulse signal gates another P1 pulse signal through gate G2 which switches the counter VC to zero turning off the electron beam through the agency of the video drive circuits VDC.

This second DEQ pulse signal also steps counter SDK resulting in the generation of the SDD3 signal. However, since the third group of eight flip-flops in the B-register store zero no further equalities are detected by comparator CEC before the end of the column scan and the electron beam remains off. Thus the right hand portion of column C8 has been written. At the end of the scan another EVS signal is generated. The B-register BR is again updated to provide the writing information for column C10 and the contents of the A-register AR are read out to perform the writing of column C9.

The above sequence shows the updating of writing information for columns with a single line segment by substituting a new address (left hand of column C8) and by incrementing old addresses (right half of column C8). Furthermore, the incrementing was either positive for the end address or negative (decrementing) for the start address of the line segment of the right half of column C8. In addition, it was shown how half column stepping can be selectively performed by utilizing control indicia.

The next example will be the "writing" of columns having more than one line segment per column. See, for example, columns C18 and C19 of FIG. 1. Since the signal flow through the system is similar to the signal flow described for columns C8 and C9, the discussion will not be as detailed and only the

prominent aspects will be specifically pointed out. In order to simplify the description, table II shows the flow of words from memory M.

At this time the A-B counter ABC is cleared (the UAB signal is present), counter K is cleared and the UCC1 signal is present. The word (1011) is read from memory M. It is a code word causing the decoder FD to generate the NCS signal which clears the number of column segment register NCSR and opens its input gates. The next word from memory M (0100, decimal 4) enters the register NCSR. The word indicates that there are two start-end element address pairs (two line segments) in the current column being entered into the A-register AR. The memory word $m+2$ is the data word (0001) indicating that the start address of the first line segment is to be changed by one. The counter, in the

TABLE II

Memory Word Number	Memory Word Contents	Comments	Column Number
$m+0$	1011	NCS code word	18
$m+1$	0100	Indicates two line segments (E=18)	
$m+2$	0001	DS=1	18
$m+3$	1010	SUB code word	18
$m+4$	1111	EL=15 (E=32)	18
$m+5$	0001	EM=1	18
$m+6$	1010	SUB code word (new address)	18
$m+7$	1101	SL=13 (S=45)	18
$m+8$	0010	SN=2	18
$m+9$	1010	SUB code word (new address)	18
$m+10$	0100	EL=4 (E=63)	18
$m+11$	0100	EM=4	18
$m+12$	0001	DS=1	19
$m+13$	1101	RS code word	19
$m+14$	(S 0101	DE=5	19
$m+15$	1010	SUB code word (new address)	19
$m+16$	0101	SL=5 (S=53)	19
$m+17$	0011	SM=3	19
$m+18$	0001	DE=1	19

sign register SR, associated with this start address has been set to one ever since the scan of column C9, therefore the MOD operation performs a subtraction on the contents (decimal 14) of the first group of eight flip-flops in the B-register BR and transfers the updated start address (decimal 13) to the first group of eight flip-flops in the A-register AR. Counter K is stepped by one and the UCC2 signal is generated. The memory word $m+3$ (1010) is a SUB code word followed by memory word $m+4$ (1111), a data word, and memory word $m+5$ (0001), a data word, and the second group of eight flip-flops of the A-register AR are located to contain decimal 31. Counter K is stepped by one generating the UCC3 signal.

The memory word $m+6$ (1010) is a SUB code word, followed by memory word $m+7$ (1101), a data word, and memory word $m+8$ (0010), a data word, and the third group of eight flip-flops of the A-register AR are located to contain decimal 45. Counter K is stepped by one and the UCC4 signal is generated.

The memory word $m+9$ (1010) is a SUB code word. The next two memory words $m+10$ (0100) and $m+11$ (0100) are loaded into the fourth group of flip-flops of the A-register AR. The counter K is stepped by one. Now the comparator in the step pulse generator SPG detects an equality between the count in counter K and the contents of the number stored in the column segments register NCSR and suspends generating the step pulses to the memory M. The "writing" information for column C18 is now in A-register AR. The EVS pulse signal, at the end of the scan out of the contents of B-register BR to the video control circuits, for writing column C17, clears counter K causing the generation of the UCC1 signal by decoder KD, and steps the A-B counter ABC causing the

generation of the UAB' signal. The B-register BR will now be updated with information for writing column C19 and the contents of the A-register AR will be scanned out to write column C18.

The next memory word $m+12$ (0001), a data word, causes the subtraction by one of the contents (decimal 13) of the first group of eight flip-flops of the A-register AR by the adder-subtractor AS and the difference (decimal 12) is stored in the first group of eight flip-flops in the B-register BR as the start element address of the first line segment of column C19. Counter K is stepped by one and the UCC2 signal is generated.

Memory word $m+13$ (1101) is a RS code word which sets the second one-stage binary counter (the one associated with the end address of the first segment) of the sign register SR to indicate subtractions.

Memory word $m+14$ (0101, decimal 5), a data word, which generates the MOD signal, subtracts five from the contents (decimal 31) of the second group of eight flip-flops in the A-register AR. The difference is stored in the second group of eight flip-flops in the B-register BR as the end element address of the first line segment. The counter K is stepped by one and the UCC3 signal is generated.

The memory word $m+15$ is a SUB code word. The memory words $m+16$ (0101) and $m+17$ (0011) are loaded into the third group of flip-flops of the B-register BR representing the start element address (decimal 53) of the second line segment. The counter K is stepped by one and the UCC4 signal is generated.

The memory word $m+18$ (0001, decimal 1) generates a MOD signal which causes the incrementing of the contents (decimal 63) of fourth group of eight flip-flops of the A-register AR via the adder-subtractor AS to the fourth group of eight flip-flops of the B-register BR to store the end element address (decimal 69) of the second line segment. Counter K is stepped by one. The contents of the counter K now equal the number stored in number of column segments register NCSR and memory transfers are suspended. The "writing" information for column C1 is now stored in the B-register BR which will be scanned out at the appropriate time in the usual manner.

It should be noted that none of the information concerned with columns C18 and C19 include the code word (1000), half increment a column, therefore, function decoder FD never generated and HHS signal and flip-flop was never set. Therefore every EVS signal passes through gate G5 to the clear input of flip-flop FF2 and to an input of OR circuit 02 indicating a full column incrementing if flip-flop FF2 were set it would be cleared to return the beam intensity to normal if it had been attenuated. In addition the EVS signal passes through OR circuit 02 to the step input of counter HC. The combination of signals from counters HC and BC2 then represent a full column increment and the electron beam is so deflected.

The next example is concerned with the generation of a half length column element, and the writing of column C29 will be used as an example.

Table III shows the type of words transferred from the memory.

TABLE III

Memory Word Number	Memory Word Contents	Comments	Column Number
P+0	0001	DS=1	29
P+1	0001	DE=1	29
P+2	0001	DS=1	29
P+3	0000	DE=0	29
P+4	0000	DS=0	30
P+5	1001	Half increment of length unit	30 (29)
P+6	0000	DE=0	30
P+7	0000	DS=0	30
P+8	0000	DE=0	30

At this time the A-B counter ABC is set (the UAB' signal is present) counter K is cleared and the UCCI signal is present. The B-register BR will now be updated (for column C29) and the contents of the A-register AR will be scanned out to write column 28.

Memory word P+0 (0001), a data word, causes the subtraction by one of the contents (decimal 6) of the first group of eight flip-flops of the A-register AR by the adder-subtractor AS and the difference (decimal 5) is stored in the first group of eight flip-flops of the B-register BR as the start element address of the first line segment of column C29. Counter K is stepped by one and the UCC2 signal is generated.

Memory word P+1 (0001), causes a subtraction by one of the contents (decimal 12) of the second group of flip-flops of the A-register AR by the adder-subtractor AS and the difference (decimal 11) is stored in the second group of eight flip-flops of the B-register BR as the end element address of the first line segment of column C29. Counter K is stepped by one and the UCC3 signal is generated. Memory word P+2 (0001), a data word, causes the addition by one of the contents (decimal 68) of the third group of eight flip-flops of the A-register AR by the adder subtractor AS and the sum (decimal 69) is stored in the third group of eight flip-flops of the B-register BR as the start element address of the second line segment of column C29. Counter K is stepped by one and the UCC4 signal is generated.

Memory word P+3 (0000), a data word, causes the addition by zero of the contents (decimal 75) of the fourth group of eight flip-flops of the A-register AR by the adder subtractor AS and the sum (decimal 75) is stored in the fourth group of eight flip-flops of the B-register as the end element address of the second line segment of column C29. Counter K is stepped by one. Now the comparator in the step pulse generator SPG detects an equality between the count in counter K and the contents of column segments register NCSR and suspends generating of the step pulse to the memory M. The "writing" information for column C29 is now in B-register BR. However, it should be noted that the end address for the first line segment is decimal 11 whereas the pattern requires it be decimal 11.5. A half increment will be applied during the scanning out as will hereinafter be apparent. The EVS pulse signal at the end of the scan out for column C28 clears counter K causing the generation of the UCC1 signal by decoder KD, and step the A-B counter ABC causing the generation of the UAB signal. The A-register AR will now be updated for writing column C30 and the contents of the B-register BR will be scanned out to write column C29.

The next memory word P+4 (0000), a data word, causes the subtraction by zero of the contents (decimal 5) of the first group of eight flip-flops of the B-register BR by the adder-subtractor AS and the difference (decimal 5) is stored in the first group of eight flip-flops in the A-register AR as the start element address of the first line segment of column C30. Counter K is stepped by one and the UCC2 signal is generated.

The next memory word P+5 (1001), a half increment column element code word, is received by function decoder FD which transmits a VHS signal to half length register HLR where it cooperates with the UCC2 signal to set the binary counter therein associated with the end element address of the first line segment of a column.

The remainder of the memory words for updating the A-register, AR for the writing of column C30 present nothing unusual so there is no point in proceeding further. Instead the scanning out of the B-register BR for column C29 will be described.

In particular, the EVS signal that initiates the updating of the A-register AR cleared the segment data counter SDK signal causing the generation of the SDD1 signal by decoder SDD.

The SDD1 signal cooperating with the UAB signal in the column data switch CSD connects the FBR1 to FBR8 signal lines to the SD1 to SD8 signal lines, the contents (decimal 5) of the first group of eight flip-flops of the B-register BR are

transferred to one set of inputs of the column element comparator CEC. The outputs of the column element counter CEK are fed to the other set of inputs of the comparator CEC. When an equality is sensed the comparator CEC emits a DEQ pulse signal. The SDD1 signal is also fed to half-length register HLR when it gates out the value of the binary counter associated with the start element address of the first line segment.

Since, this counter is cleared no HL signal is fed to amplifier AMP. Accordingly, its direct output (+) blocks gate G3 and its inverting output (=) opens gate G2. The DEQ pulse signal gates a P1 clock pulse through the gate and the OR circuit 01 to set the video counter VC without a delay. Counter VC energizes the video drive circuits VDC which turn on the electron beam.

The DEQ signal also steps the counter SDK which is decoded to generate the SDD2 signal. Signal SDD2 cooperates with the UAB signal in switch CSD to connect the FBR9 to FBR16 signal lines to the SD1 to SD8 signal lines and another comparison operation is performed by comparator CEC. Upon equality a DEQ pulse signal is generated. The SDD2 signal gates out the contents of the binary counter of the half length register HLR associated with the end element address of the first line segment. This counter had been set by memory word P+5. Therefore, an HL signal is transmitted from register HLR to amplifier AMP whose direct output (+) opens gate G3 and whose inverting output (=) blocks gate G2. Consequently, the DEQ pulse signal gates a P2 clock pulse through gate G3 to line OG3 and through OR circuit 01 to clear video counter VC with half an element delay (see FIG. 3 for the timing). The electron beam is turned off at the equivalent of address R11.5. The remainder of the writing of column C29 and column C30 is straight forward and will not be described.

Thus, it has been shown how by using control indicium, the vertical resolution can be doubled as required.

The next example will be the use of a special code word imbedded in the memory to repeat in its entirety the writing information for a plurality identical columns. This occurs for columns C35 through C37 of FIG. 1.

The writing information for column C34 is stored in the A-register AR as a start element address (decimal 4) and an end element address (decimal 10) for the first line segment, and a start element address (decimal 70) and end element address (decimal 76) for the second line segment.

The memory word following the updating of the information for column C35 is the RC code word which is decoded by decoder FD to an RC signal fed to the input gates of repeat counter RCC. The next memory word (0010, decimal 2) now stores a count other than zero it stops generating the RZ signal.

The disappearance of the RZ signal at the control input of gate G prevents EVS pulse signals from stepping counter K. The disappearance of the RZ signal at the clear gates of the A-register AR and the B-register BR prevents EVS pulse signals from clearing these registers from scan outs. The disappearance of the RZ signal at the control input of gate G1 prevents the EVS pulse signal from stepping A-B counter ABC. And the absence of the RZ signal to a control input of the gate in step pulse generator SPG suspends further memory transfers. The appearance of the RZ' signal at the input gate of the counter RCC will allow subsequent EVS pulse signals to step the counter. The result is that further memory transfers are suspended, the contents of the A-register AR and the B-register BR are frozen and successive scan outs of one of the registers (in this case the A-register AR occur until the counter RCC is stepped down from two to zero. Each EVS pulse signal following the scan out of the A-register AR steps counter RCC down by one. After two such EVS pulse signals resulting in the "writing" of columns C36 and C37 counter RCC again contains zero. Then the RZ signal reappears, memory transfers resume, the A-register AR and the B-register BR are clearable, the counter K and the A-B counter ABC are steppable.

The disappearance of the RZ' signal at the input gate of the counter RCC prevents further EVS pulse signals from stepping this counter.

This next example concerns the writing of columns C50 and C51. Column C50 contains two line segments. The start element address of the second line segment (set to decimal 43 during the updating of column C49) requires no modification for the next eleven columns (from column C50 through column C60). The other start and end element addresses require occasional modification during this section of the pattern. Table IV shows the memory words associated with column segments C50 and C51 which are typical for this section.

TABLE IV

Memory Word Number	Memory Word Contents	Comments	Column Number
q+0	0001	DS=1	50
q+1	0001	DE=1	50
q+2	1110	RSR code word	50
q+3	0001	DE=1	50
q+4	0000	DS=0	51
q+5	0001	DE=1	51
q+6	0000	DE=0	51

At this time the A-B counter ABC is cleared (the UAB signal is present), counter K is cleared and the UCC1 signal is present. B-register BR contains the start element address (decimal 8) and the end element address (decimal 15) of the first line segment and the start element address (decimal 43) and the end element address (decimal 73) of the second line segment of column C49.

The memory word q+0 (0001) is a data word which also generates the MOD signal for incrementing by one the contents (decimal 8) of the first group of eight flip-flops of the B-register BR which it passes via the adder-subtractor AS to the first group of eight flip-flops of the A-register AR to become the start element address (decimal 9) of the first line segment of column C50. Counter K is stepped by one and the UCC2 signal is generated.

The memory word q+1 (0001) is a data word which also generates the MOD signal for incrementing by one of the contents of the second group of eight flip-flops of the B-register BR while it passes via the adder-subtractor AS to the second group of eight flip-flops of the A-register AR to become the end element address (decimal 16) of the first line segment of column C50. Counter K is stepped by one and the UCC3 signal is generated.

The next memory word q+2 (1110) is a reverse selective repeat code word which generates the RSR signal. The RSR signal cooperates with the UCC3 signal in selective repeat register SRR to set to one the counter associated with the start address element of the second line segment. The output of this counter cooperating with the UCC3 signal generates the SRR signal. The SRR signal cooperates with the UCC3 signal in adder-subtractor switch ASS to connect the FBR17 to FBR24 signal lines to the AUG1 to AUG8 signal lines. Thus the contents of the third group of eight flip-flops in the B-register BR pass through the adder-subtractor AS to the RES1 to RES8 signal lines. Note the addend is zero at this time since gates GS are blocked (no MOD signal present). The SSR signal cooperates with the UCC3 signal in column segment storage switch CSS to connect the RES1 to RES8 signal lines to the inputs of the third group of eight flip-flops of the A-register AR. The start element address of the second line segment of column C50 is thus stored. The RSR signal causes the pulse generator to step the counter K by one and the UCC4 signal is generated.

Memory word q+3 (0001) is a data word which also generates the MOD signal for decrementing by one the con-

tents of the fourth group of eight flip-flops of the B-register BR while it passes via the adder-subtractor AS to the fourth group of eight flip-flops of the A-register AR to become the end element address (decimal 72) of the second line segment of column C50. The counter K is stepped by one. Now the comparator in the step pulse generator SPG detects an equality between the count in counter K and the number stored in the register NCSR and suspends memory transfers. The "writing" information for column C50 is now in A-register AR. The EVS pulse signal, at the end of the scan out of the contents of the B-register BR, clears counter K causing the generation of the UCCI signal and steps the A-B counter ABC causing the generation of the UAB' signal. The B-register BR will now be updated with information for the writing of column C51 and the contents of the A-register AR will be scanned out to write the column C50.

The next memory word $q+4$ (0000) is a data word which also generated the MOD signal for incrementing by zero the contents of the first group of eight flip-flops in the A-register AR in its transfer via the adder-subtractor AS to the first group of eight flip-flops in the B-register BR to give the start element address (decimal 9) for column C51. Counter K is stepped by one and the UCC2 signal is generated.

The next memory word $q+5$ (0001) is a data word which also generates the MOD signal for incrementing by one the contents of the second group of eight flip-flops of the A-register AR while it passes via the adder-subtractor AS to the second group of flip-flops of the B-register BR to become the end element address (decimal 17) of the first line segment of column C51. Counter K is stepped and the UCC3 signal is generated. The UCC3 signal gates out the "one" now stored in the one-stage binary counter associated with the start element address of the second line segment as the SRR signal. The SRR signal cooperates with the UCC3 signal in the adder-subtractor switch ASS to connect the FAR17 to FAR24 signal lines to the AUG1 to AUG8 signal lines. Thus, the contents of the third group of eight flip-flops of the A-register AR pass through the adder-subtractor AS unmodified (gates GS are blocked). The UCC3 signal cooperates with the SSR signal in switch CSS to connect the RES1 to RES8 signal lines to the TBR17 to TBR24 signal lines and the start element address of the second line segment of column C50 is repeated and becomes the start element address of the second line segment of column C51. The SRR signal cooperates with the RSR' signal at D-gate DG4 to emit a pulse to the step input of counter K. (D-gate DG4 can be an AND circuit which drives a delay multivibrator). Counter K is stepped by one and the UCC4 signal is generated. The SRR' signal disappears from the gate within the step pulse generator SPG permitting the memory M to transfer the next memory word $q+6$ (0000).

Memory word $q+7$ is a data word which also generates the MOD signal for incrementing by zero the contents of the fourth group of eight flip-flops in A-register AR in its transfer via the adder-subtractor AS to the fourth group of eight flip-flops in B-register BR to give the end element address (decimal 72) of the second line segment for C51. The counter K is stepped by one. Now the comparator in the step pulse SPG SPG detects an equality between the count in counter K AND THE NUMBER STORED IN THE NCSR NCSR and suspends memory transfers. The "writing" information for C51 C51 is now in B-register BR ready for scanning out.

The remainder of the pattern is generated by combinations of the cited examples.

Finally the memory transfers the word (1111), an EOP code word, indicating an end of pattern which can be used to stop the processing by suitable means (not shown) to prime the system by suitable means (not shown) for generating further patterns. It should be noted that an initial clear signal is required to initialize all counters and registers. The source of this signal and its feeding network to the appropriate devices was not shown merely for the sake of simplicity, it being realized that good engineering practice requires such initializing.

Since the various elements shown in the system are made up of standard components, and standard assemblies, reference may be had to "High Speed Computing Devices," by the staff of Engineering Research Associates, Inc. (McGraw-Hill Book Company, Inc., 1950); and appropriate chapters in "Computer Handbook" (McGraw-Hill, 1962) edited by Harvey D. Huskey and Granino A. Korn, and for detailed circuitry, to the example "Principles of Transistor Circuits," edited by Richard F. Shea, published by John Wiley and Sons, Inc., New York and Chapman and Hall, Ltd., London, 1953 and 1957. In addition, other references are: For system organization and components: "Logic Design of Digital Computers," by M. Phister, Jr., (John Wiley and Sons, New York); "Arithmetic Operations in Digital Computers" by R. K. Richards (D. Van Nostrand Company, Inc., New York). For circuits and details: "Digital Computer Components and Circuits," by R. K. Richards (D. Van Nostrand Company, Inc., New York).

An especially worthwhile book for finding the components mentioned in the specification, and the hardware for realizing the components as well as the techniques for mechanizing Boolean equations to actual logic networks is "The DIGITAL Logic Handbook," 1966-67 edition, copyrighted in 1966 by the Digital Equipment Corporation of Maynard, Mass.

While only one embodiment of the invention has been shown and described in detail, it will now be obvious to those skilled in the art, many modifications and variations which do not depart from the spirit of the invention as defined in the appended claims.

Although, the half incrementing of column elements has been described by selectively gating one of two phases of clock pulses with a comparison sign, it is equally possible to use other techniques such as using different counting rates for the column element counter and selectively gating the output signals therefrom to the column element comparator.

In addition, while only a cathode-ray tube system has been shown, the scanning means could equally well be electrostatically changed streams of ink printing on paper or electron or ion beams directly etching a record medium, or light (or basic) beams scanning a photographic film.

Furthermore, although double resolution has been shown separately in each of the two directions it should be apparent that it can be simultaneously employed in both of the directions by suitably programming the word flow from the memory.

Finally, although the system describes to generating of characters by vertical strokes it is equally applicable to generating characters by horizontal strokes.

What is claimed is:

1. In a system for presenting at least one graphic symbol to a record medium wherein said graphic symbol includes an area divisible into linear regions, each of said linear regions having a given width dimensions and being divisible into a plurality length elements, each of said length element having a given length dimension and each of said linear regions including at least one contiguous array of length elements having a first visual state and the remainder of said length elements having a second visual state, said contiguous array having a terminal length element at each end thereof, the combination comprising means for storing a graphic symbol block of data which is a representation of said graphic symbol, said graphic symbol block including a plurality of blockettes, each of said blockettes being associated with one of the linear regions of the area of the graphic symbol, each of said blockettes including at least a coded group of indicia for indicating at least one of said terminal length elements, and said graphic symbol block including at least one dimension control indicium for indicating either a different width dimension for one of said linear regions or a different length dimension of a terminal length element, means for scanning said record medium in a linear manner wherein each linear scan is associated with a linear region of said graphic symbol, first control means for directing said scanning means before the start of a scan to move transversely to the direction of the scans by a distance

related to at least the given width dimension of one linear region, second control means, included in said scanning means which is responsive, during each scan, to said coded group of indicia of the associated blockette for selectively energizing said scanning means for a period of time during the related scan to cause the portion of the record medium then being scanned to manifest a representation of said first visual state whereby a line having a length related to the number of length elements of said contiguous array of length elements is traced on said record medium, and means responsive to the dimension-control indicium for causing one of said control means to change the associated dimension of the trace on said record medium.

2. The system of claim 1 wherein said scanning means includes a beam of electromagnetic energy.

3. The system of claim 2 further comprising means for changing the intensity of said beam of electromagnetic energy in a manner related to the dimensions of the trace on said record medium.

4. The system of claim 2 wherein said scanning means is a cathode-ray tube assemblage

5. Apparatus for recording at least one graphic symbol on a record medium wherein said graphic symbol includes an area divisible into linear regions, each of said linear regions having a given width dimension and including at least one portion having a first visual state and the remainder having a second visual state, said apparatus comprising means for storing at least one graphic symbol block of data which is a representation of said graphic symbol, said graphic symbol block including a plurality of blockettes, each of said blockettes being associated with one of the linear regions of the area of the area of the graphic symbol represented by the graphic symbol block, each of said blockettes including a coded group of indicia for indicating the position within the linear region of the portion having the first visual state, said storing means further including means for storing at least one control indicium associated with a particular linear region of the graphic symbol means for scanning said record medium in a linear manner wherein each scan is associated with a linear region of the graphic symbol, transverse displacing means, operative before the start of a scan, for transversely displacing the upcoming scan path by a first distance related to the given width dimension of one linear region, means responsive to said control indicium for controlling said transverse displacing means to transversely displace the upcoming scan path by a distance different from said first distance when the linear scan of said record medium is associated with said particular linear region, and means responsive to at least one of the coded groups of indicia during each linear scan for selectively energizing said scanning means to cause the portion of the record medium then being scanned to manifest a representation of said first visual state.

6. The apparatus of claim 5, wherein said scanning means includes a beam of electromagnetic energy.

7. The apparatus of claim 6, further comprising means for changing the intensity of said beam in accordance with the width of the linear region being scanned.

8. The apparatus of claim 6 wherein said scanning means is a cathode-ray tube assemblage.

9. Apparatus for recording at least one graph is symbol on a record medium wherein said graphic symbol includes an area divisible into linear regions, each of said linear regions being divisible into a plurality of equal length elements wherein at least one contiguous array of length elements has a first visual state and the remainder of the length units have a second visual state, said apparatus comprising means for storing at least one graphic symbol block of data which is a representation of said graphic symbol, said graphic symbol block including a plurality of blockettes, each of said blockettes being associated with one of the linear regions of the area of the graphic symbol represented by the graphic symbol block, each of said blockettes including at least one coded group of indicia for indicating which equal length elements are in said contiguous array, said storage means further including means for storing at least one control indicium associated with a particular linear region of the graphic symbol, and means for scanning said record medium in a linear manner wherein each successive scan is transversely displaced from the preceding scan, and each of said scans is associated with one of said linear regions, energizing means connected to said storing means for receiving indicia therefrom, said energizing means during each scan energizing said scanning means for a period of time and at a time related to the number and position of the equal length elements in said contiguous array of the associated linear region to cause the portion of the record medium then being scanned to manifest a representation of said second visual state, and means responsive to said control indicium for controlling said energizing means to change the time of energizing said scanning means so that only a fraction of the length element at one end of the contiguous array associated with said particular linear region has a second-visual-state-representation manifestation on said record medium.

10. The apparatus of claim 9 wherein said scanning means includes a beam of electromagnetic energy.

11. The apparatus of claim 9, wherein said scanning means is a cathode-ray tube assemblage.

12. The apparatus of claim 9 wherein said linear regions have a given width dimension and wherein said storing means further includes means for storing at least a second control indicium associated with a particular linear region of the graphic symbol, and further comprising transverse displacing means operative before the start of a scan, for transversely displacing the upcoming scan path by a first distance related to the given width dimension of one linear region, and means responsive to said second control indicium for controlling said transverse displacing means to transversely displace the upcoming scan path by a distance which is less than said first distance when the linear scan of said record medium is associated with said particular linear region.

13. The apparatus of claim 12 wherein said scanning means includes a beam of electromagnetic energy.

14. The apparatus of claim 13 further comprising means for changing the intensity of said beam of electromagnetic energy in accordance with the presence or absence of a control indicium associated with the scan being performed.

15. The apparatus of claim 12 wherein said scanning means is a cathode-ray tube assemblage.