# United States Patent [19]

Nathan

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[45] Aug. 20, 1974


[54] **FUNCTION INTERPOLATOR**


[76] Inventor: **Amos Nathan,** 11, Habroshim Ave., Haifa, 34483, Israel



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July 7, 1971 Great Britain ..... 31851/71

[52] **U.S. Cl.** ..... **235/197,** 235/150.53

[51] **Int. Cl.** ..... **G06g 7/26**

[58] **Field of Search** ..... 235/197, 150.53, 150.52, 235/150.51, 150.5, 194; 340/347 AD, 347 PA



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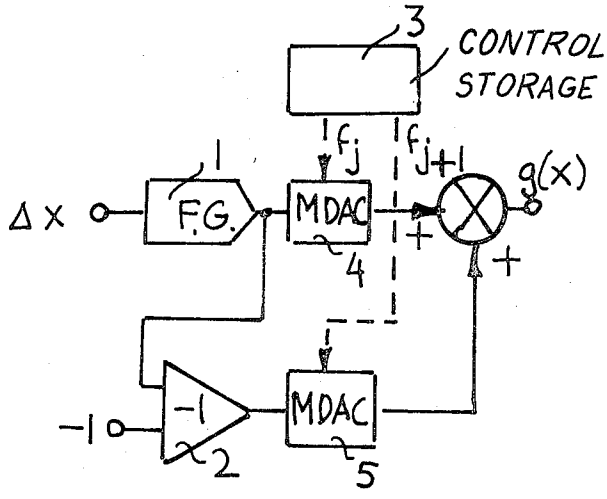
*Primary Examiner*—Joseph F. Ruggiero



[57] **ABSTRACT**

Methods and apparatus are disclosed for producing an output signal by interpolation from a finite plurality of samples representing values of a function at sample points thereof. The output signal is produced as the sum of reconstruction functions having similar shape, one each associated with each sample point and so chosen as to ensure a frequency spectrum that is substantially band-limited and an output signal that is substantially continuous when the samples are updated and to produce a constant output signal when the accepted samples are all equal.


**19 Claims, 15 Drawing Figures**



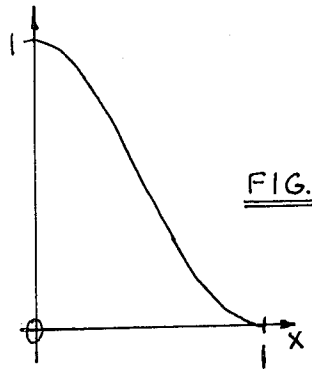



FIG. 1

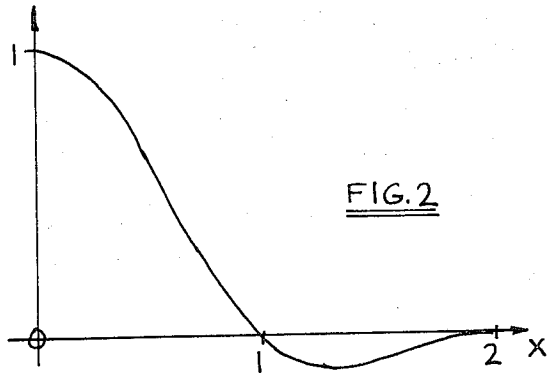



FIG. 2

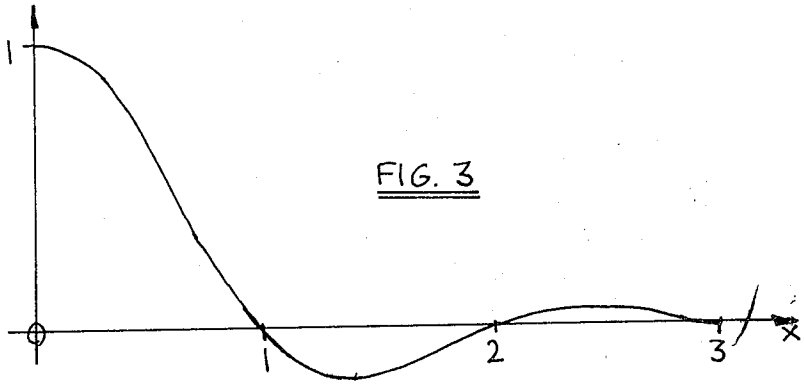



FIG. 3

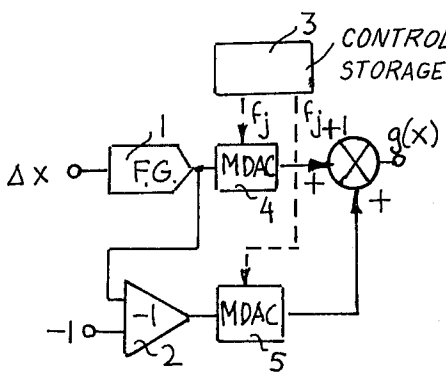



FIG. 4

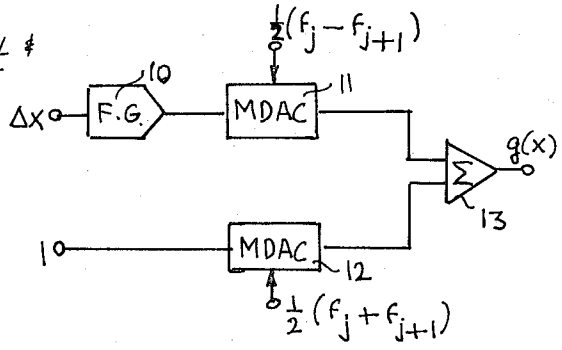



FIG. 5

BY

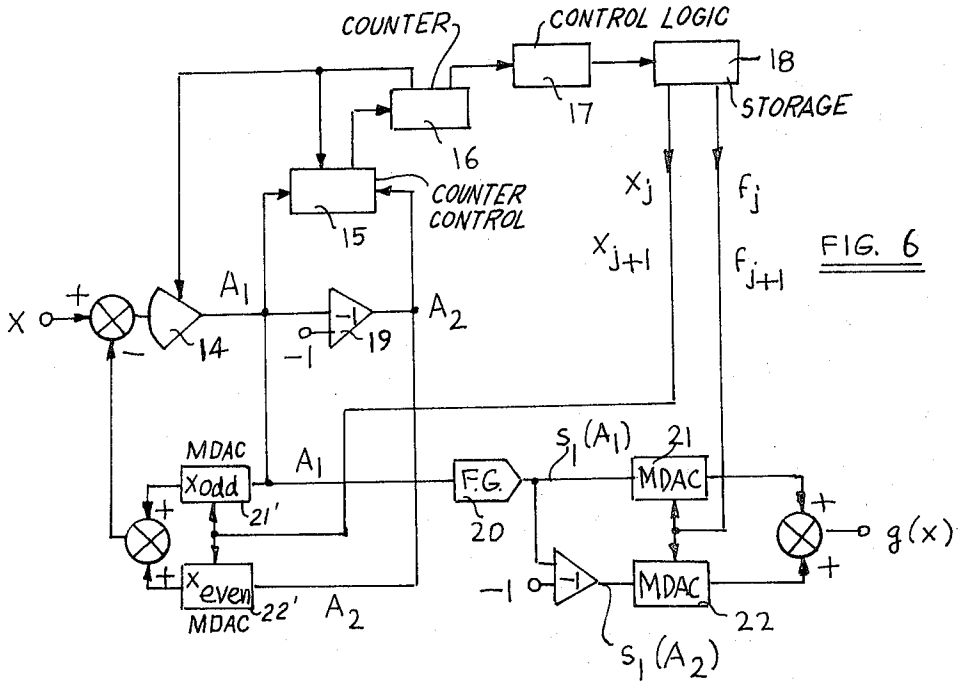



FIG. 6

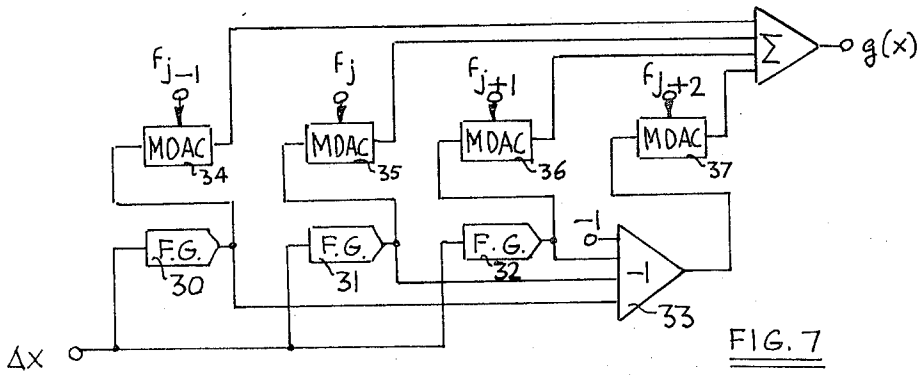



FIG. 7

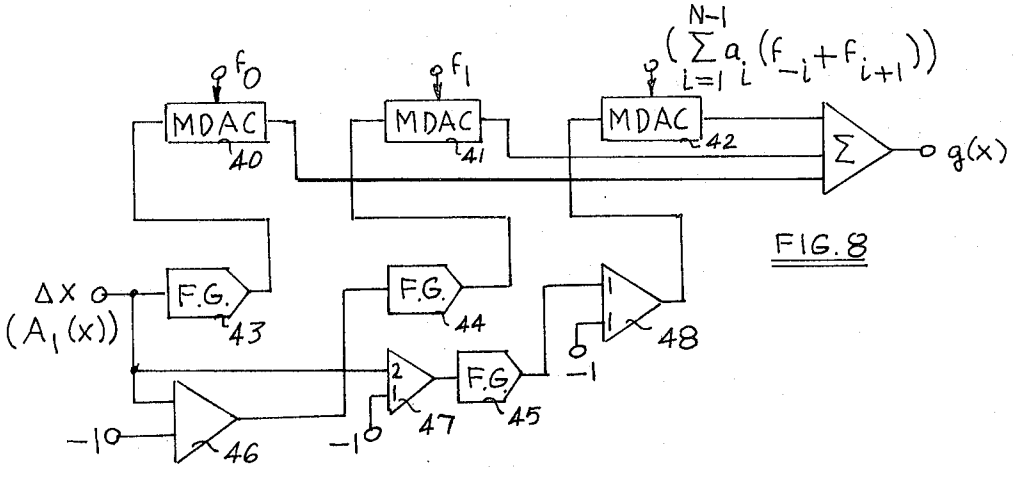



FIG. 8

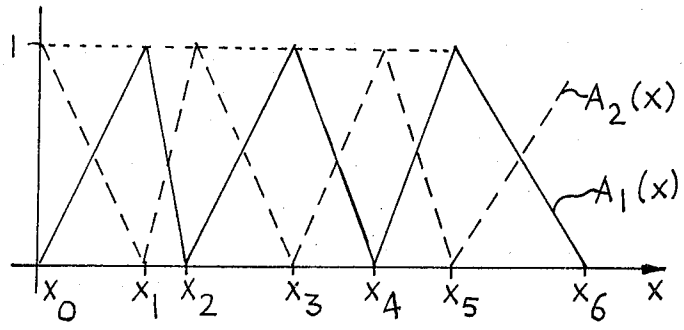



FIG. 9

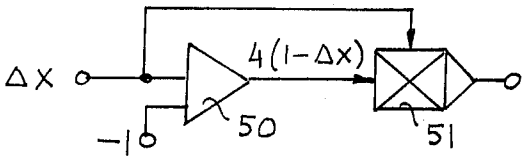



FIG. 10

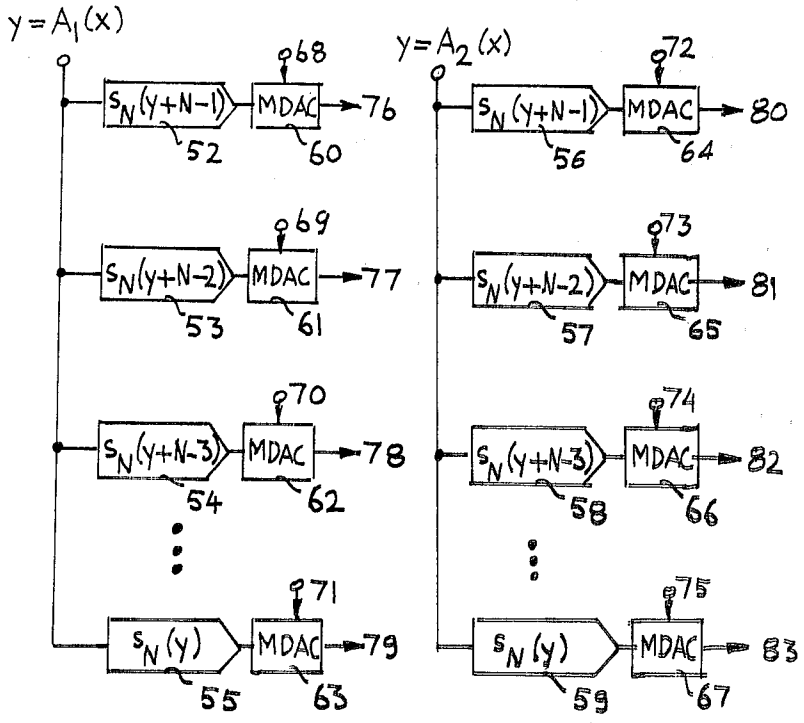



FIG. 11

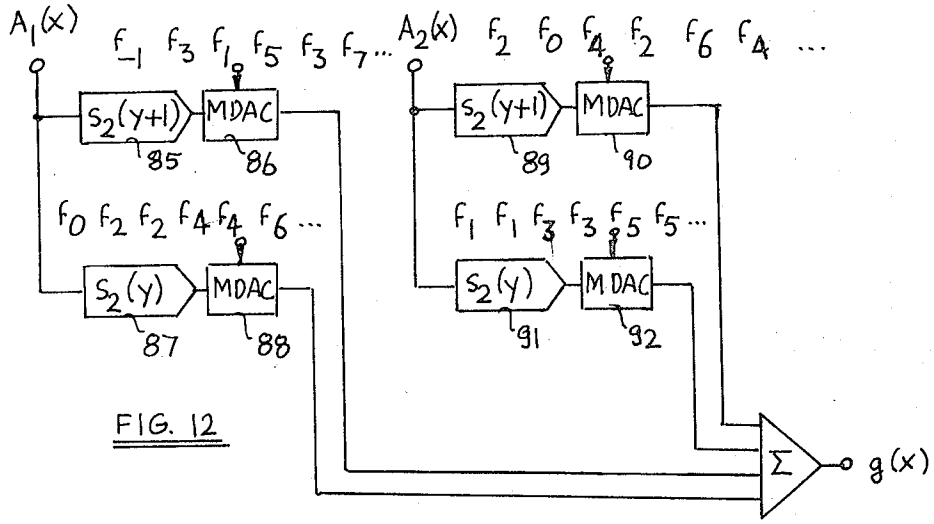

A1(x)
f-1 f3 f1 f5 f3 f7 ...
A2(x)
f2 f0 f4 f2 f6 f4 ...
S2(y+1)
MDAC
85
86
89
90
f0 f2 f2 f4 f4 f6 ...
f1 f1 f3 f3 f5 f5 ...
S2(y)
87
88
91
92
Σ
g(x)

FIG. 12

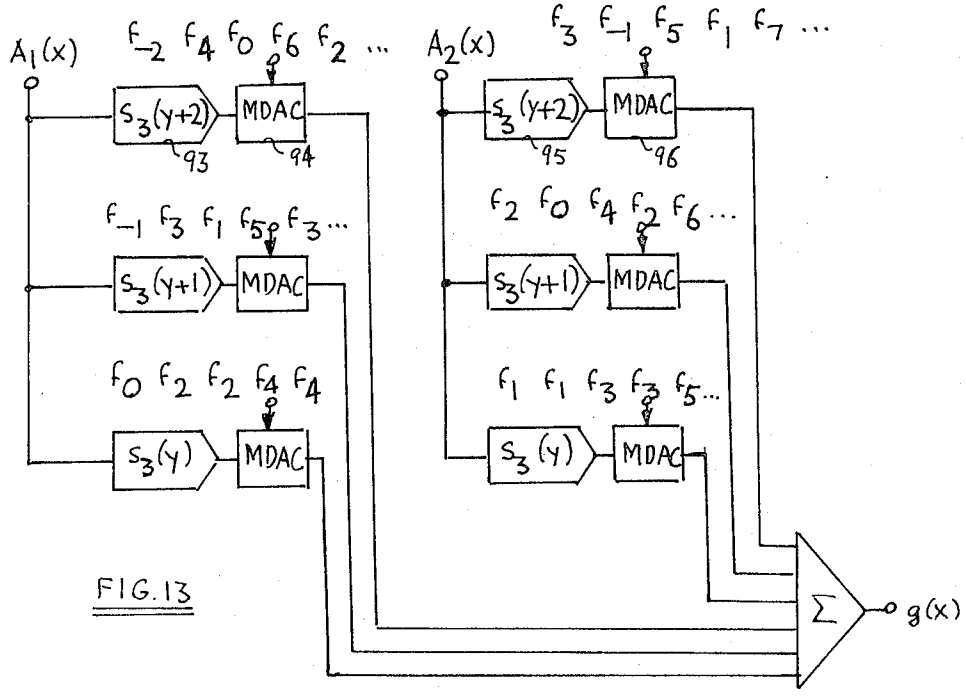

A1(x)
f-2 f4 f0 f6 f2 ...
A2(x)
f3 f-1 f5 f1 f7 ...
S3(y+2)
MDAC
93
94
95
96
f-1 f3 f1 f5 f3 ...
f2 f0 f4 f2 f6 ...
S3(y+1)
f0 f2 f2 f4 f4
f1 f1 f3 f3 f5 ...
S3(y)
Σ
g(x)

FIG. 13

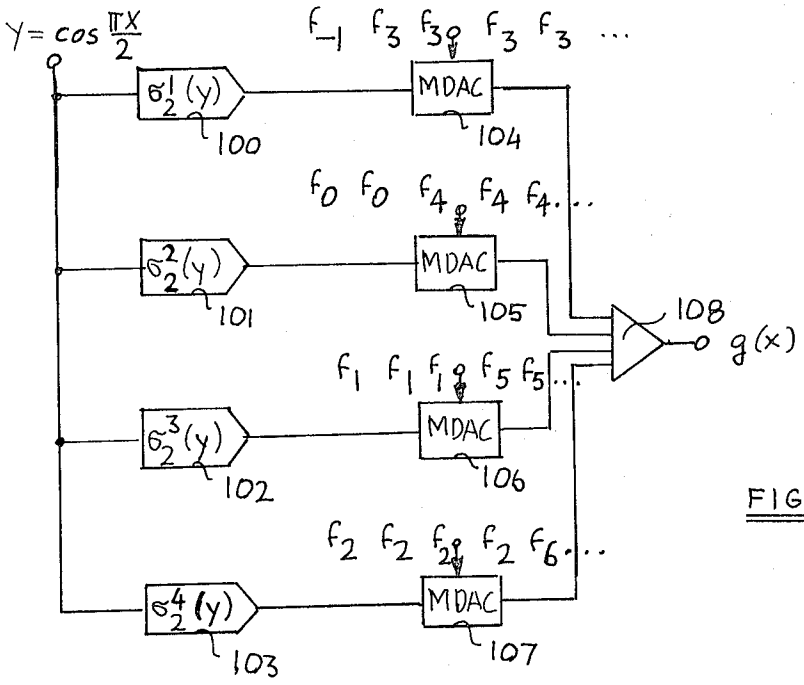

Y = cos πX/2
f-1 f3 f3 f3 f3 ...
MDAC
104
100
f0 f0 f4 f4 f4...
MDAC
105
101
108
g(x)
f1 f1 f1 f5 f5...
MDAC
106
102
f2 f2 f2 f6...
MDAC
107
103

FIG. 14

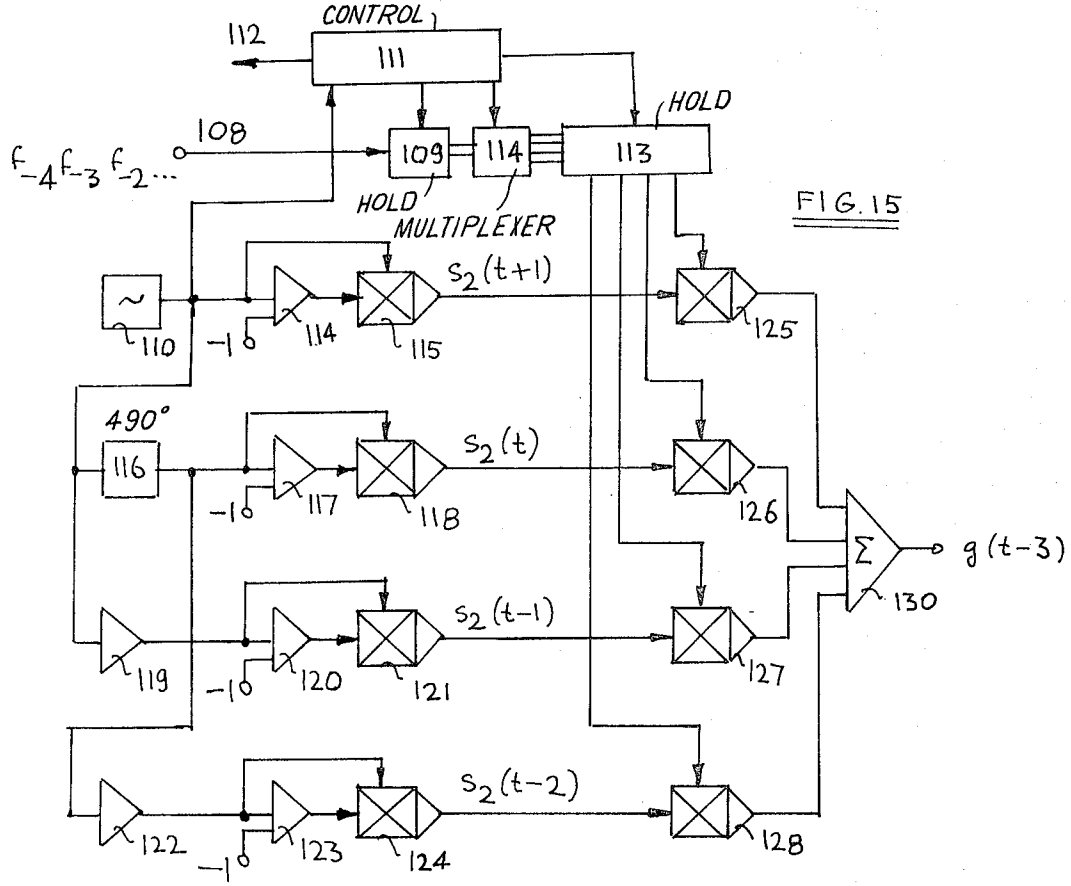

CONTROL
112
111
HOLD
108
f-4 f-3 f-2...
109
114
113
HOLD
MULTIPLEXER
S2(t+1)
110
-1
114
115
125
490°
116
S2(t)
-1
117
118
126
Σ
g(t-3)
130
S2(t-1)
119
-1
120
121
127
S2(t-2)
122
-1
123
124
128

FIG. 15

# FUNCTION INTERPOLATOR

The invention relates to interpolators, or "function generators," for a function of one or more variables wherein a substantially continuous output is produced from a finite number of samples accepted at any one instant.

Let $f(x)$ be a function of the variable $x$ and denote the samples at $x = i$ by $f_i = f(i)$, where $i$ is an integer. Given M adjacent samples, $f_j, \ldots, f_{j+M-1}$, and assuming $f(x)$ to be sufficiently smooth function, in some domain of $x$ between $x = j$ and $x = j + M - 1$, it is required to produce an approximation $g(x)$ to $f(x)$ with the help of a sampling function $s^m(x)$ such that

$$g(x) = \sum_{i=j}^{j+M-1} f_i s^M(x-i).$$

Whenever $x$ traverses an integer value the process is updated, i.e., when $x$ increases and passes through an integer value, $j$ is replaced by $j' = j + 1$ so that interpolation subsequently proceeds with the help of the samples $f_{j+1}, \ldots, f_{j+M}$. Similarly, when $x$ decreases and passes through an integer value, $j$ is replaced by $j - 1$.

According to this invention, interpolation proceeds so that $g(x)$ remains continuous during the updating process.

One prior method uses as sampling functions

$$S^M(x) = s(x) = \sin(\pi x)/(\pi x)$$

independently of the value of M. Unless M is very large, this method has the disadvantage that the resulting function $g(x)$ is far from band-limited. By band-limited is meant the restriction of the spectrum $G(f)$ of $g(x)$ to a finite frequency domain, where $f$ is the frequency and $G(f)$ is the Fourier integral of $g(x)$ defined by

$$G(f) = \int_{-\infty}^{\infty} g(x) e^{-2\pi\sqrt{-1}fx} dx.$$

Therefore, even if $f(x)$ is sufficiently closely band-limited, $g(x)$ does not, in general, provide a good reconstruction of $f(x)$ according to this prior art.

The invention will now be set forth by way of example in the following description taken in conjunction with the appended drawings in which

FIGS. 1–3 are plots of sampling or reconstruction functions used in carrying out the invention;

FIG. 4 is a schematic diagram illustrating one of the ideas underlying embodiments according to the invention;

FIG. 5 illustrates a device for producing the same function as that of FIG. 4 in a different fashion;

FIG. 6 Is a schematic diagram relating to the prior art for the production of triangular input functions $A_1(x)$ and $A_2(x)$ which are useful in connection with the invention, also shows an embodiment for the conversion of the input signal into a digital and an analog part according to the prior art and finally shows how these signals can be applied to the ideas of the invention;

FIG. 7 is a schematic diagram of an embodiment of the invention for M = 4;

FIG. 8 is a schematic diagram of an embodiment of the invention for M = 2N;



FIG. 9 are plots of triangular functions $A_1(x)$ and $A_2(x)$;

FIG. 10 is a schematic diagram of an auxiliary device used in one embodiment of the invention;

FIG. 11 relates to another embodiment of the invention for M = 2N;

FIGS. 12 and 13 relate to the special cases of FIG. 11 wherein N = 2 and N = 3, resp.;

FIG. 14 relates to yet another embodiment of the invention for N = 2; and

FIG. 15 is a schematic diagram of an embodiment of the invention for interpolating a pulse train accepted in time sequence.

The spectrum of $s(x) = \sin(\pi x)/(\pi x)$ is given by

$$S(f) = \begin{cases} 1, & |f| < \frac{1}{2} \\ \frac{1}{2}, & |f| = \frac{1}{2} \\ 0, & |f| > \frac{1}{2} \end{cases}$$

The functions $s^M(x)$ used in the method according to the invention are defined by their spectra $S^M(f)$ which are obtained from said $S(f)$ by sampling it as follows:

$$S^M(f) = \frac{1}{M} \sum_{i=-\infty}^{\infty} S(f)\delta\left(f = \frac{i}{M}\right)$$

where $\delta(f)$ is a "delta function," zero unless $f = 0$ and such that

$$\int_{-\infty}^{\infty} 8(f)G(f)df = G(0)$$

where $G(f)$ is any function that is continuous at $f = 0$; and the factor 1/M is introduced as a convenient normalization. (In the above notation, the superscript M does not denote the M-th power.) Thus $S^M(f)$ is produced by uniformly sampling at intervals of 1/M a uniform band-limited spectrum. Sampling at jump discontinuities here means taking the average of the right- and left-hand values of the function at the sampling point. The corresponding functions of $x$ are as follows:

For odd values of M :

$$S^M(x) = 1/M\,[1 + 2\cos(2\pi x/M) + 2\cos(4\pi x/M) + \ldots + 2\cos(m-1)\pi x/M],$$

For even values of M I write N = M/2 and then

$$s_N(x) = s^M(x) = 1/2N\,[1 + 2\cos\pi x/N + 2\cos 2\pi x/N + \ldots + 2\cos(N-1)\pi x/N + \cos\pi x]$$

These functions and approximations thereto are used as sampling functions in the method according to the invention.

The first few functions are therefore explicitly:

$$s_1(x) = \tfrac{1}{2}(1 + \cos\pi x)$$
$$s_2(x) = \tfrac{1}{4}(1 + 2\cos(\pi x/2) + \cos\pi x)$$
$$s_3(x) = 1/6\,(1 + 2\cos(\pi x/3) + 2\cos(2\pi/3) + \cos\pi x)$$

$$s_4(x) = \tfrac{1}{8}(1 + 2\cos(\pi x/4) + 2\cos 2\pi x/4) + 2\cos(2\pi x/4) + \cos\pi x) \ldots$$
$$s^3(x) = \tfrac{1}{3}(1 + 2\cos(2\pi x/3))$$
$$s^5(x) = 1/5\,(1 + 2\cos(2\pi x/5) + 2\cos(2\pi x/5))$$
$$s^7(x) = 1/7\,(1 + 2\cos(2\pi x/7) + 2\cos(4\pi x/7) + 2\cos(6\pi x/7)) \ldots$$

These sampling functions, for even and odd M, resp., can also be transformed into the following more concise forms:

$$s_n(x) = 1/2N\ [\ \sin\ [(1 - 1/2N)\pi x]/\sin\ (\pi x/2N) + \cos\ \pi x]$$
$$s^m(x) = 1/m\ \sin(\pi x)/\sin(\pi x/M).$$

For purposes of implementation, these last expressions are usually found to be disadvantageous, because of the zeros in the denominators.

The sampling functions have the following useful properties: ($i$,I are integers)

Symmetry:
$s_m(x) = s^m(-x)$;
$s_n(x) = s_n(-x)$

Pointwise orthogonality:
$s^m(0) = s_n(0) = 1$;
$s^m(1) = s_n(1) = 0,\ 1 \neq 0.$

Periodicity:
$s^M(x) = s^m(x + Mi)$;
$s_n(x) = s_n(x + 2Ni)$.

Restoration of unity:

$$\sum_{i=I}^{I+M-1} s^M(x-i) = 1; \quad \sum_{i=I}^{I+2N-1} s_N(x-i) = 1.$$

The last property causes the restauration of constants; i.e., if all M samples in the sum for $g(x)$ have the same value, then $g(x)$ is constant and equal to said value, in a suitable interval that is included in the sampled $x$-domain.

The above expressions for the sampling functions $s^M(x)$ and $s_N(x)$ assume sample points at integer values of the variable $x$. They are, however, quite general, because the unit interval along $x$ is arbitrary. Alternatively, taking a spacing of sampling points of X these sampling functions can be written as follows:

$$s^M(x) = 1/M\ [1 + 2\cos\ (2\pi x Mx) + 2\cos\ (4\pi x/Mx) + \ldots + 2\cos\ (M-1)\ \pi x/Mx]$$
$$s_N(x) = 1/2N\ [1 + 2\cos\ (\pi x/Nx) + 2\cos\ (2\pi x/Nx) + \ldots + 2\cos\ (N-1)\ \pi x/Nx + \cos\ (\pi x/x)\ ],$$

and $g(x)$ becomes, for even and odd M, resp.,

$$g(x) = \sum_{i=j}^{j+M-1} f_i s^M(x - iX) \quad \text{or}$$

$$g(x) = \sum_{i-j}^{j+2N-1} f_i s_N(x - iX).$$

It will be noticed that any such sampling function is a linear combination of a constant and $k$ sinusoidal functions, where $k$ is the greatest integer that is not greater than ½M. Thus for even M, $k = N = ½M$, and for odd M, $k = ½(M-1)$. Further, said $k$ sinusoidal functions have a linear frequency progression. For $s_4(x)$, for example, the basic angular frequency is seen to be $\pi/4$, and the three further frequencies are $2\cdot(\pi/4)$, $3\cdot(\pi/4)$, and $4\cdot(\pi/4) = \pi$.

FIGS. 1, 2, and 3 are plots of the functions $s_1(x)$, $s_2(x)$, and $s_3(x)$, resp.. The sampling functions are seen to assume their greatest value at $x = 0$. This property is general.

If the spectrum of $f(x)$ is substantially band-limited to the frequency domain O to F, $f(x)$ is very closely reconstructed by $g(x)$ provided that the sampling interval X is at most equal to about $(M-2)/(2MF)$, which is, for even M, equal to $(N-1)/(2NF)$, and reconstruction of $f(x)$ is still quite good for values of X up to about $(M-0.35)/(2MF)$, or, for even values of M, up to $(N-0.7)/(2NF)$. It is here assumed that M is at least equal to 3, and N is at least equal to 2.

For N = 1, reconstruction is quite close as long as $X < (0.10)/F$, approximately, and fair for

$$0.10/F \leqq x \leqq 0.15/F.$$

It is advantageous to give yet another representation of the method of interpolation and updating used in the invention. Defining

$$\text{rect } x = \begin{cases} 1, & |x| \leqq ½ \\ 0 & \text{otherwise} \end{cases}$$

and

$$t_N(x) = s_N(x)\ \text{rect}\ (x/(2N))$$

so that $t_N(x)$ represents the march of $s_N(x)$ for the duration of one period centred on $x = 0$ and vanishes outside this period, then

$$g(x) = \sum_{i=-\infty}^{\infty} f_i t_N(x-i)$$

where the sampling interval X is taken as unity without loss of generality. The advantage of this representation lies in the fact that it includes updating in as much as it holds for all values of $x$, from minus to plus infinity. The summation is seen to be over all integer values of $i$. One sampling function (or "interpolation function" — these expressions being here synonymous) $t_N(x)$ is thus associated with each sample point but it is seen that at most 2N sample values affect $g(x)$ for any given value of $x$, because the domain of $t_N(x)$ extends only over the values of $x$ for which $-N \leqq x \leqq N$. (Again, analogous results hold for odd values of M.)

Denoting by $\lfloor x \rfloor$ the greatest integer that is not greater than $x$, the last formula can also be written in the form

$$g(x) = \sum_{i=\lfloor x \rfloor - N+1}^{\lfloor x \rfloor + N} f_i s_N(x-i).$$

Similarly, for odd M,

$$g(x) = \sum_{i=\lfloor x \rfloor - 1/2M+1/2}^{\lfloor x \rfloor + 1/2M - 1/2} f_i s_M(x-i).$$

In the following examples of the invention these relations will be relied upon.

The examples relate mainly to hybrid (i.e., analog-digital) embodiments, but it will be quite clear therefrom how purely digital and purely analog embodiments can be implemented.

In hybrid embodiments, the variable $x$ is decomposed into a digital part $x_d$ and an analog part $\Delta x$, such that

$$x = x_d + \Delta x$$

where

$$x_d = \lfloor x \rfloor .$$

It follows that $O \leqq \Delta x < 1$. If the implementations are shown to hold for $\lfloor x \rfloor = 0$, they will properly perform quite in general, provided only that updating of the $f_i$

is taken care of. It is then only necessary to verify that the implementations correspond to

$$g(x)=\sum_{i=-N+1}^{N} f_i s_N(x-i);\ 0 \leqq x < 1$$

or

$$g(x)=\sum_{i=-1/2M+1/2}^{1/2M-1/2} f_i s^M(x-i);\ 0 \leqq x < 1;$$

for even or odd values of M, resp.

FIG. 4 relates to the method of this invention for the case N =1. An analog signal $x$ is first converted into the sum

$$x = x_d + \Delta x$$

where $0 \leqq \Delta x < 1$ and where $x_d$ is in digital form and $\Delta x$ is in analog form. The prior art teaches how this can be achieved and will be described in some detail later in this specification.

$\Delta x$ , in the form of a voltage, is accepted by analog function generator **1** having the transfer characteristic $s_1(y)$ for $0 \leqq y < 1$, i.e., producing from any input signal $y$ the output signal

$$s_1(y) = \tfrac{1}{2}(1+\cos\pi y) \text{ for } 0 \leqq y < 1.$$

For $0 \leqq x < 1$ there holds $s_1(\Delta x) = s_1(x)$. $s_1(x)$ is therefore produced at the output terminal of function generator **1**, because, in this instance, input signal $y$ is equal to $\Delta x$ which is equal to x. Signal changing adder **2** accepts $s_1(x)$ and $-1$ and produces therefrom

$$1 - s_1(x) = \tfrac{1}{2}(1-\cos\pi\Delta x) = \tfrac{1}{2}(1+\cos[\pi(1-\Delta x)] = s_1(1-\Delta x).$$

$s_1(x)$ and $s_1(1-\Delta x)$ are accepted by the analog terminals of the multiplying analog to digital converters ("MDAC"s) **4** and **5**, respectively, and the values $f_j$ and $f_{j+1}$ , where $j = x_d = x$, are applied in digital form to the digital input means of MDACs **4** and **5**, resp., from control and storage unit **3**, and their outputs are added to produce $g(x)$ in the $x$ domain corresponding to $x_d \leqq x < x_d + 1$. MDACs are provided by the prior art. They have an input terminal for the acceptance of an analog signal in the form of an electrical voltage (or current) and input means for the acceptance of a digital signal and produce at their output terminal an analog signal representing the product of the two input signals. In the example of FIG. **4**, the MDAC output is in the form of an electrical voltage and the addition of the outputs of the two MDACS is carried out in a non-sign changing adder, including an operational amplifier, by well-known prior art techniques. Control and storage unit **3** is a digital computer and in itself not included in the inventive matter of this invention. Function generator **1** is an analog function generator whose input and output signals are in the form of electrical potentials and whose transfer characteristic is as specified above.

The device thus produces

$$g(x)=f_j s_1(\Delta x)+f_{j+1}s_1(1-\Delta x)=f_j s_1(\Delta x)$$

$$+f_{j+1}s_1(\Delta x-1)=\sum_{i=j}^{j+1} f_i s_1(x-i)$$

$$=\sum_{i=j+N-1}^{j+N} f_i s_1(x-i), \quad \text{for} \quad N=1 \quad \text{and}$$

$$x = j+\Delta x,$$

as required, in the interval $j \leqq x < j+1$ , and, since $j$ is any integer, g(x) is properly produced for any $x$ because updating is automatically taken care of in the device as described.

The device according to FIG. **5** uses analog function generator **10** to produce from $\Delta x$ as input the output $\cos(\pi\Delta x)$ . MDAC **11** accepts at its digital input the value of $\tfrac{1}{2}(f_j - f_{j+1})$ to produce analog signal $\tfrac{1}{2}(f_j - f_{j+1})\cos(\pi\Delta x)$. MDAC **12** need not be a multiplying digital-to-analog-converter but merely a DAC (digital-to-analog-converter), its analog input being a (constant) reference voltage. **12** accepts the digital signal $\tfrac{1}{2}(f_j+f_{j+1})$ to produce analog $\tfrac{1}{2}(f_j+f_{j+1})$. These are combined in adder **13** to produce the analog signal

$$\frac{1}{2}(f_j - f_{j+1})\cos(\pi\Delta x)+\frac{1}{2}(f_j+f_{j+1})$$

$$=\frac{1}{2}f_j(1+\cos\pi\Delta x)+\frac{1}{2}f_{j+1}(1-\cos\pi\Delta x)$$

$$=f_j s_1(\Delta x)+f_{j+1}s_1(1-\Delta x)=g(x)$$

as required. Control and storage unit **3** is a digital computer which controls the supply of the digital signals.

In both examples, according to FIGS. **4** and **5**, the digital control unit is responsive to the instantaneous value of $x_d = \lfloor x \rfloor = j$. As long as $x$ is in the domain

$$x_d \leqq x < x_d + 1$$

the value of $j$ is fixed and the unit supplies $f_j$ and $f_{j+1}$ in the example of FIG. **4** and $\tfrac{1}{2}(f_j - f_{j+1})$ and $\tfrac{1}{2}(f_j+f_{j+1})$ in the example of FIG. **5**. If, now, $x$ increases through $x_d + 1$ and beyond, than $j$ is replaced by $j' = j+1$. Similarly, if $x$ decreases then as $x$ goes through $j$, $j$ is replaced by $j' = j - l$. Similarly at all integer values of $x$. Thus updating is simply taken care of by this method of implementing the invention.

One disadvantage of the methods according to FIGS. **4** and **5** is the discontinuity of the analog signal $\Delta x$ during updating. This can be overcome by the replacement of $\Delta x$ by a "saw-tooth" or "triangular" input, such as that shown as $A_1(x)$, FIG. **9**. At the same time it is shown how to adapt the invention for use with non-uniform spacing of sample points. The sample points are now at values of $x$ equal to $x_0, x_1, \ldots, x_j, \ldots$ where $x_j < x_{j+1}$ for $j = \ldots, -1, 0, 1, \ldots$. In the domain defined by $x_j \leqq x \; 21 \; x_{j+1}$ there now hold $x_d = x_j$ and the definition

$$\Delta x = (x - x_j)/(x_{j+1} - x_j).$$

The functions $A_1(x)$ and $A_2(x)$ shown in FIG. **9** are piecewise linear; they are linear between any two adjacent sample points and assume at adjacent sample points alternately the values 0 and 1. Thus the variation of $A_1(x)$ and of $A_2(x)$ is between 0 and 1. Moreover, $A_1(x) + A_2(x) = 1$.

FIG. **6** is a schematic block diagram relating to the production of $A_1(x)$ and $A_2(x)$ from x as input, given in analog form. The FIGURE also illustrates a method for the production of $x_d$ and includes means for the production of the function $g(x)$ for the case N = 1 according to the relations given above.

The part of the FIGURE relating to production of $x_d$, $A_1(x)$, and $A_2(x)$ is prior art and is taken from the following reference:

W. E. Chapelle, "Hybrid Techniques for Analog Function Generation," Proceedings Joint Spring Computer Conference 1963, pages 213–227. (In particular: Chapelle's FIG. 7 which, as far as here relevant, is included and reproduced in FIG. 6 of this specification.)

14 is a high-gain amplifier (the sign of its gain is appropriately switched in order to assure stability of the device.) 15 is the counter control, 16 the counter, 17 the control logic, and 18 the storage unit. 21′ and 22′ are MDACs receiving, from storage unit 18, $x_{odd}$ and $x_{even}$, respectively, in parallel binary digital form, and $A_1(x)$ and $A_2(x)$, respectively, in analog form to produce $A_1x_{odd}$ and $A_2x_{even}$, respectively, in analog form. For $x$ such that $x_j \leqq x < x_{j+1}$, $x_{odd}$ denotes $x_j$ or $x_{j+1}$ if $j$ or $j+1$ is odd, resp., and $x_{even}$ denotes $x_j$ or $x_{j+1}$ if $j$ or $j+1$ is even, resp.

$A_1x_{odd}$ and $A_2x_{even}$ are added and the result is differenced with x received in analog form, the resulting difference signal being fed to the input of amplifier 14 to produce analog output signal $A_1 = A_1(x)$. $A_2 = A_2(x)$ is produced therefrom in sign changing adder 19.

The feedback loop of amplifier 14 solves the equation

$$x = A_1x_{odd} + A_2x_{even}$$

where $A_2 = 1 - A_1$. Thus

$$x = A_1x_{odd} + (1 - A_1)x_{even}$$

Therefore, solving for $A_1$,

$$A_1 = A_1(x) = \frac{x - x_{\text{even}}}{x_{\text{odd}} - x_{\text{even}}} = \begin{cases} \Delta x & \text{for } x_0 \leqq x \leqq x_1,\ x_2 \leqq x \leqq x_3, \ldots \\ 1 - \Delta x & \text{for } x_1 \leqq x \leqq x_2,\ x_3 \leqq x \leqq x_4, \ldots \end{cases}$$

for $x_j \leqq x \leqq x_{j+1}$, and if $j$ is even, so that $x_{even} = x_j$, $x_{odd} = x_{j+1}$, the above relation follows at once from the definition of $\Delta x$, and if $j$ is odd, so that $x_{odd} = x_j$, $x_{even} = x_{j+1}$,

$$\frac{x - x_{\text{even}}}{x_{\text{odd}} - x_{\text{even}}} = \frac{x - x_{\text{odd}} + x_{\text{odd}} - x_{\text{even}}}{x_{\text{odd}} - x_{\text{even}}} = 1 - \frac{x - x_j}{x_{j+1} - x_j} = 1 - \Delta x.$$

It follows that $A_1(x)$ and $A_2(x)$ are indeed produced in this prior art circuit in accordance with their definitions in FIG. 9.

The production of $x_j$, $x_{j+1}$ in digital form is likewise taught by the prior art. Counter 16 is stepped up or down by unity whenever, while $x$ increases or decreases, resp., either $A_1(x)$ or $A_2(x)$ pass through zero. This is effected through counter control 15 which includes comparator circuits to detect the passage of $A_1(x)$ and $A_2(x)$ through zero as well as decision circuits to determine whether counter 16 is to be incremented or decremented. All relevant values of $x_j$ and $f_j$ are stored in storage means 18. Control logic 17 is activated by contents ($j$) of counter 16, where $j$ is determined by the relation $x_j \leqq x < x_{j+1}$ for the instantaneous value of $x$; it assigns to $x_{odd}$, $x_{even}$ the values $x_j$, $x_{j+1}$ for odd $j$, resp., and $x_{j+1}$, $x_j$ for even $j$, resp.; it also identifies the associated values $f_{odd}$ and $f_{even}$ and feeds $x_{odd}$, $x_{even}$, $f_{odd}$ and $f_{even}$ in digital form to the digital inputs of MDACs 21′, 22′, 22, and 21, resp.

$f_j$ here denotes $f(x)$ at $x = x_j$. $f_{odd}$, $f_{even}$ denote $f(x)$ for $x = x_{odd}$ and $x = x_{even}$, resp.

$A_1(x)$ is accepted by analog function generator 20 having the transfer characteristic $y$ to $s_1(y)$ and thus producing $s_1(A_1(x))$; $s_1(A_2(x)) = 1 - s_1(A_1(x))$ is produced therefrom at the output of a sign changing adder accepting $-1$ and $s_1(A_1(x))$. $s_1(A_1(x))$ and $s_1(A_2(x))$ are accepted at the analog input terminals of MDACs 21 and 22. $g(x)$ is produced from MDAC outputs $f_{odd}s(A_1(x))$ (at the output terminal of MDAC 21) and $f_{even}s(A_2(x))$ (at the output terminal of MDAC 22), by addition.

A description of the part of FIG. 6 relating to the prior art will be found in the reference paper.

$A_1(x) = 0$ whenever $x = x_j$ and $j$ is an even integer.

$A_2(x) = 0$ whenever $x = x_j$ and $j$ is an odd integer.

$A_1(x) = 1$ whenever $x = x_j$ and $j$ is an odd integer.

$A_2(x) = 1$ whenever $x = x_j$ and $j$ is an even integer.

For $x_0 \leqq x \leqq x_1$, $x_2 \leqq x \leqq x_3$, . . . , $\Delta x = A_1(x)$ and $A_1(x)$ can replace $\Delta x$.

For $x_1 \leqq x \leqq x_2$, $x_3 \leqq x \leqq x_4$, . . . , $\Delta x = A_2(x)$ and $A_2(x)$ can replace $\Delta x$.

Similarly, for $x_0 \leqq x \leqq x_1$, $x_2 \leqq x \leqq x_3$, . . . ,

$\Delta x = 1 - A_2(x)$ and therefore $1 - \Delta x = A_2(x)$;

and for $x_1 \leqq x \leqq x_2$, $x_3 \leqq x \leqq x_4$, . . . ,

$\Delta x = 1 - A_1(x)$ and therefore $1 - \Delta x = A_1(x)$.

FIG. 7 is an embodiment of the invention for N = 2. $x = \Delta x + x_d$, as before. $\Delta x$ is accepted by analog function generators 30–32 producing at their output terminals the signals $s_2(\Delta x + 1)$, $s_2(\Delta x)$ and $s_2(1 - \Delta x)$, resp. Signal $s_2(2 - \Delta x)$ is produced in this example at the output terminal of sign changer 33 according to the relation

$$s_2(2 - \Delta x) = -[-1 + s_2(\Delta x + 1) + s_2(\Delta x) + s_2(1 - \Delta x)]$$

which follows from

$$\sum_{i=-1}^{2} s_2(\Delta x - i) = 1$$

in view of the relation of symmetry $s_2(x) = s_2(-x)$. Each one of the function generators 30–32 operates only over the domain 0 . . . 1 of input signal $\Delta x$. Thus the transfer characteristics of function generators 30, 31, 32 are represented by those parts of $s_2(x)$, FIG. 2, from $x = 1$ to $x = 2$; $x = 0$ to $x = 1$; and $x = -1$ to $x = 0$ (the mirror image of the part from 0 to 1 ) resp. Production of $s_2(2 - \Delta x)$ could similarly be effected through the use of a further analog function generator, having a transfer characteristic represented by $s_2(x)$ in the domain $x = -2$ to $x = -1$ and fed by $\Delta x$. 34–37 are MDACs accepting the analog outputs of 30–33 and the digital inputs representing $f_{j-1}$, $f_j$, $f_{j+1}$, $f_{j+2}$, resp. $g(x)$ is produced by summing the outputs of MDACs 34–37. Alternatively, function generator 32 can be replaced by another function generator having the same transfer characteristic as does function generator 31 but fed by input signal $1 - \Delta x$, and the analog input signal to MDAC 37 can similarly be produced in a function generator having the transfer characteristic of function generator 30 and also fed by $1 - \Delta x$.

It will be quite clear how the method of FIG. 7 can be extended for embodiments of the invention corresponding to other values of N or of M.

FIG. 8 relates to a further embodiment of the invention. It uses approximations to the sampling functions $s_N(x)$ in order to achieve simplifications of method and

apparatus. In this example, 43 and 44 are analog function generators having transfer characteristics $\Delta x$ to $s_N(\Delta x)$, for $0 \leqq \Delta x < 1$. Sign changing adder 46 produces from $\Delta x$ the signal $1 - \Delta x$ and the outputs of 43 and 44 are therefore $s_N(\Delta x)$ and $s_N(1 - \Delta x)$, resp. During the first computing interval $x = \Delta x$ and $x_d = j = 0$, and MDACs 40 and 41 receive said analog inputs and digital signals $f_0$ and $f_1$, resp., to produce $f_0 s_N(\Delta x)$ and $f_1 s_N(1 - \Delta x)$ which are received by adder $\Sigma$. The function $s_N(x)$ is approximated for $1 \leqq |x| \leqq N$ by polynominal approximations. In this example, the approximations consist of one parabolic arc between any two adjacent sample points, such that $s_N(i + \Delta x)$ is replaced by

$$a_i \bar{s}_N(\Delta x) = a_i[1 - (2\Delta x - 1)^2] = a_i \bar{s}_N(1 - \Delta x)$$

where the constants $a_i$ (which depend upon the value of N) are suitably chosen. One set of useful values for the $a_i$ is given by the relation

$$a_i = s_N(i + \tfrac{1}{2}); \; i = 1, 2, \ldots$$

$a_1, a_3, a_5$, etc., are negative and $a_2, a_4, a_6$, etc. are positive.

Thus, approximately,

$$g(x) = f_0 s_N(\Delta x) + f_1 s_N(1 - \Delta x) + \left[\sum_{i-1}^{N-1} a_i(f_i + f_{i+1})\right] \bar{s}_N(\Delta x).$$

Sign changing adder 47 produces from $\Delta x$ and $-1$ as its inputs the output $1 - 2\Delta x$. Squarer 45 produces therefrom the signal $(1 - 2\Delta x)^2$ which is accepted by sign changing adder 48 to produce

$$[1 - (1 - 2\Delta x)^2].$$

This signal is the analog input of MDAC 42 whose digital input is

$$\sum_{i=1}^{N-1} a_i(f_{-i} + f_{i+1})$$

which is produced by digital computer means. The outputs of 40 and 41 are combined to produce an approximation to $g(x)$ for $0 \leqq x < 1$. Upon updating, the function samples $f_i$ are stepped up so that $f_0, f_1, f_2, \ldots$ are replaced by $f_1, f_2, f_3, \ldots$ resp.; subsequently by $f_2, f_3, f_4, \ldots$, resp., etc.

Alternatively, $\Delta x$ in FIG. 8 is replaced by $A_1(x)$ defined as $\Delta x$ in an even numbered interval and as $1 - \Delta x$ in an odd numbered interval, where an even or odd interval corresponds to even or odd values of $j$ in the inequality $j \leqq x < j + 1$ and $\Delta x = x - j$; $0 \leqq \Delta x < 1$. MDAC 40 now receives in successive intervals the digital input signals $f_0, f_2, f_2, f_4, f_4, f_6$, etc., and MDAC 41 receives successively $f_1, f_1, f_3, f_3, f_5, f_5$, etc.

Updating of the digital input to MDAC 42 is as before, i.e., $f_j$ is replaced by $f_{j+1}$ for all integer values of $j$. This is so because, in this example,

$$\bar{s}_N(\Delta x) = \bar{s}_N(1 - \Delta x) = \bar{s}_N[A_1(x)],$$

for all values of $x$.

FIG. 10 is a schematic diagram of another circuit for the production of the parabolic function used above. There holds the relation

$$1 - (2\Delta x - 1)^2 = 4\Delta x - 4(\Delta x)^2 = 4(1 - \Delta x)\Delta x.$$

In FIG. 10, the signal $4(1 - \Delta x)$ is produced from $\Delta x$ as input signal in sign changing adder 50 whose second input receives the signal representing $-1$. The output of 50 is multiplied in analog multiplier 51 by $\Delta x$ to produce the required function. A yet further embodiment performing the same function produces $-(\Delta x)^2$ from $\Delta x$ in a sign changing squarer and subsequently combines $\Delta x$ and $-(\Delta x)^2$.

Yet other embodiments of the invention replace the said approximation with parabolic arcs by approximations with half wave sinusoids. Thus $1 - (2\Delta x - 1)^2$ is replaced by $\sin(\pi \Delta x)$.

The function $S_N(x)$ can also be conveniently approximated in the interval $x = 0 \ldots 1$. One such method produces this function as the sum of $(1 - x)$ and $(s_N(x) - (1 - x))$ where the latter function is approximated in an analog function generator for convex functions or by polynomial approximation; it is in general sufficient to use a polynomial of the third order.

FIG. 11 relates to a general N-th order interpolator using $A_1(x)$ and $A_2(x)$ as defined in connection with FIG. 9 as input signals. Only if sampling is uniform, so that $x_j = j$, do the frequency spectrum relations described earlier hold. Nevertheless, even for non-uniform spacing there results a useful interpolator according to the method of the invention.

$A_1(x)$ is accepted by analog function generators 52, 53, 54, . . . , 55 and $A_2(x)$ is accepted by analog function generators 56, 57, 58, . . . , 59 which have the transfer characteristics defined by $y$ (as input) to

$s_N(y + N - 1), s_N(y + N - 2), s_N(y + N - 3), \ldots, s_N(y)$;
$s_N(y + N - 1), s_N(y + N - 2), s_N(y + N - 3), \ldots, s_N(y)$,

(as outputs) resp. MDACs 60, 61, 62, . . . , 63, 64, 65, 66, . . . , 67 have digital input terminals at 68, 69, 70, . . . , 71, 72, 73, 74, . . . , 75, resp. and produce one analog output signal each. These outputs are summed in summing means (not shown in the FIGURE) to yield $g(x)$.

In an even numbered interval such as

$$x = x_0 \ldots x_1, x_2 \ldots x_3, \ldots;$$

there holds

$$\Delta x = A_1(x); \; 1 - \Delta x = \Delta_2(x)$$

and in an odd numbered interval, such as

$$x = x_{-1} \ldots x_0, x_1 \ldots x_2, \ldots;$$

there holds

$$\Delta x = A_2(x), \; 1 - \Delta x = A_1(x).$$

Interval $j$, where $j$ is an integer, is here defined as $x_j \ldots x_{j+1}$.

It follows that the digital inputs to said MDACs must be as follows, during interval $j$: If $j$ is even: 60, 61, 62, . . . , 63; 67, . . . , 66, 65, 64 receive respectively

$$f_{-N+j+1}, f_{-N+j+2}, f_{-N+j+3}, \ldots, f_j;$$
$$f_{j+1}, \ldots, f_{N+j-2}, f_{N+j-1}, f_{N+j};$$

and if $j$ is odd they receive, respectively

$$f_{N+j}, f_{N+j-1}, f_{N+j-2}, \ldots, f_{j+1};$$
$$f_j, \ldots, f_{-N+j+3}, f_{-N+j+2}, f_{-N+j+1},$$

which is the same sequence in reversed order. Thus stepping up by unity entails the replacement of each $f_j$ by $f_{j+1}$ and the reversal of order.

This scheduling of digital input signals is controlled by digital computer means.

FIG. **12** relates to the special case N=**2** corresponding to FIG. **11**. The scheduling of digital inputs in successive computing intervals is explicitely noted in the FIGURE. For example, $f_{+1}, f_3, f_1, \ldots$ are the digital inputs to MDAC **86** during $x = x_0 \ldots x_1, x_1 \ldots x_2, x_2 \ldots x_3$, resp., etc. FIG. **13** similarly, relates to case N = 3 of FIG. **11**.

In FIGS. **11–13**, $s_N(y + N - 1), \ldots, s_2(y + 1), \ldots, s_3(y + 2)$, etc. define the transfer characteristics of the corresponding analog function generators. For example, function generator **85** produces output signal $s_2(y + 1)$ when receiving input signal $y$; since the input signal is, in this instance, equal to $A_1(x)$, it produces the output signal $s_2(A_1(x) + l)$.

In all previous examples of the invention the MDACs can be replaced by DACs receiving digital signals in conjunction with analog multipliers multiplying DAC outputs with the analog function generator outputs.

While the examples relate to hybrid analog-digital embodiments of the invention, it is by no means restricted thereto. For example, the invention can be carried out in purely analog or purely digital form.

Thus the functions $A_1(x)$ and $A_2(x)$ are readily produced by digital means and the analog function generators are described for example in connection with FIGS. **11–13** are readily replaced by digital computer means. This is so, in part, as the produced functions can be approximated with sufficient accuracy by polynomials of low order. For many applications it is quite sufficient to use polynomials of order three, i.e., expressions of the form

$$a + b\,(x + c(x + d(x + e)1)$$

In fact, in these expressions $a = 0$ for all function generators **52–59** with the exception of **55** and **59**.

A still further embodiment of the invention will be described in connection with FIG. **14**. $y$ is a secondary input signal defined in terms of the primary input signal $x$ by

$$y = \cos \pi x$$

The example relates to N=**2**. The identity

$$\cos \pi x = 2 \cos^2 (\pi x/2) - 1$$

yields the following expressions for $s_2$:

$$s_2(x+1) = \frac{1}{4}\left[1 - \sqrt{2}\sqrt{1 - y(x)} - y(x)\right] \equiv G_2^1(y)$$

$$s_2(x) = \frac{1}{4}\left[1 + \sqrt{2}\sqrt{1 + y(x)} + y(x)\right] \equiv G_2^2(y)$$

$$s_2(x-1) = \frac{1}{4}\left[1 + \sqrt{2}\sqrt{1 - y(x)} - y(x)\right] \equiv G_2^3(y)$$

$$s_2(x-2) = \frac{1}{4}\left[1 - \sqrt{2}\sqrt{1 + y(x)} + y(x)\right] \equiv G_2^4(y)$$

$y$ is accepted by function generators **100-103** having transfer characteristics corresponding with

$$G_2^1(y), \quad G_2^2(y), \quad G_2^3(y), \quad G_2^4(y),$$

and feeding analog output signals to MDACs **104–107**, resp. The digital MDAC inputs are: During the $j = 0$ interval (i.e., when $0 \leqq x < 1$), $f_{1181}, f_0, f_1, f_2$, resp.; during the following interval, $j = 1$ (i.e., $1 \leqq x < 2$); $f_3$, $f_0, f_1, f_2$, resp.; etc. as indicated in FIG. **14**. Thus each MDAC digital input is updated every fourth interval, when subscript $j$ advances by four (assuming increasing $x$). MDAC outputs are added in summer **108** to produce $g(x)$ as output. Function generators **100–103** are comprised of devices performing linear operations and square root extraction in accordance with the above specified relations, in well-known prior art manner.

Interpolation functions $s_N(x)$ can be expressed in terms of $\cos(\pi x/N)$ with the help of the following identities:

$$\cos 2\beta = 2\cos^2\beta - 1$$
$$\cos 3\beta = 4\cos^3\beta - 3\cos\beta$$
$$\cos 4\beta = 8\cos^4\beta - 8\cos^2\beta + 1 \ldots$$

It follows that

$$s_1(x) = \tfrac{1}{2}(1 + \cos \pi x)$$
$$s_2(x) = \tfrac{1}{2}\cos(\pi x/2)\,(1 + \cos(\pi x/2))$$
$$s_3(x) = 1/6\,(1 + \cos(\pi x/3))\,(1 + 2\cos(\pi x/3))(-1 + 2\cos(\pi x/3))$$
$$s_4(x) = \tfrac{1}{2}\cos(\pi x/4)(1 + \cos(\pi x/4))\,1 + \sqrt{2}\cos(\pi x/4))(-1 + \sqrt{2}\cos(\pi x/4)) \ldots.$$

These relations lead to yet another embodiment of the invention which is particularly useful when variable $x$ denotes time so that samples $f_i$ are now received in a temporal succession. Assuming now that this is the case we shall therefore, in conformity with common usage, replace $x$ by time $t$. The invention provudes

$$g(t-\infty) = \sum_{i=\lfloor t-\infty \rfloor - N+1}^{\lfloor t-\infty \rfloor + N} f_i s_N(t - \infty - i)$$

where $\alpha$ is a predetermined delay equal to at least N. We shall take, by way of example, $\alpha$ 3' N + 1. The example of FIG. **15** corresponds to N = 2 and a delay $\alpha = 3$. The uniformly spaced sample train $\ldots f_{-4}, f_{-3}, f_{-2}, \ldots$ is accepted at terminal **108**. Hold circuit **109** includes two hold devices which accept $f_i$ for even and odd values of $i$, resp., and hold them for the duration of two intervals, being updated thereafter. Thus $f_{-1}$, for example, is held from $t = -i$ to $t = -i + 2$ and subsequently replaced by $f_{-i+2}$. Digital control unit **111** controls the sample holding and updating operations. In this example, sinusoidal wave generator **110** (an oscillater) serves as timer for the interpolator. Its negative to positive zero crossings are accepted by control unit **111** both to time sampling through connection **112** and a sampling device connected thereto (not shown in the FIGURE) and to time the operation of hold **109**. Clock or timing circuit **110** produces the output voltage

$$\sin(\pi\, t/N) = \sin(\pi\, t/2)$$

In other examples of the invention, the incoming pulse train is used to synchronize oscillator **110** which is phase-locked thereto.

Four-channel analog multiplexer **114** distributes the contents of **109** after a delay of one interval to appropriate hold circuits in the four-hold-circuit device **113**. Operation of **114** and **113** is controlled by control unit **111**. the schedule of operations is as listed in the following TABLE I in which the contents of the two hold circuits in hold **109** and the contents of the four hold circuits in hold **113** are listed against time t. Subcolumns 1 and 2 for hold **109** and 1 through 4 for hold **113** refer to the separate hold devices included in **109** and **113**, resp.

Block **109** also contains a two-channel multiplexer controlled by **111** for scheduling the incoming signals alternately to its two separate hold circuits.

TABLE I

| Time | Hold 109 | | Hold 113 | | | |
|---|---|---|---|---|---|---|
| t | 1 | 2 | 1 | 2 | 3 | 4 |
| 0 | $f_0$ | $f_{-1}$ | $f_{-4}$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 1 | $f_0$ | $f_1$ | $f_0$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 2 | $f_2$ | $f_1$ | $f_0$ | $f_1$ | $f_{-2}$ | $f_{-1}$ |
| 3 | $f_2$ | $f_3$ | $f_0$ | $f_1$ | $f_2$ | $f_{-1}$ |
| 4 | $f_4$ | $f_3$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ |
| 5 | $f_4$ | $f_5$ | $f_4$ | $f_1$ | $f_2$ | $f_3$ |
| 6 | $f_6$ | $f_5$ | $f_4$ | $f_5$ | $f_2$ | $f_3$ |
| 7 | $f_6$ | $f_7$ | $f_4$ | $f_5$ | $f_6$ | $f_3$ |
| 8 | $f_8$ | $f_7$ | $f_4$ | $f_5$ | $f_6$ | $f_7$ |

For example, at t=1 hold circuit 1 of hold **109** transfers its contents to hold circuit 1 of hold **113** and hold circuit 2 of hold **109** is updated by replacement of its previous contents $f_{-1}$ by $f_1$. At $t = 2$, the contents of hold circuit 2 of hold **109** are transferred to hold circuit 2 of hold **113** and hold circuit 1 of hold **109** is updated by substitution of $f_2$ for $f_0$. The TABLE is readily completed for all values of t by noticing that hold **113** holds any value for the duration of four intervals and is subsequently updated so that any $f_i$ previously held is replaced by $f_{i+4}$.

What is required in this instance according to the previously given relation is

$$g(t-3)=\sum_{i=[t-3]-2+1}^{[t-3]+2} f_i s_2(t-3-i)$$

and for $0 \leqq t < 1$ therefore

$$g(t-3)=\sum_{i=-4}^{-1} f_i s_2(t-3-i)$$

$$=f_{-4}s_2(t+1)+f_{-3}s_2(t)+f_{-2}s_2(t-1)+f_{-1}s_2(t-2)$$

Now,

$$s_2(t+1) = \tfrac{1}{2}\cos(\pi\,(t+1)/2)(1+\cos(\pi\,(t+1)/2)$$

$$= \tfrac{1}{2}\sin(\pi\,t/2)(-1+\sin(\pi\,t/2))$$

In FIG. **15**, **114** is a sign preserving scaling adder receiving as inputs $-1$ and $\sin(\pi\,t/2)$ and producing their sum multiplied by ½ as output, i.e., $\frac{1}{2}(-1+\sin(\pi\,t/2))$, which is accepted by analog multiplier **115** and therein multiplied by the output $\sin(\pi\,t/2)$ of oscillator **110**. The output of multiplier **115** thus represents $s_2(t+1)$ in the form of an electrical voltage. Analog multiplier **125** receives this voltage and multiplies it by the instantaneous contents of hold circuit No. 1 of hold **113**, also supplied in the form of a voltage, to produce at the output terminal of **125** a voltage representing at $t = 0$ the signal

$$f_{-4}s_2(t+1)$$

**116** is a 90° phase shifter responsive to the output of oscillator **110** and producing therefrom the voltage $\sin(\pi(t-1)/2)$ from which there is produced the signal $s_2(t)$ by means of scaling sign preserving adder **117**, having a scaling factor of ½, and analog multiplier **118**; $s_2(t)$ is subsequently multiplied in analog multiplier **126** by the instantaneous contents of hold circuit No. 2 of hold **113** to produce at $t = 0$ the signal

$$f_{-3}s_2(t).$$

**119** is a sign changer producing from oscillator output the voltage $-\sin(\pi t/2)$, i.e., introducing a 180° phase-shift, and **122** is a sign changer connected to the output of phase shifter **116** and produces at its output terminal the voltage $\sin(\pi(t-3)/2)$. $s_2(t-1)$ and $s_2(t-2)$ are produced at the outputs of multipliers **121** and **124** with the help of sign preserving scaling adders **120** and **123**, resp., in a manner similar to that of production of $s_2(t+1)$, and they are multiplied in analog multipliers **127** and **128**, resp., by the instantaneous contents of hold circuits Nos. 3 and 4, resp., of hold **113** to yield $f_{-2}s_2(t-1)$ and $f_{-1}s_2(t-2)$, resp., at $t=0$. The expressions for the outputs of multipliers **125–128** that hold at $t=0$ continue to hold throughout $0 \leqq t < 1$. At $t = 1$ there occurs updating according to TABLE I and again at any other integer value of $t$. Adder **130** combines the four multiplier outputs to produce $g(t-3)$ according to the relation noted before. Updating takes care of the correct production of $g(t-3)$ for all values of $t$.

The circuits associated with **116** through **124** merely produce the instantaneous value of $s_2(t+1)$, which is present at the output of multiplier **115**, for an argument t shifted by one, two and three intervals. Thus $s_2(t)$ is equal to the value assumed by $s_2(t+1)$ one interval earlier. Other devices of this invention use different methods to produce $s_2(t)$, $s_2(t-1)$, and $s_2(t-2)$. In particular, storage means are used in order to introduce the required delays.

For values of N other than N = 2, there exist analogous embodiments as will be quite clear from the above illustrative example. Thus for N = 3, among other obvious changes in the circuit, hold **113** includes six hold devices and in order to be quite explicit the scheduling of values held will be given for N = 3 in TABLE II, delay $\alpha$ of 4 intervals being used.

TABLE II

| Time | Hold 109 | | Hold 113 | | | | | |
|---|---|---|---|---|---|---|---|---|
| t | 1 | 2 | 1 | 2 | 3 | 4 | 5 | 6 |
| 0 | $f_0$ | $f_{-1}$ | $f_{-6}$ | $f_{-5}$ | $f_{-4}$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 1 | $f_0$ | $f_1$ | $f_0$ | $f_{-5}$ | $f_{-4}$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 2 | $f_2$ | $f_1$ | $f_0$ | $f_1$ | $f_{-4}$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 3 | $f_2$ | $f_3$ | $f_0$ | $f_1$ | $f_2$ | $f_{-3}$ | $f_{-2}$ | $f_{-1}$ |
| 4 | $f_4$ | $f_3$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_{-2}$ | $f_{-1}$ |
| 5 | $f_4$ | $f_5$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_{-1}$ |
| 6 | $f_6$ | $f_5$ | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ |
| 7 | $f_6$ | $f_7$ | $f_6$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ |
| 8 | $f_8$ | $f_7$ | $f_6$ | $f_7$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ |

The structure of the TABLE for the general case will now be quite clear. One way of seeing this is as follows: the first row has 0, $f_0$, $f_{-1}$ in the first three columns, resp. Subsequently there appear, in this order, $f_{-2N}, f_{-2N-1}, \ldots, f_{-1}$. The first three columns are completed in an obvious manner. The last 2N columns can be written down as follows: The first thereof begins, as noted, with $f_{-2N}$. Subsequently, below, there are 2N entries $f_0$; then 2N entries $f_{2N}$; then 2N entires $f_{4N}$; then $f_{6N}$; etc. . The rest of the entries follow by noting that, starting at any position with $f_k$, say, and going one to the right and subsequently one position down, there is $f_{k+1}$.

As a further example, let the samples $f_i$ be stored in digital form. Take e.g. N = 3. From $x$, whether given in digital form or converted through analog to digital conversion from analog into digital form, digital computing means determine the function cos $[\pi(x-i)/N]$ for the instantaneous value of $x$ and for $i = -N + 1 = -2$, and subsequently compute the value of the expression

$$f_{i\ s3}(x-i) = fi/6\ (/ + \cos \pi(x-i)/3)\ (4 \cos 2(\pi(x-i)/3) - 1)$$

Next, $i$ is stepped up one to $i = -1$ and the process is repeated. Adding the results yields

$$f_{-2}s_2(x+2) + f_{-1}s_2\ (x+1)$$

The process is repeated again and again up to $i = N = 3$, inclusive, and the final result is

$$g(x) = \sum_{i=-2}^{3} f_i s_3(x-i); \quad 0 \leqq x < 1.$$

The process can be simplified by first computing all required values of cos $[\pi(x-i)/N]$and storing them. Thus,

$$\cos \pi[x-(i+N)]/N = -\cos \pi(x-i)/N\ ,$$

which halves the cosine function computation effort and also the storing requirements, for it is seen that only the N values for $= -N + 1, -N + 2, \ldots, 0$ are required. This number of values can be further reduced if $x$ is confined to the values $k/K$, where $k = 0, 1, \ldots, K-1$ and K is a positive integer. To obtain $g(k/K)$; $k = 0, 1, 2, \ldots, K-1$; there are first required the KN functions

$$\phi(i\ k) = \cos \pi(k/K - i)/N = \cos \pi(k - iK)/KN:$$

$$i = -N + 1, -N + 2, \ldots, N;$$
$$k = 0,1, \ldots, K-1.$$

But

$$\phi(i,k) = -\phi(i+N, k)$$

and in addition

$$\phi(i, k) = -\phi(N - i + 1, K - k),$$

and it is seen that the number of computed functions can be reduced.

In the above methods of interpolators according to the invention, if there is given a finite data field, i.e., a finite number of samples $f_i : f_0, f_1, \ldots, f_k$, say, and $s_N(x)$ is used as interpolating function (analogous relations holding for odd values of M) and if $g(x)$ is required at the edges of the data field, i.e., for $x < x_{N-1}$ or $x > x_{k-N+1}$, then the method cannot give results because, in the first instance $f_{-1}, f_{-2}, \ldots$ are unknown, and in the second instance $f_{k+1}, f_{k+2}, \ldots$ are unknown. This matter is readily dealt with by means of data completion. One such method uses $f_i = f_0$ ; $i > o$ and $f_i = f_k$ , $i > k$ . Another method simply sets all missing values equal to zero.

While the above descriptions are for funbsions of omd v[riable, it is evident that the method can also be applied for functions of two or more variables, provided that the samples are given at the lattice points of a rectangular or higher order cubic grid. In two dimensions, let $x_i$ , $y_j$ denote the point for which $x = i$ and $y = j$ and let $f_{ij}$ be the associated value of $f(x,y)$, and $g(x,y)$ the required approximation which is to be determined with the help of an interpolating device. Then the method is applied first for a plurality of adjacent values of $j$ and the given value of $x$, and subsequently, from the values $g(x,y_j)$ thus determined, for the given value of $y$, in complete conformity with the teachings of the prior art applying to a plurality of one dimensional function generators and their use for the generation of functions of two or more variables.

If fixed spacing of samples of $f(x)$ is used and the method is applied, and if additional function values, likewise equally spaced but with smaller spacing, are known, then it is possible to apply the method once again in order to obtain an improved "fine resolution" interpolation. For this purpose, the difference of the function $g(x)$ first computed and said additional samples is determined and subsequently the method is reapplied to these difference sample values and their (smaller) spacing, the result being added to $g(x)$.

Although this invention has been described and illustrated in detail, it is to be clearly understood that this is by way of illustration and example only and is not to be taken by way of limitation.

What I claim is:

1. A function interpolator producing an output signal in accordance with a desired function of an independent variable from a plurality (M) of samples of a function of said variable at corresponding sampling points comprising:

First circuit means for the production of at least one analog input signal representing a predetermined function of said variable;

Second circuit means for storing a plurality (M) of signals respresenting said plural samples, respectively;

Nonlinear circuit means connected to said first circuit means for producing a plurality of second output signals each representing the value of a reconstruction function for the instantaneous value of said input signal, wherein each of said reconstruction functions represents a predetermined nonlinear function of said variable;

a plurality of multiplier means each having input means for receiving one of said second output signals and at least one of said sample respresentative

signals and output means for producing thereat a third output signal;

summing circuit means connected to said plural multiplier output means summing said plural third output signals for producing said generator output signal.

2. The interpolator as defined in claim 1 wherein said predetermined nonlinear function represents a linear combination of ($k$) sinusoidal functions of said variable of predetermined relative phase, ($k$) being the greatest integer that is not greater than (½M).

3. The interpolator as defined in claim 2 wherein (M) is an even positive integer, (N) is defined as (½M), and said nonlinear function corresponds to

$$1/2N\ [\ 1 + 2\cos(\pi x/N) + 2\cos(2\pi x/N) + \ldots + 2\cos(N-1)\pi x/N + \cos\pi x],$$

($x$) representing said variable.

4. The interpolator as defined in claim 2 wherein (M) is an odd integer greater than two and said nonlinear function corresponds to

$$1/M\ [\ 1 + 2\cos(2\pi x/M) + 2\cos(4\pi x/M) + \ldots + 2\cos(M-1)\pi x/M\ ],$$

($x$) representing said variable.

5. The interpolator as defined in claim 1 wherein said second circuit means include digital circuit means and said sample representative signals are stored therein in digital form; and wherein said multiplier means receive said sample representative signals in digital form.

6. The interpolator as defined in claim 5 further comprising:

Digital control means responsive to a signal representing a predetermined function of said independent variable for updating said plural stored sample signals whenever said independent variable traverses one of said sampling points

7. The interpolator as defined in claim 5 wherein said second output signals are produced in analog form and said multiplier means are comprised of multiplying analog-to-digital converter (MDAC) means.

8. The interpolator as defined in claim 1 wherein said one analog signal produced in said first circuit means is in the form of a sinusoidal function of said independent variable.

9. The interpolator as defined in claim 8 wherein said nonlinear circuit means include analog multiplier means for the provision of the nonlinearity thereof.

10. The interpolator as defined in claim 8 wherein said second circuit means comprise digitally controlled means for storing said plural stored signals in analog form and updating said stored signals whenever said independent variable traverses a sampling point; each of said plural multiplier means being comprised of analog multiplier means.

11. The interpolator as defined in claim 1 wherein said nonlinear circuit means include linear circuit means receiving all but one of said plural second output signals for the production of a further second output signal.

12. The interpolator as defined in claim 1 wherein said one analog signal produced in said first circuit means is in the form of a sawtooth function, changing linearly as a function of said variable from a first preassigned constant value at any one sampling point to a second preassigned constant value at the adjacent sampling point and changing in value from one to the other of said first and second constant values on traversal of a sampling point.

13. The interpolator as defined in claim 1 wherein said one analog signal produced in said first circuit means is in the form of a continuous triangular wave function of said variable, being a linear function of said variable between any two adjacent sampling points and alternately assuming one and another of two preassigned constant values at adjacent sampling points.

14. The interpolator as defined in claim 13 wherein said first circuit means comprise means for the production of a second triangular input signal such that the sum of said first and second triangular signals is substantially independent of the value of said variable.

15. A nonlinear function generator responsive to a digital signal for the production of an analog output signal as a digitally controlled nonlinear function of an analog input signal comprising:

Nonlinear circuit means having input means for receiving the analog input signal and output means for producing thereat a plurality of analog reconstruction signals each characterised by a nowhere linear function of said input signal;

Digitally controlled storage circuit means for receiving the digital signal, storing a plurality of signals representing function values, and issuing selected stored signals;

Multiplier means connected to said nonlinear circuit means and said storage circuit means for receiving and multiplying each of said plural reconstruction signals and a respective stored and issued signal for producing a plurality of product signals;

Summing circuit means connected to said multiplier means summing said plural product signals to produce said analog output signal.

16. A nonlinear function interpolator responsive to a sample signal sequence for the production of an analog output signal representing an interpolation function to the sample sequence comprising:

Digitally controlled storage circuit means for storing and sequentially issuing said sample signals;

Signal generator means having output means for producing thereat, as a function of time, a plurality of reconstruction function signals, wherein said reconstruction functions are periodic in time and any one thereof represents any other thereof shifted by a predetermined time interval;

Multiplier means connected to said signal generator output means and said storage circuit means for receiving said plural reconstruction function signals and said issued signals for the production of a plurality of analog product signals;

Summing circuit means connected to said multiplier means summing said plural product signals to produce said analog output signal.

17. The interpolator as defined in claim 16 wherein said signal generator means include delay circuit means receiving one of said reconstruction function signals for the production of at least one further said reconstruction function signal.

18. The interpolator as defined in claim 16 wherein said signal generator means include means for the production of a sinusoidal signal and nonlinear circuit means receiving said sinusoidal signal for the production of said plural reconstruction function signals.

19. The interpolator as defined in claim 18 wherein said nonlinear means are comprised of linear circuit means and plural analog multiplier means.

* * * * *

# UNITED STATES PATENT OFFICE
# CERTIFICATE OF CORRECTION

Patent No. 3,831,016 Dated August 20, 1974

Inventor(s) Amos Nathan - 

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the drawing

Sheet 1, delete "BY" at bottom of page.

Sheet 5, FIGURES 14 and 15, should appear as shown on the attached sheet.

Column 1, line 10, between "be" and "sufficiently" insert -- a --.

Column 2, line 25, "f = i/M" should read -- f - i/M --.

Column 2, line 63, "2" should read -- 3 --.

Column 2, line 65, "2πx/5" should read -- $4\pi x/5$ --.

Column 3, line 54, "i-j" should read -- i=j --.

Column 4, line 10, "x" should read -- X --.

Column 5, line 30, "Signal" should read -- sign --.

Column 5, line 39, "=x" should read -- = [x] --.

Column 5, line 33, "](" should read -- ]) --.

Column 6, line 49, "21" should read -- < --.

Column 8, line 54, "$f_{j\ 1}^{-}$" should read -- $f_{j-1}$ --.

UNITED STATES PATENT OFFICE

# CERTIFICATE OF CORRECTION

Patent No. 3,831,016 Dated August 20, 1974

Inventor(s) Amos Nathan 

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 4, column 2, line 46 and column 3, lines 8, 16, 19, 20 and 22, "m" should read -- M --, all occurrences.

Column 3, lines 42 and 43, "Mx" should read -- MX --, all occurrences.

Column 3, lines 44 and 45, "Nx" should read -- NX --, all occurrences.

Column 3, lines 6, 17 and 23, "n" should read -- N --, all occurrences.

Column 3, line 45, "$\pi x/x$" should read -- $\pi x/X$ --.

# UNITED STATES PATENT OFFICE
# CERTIFICATE OF CORRECTION

Patent No. 3,831,016 Dated August 20, 1974

Inventor(s) Amos Nathan 

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 9, line 10, "1x1" should read -- |x| --.

Column 9, line 29, "i-1" should read -- i=1 --.

Column 9, line 55, "-0" should read -- - --.

Column 10, line 51, "$\Delta_2(x)$" should read -- $A_2(x)$ --.

Column 11, line 2, "$f_{-N+j+I}$" should read -- $f_{-N+j+1}$ --.

Column 11, line 12, "$f_{+1}$" should read -- $f_{-1}$ --.

Column 11, line 22, "+$\ell$" should read -- + 1 --.

Column 12, line 8, "$f_{1181}$" should read -- $f_{-1}$ --.

Column 12, line 32, between "))" and "1" insert -- ( --.

Column 12, line 39, "provudes" should read -- produces --.

Column 12, line 41, "∞" should read -- α --, all four occurrences

Column 12, line 46, "3'" should read -- = --.

Column 12, line 53, "-1" should read -- -i --.

Column 12, line 58, "later" should read -- lator --.

Column 15, line 5, "N-1" should read -- N+1 --.

Column 15, line 21, "$f_{is3}$" should read -- $f_{i}s_{3}$ --.

# UNITED STATES PATENT OFFICE

# CERTIFICATE OF CORRECTION

Patent No. 3,831,016 Dated August 20, 1974

Inventor(s) Amos Nathan 

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 15, line 21, "fi" should read -- $f_i$ --.

Column 15, line 21, "cos2(" should read $\cos^2($ --.

Column 16, line 16, "funbsions of omd" should read -- functions of one --.

Column 16, line 17, "v|riable" should read -- variable --.

Signed and Sealed this

*thirtieth* Day of *March 1976*

[SEAL]

*Attest:*

**RUTH C. MASON**
*Attesting Officer*

**C. MARSHALL DANN**
*Commissioner of Patents and Trademarks*

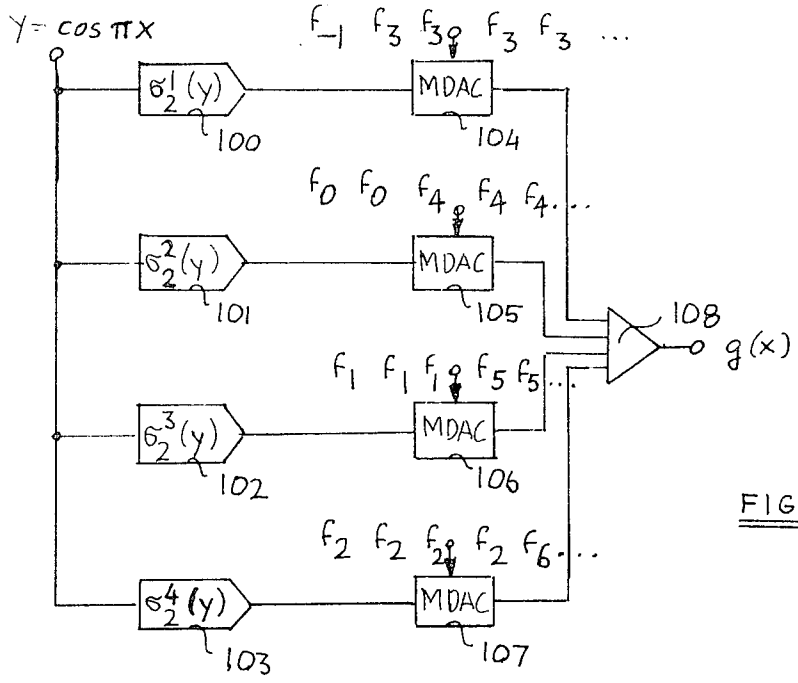

Y = cos πX
f_1 f_3 f_3 f_3 f_3 ...
MDAC
100
104
f_0 f_0 f_4 f_4 f_4 ...
101
105
108
g(x)
f_1 f_1 f_1 f_5 f_5 ...
102
106
f_2 f_2 f_2 f_2 f_6 ...
103
107

FIG. 14

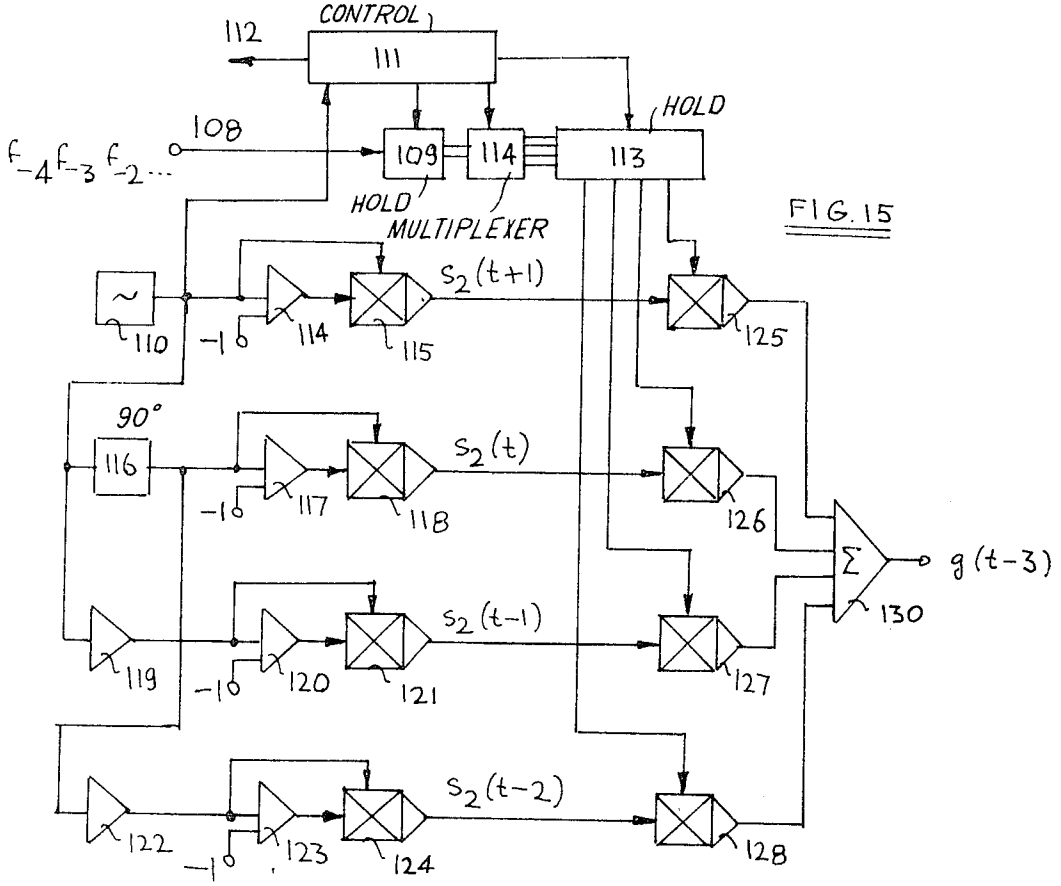

CONTROL
112
111
HOLD
108
f_-4 f_-3 f_-2 ...
109
114
113
HOLD
MULTIPLEXER
S_2(t+1)
110
-1
114
115
125
90°
116
S_2(t)
-1
117
118
126
g(t-3)
S_2(t-1)
119
-1
120
121
127
130
S_2(t-2)
122
-1
123
124
128

FIG. 15