

[54] **NON-LINEAR QUANTIZATION OF REFERENCE AMPLITUDE LEVEL TIME CROSSING INTERVALS**

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[58] Field of Search179/1 SA, 15.55 R; 328/111, 328/112

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[57] **ABSTRACT**

Method and apparatus for digitally encoding and decoding an electrical waveform such as a speech signal. The method of digitally encoding includes the steps of determining the time interval between successive occurrences of predetermined amplitudes, producing a quantized digital output indicative of the length of each time interval, modifying the quantized digital signal by the transposition of selected quantized pulse lengths into predetermined quantized pulse lengths thus producing a non-linear quantization of the digital output signal. The method of decoding comprises the steps of determining the length of each pulse of the digital signal, delaying the digital signal while adjusting the frequency response of a variable output circuit in dependence on the pulse length, and passing the signal through the now adjusted output circuit.

22 Claims, 3 Drawing Figures

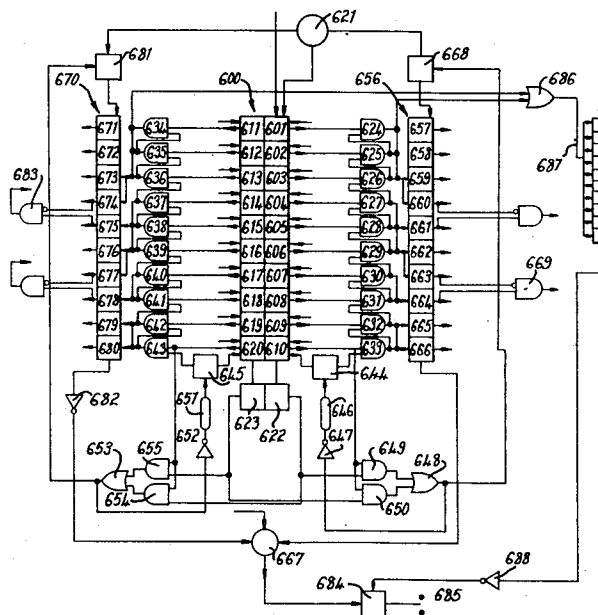
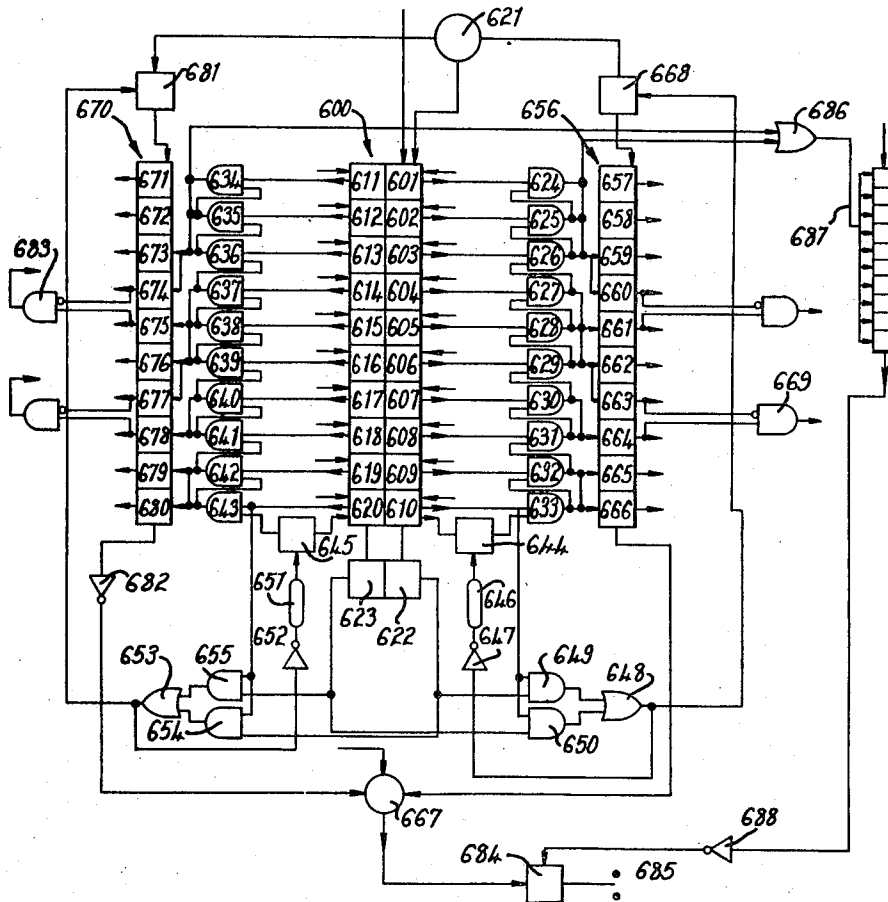


FIG. 1.

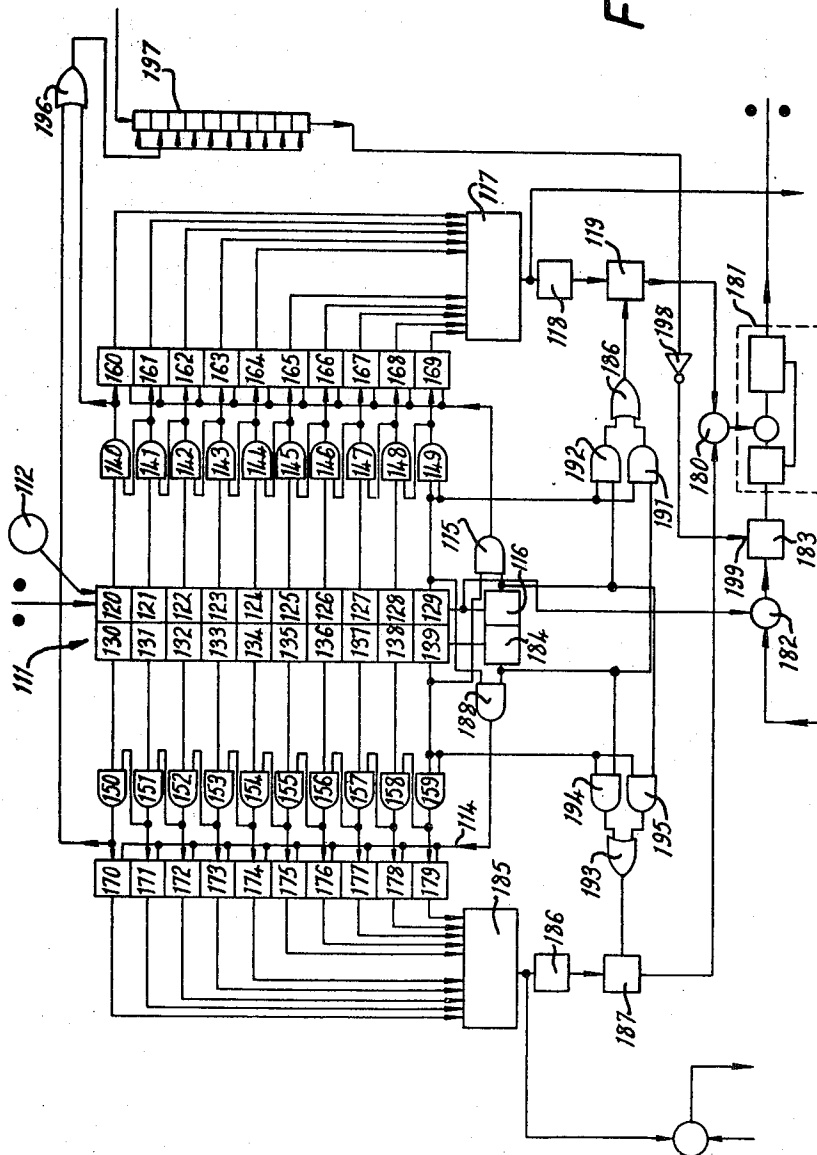


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FIG. 2.

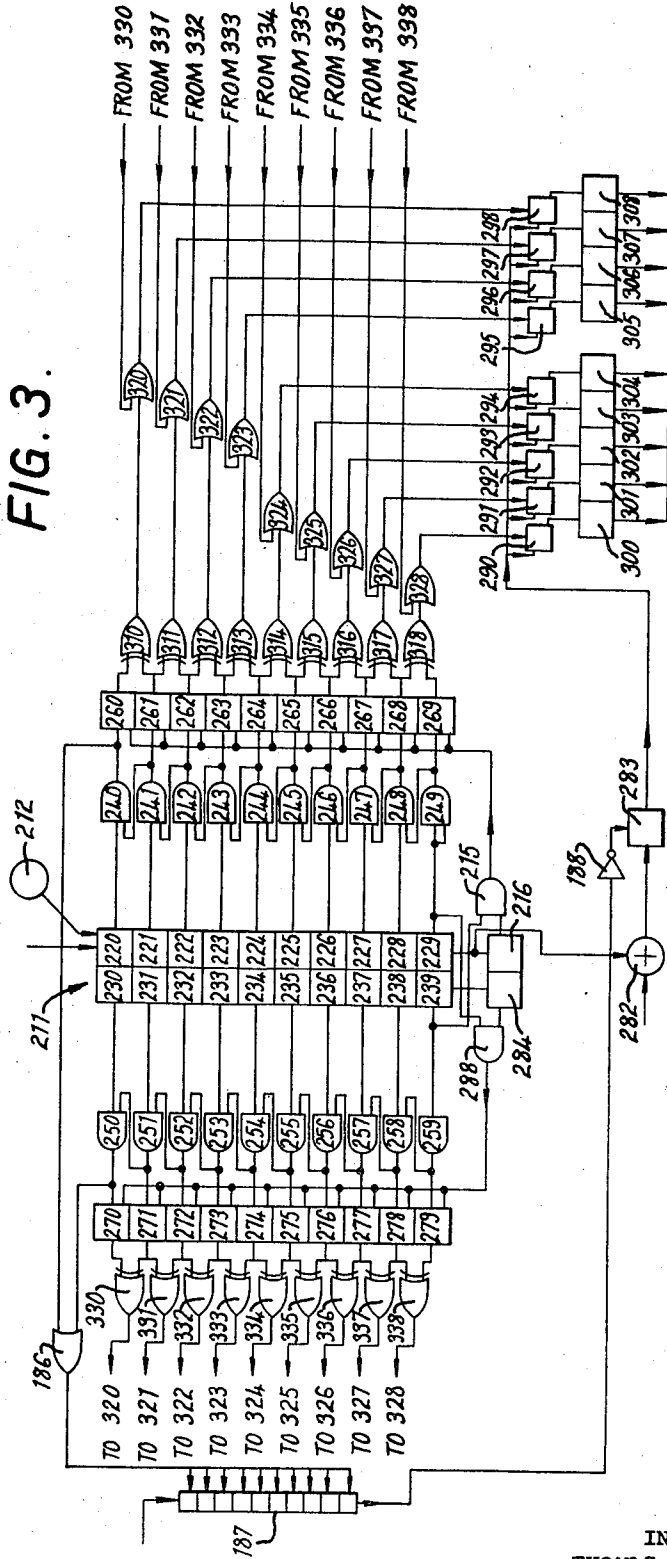


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FIG. 3.



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NON-LINEAR QUANTIZATION OF REFERENCE AMPLITUDE LEVEL TIME CROSSING INTERVALS

The present invention relates to encoding and decoding methods and circuits, and particularly, but not exclusively, to improved methods and circuits for encoding and decoding electrical signals corresponding to speech waveforms to and from a digital form.

Previously known systems for encoding speech waveforms, in general, provide an output signal which is related to the instantaneous height of the speech waveform. For example, in the so-called pulse code modulation system a speech waveform is sampled at regular intervals and a digital output signal related to the instantaneous height of the waveform is produced. This system suffers from the disadvantage that in order to produce intelligible results the frequency at which the speech waveform is sampled needs to be considerably greater than the highest frequency in the speech waveform. Thus a relatively broad bandwidth is required for transmission.

A signal which represents a function corresponding to the intervals at which a speech waveform changes sign, or achieves predetermined amplitudes, may contain substantially the whole of the information content of the speech waveform.

According to the present invention a method of digitally encoding an electrical signal representing a waveform such as a speech waveform comprises the steps of determining the time intervals between successive occurrences of predetermined amplitudes, and producing a quantized digital output indicative of the length of each said time interval.

A digital output signal produced in this manner comprises a series of time periods defined between instants when the signal changes state. The term "quantized digital output" will be understood to mean a signal which can be represented by an integral number of pulses of finite length. For example a two state digital signal comprises a rectangular waveform all the crests of which are at one level and all the troughs of which are at another. The information carried by the signal is determined by the time periods between each change of state. For convenience these time periods will be referred to herein as the "pulse length" of the signal and this term will be understood to refer to the length of a trough of a rectangular wave as well as to the length of a crest. Similarly, a multi-state signal may have, for example, a plurality of discrete amplitude states the "pulse length" of such a signal being the time period for which the signal remains in any one state.

The amplitudes which are used to determine the time intervals between successive occurrences thereof may be equal and of constant value, such as zero, or may vary in dependence on the amplitude of the waveform to be encoded or the frequency of the waveform to be encoded. A speech waveform for example, normally varies in amplitude according as the frequency varies so that the higher frequency components of the waveform are of substantially smaller amplitude than the lower frequency components. If a constant amplitude level is used to determine the said intervals the input waveform may be suitably shaped by selective amplification of the low amplitude components to ensure that they all achieve the said amplitude. The

waveform may, for example, be reduced to a square wave by infinite clipping which may be achieved by passing the signal through a high gain amplifier operated under overload conditions.

The digital output may be regarded as a train of quanta where a quantum is represented by the longest pulse which can be used in integral number to represent the waveform. Conveniently the pulse length is made at most the length of the shortest pulse of the electrical waveform to be quantized. The square waveform may be linearly quantized by passing the electrical waveform through a coincidence circuit which is also fed with the quantizing pulses in such a way that output pulses are produced which are of the same length as the quantizing pulses. A train of "1" and "0" pulses will then represent the input waveform which is however adjusted so that the pulse length of the signal is an integral number of quantizing pulses.

It will be apparent that the number (n) of quantizing pulses which represents any given pulse length of the waveform will depend on the rate of the quantizing pulses (Q) and the frequency (f) of the component of the waveform which the pulse represents in the relation:

$$n = (Q)/2f$$

Thus the lowest rate of quantizing pulses will be $Q = 2f$ so that the highest frequency will have a pulse length of 1 quantizing pulse. It can also be shown that the next longer pulse length will represent a frequency of half the highest frequency, and similarly that each longer pulse will represent a frequency which is a larger fraction of the frequency represented by the preceding pulse. For example, whereas the second shortest pulse represents a frequency of half that represented by the shortest pulse, the fifteenth shortest pulse represents a frequency of a fifteenth of that represented by the shortest pulse. In other words the lower frequency components of the waveform are quantized more finely and the higher frequency components are quantized more coarsely.

The higher frequency components of speech waveforms are, in general, more important than the lower frequency and so, in order to get these components quantized more finely the waveform may be frequency inverted before being passed to the infinite clipping circuit. This may be done, for example, by double side band modulating the signal waveform and filtering out the upper side band to leave just the lower side band which will be frequency inverted with respect to the signal waveform.

Alternatively, or in addition, the waveform may be quantized in a non-linear manner.

Preferably the quantized signal is modified by the transposition of selected quantized pulse lengths into predetermined quantized pulse lengths. Preferably the transposition is effected in such a way as to produce a substantially equal number of different pulse lengths to represent each octave within the frequency range of the original signal waveform.

According to another aspect of the invention there is provided a circuit for digitally encoding an electrical signal representing a waveform such as a speech waveform comprising means for determining the time intervals between successive occurrences of predetermined amplitudes, and means for producing a quan-

tized digital output signal indicative of the length of each said time interval.

Preferably there is provided an infinite clipping circuit for transforming the signal waveform into a rectangular waveform.

The quantized digital signal is especially suitable for processing using digital techniques such as grouping, digital addition, subtraction or multiplication to provide a coded signal of narrower bandwidth. Also the digital signal could be used with a computer programmed to recognize sequences of digits to provide, say, a typewritten output from a spoken input.

The digital signal may be decoded by filtering through a low pass filter which "rounds" the signal but this process is "noisy" and produces harmonic distortions which reduce the quality of the signal.

According to another aspect of the present invention a circuit for decoding a quantized digital signal of the type encoded in dependence on the time intervals between successive occurrences of predetermined amplitudes in the original information signal, comprising means for determining the length of each successive pulse of the signal, means for delaying the digital signal while a variable output circuit is adjusted, in dependence on the said pulse length, and then passing the digital signal to the output circuit, to provide an output waveform related to the digital signal.

Preferably the output circuit is a variable low-pass filter circuit the frequency response of which is adjusted such that the cut-off frequency is decreased to a relatively low value for a long pulse and increased to a relatively high value for a short pulse.

Thus the frequency response of an output circuit is adjusted in dependence on the pulse length of the signal such that harmonic distortion of the signal by the output circuit is reduced.

Conveniently the filter circuit is an n-pole Bessle filter.

Alternatively the variable filter circuit may comprise a plurality of fixed filter circuits each having a different frequency response and a cooperating switching circuit for selecting the appropriate filter circuit in accordance with the length of the pulse to be decoded.

The present invention also provides a method of decoding a digital signal of the type encoded in dependence on the time intervals between successive occurrences, in the original information signal, of predetermined amplitudes comprising the steps of determining the pulse length of the signal, delaying the signal while the frequency response of a variable output circuit is adjusted in dependence on the pulse length and then passing the signal through the output circuit to provide an output waveform corresponding to the digital signal.

Various embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of one embodiment of an encoding circuit;

FIG. 2 is a schematic diagram of one embodiment of a decoding circuit, and

FIG. 3 is a schematic diagram of an alternative embodiment of a decoding circuit.

FIG. 1 shows one embodiment of a non-linear encoder. A linear encoder could comprise, in its simplest

form, merely one bistable circuit or an AND gate fed with clock pulses and the signal waveform to be encoded. The output from such a circuit would be a series of "1" pulses corresponding to the peaks of the signal waveform and a "0" output corresponding to the troughs of the signal waveform. Clearly the higher the clock rate the more nearly the envelope of the output waveform will resemble the input waveform.

Referring now to FIG. 1 there is shown a circuit for encoding an input waveform in a non-linear manner. The circuit is shown simplified for the sake of clarity by the omission of a number of stages of each shift register. In FIG. 1 the shift registers are shown having 10 stages although it will be realized that the maximum number of stages used in any shift register in the encoder will be dependent on the lowest frequency, that is the longest pulse, it is wished to transmit.

The input signal is fed into the serial input of a dual shift register 600 comprising ten bistable circuits 601 to 610 and ten associated dual bistable circuits 611 to 620 the dual bistable circuits 611 to 620 are interconnected with bistable circuits 601 to 610 such that associated with each bistable circuit 601 to 610 is a dual bistable circuit which is always in the opposite state. The serial input of the shift register is also fed with clock pulses at a predetermined rate from a clock 621. The serial output from shift register 600 is fed to a bistable circuit 622 which has a dual circuit 623. The parallel output of each bistable circuit 601 to 610 is fed to one input of a respective AND gate in a bank of AND gates 624 to 633. Similarly the parallel outputs of the dual circuits of the shift register are coupled each to a respective input of AND gates 634 to 643. The other input of each AND gate is coupled to the output of its neighboring AND gate down the chain from 624, the second input of which is coupled to the output of AND gate 625, as far as 632. The second input of AND gate 633 is coupled via a controlled gate 644 to the parallel output of bistable circuit 610. The AND gates 634 to 643 are similarly interconnected, the second input of AND gate 643 being coupled to the parallel output of dual circuit 620, the last dual stage of shift register 600, via a controlled gate 645.

The control input of the controlled gate 644 is fed from a delay circuit 646 via an inverting circuit 647 from the output of an OR gate 648. The inputs to the OR gate 648 are coupled to the outputs of two AND gates 649 and 650. One input of both AND gates 649 and 650 is connected to the parallel output of the last stage 610 of the shift register 600, the other input of AND gate 649 is coupled to the output of bistable circuit 622 and the other input of AND gate 650 is coupled to the output of dual circuit 623. Thus if the last stage 610 of the shift register is in a "0" state neither AND gate 649 nor AND gate 650 will produce an output; thus OR gate 648 produces no output and the inverting circuit 647 produces a "1" output so that controlled gate 644 is open.

A similar arrangement of components 651 to 655 controls gate 645 from the parallel output of the last dual stage 620 of the shift register 600 and the output of the two bistable circuits 622 and 623. However, since circuit 610 is in a "0" state its dual circuit must be in a "1" state and similarly one or other of the circuits 622 and 623 must be in a "1" state since one is the dual

of the other, thus there will be an output from one or other of the AND gates 654, 655 and OR gate 653 will consequently produce a "1" signal which is converted to a "0" by the inverting circuit 652 and passed via delay circuit 651 to the control input of gate 645. Thus control gate 645 is shut. It will be appreciated that gates 644 and 645 are open and closed alternatively, that is if one is open the other is always shut.

Consider, for example, an input signal comprising a train of approximately four "1" clock pulses in length followed by a train of approximately four "0" clock pulses in length entering the serial input of the shift register 600. Since the register operates only when a synchronizing clock pulse is received the input signal will be accepted by the shift register as trains of exactly four clock pulses in length. The signal is passed down the shift register and has no effect until it reaches the last stage 610 of the shift register 600. Since the first element of the signal is a "1" pulse the last stage 610 of the shift register 600 must previously have been in a "0" state and thus, for reasons discussed above the gate 644 is open. The parallel output of circuit 610 passes to both inputs of AND gate 633 which therefore switches to a "1" state. The "1" output of AND gate 633 is passed to one input of AND gate 632 which, since its other input is coupled to the parallel output of circuit 609 which is in a "1" state, switches to a "1" state and passes its output to AND gate 631. This process continues until a "1" pulse is received by AND gate 629 from AND gate 630 which, since the second input is connected to the parallel output of circuit 606 which is in a "0" state, does not switch on.

The switching time of the AND gates is very much shorter than the clock pulse intervals and so this switching will be accomplished substantially instantaneously. As discussed above once the circuit 610 switches to a "1" state the gate 644 switches off after a delay determined by the delay circuit 646. This delay, although only a fraction of a clock pulse will still be substantially longer than the time taken for the AND gates 630 to 633 in the chain to switch on so that when the gate 644 closes the AND gates will have switched, as described, but will not again be affected by the parallel outputs of the shift register until the gate 644 is opened when the last stage 610 of the shift register 600 next switches to a "0" state.

The outputs of the AND gates are also coupled to the parallel inputs of a shift register 656 comprising, in this case, 10 bistable circuits 657 to 666. The connections between the AND gates 624 to 633 and the bistable circuits 657 to 666 are made in accordance with the non-linear quantization encoding pattern to be used. In this case the encoding pattern is:

IN	OUT
1	2
2	2
3	3
4	3
5	6
6	6
7	6
8	8
9	8
10	8

Thus although the input signal may vary by integers between 1 and 10 the output of the encoder will only be

pulses of one of four lengths, that is the output signal pulses will be either 2, 3, 6 or 8 clock pulses long.

In order to achieve this pattern the outputs of AND gates 633 and 632 are both connected to the inputs of bistable circuits 665 and 666 so that if only AND gate 633 is switched on its output will switch both circuits 665 and 666 to a "1" state. Similarly the outputs of both AND gates 630 and 631 are connected to bistable circuit 664 so that whether one or both of them is/are switched on the circuit 664 will be switched to a "1" state. The serial output of shift register 656 is fed out at the clock rate, (the serial input being fed from the clock 621) so that, in the example under discussion the four "1" pulses on shift register 600 will switch on the four AND gates 630 to 633 which in turn will switch the three bistable circuits 664 to 666 to a "1" state. These will be pulsed out of the serial output of shift register 656 to an adding circuit 667 where the voltage level is adjusted so that "1" and "0" signals are spaced equally on either side of a datum value, normally zero.

Meanwhile, before the first clock pulse occurs to start feeding out the "1" signals from the shift register 656, the parallel outputs from the bistable circuits 664 to 666 are fed back to the preset inputs of bistable circuits 608 to 610 to preset the state of these circuits to "1" to conform with the state of the last three stages of shift register 656. In the present case these circuits are already in a "1" state and so no change is made but if it had merely been a single "1" pulse on circuit 610 this would have caused both circuits 665 and 666 to switch to a "1" state and thus when these parallel outputs are fed back the circuit 609 would be switched from a "0" to a "1" state. It is necessary for the "1" states of the end stages of both shift registers to be the same so that controlled gate 668 which controls the serial input of shift register 656 is not prematurely closed.

Similarly to ensure that gate 668 is closed at the right time the inputs of an AND gate 669 are coupled to the parallel outputs of circuits 663 and 664 as well. The input from circuit 663 is inverted so that a "1" signal is produced by AND gate 669 whenever circuit 664 is in a "1" state while circuit 663 is in a "0" state. The output of this AND gate is coupled to the preset input of dual circuit 617 to preset this to a "1" state when a "1" pulse is produced. The circuit 607 is thus switched to a "0" state so that the last stage of shift register 600 will switch to a "0" state at the same time as the last stage of shift register 656.

This means that the four "1" pulses followed by four "0" pulses in shift register 600 have been converted to three "1" pulses followed by five "0" pulses. Thus after three clock pulses the last stage of shift register 600 will switch to a "0" state. This via OR gate 648 will switch off gate 668.

Dual circuit 620 will now switch to a "1" state. While the "1" signals were passing out of shift register 600 the last dual stage 620 of the register was in a "0" state and thus the gate 645 is open. The five AND gates 639 to 643 will be switched on as described in relation to the bank of AND gates 624 to 623. A controlled gate 681 which controls the serial input clock pulses to a shift register 670 is opened, and, after a delay determined by delay circuit 651, the gate 645 is closed.

The outputs of AND gates 634 to 643 are coupled to the parallel inputs of bistable circuits 671 to 680 form-

ing shift register 670 in a manner identical to that of the connections between AND gates 624 to 633 and shift register 656 to produce the quantizing pattern shown above. The outputs from the five AND gates 639 to 643 switch the six bistable circuits 675 to 680 to a "1" state and the six "1" pulses are passed out of the shift register, they are converted to six "0" pulses by an inverter 682 and passed to adding circuit 667.

As before the parallel outputs of the bistable circuits 671 to 680 are fed back to the preset inputs of the bistable circuits 611 to 620 to ensure that there are six "1" pulses within the dual side of shift register 600 to correspond to the six "1" pulses. Similarly an AND gate 683, having its inputs connected to the parallel outputs of circuits 674 and 675, the input from 674 being inverted, provides an output fed back to the preset input of bistable circuit 604 so that dual circuit 613 will be converted to a "0" state if seven "1" pulses are on shift register 600 since they would be transferred to form six "1" pulses on shift register 670.

If the four "0" pulses of the initial signal are followed by a further four "1" pulses these will have been shortened to three (when circuit 675 fed back a "1" pulse to dual circuit 615 to "adjust" the train of five "1" pulses in the dual side of shift register 600 to correspond with the six "1" pulses in shift register 670) and thus will pass, unadjusted, through to shift register 656 as three "1" pulses. A following four "0" pulses will be transmitted as three "0" pulses and as described above, a further following four "1" pulses will be transmitted as six "1" pulses. A continuous train of four "1" pulses and four "0" pulses will give rise to a transmitted series of three "1" pulses, six "0" pulses, three "1" pulses, three "0" pulses, six "1" pulses, three "0" pulses, three "1" pulses, six "0" pulses, and so on.

The output of the adding circuit 667 which is alternately fed with "1" pulses from shift register 656 and "0" pulses from shift register 670 is passed via a control gate 684 to an output line 685.

The gate 684 operates to cut off the output line 685 in the intervals between information signals such as the gaps between words in a speech waveform. In such cases the shift register 600 "fills up" with like pulses and this could lead to the generation of spurious signals. To prevent this the input lines of an OR gate 686 are coupled to the outputs of AND gates 624 and 634 so that if either side of shift register 600 "fills up" with "1" pulses the OR gate will switch. The output of OR gate 686 is coupled to the parallel input of a shift register 687. The serial input of shift register 687 is fed with clock pulses and the serial output is fed via an inverter 688 to the control input of gate 684. Thus if OR gate 686 produces a "1" output the whole of shift register 687 fills with "1" pulses which, after passing through inverter 688, switch off gate 684 and keep it off until the shift register 687 has cleared which, in this case, will be 10 clock pulses after the last "1" pulse from OR gate 686.

Referring now to FIG. 2 there is shown a schematic diagram of one embodiment of a decoding circuit. The input stage of the decoding circuit comprises a synchronous dual shift register generally indicated 111. The synchronization of the shift register is controlled by a clock 112. The dual shift register comprises on one side a plurality of bistable elements 120 to 129 and on

the dual side a plurality of bistable elements indicated 130 to 139. It will be understood that although only 10 bistable elements have been shown in the drawing there are considerably more than this, the total number required being determined by the longest pulse, representing the lowest frequency, to be decoded.

The one side of the shift register 111, that is the side comprising bistable elements 120 to 129, is fed with the signal to be decoded, and the dual side of the shift register 111, that is the side comprising the bistable elements 130 to 139 is fed with the inverse signal. Thus when the one side is fed a "1" the dual side is fed a "0" and vice versa.

Each bistable element 120 to 129 in the one side of the shift register 111 has a parallel output line to one input of an AND gate 140 to 149 respectively and each bistable element 130 to 139 in the dual side of the shift register 111 has a parallel output line to one input of an AND gate 150 to 159 respectively. The other input of each AND gate is connected to the output of the next succeeding AND gate in the chain apart from AND gates 149 and 159 each of which have both inputs connected together so that when the parallel output of bistable 129 or 139 transmits a "1" output the AND gates 149 and 159 respectively transmit a "1" output. Thus, for example, the output of AND gate 144 is coupled to one input of AND gate 143 the other input of which is coupled to the parallel output of bistable element 123.

The output of each AND gate is also coupled to one input of a respective bistable circuit, AND gates 140 to 149 being coupled to bistable circuits 160 to 169 respectively and AND gates 150 to 159 being coupled to bistable circuits 170 to 179 respectively. The groups of bistable circuits 160 to 169 and 170 to 179 each have a "clear" input 113 and 114 respectively which sets each circuit to give a "0" output. The bistable circuits 160 to 169, and 170 to 179 are of the type which give a "1" output after a "1" from the input line and then continue to give a "1" output regardless of the state of the input line until a "1" input is received on the "clear" line. The circuit then produces a "0" output until the next "1" signal from the input line.

The "clear" line 113 is fed from the output of an AND gate 115 the inputs from which are fed from the output of the dual bistable circuit 139 and the output of a bistable circuit 116 the input to which is fed from the output of bistable circuit 129. Since the dual bistable circuit 139 is always in the opposite state to that of bistable circuit 129 the AND gate 115 will only produce an output when the output from bistable circuit 116 is opposite to that of bistable 129, that is at the end of a train of like pulses.

For example, assuming a train of "0" signals has just passed there will be a "0" output state from bistable circuit 116 and a "1" output state from bistable circuits 126, 127, 128 and 129; bistable circuit 125 will have a "0" output state. As the bistable circuit 129 changes from its "0" state to its "1" state, passing the "0" signal to bistable circuit 116, the AND gate 149, both inputs of which are fed from the parallel output of bistable circuit 129, will produce a "1" output signal. This is passed to bistable circuit 169 to produce a "1" state of that circuit and also to one input of AND Gate 148. Since bistable circuit 128 is in a "1" state AND gate

148 produces a "1" output which switches bistable circuit 168 to a "1" state and passes to one input of AND gate 147. This process is repeated setting bistable circuits 167 and 166 to their "1" states. When the "1" output of AND gate 146 is passed to the input of AND gate 145 the process stops because bistable circuit 125 is in a "0" state and thus no output is produced by AND gate 145. Thus only bistable circuits 166 to 169 are set into a "1" state even though one or more of the bistable circuits 120 to 124 in the shift register may be in a "1" state it is not transmitted via its appropriate AND gate as the chain is broken by the first "0" state. Since the switching time of the AND gates is in the region of microseconds and the clock pulse rate is in the region of milliseconds the time taken to set the bistable circuits 166 to 169 to their "1" states is negligible.

The "1" outputs of the bistable circuits are all passed to an adding circuit 117 which produces a voltage signal proportional to the number of circuits in the "1" state. The output of the adding circuit is passed to a reciprocal circuit 118 which gives an output voltage inversely proportional to the sum of the number of circuits in the "1" state and thus inversely proportional to the number of pulses in the train and approximately proportional to the frequency which this pulse train represents. The output of the reciprocal circuit is passed via a gate 119 to the control input 180 of a variable filter 181 the pass band of which is variable in dependence on the voltage applied to the control input 180. That is a relatively high voltage at the control input 180 produces a relatively wide pass band of the filter and a relatively low voltage at the control input 180 produces a relatively narrow pass band of the filter.

As mentioned above the switching time for the AND gates and bistable circuits is very much less than the clock pulse intervals and so the pass band of the variable filter is adjusted effectively as soon as the bistable circuit changes to a "1" state. The output of the bistable circuit is connected via an adjusting circuit 182 and a controlled gate 183 to the input of the variable filter 181. The purpose of the adjusting circuit 182 is to make the "0" and the "1" signals equally spaced about a datum voltage, normally zero, as most bistable circuits produce an output which is not equi-polar. The purpose of the gate 183 will be described later.

The bistable circuit 116 has a dual bistable circuit 184 which is fed from the output of bistable circuit 139 which is the dual circuit of bistable circuit 129. When the first of a train of "0" pulses arrives at circuit 129 there will be a "1" pulse in circuit 116 a "0" pulse in circuit 184 and a "1" pulse in circuit 139. The AND gate 115 thus produces a "1" output which is transmitted along the "clear" line 113 to set all the bistable circuits 160 to 169 to their "0" state. The inputs to AND gate 149 from bistable circuit 129 are two "0" pulses, thus AND gate 149 produces a "0" output and consequently all the AND gates 140 to 148 are similarly set to a "0" state in which they will all remain until a "1" pulse next reaches bistable circuit 116.

The AND gate 159 however has both its inputs connected to the output of dual bistable circuit 139 thus a "1" output from AND gate 159 is produced when a "0" pulse is received by bistable circuit 129. The AND gates 150 to 159 are coupled together and to bistable circuits 170 to 179 in the manner described in relation

to AND gates 140 to 149 and bistable circuits 160 to 169 so that a train of "1" pulses on dual bistable circuits 130 to 139 with one end at bistable circuit 139 will cause the corresponding AND gates in the chain 150 to 159 to produce a "1" output and set the corresponding bistable circuits in the chain 170 to 179 to a "1" state. Thus a chain of "0" pulses on the shift register with one end at bistable 129 will cause a corresponding number of shift registers in the chain to switch to a "1" state and produce a "1" output to be added in an analogue adding circuit 185. The adding circuit 185 produces an output voltage proportional to the number of bistable circuits in the chain 170 to 179 which are in the "1" state. The output from the analogue adder passes through a reciprocal circuit 186 which is identical with reciprocal circuit 118, a gate 187, the purpose of which will be described later, to the control input 180 of the variable filter 181. Thus the variable filter is set in accordance with the number of "0" pulses in the train in a like manner to that described for the train of "1" pulses.

The state of the bistable circuits 170 to 179 remains the same while the train of "0" pulses is passed through the filter until a "1" pulse is received at the bistable circuit 129. The dual bistable circuit 139 is then in a "0" state. Circuit 116 is then in a "0" state (the last "0" of the train) and dual bistable circuit 184 is in a "1" state. The two inputs of an AND gate 188 the output of which is coupled to the "clear" line 114 of the group of bistable circuits 170 to 179 are connected respectively to the outputs of bistable circuit 129 and bistable circuit 184. Thus when the state of bistable 129 becomes different from that of bistable circuit 116 a "1" output is produced by the AND gate 188 to clear all the bistable circuits in the group 170 to 179.

Thus the pass band of the filter 181 is adjusted by a signal from the shift register comprising bistable circuits 120 to 129 via the AND gates 140 to 149 and the bistable circuits 160 to 169 for a series of "1" pulses in the digital signal and the pass band of the filter 181 is adjusted by a signal from the dual shift register comprising bistable circuits 130 to 139 via AND gates 150 to 159 and bistable circuits 170 to 179 for a series of "0" pulses in the digital signal. Since the signal comprises alternate trains of "1" and "0" pulses the groups of circuits associated with one "side" of the shift register 111 and the groups of circuits associated with the dual "side" of the shift register 111 operate alternately to control the filter 181.

During periods when the dual side is in operation, that is when a train of "0" pulses is being passed through the filter 181, the group of AND gates 140 to 149 produce no output signal and the group of bistable circuits 160 to 169 are all in a "0" state. The analogue adding circuit 117 thus produces no output and as a consequence the reciprocal circuit 118 produces its highest output, this output is unwanted and would produce a spurious adjustment of the filter 183 if it were to be passed to the filter control gate 180. This is prevented however by the gate 119 which is controlled by the output of an OR gate 189. The gate 119 is open when a "1" pulse is applied to the control input 190 whereupon the output is the same as the input: when a "0" pulse is applied to the gate 190 however the output is held at "0." Each of the two inputs to the OR gate

189 is fed by the output of an AND gate 191 and 192 respectively. The inputs to AND gate 191 are taken from the output of bistable circuit 129 and dual bistable circuit 184, and the inputs to AND gate 192 are taken from the outputs of bistable circuit 129 and bistable circuit 116. Thus providing there is a "1" pulse at bistable circuit 129 forming the last stage of the shift register 111 and either bistable circuit 116 or its dual circuit 184 is in a "1" state the gate 119 will be open. Now since at all times one or other of the dual circuit 184 and bistable circuit 116 is in a "1" state the gate 119 will be open whenever there is a "1" pulse at the last stage 129 of the shift register 111. Conversely, since the inputs of both AND gates 191 and 192 are tied to the output of bistable circuit 129 the gate 119 will always be closed whenever a "0" pulse reaches the last stage 129 of the shift register 111.

Similarly the output of an OR gate 193 is connected to a control gate 194 of the controlled gate 187. The inputs to the OR gate 193 are connected to the outputs from two AND gates 194 and 195 the inputs of which are both coupled to the output of the last dual stage 139 of the shift register 111 and respectively coupled one to the output of bistable circuit 116 and one to its dual circuit 184. Thus, in the same way as discussed for gate 119 the gate 187 is open whenever there is a "0" pulse at the last stage 129 of the shift register 111 and closed whenever there is a "1" pulse at the last stage 129 of the shift register 111.

There may be intervals, during the transmission of the digital signal when no information is being transmitted, for example, if a speech waveform is being transmitted these intervals occur between words. During these intervals the bistable circuits 120 to 129 all achieve a "0" state and their dual circuits 130 to 139 all achieve a "1" state. An unwanted adjustment of the variable filter 181 would then take place and a spurious low frequency "noise" signal would result. The gate 183 mentioned above is arranged to close in these circumstances so that no signal is passed to the filter 181. A respective input to an OR gate 196 is coupled to the output of each AND gate associated with the first stage of the shift register 111, that is AND gates 140 and 150, (a low frequency signal filling the shift register with "1" signals and the dual register with "0" signals will likewise produce an unwanted "noise" signal). The output of the OR gate 196 is fed to the parallel input of each stage of a shift register 197 having the same number of stages as the shift register 111. The serial input of the shift register 197 is fed with clock pulses from the clock 112 which feeds the shift register 111. The serial output of the shift register 197 is fed via an inverter 198 to the control gate 199 of the controlled gate 183. Thus when the shift register 111 fills with "0" or "1" pulses the OR gate produces a "1" pulse which is fed to the parallel input of each stage of the shift register 197. While the shift register remains filled with "1" or "0" pulses the OR gate remains open and the shift register 197 produces a series of "1" pulses at its serial output, these are passed to the inverter 198 which produces a "0" pulse output for every "1" pulse input. The controlled gate 183 is thus closed and kept closed so that there is no input to the variable filter, and therefore no output, as required. When the first "signal" pulse (a "0" or a "1" depending on what the

shift register 111 is filled with) is received at the first stage 120 of the shift register 111 the OR gate 196 is closed. The next clock pulse produces a "0" pulse at the first stage of the shift register 197. With successive clock pulses this "0" pulse is passed along the shift register 197 in unison with the first "signal" pulse in the shift register. When the "0" pulse reaches the last stage of the shift register 197 the "signal" pulse will be at the last stage 129 of the shift register 111 and the frequency response of the variable filter 181 will be set in accordance with the number of like pulses following the first "signal" pulse as described above. With the next clock pulse the "0" signal is passed out of the shift register 197 to the inverter 198 which produces a "1" pulse to open the gate 183 and thus let through the "signal" pulse from the shift register 111.

The shift register 197 continues to produce output "0" pulses and so keep the gate 183 open until the shift register again fills with like signal pulses ("1" or "0") when the OR gate 196 will again produce a "1" pulse to set the whole of the shift register to a "1" state and thus close the gate 183 at least until the shift register 187 (and consequently the shift register 111) completely passes through its contents at the time when the OR gate 196 was opened. This therefore provides a convenient limit on the lowest frequency which the decoder will produce since any frequency lower than that producing a number of pulses equal to the number of stages in the shift registers 111 and 197 will automatically produce no output signal from the filter 181.

In this embodiment the variable filter is of the kind whose pass band can be varied by the variation of an analogue control signal, as described above. In an alternative embodiment, described below, a plurality of filters, each having a different pass band, are provided and a digital control signal is used to select the appropriate filter. A suitable circuit is illustrated in FIG. 3.

Referring now to FIG. 3 a dual shift register 211 is connected to receive clock pulses from a clock 212 and the data input signal to be decoded. The parallel output of bistable circuits 220 to 229 and dual bistable circuits 230 to 239 of the dual shift register 211 are connected to AND gates 240 to 249 and 250 to 259 the outputs of which are coupled to respective shift registers 260 to 269 and 270 to 279 in an identical manner to the similar circuits of the embodiment of FIG. 2. A bistable circuit 216 having a dual bistable circuit 284 is connected to the serial output of the shift register 211 to control AND gates 215 and 288 which respectively provide appropriate "clear" outputs to the banks of bistable circuits 260 to 269 and 270 to 279 whenever the state of bistable circuit 216 is different from that of bistable circuit 229 as described in relation to the similar elements in the embodiment of FIG. 2. The data signal passes from the output of bistable circuit 229 to an adjusting circuit 282 where it is adjusted so that the "1" and the "0" signals are equally spaced on either side of a datum level (normally zero) and thence via a gate 283 to a bank of gates 290 to 298 and, depending on which gate is open, to one of a bank of filters 300 to 308.

The gate 283 is controlled by an OR gate 186 the inputs to which are coupled to the outputs of the AND gates 240 and 250 associated respectively with the first

stages 220 and 230 of the dual shift register 211; the output of the OR gate 186 is coupled via a shift register 187 and an inverter 188 to the control input of the gate 283 to cut off the output signal when the shift register "fills up" with like pulses during the intervals between units of information in the signal.

The appropriate filter for any series of pulses is selected as follows. Consider a train of four "1" pulses arriving down the shift register when the first "1" pulse has just been transferred to bistable circuit 229. The dual bistable circuit 239 will thus be in a "0" state as will bistable circuit 216 and the dual circuit to 216 will thus be in a "1" state. The AND gate 288 produces a "1" signal to clear the bank of shift registers 270 to 279 and because of the way the AND gates 250 to 259 are connected this bank of shift register (270 to 279) will remain cleared until the end of the train of "1" pulses the head of which has just reached bistable circuit 229.

The inputs of AND gate 249 are both connected to the parallel output of bistable circuit 229 so it will produce a "1" pulse and trigger AND gates 248, 247 and 246 in succession, that is up to the last "1" pulse in the train. The chain is broken there and the remaining AND gates in the chain will remain closed. The outputs of the AND gates passes to a bank of parallel connected shift registers 260 to 269 and shift registers 266 to 269 will switch to a "1" output state due to the "1" input produced by the appropriate AND gates. A bank of exclusive OR gates 310 to 318 are connected with each of two inputs coupled to the output of one of a pair of adjacent bistable circuits in the bank 260 to 269. Thus the exclusive OR gate 310 has one input coupled to the outputs of bistable circuit 260 and one input coupled to the output of bistable 261 and exclusive OR gate 311 has an input from circuit 261 and an input from circuit 262 and similarly down the chain so that an output from the exclusive OR bank 310 to 318 occurs in the present example from exclusive OR gate 315, which is coupled to the last bistable circuit of the chain in the "1" state and the first bistable circuit in a "0" state.

The output from the exclusive OR gate 315 is passed to the control gate of the controlled gate 293 in the bank 290 to 298 via an OR gate 325 in a bank 320 to 328 to couple the serial output of the shift register 211 to the filter circuit 303. A second input to each OR gate in the bank 320 to 328 is coupled to the appropriate output of a bank of exclusive OR circuits 330 to 338 coupled in the same way as the bank 310 to 318 but to the dual side of the decoder to handle the "0" pulses of the signal. Thus depending on the length of the pulses, an appropriate filter circuit is selected from the bank 300 to 308 by opening a gate determined by the position of the last pulse in the train when the first one reaches the end of the shift register 211 and is about to be passed to the filter bank. The bistable circuits will remain in the state determined at this instant until a "clear" signal is received along the "clear" line whereupon the dual side of the decoder will be set to handle the next train of pulses which will be a train of "0" pulses. As mentioned earlier the switching time of the AND gates and bistable circuits is very much shorter than the clock pulse intervals and so the gate to the appropriate filter circuit is opened substantially instantaneously with the reception by circuit 129 of the first of a train of pulses.

What we claim is:

1. A method of digitally encoding an electrical input signal representing a waveform such as a speech waveform, comprising the steps of:

- a. determining the time intervals between successive occurrences of predetermined amplitudes,
- b. producing a first electrical output signal having pulses of different lengths, each indicative of respective said time intervals,
- c. quantizing said first electrical output signal to provide a digital electrical output signal, and
- d. providing pulses of a predetermined length from selected quantized pulse lengths of said digital electrical output signal to effect a non-linear quantization of said first electrical output signal.

2. The method of claim 1 wherein said predetermined amplitudes have a constant value.

3. The method of claim 1 wherein said predetermined amplitudes vary in dependence on either or both the amplitude and frequency of said electrical input signal.

4. The method of claim 1 further comprising the step of: preferentially amplifying the components of the frequency spectrum of said input signal which characteristically have a low amplitude to ensure that said components achieve said predetermined amplitudes.

5. The method of claim 1 further including: the step of frequency inversion of said electrical input signal prior to the step of determining said time intervals between successive occurrences of predetermined amplitudes.

6. The method of claim 1, wherein said quantization is effected by passing said first electrical output signal to one input of a coincidence circuit the other input of which is fed by a signal of predetermined substantially constant frequency.

7. The method of claim 6, wherein said predetermined substantially constant frequency is at least twice the highest frequency of the electrical input signal.

8. The method of claim 1, wherein said non-linear quantization is effected in such a way as to produce a substantially equal number of different pulse lengths to represent each octave within the frequency range of the original signal waveform.

9. A circuit for encoding an electrical input signal representing a waveform such as a speech waveform, comprising: means for determining the time intervals between successive occurrences of predetermined amplitudes and for providing a first electrical output signal having pulses of different lengths each indicative of the length of respective said time intervals; means for quantizing said pulse lengths of said first electrical output signal to produce a digital electrical output signal; and means for providing quantized pulses of a predetermined length from selected quantized pulse lengths of said digital electrical output signal to effect a non-linear quantization of said first electrical output signal.

10. The circuit of claim 9 wherein there are provided means for selectively amplifying components of the frequency spectrum of the input signal which characteristically have a low amplitude to ensure that these components achieve said predetermined amplitudes.

11. The circuit of claim 9, wherein said means for providing said first electrical output signal having pulses of different lengths comprises an infinite clipping circuit.

12. The circuit of claim 9, wherein said means for providing predetermined quantized pulse lengths from selected quantized pulse lengths to effect a non-linear quantization of said first electrical output signal comprise: a first shift register having a serial input, and a plurality of parallel outputs, one for each stage of said register and a second shift register having a serial input, a serial output, and a plurality of parallel inputs, one for each stage of said register, the parallel outputs of said first shift register being interconnected with the parallel inputs of said second shift register such that the stages of said first shift register positioned to receive a selected pulse length are coupled to the stages of said second shift register positioned to hold said predetermined pulse lengths which are to be provided in place of said selected pulse lengths.

13. The circuit of claim 12, wherein said digital electrical output signal has only two discrete amplitudes and said first shift register is a dual register each side of which handles signals representing a respective amplitude of said electrical output signal.

14. The circuit of claim 13, wherein said dual register also has a plurality of parallel outputs, one for each stage of said dual register; a third shift register having a serial input, a serial output, and a plurality of parallel inputs, one for each stage of said register; said parallel outputs of said dual register being interconnected with said parallel inputs of said third shift register such that the stages of said dual register positioned to receive selected pulse lengths are coupled to stages of said third shift register positioned to hold said predetermined pulse lengths which are to be provided in place of said selected pulse lengths.

15. The circuit of claim 14, wherein said second and said third shift registers also have a plurality of parallel outputs, one from each stage of said register, said parallel outputs being fed to a preset input of each corresponding stage in said first and said dual register to ensure that corresponding stages are always in the same state when said second and third registers are in use.

16. A circuit for decoding a quantized digital signal of the type encoded in dependence on the time intervals between successive occurrences of predetermined amplitudes in the original information signal comprising:

- a. a variable output circuit,
- b. means for determining the length of each successive pulse of said digital signal,
- c. means for delaying said digital signal,
- d. means for adjusting said variable output circuit in dependence on said pulse length while said delay means is delaying said pulse length of said signal, and
- e. means for passing said digital signal to said adjusted output circuit to provide an output waveform related to said quantized digital signal.

17. The circuit of claim 16, wherein said variable output circuit is a low pass filter circuit the frequency response of which is adjustable such that the cutoff frequency is decreased to a relatively low value for a long pulse, and increased to a relatively high value for a short pulse.

18. The circuit of claim 17, wherein said means for determining the length of successive pulses comprises: a dual shift register having a plurality of parallel outputs, one for each stage of said register; second and third shift registers having a plurality of parallel inputs, one for each stage of each said register; said parallel outputs of said dual register being interconnected with said parallel inputs of said second and third shift registers whereby a train of like pulses which is about to pass out of said dual register will switch a corresponding number of stages of said second or said third register to provide an indication of the pulse length of the signal about to pass to said variable filter circuit.

19. The circuit of claim 18, wherein said means for determining the length of successive pulses further includes: said second and third shift registers having a plurality of parallel outputs, one for each stage of said registers; two analogue adding circuits, the inputs of respective said analogue adding circuits being coupled to respective said parallel outputs of said second and third shift registers; the outputs of said analogue adding circuits being coupled to a control input of said variable filter circuit.

20. The circuit of claim 17, wherein said variable filter circuit comprises a plurality of fixed filter circuits each having a different frequency response, and a cooperating switching circuit for selecting the appropriate filter in dependence on the length of the pulse to be decoded.

21. The circuit of claim 20, wherein said means for determining the length of successive pulse comprises: a dual shift register having a serial input, a serial output to the variable filter circuit, and a plurality of parallel outputs, one for each stage of the register; second and third shift registers each having a plurality of parallel inputs and a plurality of parallel outputs, one of each for each stage of each of said registers; means interconnecting said parallel outputs of respective sides of said dual register with said parallel inputs of said second and third registers respectively, whereby a train of like pulses which is about to pass out of said dual register will switch a corresponding number of stages of whichever of said second or third registers is connected to that side of said dual register; and a plurality of exclusive OR gates coupled to said parallel outputs of said second and third registers whereby the end of said train of like pulses is detected and a signal passed to the appropriate part of said switching circuit.

22. A method of decoding a digital signal of the type encoded in dependence on the time intervals between successive occurrences, in the original information signal, of predetermined amplitudes, comprising the steps of:

- a. determining the length of each successive pulse of the digital signal,
- b. delaying the digital signal while adjusting the frequency response of a variable output circuit in dependence on the pulse lengths, and
- c. then passing said signal through said, now adjusted, output circuit to provide an output waveform corresponding to said digital signal.

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