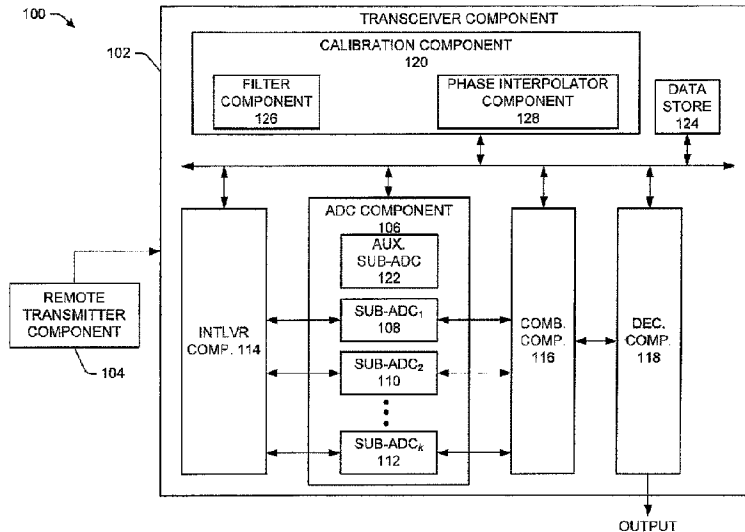




(86) Date de dépôt PCT/PCT Filing Date: 2015/07/30
 (87) Date publication PCT/PCT Publication Date: 2016/12/15
 (45) Date de délivrance/Issue Date: 2023/01/03
 (85) Entrée phase nationale/National Entry: 2017/12/07
 (86) N° demande PCT/PCT Application No.: US 2015/042795
 (87) N° publication PCT/PCT Publication No.: 2016/200409
 (30) Priorité/Priority: 2015/06/11 (US14/736,874)

(51) Cl.Int./Int.Cl. *H03M 1/10* (2006.01),
H03M 1/12 (2006.01)
 (72) Inventeurs/Inventors:
MALKIN, MOSHE, US;
GUPTA, TARUN, US
 (73) Propriétaire/Owner:
MACOM CONNECTIVITY SOLUTIONS, LLC, US
 (74) Agent: CPST INTELLECTUAL PROPERTY INC.

(54) Titre : ETALONNAGE ET SUIVI DE RECEPTEUR
 (54) Title: CALIBRATION AND TRACKING OF RECEIVER



(57) **Abrégé/Abstract:**

Techniques for calibrating interleaved analog-to-digital converter (ADC) arrays are presented. A transceiver comprises an ADC component comprising an array of interleaved sub-ADCs, and an auxiliary path associated with an auxiliary sub-ADC used to facilitate calibrating a sampling array by comparing the auxiliary path signal to signals of the sub-ADCs in the array. A calibration component employs a phase-interpolator and analog delay lines to adjust the auxiliary sub-ADC to enable the auxiliary sub-ADC to be lined up to any one of the sampling instants of the sampling array. The calibration component compares the auxiliary signal to sub-ADC signals, determines path differences between the sub-ADC paths based on the comparison results, and calibrates the sub-ADCs and sub-ADC paths to reduce the path differences to mitigate distortion in a digital stream produced from combining the digital substreams produced by the sub-ADCs in the array.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau(10) International Publication Number
WO 2016/200409 A1(43) International Publication Date
15 December 2016 (15.12.2016)

- (51) International Patent Classification:
H03M 1/10 (2006.01) *H03M 1/12* (2006.01)
- (21) International Application Number:
PCT/US2015/042795
- (22) International Filing Date:
30 July 2015 (30.07.2015)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
14/736,874 11 June 2015 (11.06.2015) US
- (71) Applicant: **APPLIED MICRO CIRCUITS CORPORATION** [US/US]; 215 Moffett Park Drive, Sunnyvale, California 94089 (US).
- (72) Inventors: **MALKIN, Moshe**; 3115 Sheridan Ave, #212, Palo Alto, California 94306 (US). **GUPTA, Tarun**; 4242 Tobin Cir., Santa Clara, California 95054 (US).
- (74) Agent: **TUROCY, Gregory**; Amin, Turocy & Watson, LLP, 57th Floor - Key Tower, 127 Public Square, Cleveland, Ohio 44114 (US).

- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: CALIBRATION AND TRACKING OF RECEIVER

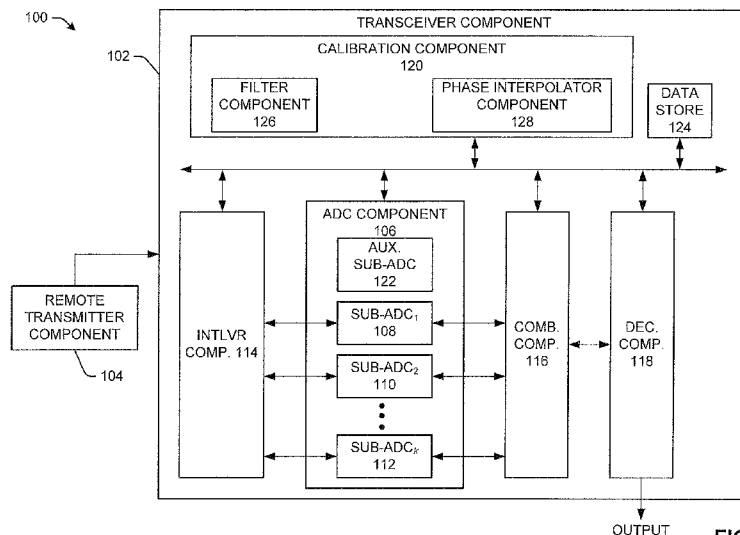


FIG. 1

(57) Abstract: Techniques for calibrating interleaved analog-to-digital converter (ADC) arrays are presented. A transceiver comprises an ADC component comprising an array of interleaved sub-ADCs, and an auxiliary path associated with an auxiliary sub-ADC used to facilitate calibrating a sampling array by comparing the auxiliary path signal to signals of the sub-ADCs in the array. A calibration component employs a phase-interpolator and analog delay lines to adjust the auxiliary sub-ADC to enable the auxiliary sub-ADC to be lined up to any one of the sampling instants of the sampling array. The calibration component compares the auxiliary signal to sub-ADC signals, determines path differences between the sub-ADC paths based on the comparison results, and calibrates the sub-ADCs and sub-ADC paths to reduce the path differences to mitigate distortion in a digital stream produced from combining the digital substreams produced by the sub-ADCs in the array.



WO 2016/200409 A1

CALIBRATION AND TRACKING OF RECEIVER

TECHNICAL FIELD

[0001] This disclosure relates to communication of information.

BACKGROUND

[0002] Communication devices, such as transceivers, can be used to transmit or receive voice data or other data from other communication devices. The voice data or other data can be communicated via a wireline or wireless communication connection. One trend is to increase the amount of data that can be communicated and the speed of communication of data.

[0003] As communication data rates, speeds, and bandwidths grow, the circuits used to transmit, process, and receive data also have to process high bandwidth signals. One component used by many systems using digital signal processing is an analog-to-digital converter (ADC) that can be used to convert analog signals (e.g., voice signals) into a digital form for further digital signal processing. One approach for designing an ADC that can support relatively high bandwidth with high sampling speeds is to interleave an array of ADCs (e.g., an array of sub-ADCs), wherein each sub-ADC of the array can operate at a relatively lower speed. The lower sampling digital data samples from the sub-ADCs of the array can be combined to generate a high-speed digital data stream. This can enable the sub-ADCs of the array to operate at lower speeds and so the sub-ADCs can be designed with the limitation of current integrated circuit processing technology. A challenge with such a conventional interleaved ADC design can be that any processing differences between the sub-ADCs can contribute to the distortion of the combined digital stream. Such processing differences or mismatches can include, for example, different low-frequency offsets, bulk gains, delays, bandwidths, and more generally, different path transfer functions associated with the sub-ADCs of the array.

[0004] System designers often can attempt to design an ADC array such that these path differences can be relatively small. However, for more efficient area and power designs for high-speed communication systems, there can be undesirable power and area penalties incurred as well as more complex circuit designs being employed to keep these distortions at an acceptable level. These penalties can be significant and can contribute significantly to the system's

power and area requirements, and it can therefore be desirable to avoid such penalties and power and area requirements.

[0005] Also, in conventional systems, auxiliary hardware, such as a digital-to-analog converter (DAC), often can be used and/or required to correct these distortions by generating a test/calibration signal that can be used to calibrate or correct the path differences. Such a conventional design can add to the cost and complexity of the system and/or can be of limited use, for example, if the test signal interferes with the communication channel's signal transmission. Thus, as a result, such calibration typically only can be allowed to be carried out during specific time periods before the actual data is received by the sampling array.

[0006] Another conventional method for correcting such distortions associated with an array of sub-ADCs can be using sampling arrays that can oversample the received signal. The information gleaned from oversampling the received signal can be used to calibrate and correct the processing path differences associated with the sub-ADCs. However, such conventional approach can significantly complicate the system design and can result in an undesirably higher amount of power and area being used for the system design because of the higher sampling speed used to obtain the oversampled channel signal.

[0007] Some other conventional methods for correcting such distortions associated with an array of sub-ADCs can include adding another receiving element that can enable detection of path differences associated with sub-ADCs using an auxiliary ADC. However, such methods also can depend on having some form of knowledge of the exact signal characteristics and can be of limited use. Further, these conventional methods also can be undesirably costly and can have complex and/or inefficient system designs.

SUMMARY

[0008] In an embodiment, disclosed herein is a system that contains a converter component comprising a set of converter sub-components for converting respective time-delayed analog signals, associated with an analog signal received from a remote communication component, to respective digital data samples, and an auxiliary converter sub-component associated with an auxiliary path, wherein respective converter sub-components of the set of

converter sub-components are associated with respective paths. The system can also contain a calibration component for determining path differences between the respective paths of the respective converter sub-components, based at least in part on a result of an analysis of an auxiliary signal associated with the auxiliary path and respective signals associated with the respective paths of the respective converter sub-components, to facilitate calibration of the respective converter sub-components to reduce the path differences, wherein the respective signals comprise the respective digital data samples.

[0009] In another embodiment, disclosed herein is a method that involves determining path differences between respective paths of respective converter sub-components of a set of converter sub-components, based at least in part on a result of analyzing of an auxiliary signal associated with an auxiliary path that is associated with an auxiliary sub-component and respective signals associated with the respective paths of the respective converter sub-components of the set of converter sub-components, to facilitate calibrating the respective converter sub-components to mitigate the path differences. The method can also involve adjusting the respective converter sub-components or the respective paths to facilitate the mitigating of the path differences between the respective converter sub-components or the respective paths.

[0010] In another embodiment, disclosed herein is a system that contains a means for determining path differences between respective paths of respective converter sub-components of a set of converter sub-components, based at least in part on a result of comparing an auxiliary signal associated with an auxiliary path that is associated with an auxiliary sub-component with respective signals associated with the respective paths of the respective converter sub-components of the set of converter sub-components, to facilitate calibrating the respective converter sub-components to reduce the path differences. The system can also contain a means for calibrating the respective converter sub-components or the respective paths to facilitate the reducing of the path differences between the respective converter sub-components or the respective paths.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1** illustrates a block diagram of an example system that can facilitate calibrating sub-analog-to-digital converters (sub-ADCs) of an array of

sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences.

[0012] FIG. 2 is an illustration of an example sampling timing diagram illustrating sampling by an auxiliary sub-ADC, a first sub-ADC, and a second sub-ADC of the sub-ADC array.

[0013] FIG. 3 is an illustration of an example sampling timing diagram illustrating sampling instants of the auxiliary sub-ADC, the first sub-ADC, and the second sub-ADC of the sub-ADC array.

[0014] FIG. 4 is an illustration of an example sampling timing diagram illustrating sampling instants of the auxiliary sub-ADC, the first sub-ADC, and the second sub-ADC of the sub-ADC array, after adjustment to align the auxiliary sub-ADC with the first sub-ADC.

[0015] FIG. 5 depicts a diagram of an embodiment of a system that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences.

[0016] FIG. 6 illustrates a block diagram of an embodiment of a transceiver component.

[0017] FIG. 7 illustrates a flow diagram of an embodiment of a method that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences.

[0018] FIG. 8 depicts a flow diagram of another embodiment of a method that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences.

[0019] FIG. 9 is a flow diagram of an embodiment of a method that can align or calibrate an auxiliary sub-ADC (and associated auxiliary path) with a sub-ADC (and associated sub-ADC path) of a set (e.g., an array) of sub-ADCs.

[0020] FIG. 10 illustrates a block diagram of an example electronic computing environment.

[0021] FIG. 11 illustrates a block diagram of an example data communication network.

DETAILED DESCRIPTION

[0022] Techniques for calibrating interleaved analog-to-digital converter (ADC) arrays are presented. A transceiver component can comprise an ADC component comprising an array of interleaved ADC sub-components (also

referred to herein as sub-ADCs), and an auxiliary path associated with an auxiliary sub-ADC that can be used to facilitate calibrating the sub-ADCs in the array by comparing the auxiliary path signal to signals of the sub-ADCs in the array. The auxiliary path can be designed to closely match the processing paths of the other sub-ADCs.

[0023] The transceiver component can receive signals (e.g., analog signals), comprising data, from a remote transmitter component (e.g., a transmitter, a transceiver, or another type of communication device). When an analog signal is received by the transceiver component, an interleaver component can interleave the received analog signal across the sub-ADCs of the array, wherein the interleaver component or a calibration component can process the analog signal to implement or introduce respective time delays to the analog signal to generate a set of time-delayed analog signals (e.g., having respective time delays) prior to it being input to the respective sub-ADCs of the array. The sub-ADCs of the array, and/or another component(s) of the transceiver component, can process (e.g., sample, convert, decode, and/or otherwise process) the respective time-delayed analog signals to facilitate recovering (e.g., facilitate determining, identifying, decoding, and/or decrypting, etc.) the data (e.g., in digital form) sent by the remote transmitter.

[0024] The transceiver component can comprise a calibration component that can be associated with the auxiliary sub-ADC and the sub-ADCs in the array. The calibration component can employ a phase-interpolator and/or analog delay lines to adjust the auxiliary sub-ADC to enable the sampling of the auxiliary sub-ADC to be lined up to any one of the sampling instants of the sub-ADCs in the array. An auxiliary path sampling rate, phase-interpolator, and analog delay lines can be designed (e.g., by the calibration component or another component) to facilitate establishing an initial match between respective sampling instants of the auxiliary sub-ADC and another sub-ADC in the array, and the sub-ADCs in the array can thereby be calibrated because it is known the sampling clock of the auxiliary path passes through all the sampling points of the sub-ADCs in the array. The calibration component also can determine and/or set the rate at which the auxiliary sub-ADC for the auxiliary path (e.g., auxiliary signal or sampling path) operates such that the auxiliary sub-ADC can pass through the sampling times of all of the desired samples from the actual

sampling array to facilitate determining path differences between the auxiliary sub-ADC and the sub-ADCs in the array.

[0025] The calibration component can compare the auxiliary signal to sub-ADC signals (e.g., compare the auxiliary samples at sampling instants with the respective samples of the sub-ADCs in the array at respective sampling instants). The calibration component can determine path differences (e.g., timing skew, bandwidth differences, or other path differences) between the sub-ADC paths (e.g., sub-ADC signal or sampling paths) based at least in part on the results of the comparison of the auxiliary signal and the respective sub-ADC signals. The calibration component also can determine a calibration to apply to the sub-ADCs or sub-ADC paths, and can calibrate the sub-ADCs and sub-ADC paths, based at least in part on the determined calibration (e.g., calibration metric) to correct or reduce the path differences to mitigate distortion in a digital stream produced from combining the digital substreams produced by the sub-ADCs in the array.

[0026] The respective sub-ADCs of the array, as calibrated by the calibration component, can facilitate providing respective digital data substreams, which can correspond to the received signal (e.g., analog signal), as an output. The ADC component or another component (e.g., a combiner component) can combine, integrate, or deinterleave the respective digital data substreams of the respective sub-ADCs to generate a digital data stream that can accurately represent the data contained in the received analog signal.

[0027] FIG. 1 illustrates a block diagram of system 100 that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences. The system 100 can be or can comprise, for example, a high-speed communication and/or sampling system that can perform analog to digital conversion of analog signals at a desirably high rate of speed. The system 100 can be used to facilitate voice or data communications at one or more desired speeds, such as, for example, 10 gigabit per second (G), 40G, 100G, and/or a faster or different communication rate of speed. The system 100 can be employed in connection with an electrical transceiver, an optical transceiver, a wireless transceiver, a backplane transceiver, a chip-to-chip transceiver, or any of a variety of other types of transceivers.

[0028] The system 100 can comprise a transceiver component 102 (e.g., transceiver) that can be employed to communicate traffic (e.g., voice or data traffic), wherein the transceiver component 102 can receive traffic from a communication device, such as a remote transmitter component 104, and can transmit traffic to another communication device. The transceiver component 102 can be, or can be part of, a device that can communicate traffic. For example, the transceiver component 102 can be, or can be part of, a modem or router (e.g., a 10G modem or router (e.g., a 10G-baseT modem or router), a 40G modem or router (e.g., a 40G-baseT modem or router), a 100G modem or router (e.g., a 100G-baseT modem or router), or a modem or router that can employ another (e.g., a faster or different) communication rate), a switch that can facilitate communication of traffic, a communication device that can employ optical communications technology and/or wireless communications technology, or another type of communication device.

[0029] The transceiver component 102 can comprise one or more (e.g., 1, 2, 3, 4, ...) transmitters and one or more (e.g., 1, 2, 3, 4, ...) receivers that can facilitate transmitting and receiving voice or data communications. In some implementations, the transceiver component 102 can employ a full-duplex system that can allow simultaneous communication in both directions. The transceiver component also can employ one or more sensing devices such as one or more antennas that can facilitate voice or data communications.

[0030] The transceiver component 102 also can comprise an ADC component 106 that can convert analog signals received from another communication device, such as the remote transmitter component 104, to corresponding digital signals. The ADC component 106 can comprise a set of ADC sub-components (also referred to herein as sub-ADCs) that can be employed to process received signals (e.g., to convert received analog signals to corresponding digital signals). The set of ADC sub-components can comprise, for example, ADC sub-component₁ 108, ADC sub-component₂ 110, up through ADC sub-component_k 112, wherein k can be virtually any desired number. The set of ADC sub-components (e.g., 108, 110, 112, etc.) can be structured in the form of an array of ADC sub-components that can be interleaved and can operate in parallel to facilitate supporting a desired high bandwidth and performing high-speed processing of the received signals, as more fully disclosed herein.

[0031] To facilitate interleaving the sub-ADCs, the transceiver component 102 also can comprise an interleaver component 114 (INTLVR COMP.) that can be employed to interleave the received analog signal across the respective interleaved sub-ADCs (e.g., 108, 110, 112, etc.) of the array, wherein the interleaver component 114 or the calibration component 120 can process the analog signal to implement or introduce respective time delays to the analog signal to generate time-delayed analog signals (e.g., having respective time delays) prior to the signal being input to the ADC component 106. The interleaver component 114 can comprise a desired number of outputs, such as k outputs, that can provide the time-delayed analog signals (e.g., with respective delays) to the respective inputs of the respective sub-ADCs (e.g., 108, 110, 112, etc.). The respective sub-ADCs (e.g., 108, 110, 112, etc.) can sample or perform other processing on the respective time-delayed analog signals at the specified sampling or processing rate of the sub-ADCs to facilitate determining an analog value of each data sample and converting or digitizing the analog value of the data sample to a corresponding digital value to generate a corresponding digital data sample to facilitate recovering the data from the respective time-delayed analog signals.

[0032] For instance, the respective sub-ADCs (e.g., 108, 110, 112, etc.) can operate at a relatively lower speed to process (e.g., sample, convert or digitize, and/or otherwise process) the respective portions of the received signals, but due in part to the interleaving and parallel operation of the sub-ADCs (e.g., 108, 110, 112, etc.), the combined operation of the respective sub-ADCs (e.g., 108, 110, 112, etc.) can enable the ADC component 106 to process the received signals at a desirably high speed to produce a corresponding digital data stream as an output. For example, the respective digital data samples from the respective sub-ADCs (e.g., 108, 110, 112, etc.) produced at a relatively lower speed can be combined (e.g., by a combiner component 116 (COMB. COMP.)) to generate a higher speed digital data stream, wherein the higher speed of the generated digital data stream can be a function of the number of sub-ADCs and the sampling or processing speed of the sub-ADCs. As a specific example, if it is desired to have the ADC component 106 convert analog to signals to digital signals at a rate of 10G, and if it is desired to use 1G sub-ADCs (e.g., sampling or processing at 1G each) to form the ADC component 106, the ADC component 106 can be configured to comprise 10 1G

sub-ADCs that can be interleaved and can operate in parallel to facilitate processing received analog signals, wherein $k = 10$. The interleaving, and parallel operation, of the 10 sub-ADCs can facilitate enabling the ADC component 106 to process received analog signals at a rate of 10G.

[0033] The respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array, and/or another component(s), such as a decoder component 118 (DEC. COMP.), of the transceiver component 102, can process (e.g., sample, convert or digitize, decode, and/or otherwise process (e.g., decrypt)) the analog signal to facilitate recovering (e.g., facilitate determining, identifying, etc.) the data (e.g., in digital form) received by the transceiver component 102 from the remote transmitter component 104. For instance, each of the respective sub-ADCs can sample the analog signal to generate a sample of the analog signal, and the sample can be converted or digitized to generate a digital data sample. The respective sub-ADCs can provide (e.g., communicate) the respective digital data samples to the combiner component 116, which can combine or integrate the respective digital data samples to generate a digital data stream. The combiner component 116 can send (e.g., communicate) the digital data stream to the decoder component 118. The decoder component 118 can decode the digital data stream, comprising the combined digital data samples from the respective sub-ADCs, to facilitate recovering (e.g., generating, determining, identifying, etc.) the data from the digital data samples.

[0034] One challenge with interleaved ADC designs can be that any processing differences between the sub-ADCs can contribute to the distortion of the combined digital stream. When using an interleaved array of sub-ADCs, there can be processing path differences between the respective paths of the sub-ADCs of the array. Such path differences can cause distortion in the digital data stream when the digital data substreams of the sub-ADCs are combined. Such processing differences or mismatches can include, for example, different timing skews or delays, different low-frequency offsets, different bulk gains, different bandwidths, and more generally, different path transfer functions between the respective paths of the sub-ADCs of the array.

[0035] To facilitate mitigating these processing differences and performing other operations, the transceiver component 102 can comprise a calibration component 120 that can respectively calibrate or adjust respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array and/or information or paths

(e.g., sub-ADC paths) associated with the respective arrays to facilitate correcting or mitigating the respective sub-ADC path differences associated with the respective sub-ADCs. This can facilitate mitigating distortions that would otherwise have been caused as a result of the uncorrected or unmitigated path differences associated with the sub-ADCs. The calibration component 120 can perform such calibration or adjustment of the sub-ADCs (e.g., 108, 110, 112, etc.) at virtually any desired time, such as, for example, during start-up of the ADC component 106 or associated device (e.g., transceiver component 102), during showtime, during or in connection with a data transfer associated with the transceiver component 102, periodically, in response to occurrence of a condition (e.g., in response to detection of a condition) associated with the transceiver component 102, the ADC component 106, or other component, and/or at another desired time.

[0036] To facilitate enabling the calibration component 120 to calibrate or adjust the sub-ADCs (e.g., 108, 110, 112, etc.) of the array, the ADC component 106 also can comprise an auxiliary ADC sub-component 122 (also referred to herein as an auxiliary sub-ADC or a calibration sub-ADC, and AUX. SUB-ADC in the figures) that can be associated with (e.g., communicatively connected to or part of) an auxiliary path of the ADC component 106. The calibration component 120 can employ, and can control the operation of, the auxiliary sub-ADC 122 (and associated auxiliary path) to facilitate calibrating the array of sub-ADCs (e.g., 108, 110, 112, etc.) (also referred to herein as the sampling array), for example, by comparing the auxiliary path signal to the signals of the other processing paths of the array of sub-ADCs (e.g., 108, 110, 112, etc.) to facilitate determining and correcting path differences between paths of the sub-ADCs (e.g., 108, 110, 112, etc.).

[0037] To facilitate desirable (e.g., optimal, accurate, acceptable) calibration of the sub-ADCs (e.g., 108, 110, 112, etc.), the auxiliary path (also referred to herein as the auxiliary sampling path or sub-ADC path), including the auxiliary sub-ADC 122, can be designed to closely (e.g., substantially) match the processing paths of the other sub-ADCs of the array. For instance, the auxiliary path can closely or substantially match the signal path associated with the sub-ADCs (e.g., 108, 110, 112, etc.) with respect to programmable gain amplifiers (PGAs), bandwidth, samplers, buffers, and/or other features or components associated with the sub-ADC paths of the ADC component 106.

[0038] In some implementations, to reduce the amount of power consumed by the auxiliary sub-ADC 122 in connection with the auxiliary path, the auxiliary sub-ADC 122 can be configured to operate (e.g., run) at a rate that can be lower (e.g., operate at a lower resolution) than the full system rate (e.g., operate at a rate that can be lower than the rate of the other sub-ADCs (e.g., 108, 110, 112) of the ADC component 106). The calibration component 120 also can determine and/or set the rate at which the auxiliary sub-ADC 122 for the auxiliary path (e.g., auxiliary processor or sampling path) operates such that the auxiliary sub-ADC 122 can pass through the sampling times of all of the desired samples from the array of sub-ADCs (e.g., 108, 110, 112, etc.).

[0039] Along with **FIG. 1**, **FIG. 2** is an illustration of an example sampling timing diagram 200 illustrating sampling by the auxiliary sub-ADC 122, a first sub-ADC (e.g., sub-ADC₁ 108), and a second sub-ADC (e.g., sub-ADC₂ 110) of the sub-ADC array. The calibration component 120 (or another component) can set the respective sample rates and times of the respective sub-ADCs (e.g., 108, 110, 112, etc.) such that the respective sub-ADCs can be sampled at different times with respect to each other. In the system 100, the respective sampling times of a first set of samples performed by the auxiliary sub-ADC 122 can coincide with respective sampling times of a first set of samples performed by a first sub-ADC (e.g., 108) in the array, the respective sampling times of a second set of samples performed by the auxiliary sub-ADC 122 can coincide with respective sampling times of a second set of samples performed by a second sub-ADC (e.g., 108) in the array, and so on.

[0040] As an illustrative example with regard to a sub-ADC array of two sub-ADCs (e.g., sub-ADC₁ 108, sub-ADC₂ 110) (plus the auxiliary sub-ADC 122, which does not carry actual data from the received analog signal), the calibration component 120 (or another component) can set the sub-ADC₁ 108 (or associated sampler component) to sample a first analog signal on a first path at times 0t, 2t, 4t, 6t, 8t, 10t, 12t, 14t, 16t, 18t, 20t, and so on, as illustrated at reference numeral 202 in **FIG. 2**. The calibration component 120 (or another component) also can set the sub-ADC₂ 110 (or associated sampler component) to sample a second analog signal on a second path at times 1t, 3t, 5t, 7t, 9t, 11t, 13t, 15t, 17t, 19t, and so on, as illustrated at reference numeral 204 in **FIG. 2**. To facilitate enabling sampling by the auxiliary sub-ADC 122 to pass through the respective sampling times of all of the desired samples from the array of

sub-ADCs (e.g., 108, 110), the calibration component 120 can set the auxiliary sub-ADC 122 to have a sampling rate, such as, for example, sampling every $5t$, that can be lower than the full system rate used for the array of sub-ADCs (e.g., 108, 110) such that the auxiliary sub-ADC 122 (or an associated auxiliary sampler component) can sample the auxiliary signal at $0t$, $5t$, $10t$, $15t$, $20t$, and so on, as illustrated at reference numeral 206 in FIG. 2.

[0041] At times $0t$, $10t$, $20t$, and so on, there are samples for the first path associated with sub-ADC₁ 108 and auxiliary samples for the auxiliary path associated with the auxiliary sub-ADC 122, and at times $5t$, $15t$, $25t$, and so on, there are samples for the second path associated with sub-ADC₂ 110 and auxiliary samples for the auxiliary path associated with the auxiliary sub-ADC 122. Thus, the auxiliary sub-ADC 122 has been set to pass through sampling times (e.g., at least some of the (even numbered)- t sampling times, at least some of the (odd numbered)- t sampling times) of all of the desired samples from the array of sub-ADCs (e.g., 108, 110), as there are times when the auxiliary signal on the auxiliary path is sampled at (or at least substantially near) the same time the first signal is sampled on the first path, there are other times when the auxiliary signal on the auxiliary path is sampled at (or at least substantially near) the same time as the second signal is sampled on the second path, and there are no sub-ADCs in the array for which the auxiliary sub-ADC 122 (or associated auxiliary sampler component) does not sample the auxiliary signal on the auxiliary path at the same (or substantially same) time as a signal on a path of a sub-ADC is sampled for at least a portion of the samples of that sub-ADC.

[0042] In FIG. 1, the calibration component 120 can monitor and track the respective sampling of the respective sub-ADCs (e.g., 108, 110, 112, etc.) and the sampling of the auxiliary sub-ADC 122. The calibration component 120 can receive, sample, collect, or otherwise obtain information relating to, for example, the auxiliary samples of the auxiliary path and the respective samples from the respective paths of the respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array that correspond to the same times as the auxiliary samples. For instance, with regard to the above example, for the sampling at times $0t$, $10t$, $20t$, $30t$, and so on, the calibration component 120 can obtain information relating to the auxiliary samples and the samples of the first signal on the first path at those sampling times $0t$, $10t$, $20t$, $30t$, and so on. For the sampling at times $5t$, $15t$,

25t, 35t, and so on, the calibration component 120 can obtain information relating to the auxiliary samples and the samples of the second signal on the second path at those sampling times 5t, 15t, 25t, 35t, and so on. If there were other respective sub-ADCs of the sub-ADC array, the calibration component 120 also can obtain information relating to the auxiliary samples and the respective samples of the other signals on the other respective paths at other respective sampling times (e.g., wherein, if there were other sub-ADCs in the array, the auxiliary sampling time of the auxiliary path can have a different rate to enable the auxiliary sub-ADC 122 to pass through the sampling times of all of the desired samples for all sub-ADCs (e.g., 108, 110, 112, etc.) in the sub-ADC array).

[0043] The calibration component 120 can store the obtained information relating to the auxiliary samples of the auxiliary path and the respective samples from the respective paths of the respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array that correspond to the same times as the auxiliary samples in a data store 124 for later analysis or can analyze such information prior to storing it in the data store 124. The calibration component 120 can analyze the obtained sample-related information, for example, by comparing the auxiliary samples associated with the auxiliary sub-ADC 122 to respective corresponding samples (e.g., corresponding by time of sample) associated with the respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array. For example, the calibration component 120 can analyze the obtained sample-related information to determine differences, if any between the information relating to the auxiliary samples for the auxiliary sub-ADC 122 and the samples for sub-ADC₁ 108 at the respective times (e.g., 0t, 10t, 20t, 30t, and so on) that those respective samples occurred. The calibration component 120 also can analyze the obtained sample-related information to determine differences, if any between the information relating to the auxiliary samples for the auxiliary sub-ADC 122 and the samples for sub-ADC₂ 110 at the respective times (e.g., 5t, 15t, 25t, and so on) that those respective samples occurred.

[0044] In some implementations, to facilitate determining path differences between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.) (and/or between the paths of the sub-ADCs and the auxiliary path), for all or a desired portion of the samples, the calibration component 120 can determine (e.g., calculate) the squared error differences between an auxiliary sample for the auxiliary sub-ADC

122 and a corresponding sample associated with a sub-ADC, wherein a sample is a corresponding sample with respect to the auxiliary sample when it occurs at a same (or substantially the same) time instant as the auxiliary sample occurs. For example, for auxiliary sample x_1 at time $10t$ and sample y for sub-ADC₁ 108 at the same time instant of $10t$, the calibration component 120 can determine (e.g., calculate) the squared error difference between auxiliary sample x_1 for the auxiliary sub-ADC 122 and sample y associated with the sub-ADC₁ 108 (e.g., squared difference error (for y, x_1) = $(y-x_1)^2$). For auxiliary sample x_2 at time $15t$ and sample z for sub-ADC₂ 110 at the same time instant of $15t$, the calibration component 120 can determine the squared error difference between auxiliary sample x_2 for the auxiliary sub-ADC 122 and sample z associated with the sub-ADC₂ 110 (e.g., squared difference error (for z, x_2) = $(y-x_2)^2$).

[0045] The calibration component 120 can determine the path differences (e.g., a path difference metric) between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.) (and/or between the auxiliary sub-ADC 122 and the sub-ADC), based at least in part on the results of the analysis of the obtained sample-related information (e.g., based at least in part on differences between the auxiliary samples and the corresponding samples for the sub-ADC₁ 108, differences between the auxiliary samples and the corresponding samples for the sub-ADC₂ 110, and/or the respective squared difference errors associated with the respective samples). Based at least in part on the determined path differences between the paths, the calibration component 120 also can determine calibrations or adjustments that can be made to the sub-ADCs (e.g., 108, 110, 112, etc.) to correct, mitigate, reduce, or minimize path differences between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.) (and/or between the auxiliary sub-ADC 122 and the sub-ADC).

[0046] To facilitate correcting, mitigating, reducing, or minimizing path differences between the paths, the calibration component 120 can generate control information (e.g., control commands or instructions) relating to the calibrations or adjustments, can determine a filter (e.g., analog filter, digital filter) that can be applied by a filter component 126 to a path(s) to filter data signals or samples on the path(s) to facilitate calibrating or adjusting a sub-ADC or associated path, can determine a delay line(s) (e.g., analog delay line(s)) that can be applied to path(s) to facilitate calibrating or adjusting a sub-ADC or associated path, and/or can make other determinations or perform other

operations that can facilitate calibrating or adjusting the sub-ADCs (e.g., 108, 110, 112, etc.) or associated paths.

[0047] The calibration component 120 can communicate the control information to one or more of the sub-ADCs (e.g., 108, 110, 112, etc.) to modify the operation, parameters, etc., of the one or more sub-ADCs, and/or can communicate control information to the filter component 126 to facilitate generating or setting a desired filter(s) that can be applied to a path(s), to correct, mitigate, reduce, or minimize path differences between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.) (and/or between the auxiliary sub-ADC 122 and the sub-ADC). In addition or alternatively, the calibration component 120 can apply a delay line(s) to a sub-ADC path(s) and/or can perform other operations that can facilitate calibrating or adjusting the sub-ADCs (e.g., 108, 110, 112, etc.) and associated paths.

[0048] The collecting of the sample-related information associated with the auxiliary path of the auxiliary sub-ADC 122 and the paths of the sub-ADCs (e.g., 108, 110, 112, etc.), analyzing of the sample-related information, determining path differences between paths of the sub-ADCs, determining calibrations for the sub-ADCs (or associated sub-ADC paths) to mitigate path differences, and/or calibrations of the sub-ADCs (or associated sub-ADC paths) can be performed in parallel by the calibration component 120 and/or other components (e.g., sampler component, processor component, etc.). Also, the calibration component 120 and other components (e.g., sampler component, processor component, filter component 126, phase interpolator component 128, etc.) can perform the various operations relating to calibrating the sub-ADCs of the array as part of background operations (e.g., in data processing mode, while analog-to-digital data conversions are being performed by the ADC component 106) or foreground operations (e.g., when the ADC component 106 is not in data processing mode).

[0049] To facilitate desired (e.g., optimal, suitable, acceptable) operation of transceiver component 102, including the calibration component 120 and ADC component 106, and conversion of a received analog data stream to a digital data stream, the calibration component 120 can facilitate aligning or calibrating (e.g., initially aligning or calibrating, re-aligning or re-calibrating) the auxiliary sub-ADC 122 with or to a sub-ADC (e.g., 108, 110, or 112) of the sub-ADC array, in accordance with a defined alignment algorithm, as disclosed

herein. In some implementations, the calibration component 120 can comprise or be associated with a phase interpolator component 128 that can be associated with the auxiliary sub-ADC 122 to facilitate adjusting a phase and/or time difference between the auxiliary sub-ADC 122 and a sub-ADC to facilitate aligning or calibrating the auxiliary sub-ADC 122 with or to the sub-ADC. For instance, the phase interpolator component 128 can enable the auxiliary sub-ADC 122 to be lined up to any one of the sampling instants of a sub-ADC (e.g., 108, 110, or 112) of the array of sub-ADCs. The calibration component 120 also can employ delay lines (e.g., analog delay lines) that can be applied to an auxiliary path associated with an auxiliary sub-ADC 122 or a path associated with a sub-ADC (e.g., 108, 110, or 112) to facilitate delaying an auxiliary signal or signal, respectively, to facilitate aligning or calibrating the auxiliary sub-ADC 122 with or to the sub-ADC. An auxiliary path sampling rate, a phase interpolator of the phase interpolator component 128, and analog delay lines can be suitably designed or controlled (e.g., by the calibration component 120) to facilitate establishing an initial match (or at least substantial match) between sampling instants of the auxiliary sub-ADC 122 and another sub-ADC(s) (e.g., 108, 110, or 112) in the array.

[0050] In some implementations, the calibration component 120 can control the phase interpolator component 128 to adjust the phase of the auxiliary sub-ADC 122 for the auxiliary path and/or can facilitate adjusting or selecting an analog delay line associated with the auxiliary path to facilitate performing an alignment (e.g., initial alignment) of the auxiliary sub-ADC 122 and auxiliary path with the sub-ADC and associated sub-ADC path. For each phase interpolator delay and analog delay line delay, the calibration component 120 can examine (e.g., analyze, evaluate) the samples of all of the other sub-ADCs (e.g., 108, 110, 112, etc.) of the array for each one of their analog delay lines to determine whether the auxiliary sub-ADC 122 is aligned with a sub-ADC. If the calibration component 120 determines that the auxiliary sub-ADC 122 is not yet suitably aligned with a sub-ADC, the calibration component 120 can apply or make further adjustments to the phase interpolator delay via the phase interpolator component 128 and/or analog delay line, and can again examine the sample of the auxiliary sub-ADC 122 with respect to the samples of all of the other sub-ADCs (e.g., 108, 110, 112, etc.) of the array along their

paths to determine whether the auxiliary sub-ADC 122 is aligned with a sub-ADC of the array, in accordance with the defined alignment algorithm.

[0051] FIG. 3 (along with FIG. 1), is an illustration of an example sampling timing diagram 300 illustrating sampling instants of the auxiliary sub-ADC 122, a first sub-ADC (e.g., sub-ADC₁ 108), and a second sub-ADC (e.g., sub-ADC₂ 110) of the sub-ADC array. FIG. 4 is an illustration of an example sampling timing diagram 400 illustrating sampling instants of the auxiliary sub-ADC 122, a first sub-ADC (e.g., sub-ADC₁ 108), and a second sub-ADC (e.g., sub-ADC₂ 110) of the sub-ADC array, after adjustment to align the auxiliary sub-ADC 122 with the first sub-ADC (e.g., sub-ADC₁ 108).

[0052] As depicted in the sampling timing diagram 300 of FIG. 3, initially or at some point in the initialization process, the sampling instant 302 for the auxiliary sub-ADC 122 can be out of alignment from the sampling instant 304 for the sub-ADC₁ 108 and the sampling instant 306 for the sub-ADC₂ 110. For instance, as shown at reference numeral 308 for the sampling of the auxiliary sub-ADC 122, at reference numeral 310 for the sampling of sub-ADC₁ 108, at reference numeral 312 for the sampling of sub-ADC₂ 110, respectively, the sampling instant 302 is shown as occurring at 0.1t, the sampling instant 304 is shown as occurring at 0.0t, and the sampling instant 306 is shown as occurring at -0.1t. The calibration component 120 can obtain and analyze this sampling-related information presented in the sampling timing diagram 300. Based at least in part on the results of the analysis, the calibration component 120 can determine that the auxiliary sub-ADC 122 is not desirably aligned with any sub-ADC (e.g., 108, 110) of the array, and can determine that an adjustment is to be made to the auxiliary sub-ADC 122 or associated path to facilitate aligning the auxiliary sub-ADC 122 with a sub-ADC of the array, in accordance with the defined alignment algorithm.

[0053] The calibration component 120 can determine a time adjustment amount, or can use a defined (e.g., predefined) time adjustment amount (e.g., -0.1t, +0.1t, or some other desired time adjustment amount), to apply to the auxiliary sampling time or auxiliary path to facilitate adjusting the auxiliary sampling time or auxiliary path to facilitate aligning (or substantially (e.g., suitably) aligning) the auxiliary sub-ADC 122 (and associated auxiliary path) with a sub-ADC (and associated path) of the array, in accordance with the defined alignment algorithm. The calibration component 120 can use the phase

interpolator component 128 and/or an analog delay line to facilitate adjusting the timing of the sampling of the auxiliary signal on the auxiliary path, such as disclosed herein.

[0054] As depicted in the sampling timing diagram 400 of FIG. 4, after the sampling timing adjustment has been performed on the auxiliary path, the sampling instant 402 for the auxiliary sub-ADC 122 can be aligned with the sampling instant 404 for the sub-ADC₁ 108, but is not aligned with the sampling instant 406 for the sub-ADC₂ 110. For instance, as shown at reference numeral 408 for the sampling of the auxiliary sub-ADC 122, at reference numeral 410 for the sampling of sub-ADC₁ 108, at reference numeral 412 for the sampling of sub-ADC₂ 110, respectively, the sampling instant 402 is now shown as occurring at time $0.0t$, the sampling instant 404 is shown as occurring at time $0.0t$, and the sampling instant 406 is shown as occurring at time $-0.1t$.

[0055] The calibration component 120 can obtain and analyze this sampling-related information presented in the sampling timing diagram 400. Based at least in part on the results of the analysis, the calibration component 120 can identify or determine that the sampling instant 402 (e.g., occurring at $0.0t$) for the auxiliary sub-ADC 122 occurs at the same time as the sampling instant 404 (e.g., occurring at $0.0t$) for the sub-ADC₁ 108. Since the sampling instant 402 is determined to occur at the same time as the sampling instant 404, the calibration component 120 can determine that the auxiliary sub-ADC 122 is desirably aligned with sub-ADC₁ 108, and can determine that no further adjustment needs to be made to the auxiliary sub-ADC 122 or associated auxiliary path with respect to the alignment process, in accordance with the defined alignment algorithm.

[0056] As another example, if, instead, an analog signal of a sub-ADC (e.g., 108, 110, or 112) of the array of sub-ADCs is set or determined to be sampled at times $(0+0.1)t$, $(2+0.1)t$, $(4+0.1)t$, $(6+0.1)t$, $(8+0.1)t$, $(10+0.1)t$, ..., $(18+0.1)t$, $(20+0.1)t$, $(22+0.1)t$, and so on, the calibration component 120 can select the auxiliary sampling rate (e.g., every $5t$), and can align (e.g., via an adjustment(s)) the sampling times (e.g., $(0+0.1)t$, $(10+0.1)t$, $(20+0.1)t$, and so on) associated with the auxiliary sub-ADC 122 with the sampling time associated with that sub-ADC, to enable the sampling of the auxiliary signal associated with the auxiliary path of the auxiliary sub-ADC 122 to occur at the same or at least substantially the same time as a subset of the sampling times

(e.g., $(0+0.1)t$, $(10+0.1)t$, $(20+0.1)t$, and so on) associated with that sub-ADC that occur at the sample time instants that the auxiliary samples occur.

[0057] In FIG. 1, once the calibration component 120 determines that the auxiliary sub-ADC 122 (and associated auxiliary path) is desirably (e.g., optimally, suitably, acceptably) aligned with a sub-ADC (e.g., 108, 110, or 112), the alignment of the auxiliary sub-ADC 122 and associated auxiliary path can be completed, and the auxiliary sub-ADC 122 and auxiliary path are ready to be used to facilitate calibrating the sub-ADCs (e.g., 108, 110, 112, etc.) of the array. With the aligning of the auxiliary sub-ADC 122 with a sub-ADC (e.g., 108, 110, or 112) of the array and the arrangement of the sampling of the auxiliary path in relation to the sampling of the other paths associated with the sub-ADC array, the calibration component 120 can thereby determine calibrations or adjustments that can be made to the other sub-ADCs (e.g., 108, 110, 112, etc.), and can calibrate or adjust the other sub-ADCs accordingly, because it is known that the sampling clock of the auxiliary path passes through all the sampling points of the other sub-ADCs. The auxiliary sub-ADC 122 can operate on a clock (e.g., auxiliary clock) that can be separate from, and can operate at a different frequency than, the clock used by the sub-ADCs (e.g., 108, 110, 112, etc.) in the array. Since the auxiliary sub-ADC 122 is a single, separate sub-ADC, it can be known that there is no timing skew associated with the auxiliary sub-ADC 122 because it uses only one clock (e.g., the auxiliary clock), so there is no different clock that can affect the auxiliary sub-ADC 122. As a result, the calibration component 120 can use information (e.g., auxiliary-signal-sample-related information) relating to the auxiliary sub-ADC and associated auxiliary path to compare against information (e.g., signal-sample-related information) relating to the sub-ADCs (e.g., 108, 110, 112, etc.) in the array.

[0058] The calibration component 120 can provide a reliable metric for detecting sampling path differences between signal paths associated with the sub-ADCs (e.g., 108, 110, 112, etc.) of the array under a wide range of conditions. For instance, to eliminate any assumptions or knowledge of the signal received by the receiver component (not shown) of the transceiver component 102, the calibration component 120 can determine (e.g., calculate) or extract the path difference information between paths of the array of sub-ADCs (e.g., 108, 110, 112, etc.) by computing a squared difference error

between the auxiliary samples of the auxiliary sub-ADC 122 and the respective corresponding samples of the other sub-ADCs (e.g., 108, 110, 112, etc.) of the array, as more fully disclosed herein. In some implementations, the calibration component 120 can determine an average of the squared difference error over a desired number of auxiliary samples of the auxiliary sub-ADC 122 and the respective corresponding samples of the other sub-ADCs (e.g., 108, 110, 112, etc.), and can use the average (or median or trend) of the squared difference error to determine or extract the path difference information between paths of the array of sub-ADCs to facilitate improving the estimation accuracy of the path differences between paths of the sub-ADCs (e.g., 108, 110, 112, etc.) of the array. This can allow for accurate (e.g., exact or substantially exact) computation of the path difference between paths of the sub-ADCs (e.g., 108, 110, 112, etc.) of the array without having to make any underlying assumption of the input statistics of the receiver component.

[0059] For example, with regard to the disclosed subject matter of the system 100, there is no need for assumptions or information about the statistical properties of the signals, such as stationary properties, bandwidth occupancy or symbol rate, oscillator frequencies, jitter spectrum, or any changes in such characteristics, in connection with the sub-ADCs (e.g., 108, 110, 112, etc.) of the array in order for the calibration component 120 to desirably determine the path differences between the paths associated with the sub-ADCs of the array, determine calibrations (e.g., adjustments) to be made to the sub-ADCs of the array to reduce or minimize such path differences, and perform such calibrations with respect to the sub-ADCs. Similarly, the calibration component 120 can determine and perform calibrations for the sub-ADCs (e.g., 108, 110, 112, etc.), without the need of knowledge of the characteristics of the signal itself, such as whether the signal is a broadband or narrowband signal, whether the signal is random data, pseudo-random data, multitone data, etc., or any relation between the received signal and the received sampling array.

[0060] In some implementations, the calibration component 120 also can perform calibrations for the sub-ADCs (e.g., 108, 110, 112, etc.) of the array to carry out timing skew estimation for the sub-ADCs. For instance, the auxiliary sub-ADC 122 can be configured to operate at a higher speed than the other sub-ADCs (e.g., 108, 110, 112, etc.) in the array to facilitate minimizing bandwidth mismatches among the sub-ADCs (e.g., 108, 110, 112, etc.). At

lower rates, the matching requirements for the sub-ADCs (e.g., 108, 110, 112, etc.) can be relaxed. The calibration component 120 can calibrate the sampler path so that it can provide reliable information that can be used by the calibration component 120 to correct or adjust the timing skew associated with the path. In some implementations, the calibration component 120 can program or configure the phase interpolator component 128 for the auxiliary path and the analog delay lines for the sampler paths of the sub-ADCs (e.g., 108, 110, 112, etc.) using an the defined alignment algorithm (e.g., initial calibration algorithm) that can facilitate aligning the auxiliary path to one of the data-path samplers (e.g., one of the sub-ADCs). The calibration component 120 also can control the bandwidth/frequency response of the auxiliary path.

[0061] In certain implementations, the calibration component 120 can employ an analog delay line to facilitate correcting the timing skew between paths or correcting other path differences between paths associated with the array of sub-ADCs (e.g., 108, 110, 112, etc.). For example, the calibration component 120 can determine an analog delay line that can be applied to a sub-ADC path to adjust the timing (e.g., sampling timing) of the sub-ADC path in relation to another sub-ADC path or the auxiliary path to facilitate correcting, reducing, or minimizing a timing skew between the sub-ADC path in relation to the other sub-ADC path or auxiliary path that was detected by the calibration component 120.

[0062] As another example, to facilitate correcting the timing skew between paths or correcting other path differences between paths associated with the array of sub-ADCs (e.g., 108, 110, 112, etc.), the calibration component 120 can employ the filter component 126 (e.g., which can be controlled by the calibration component 120) that can be operating on the samples from all or desired sub-ADCs (e.g., 108, 110, 112, etc.) of the array prior to combining the data stream, wherein the filter component 126 can be designed or set based at least in part on the difference error metric (e.g., squared difference error, or average (or median or trend) squared difference error) determined or extracted by the calibration component 120, as disclosed herein.

[0063] The filter component 126 can employ an analog filter that can be applied to one or more analog signals associated with one or more of the sub-ADC paths prior to those signals being converted to digital signals by the sub-ADCs (e.g., 108, 110, 112, etc.) and/or can employ a digital filter that can be

applied to one or more digital signals (e.g., one or more digital substreams) associated with one or more of the sub-ADC paths after the analog signals have been converted to the digital signals by the sub-ADCs (e.g., 108, 110, 112, etc.). The calibration component 120 can facilitate determining filter parameters, filter configuration, type (e.g., analog and/or digital) of filter, and/or other features of the filter(s) to be employed by the filter component 126 to generate the desired filter(s) to be applied to the signals to facilitate mitigating path differences between sub-ADC paths.

[0064] In some instances, for a variety of reasons (e.g., drift, integral nonlinearity (INL) issues, differential nonlinearity (DNL) issues, or other issues), it can be desirable to employ a hybrid approach comprising an analog filter and/or analog delay line as well as a digital filter to facilitate mitigating a path difference error for a sub-ADC array. For example, an analog filter and/or analog delay line may be able to correct 90% of a path difference error, but not the remaining 10% of the error, wherein, for a high-performance system, it may be desirable to achieve 100% or almost 100% correction of the error. The calibration component 120 can facilitate controlling the filter component 126 to produce a digital filter that can be applied to the digital signal of the path to correct all or almost all of the remaining 10% error.

[0065] In other implementations, the calibration component 120 can use information relating to the auxiliary samples from the auxiliary sub-ADC 122 and samples from the other sub-ADCs (e.g., 108, 110, 112, etc.) of the array to determine a transfer function difference between the paths associated with the sub-ADCs (e.g., 108, 110, 112, etc.) of the array. The calibration component 120 can correct (e.g., reduce, minimize, eliminate) the transfer function difference (e.g., transfer function error) between the paths associated with the sub-ADCs using one or more desired digital or analog techniques (e.g., analog delay line, analog filter, digital filter, iterative or adaptive techniques), as disclosed herein.

[0066] In still other implementations, the calibration component 120 (or another component associated with the system 100) can frequency lock the sampling clock (not shown in FIG. 1) used for the auxiliary sub-ADC 122 to the sampling clock (not shown in FIG. 1) associated with (e.g., used by) the other sub-ADCs (e.g., 108, 110, 112, etc.) of the array, while having a significantly higher jitter than the jitter of the sampling clock associated with the other sub-

ADCs (e.g., 108, 110, 112, etc.). The sampling clock associated with the auxiliary sub-ADC 122 and/or the sampling clock associated with the other sub-ADCs (e.g., 108, 110, 112, etc.) can sometimes have a small deviation or error such that the sampling of a signal on a path can occur at a slightly different time than the desired (e.g., nominal or scheduled) time (e.g., occurs at time $(5+0.1)t$ instead of at time $5t$), but still can, on average, sample the signal on the path at or practically at the desired time. With regard to the sampling clock associated with the auxiliary sub-ADC, if the sampling time deviation is minimal, such that, on average, it falls within a jitter average wherein the calibration component 120 is still able to desirably (e.g., accurately or substantially accurately, acceptably, optimally) determine the timing skew (e.g., the average timing skew over a defined time period) between sub-ADC paths, the jitter associated with the sampling clock associated with the auxiliary sub-ADC 122 can be relaxed to allow sampling time deviations by that sampling clock to the extent that the calibration component 120 is still able to desirably determine such timing skews, in accordance with a defined calibration criteria.

[0067] In yet other implementations, based at least in part on the results of the analysis of the sample-related information, the calibration component 120 can determine a timing offset for the sub-ADCs (e.g., 108, 110, 112, etc.) of the array that can reduce or minimize their squared difference error metric with respect to the auxiliary sub-ADC 122. The calibration component 120 can adjust one or more of the sub-ADC paths associated with the sub-ADCs (e.g., 108, 110, 112, etc.) by the timing offset to reduce or minimize the squared difference error metric of the sub-ADCs (e.g., 108, 110, 112, etc.) with respect to the auxiliary sub-ADC 122. In this way, it can be known that all of the sub-ADC path delays are equalized without the calibration component 120 (or other component) having to perform additional computations.

[0068] Also, based at least in part on the results of the analysis of the sample-related information, the calibration component 120 can determine the estimated path differences of each sub-ADC (e.g., 108, 110, 112, etc.) of the array. The calibration component 120 can use the estimated path differences to, for example, configure a correction filter, such as a sub-ADC path correction digital filter or analog filter, for the filter component 126 that can process all or desired sub-ADC signals to equalize or at least substantially equalize path differences between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.) to

reduce or minimize path difference errors between sub-ADC paths. In accordance with various implementations, the calibration component 120 can configure the sub-ADC path correction digital filter using iterative and/or adaptive techniques (e.g., least-mean-square (LMS) or recursive least squares (RLS) techniques or processes relating to channel estimation, path differences, and/or filtering) or using direct computation. For instance, the calibration component 120 and/or filter component 126 can employ an iterative or adaptive engine or function (e.g., an LMS engine or function) that can generate or synthesize a desired filter that can produce a desired filtered output (e.g., filtered signal) in response an input (e.g., input signal). In other implementations, with regard to the analog correction filter, the calibration component 120 can control the analog correction filter, based at least in part on the estimated sub-ADC channels of the sub-ADCs (e.g., 108, 110, 112, etc.), to facilitate desirably filtering all or desired sub-ADC signals to equalize or at least substantially equalize path differences between the paths of the sub-ADCs (e.g., 108, 110, 112, etc.).

[0069] The respective sub-ADCs (e.g., 108, 110, 112, etc.) of the array, as calibrated by the calibration component 120, can facilitate providing respective digital data substreams, which can correspond to the received signal (e.g., analog signal), as an output. The combiner component 116 can receive the respective digital data substreams and can combine, integrate, or deinterleave the respective digital data substreams of the respective sub-ADCs (e.g., 108, 110, 112, etc.) to generate, at a desirably high speed, a digital data stream that can desirably (e.g., accurately or substantially accurately, optimally, acceptably) represent the data contained in the analog signal that was received by the transceiver component 102, wherein the digital data stream can be free or at least substantially and suitably free of distortion.

[0070] FIG. 5 (along with FIG.1) depicts a diagram of an embodiment of a system 500 that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences. The system 500 can illustrate aspects relating to the defined calibration algorithm.

[0071] The system 500 can comprise a calibration component 502, and an ADC component 504, comprising an auxiliary sub-ADC 506 and a set of sub-ADCs (e.g., an array of k sub-ADCs), comprising sub-ADC₁ 508 up through sub-

ADC_k 510, wherein k can equal 8 in this non-limiting example embodiment. The calibration component 502, ADC component 504, auxiliary sub-ADC 506 and set of sub-ADCs can be the same as or similar to, and/or can comprise the same or similar functionality as, respective components (e.g., respectively named components), as more fully described herein.

[0072] Each of the sub-ADCs (e.g., 508, 510, etc.) of the set of sub-ADCs can comprise a PGA, a sampler component (sampler), and a converter component (e.g., an ADC, such as a successive approximation register (SAR) ADC), among other components or features. For instance, the sub-ADC₁ 508 can comprise PGA₁ 512, sampler component₁ 514, and converter component₁ 516, and sub-ADC_k 510 can comprise PGA_k 518, sampler component_k 520, and converter component_k 522. The auxiliary sub-ADC 506 can be designed to closely (e.g., substantially) match the processing paths of the other sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) of the array. For instance, the auxiliary sub-ADC 506 can comprise a calibration PGA 524 (CAL PGA), a calibration sampler component 526 (Cal Sampler), and a calibration converter component 528 (SAR ADC), wherein the calibration PGA 524, calibration sampler component 526, and calibration converter component 528 can be the same as or similar to the corresponding components of the sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510). The sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) and auxiliary sub-ADC 506 also can be closely matched to each other with regard to other components (e.g., buffers) and features (e.g., bandwidth) that can be part of the respective paths of the sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) and auxiliary sub-ADC 506.

[0073] The respective PGAs (e.g., 512, 518, 524) can be employed in the respective paths of the auxiliary sub-ADC 506 and sub-ADCs 508 and 510 to provide signal gain (e.g., by amplifying lower-amplitude signals) to the respective paths and improve (e.g., increase) the dynamic range of the respective paths prior to the respective signals being provided to the respective converter components (e.g., 516, 522, 528). The respective sampler components (e.g., 514, 520, 526) can perform the sampling of the respective analog signals on the respective paths, in accordance with a desired sampling frequency, to facilitate the analog-to-digital conversion of the respective analog signals to corresponding digital signals (e.g., digital samples). The respective

converter components (e.g., 516, 522, 528) can convert the respective analog samples to corresponding digital samples, in accordance with the respective sampling frequencies associated with the respective converter components (e.g., 516, 522, 528), based at least in part on the respective clocks (e.g., calibration clock 530 ($f_{\text{calib_clk}}$) and clock 532 (f_{clk})) associated with the respective converter components (e.g., 516, 522, 528).

[0074] The calibration clock 530 can operate at a different (e.g., higher) frequency (e.g., 2.24 GHz, as depicted in FIG. 5) than the frequency (e.g., 437.5 MHz, as depicted in FIG. 5) at which the clock 532 operates to facilitate enabling the auxiliary sub-ADC 506 to have a different (e.g., lower) sampling timing than the sampling timing associated with the other sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) of the ADC component 504. This can enable the auxiliary sub-ADC 506 to have a sampling time (e.g., auxiliary sampling time) on the auxiliary path that can have a different rate than that of the other sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) to enable the auxiliary sub-ADC 506 to pass through the sampling times of all of the desired samples for all sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) of the sub-ADC array and to reduce power consumption associated with the auxiliary path, as more fully disclosed herein.

[0075] While the components of the auxiliary sub-ADC 506 can closely match the corresponding components of the other sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510), not every component of the auxiliary sub-ADC 506 has to be identical to the corresponding component of the other sub-ADCs. For example, the calibration converter component 528 can be similar to, but different from, the converter components (e.g., 516, 522) of the other sub-ADCs, since the calibration converter component 528 is not converting data from the received analog signals, but rather is being used to facilitate calibrating the other sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510), and since it can be desirable to, for example, reduce power consumption associated with the auxiliary path, reduce area used by the auxiliary path, and/or reduce costs associated with the auxiliary path and its components. For instance, as depicted in the system 500 of FIG. 5, while the converter components (e.g., 516, 522) of the other sub-ADCs each can comprise 16x7-bit ADC converters, the calibration converter component 528 of the auxiliary sub-ADC 506 can comprise a 1x5-bit ADC converter.

[0076] The calibration component 502 can analyze the auxiliary signals (e.g., auxiliary samples) and respective signals (e.g., samples) of the sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510) and can determine path differences (e.g., timing skew errors, bandwidth differences, and/or other types of path differences) between the respective paths of the auxiliary sub-ADC 506 and the sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510). The calibration component 502 can determine calibrations or adjustments that can be made or applied to the auxiliary sub-ADC 506, and/or the auxiliary signal on the auxiliary path, and the sub-ADCs (e.g., sub-ADC₁ 508 up through sub-ADC_k 510), and/or the respective signals on the respective sub-ADC paths, to correct or mitigate the path differences, based at least in part on the analysis results. For instance, in **FIG. 5**, the system 500 illustrates the calibration component 502 determining (e.g., computing) timing skew errors between the respective paths (at reference numeral 534, determining or generating respective timing-skew averaging blocks (at reference numeral 536), and applying or providing those respective timing-skew averaging blocks to control logic and an analog delay line(s) (at reference numeral 538) to facilitate determining calibrations and adjustments to be applied to the respective sub-ADCs (e.g., 506, 508, 510, etc.) and/or respective paths using analog and/or digital techniques (e.g., analog delay lines, analog and/or digital filtering, etc.) to correct or mitigate the path differences. The calibration component 502 can apply such calibrations or adjustments to the respective sub-ADCs (e.g., 506, 508, 510, etc.) and/or respective paths using the analog and/or digital techniques to correct or mitigate the path differences.

[0077] **FIG. 6** illustrates a block diagram of an embodiment of a transceiver component 600. The transceiver component 600 can be used to transmit or receive voice or data communications. In some implementations, the transceiver component 600 can be a full-duplex transceiver

[0078] The transceiver component 600 can comprise a transmitter component 602 that can comprise one or more transmitter sub-components (e.g., transmitters) that can facilitate transmitting voice information or data from the transceiver component 600 to a communication device that is communicatively connected to the transceiver component 600 via a wireline, optical, or wireless communication connection (e.g., communication channel).

In some implementations, the transmitter component 602 can include, for example, a set (e.g., 2, 3, 4, ...) of transmitter sub-components.

[0079] The transceiver component 600 also can comprise a receiver component 604 that can comprise one or more receiver sub-components (e.g., receivers) that can facilitate receiving voice information or data from a communication device that is communicatively connected to the transceiver component 600 via a wireline, optical, or wireless communication connection (e.g., communication channel). In some implementations, the receiver component 604 can include, for example, a set (e.g., 2, 3, 4, ...) of receiver sub-components.

[0080] The transceiver component 600 also can comprise an interleaver component 606 that can be employed to interleave a received analog signal across the respective interleaved sub-ADCs of a sub-ADC array of the ADC component 608. In some implementations, the interleaver component 606 (or the calibration component 614) can process the analog signal to implement or introduce respective time delays to the analog signal to generate time-delayed analog signals (e.g., having respective time delays) prior to the signal being input to the ADC component 608.

[0081] The transceiver component 600 can include an ADC component 608 that can comprise a set of sub-ADCs 610 that can be arranged or configured in an interleaved structure to facilitate converting analog signals to digital signals. The respective sub-ADCs of the set 610 of the ADC component 608 can receive respective analog signals (e.g., respectively time-delayed analog signals) in connection with an analog signal received from a remote communication device, can sample (e.g., using a sample component(s)) the respective analog signals, and can convert or digitize (e.g., via a converter or digitizer component(s)) the respective analog signals to respective digital data samples that can have digital values that can correspond to the respective analog signals (e.g., can correspond to the analog values of the analog signal samples).

[0082] The ADC component 608 also can comprise an auxiliary sub-ADC 612 associated with an auxiliary path, wherein the auxiliary path can closely match the sub-ADCs paths of the sub-ADCs 610. The auxiliary sub-ADC 612 and associated auxiliary path can process an auxiliary signal, including sampling and converting an analog auxiliary signal to digital auxiliary signal

(e.g., sample), for use by the calibration component 614 to facilitate determining path differences between the paths of the respective sub-ADCs (e.g., the auxiliary sub-ADC 612 and the respective sub-ADCs of the set 610).

[0083] The calibration component 614 can analyze the auxiliary signal on the auxiliary path associated with the auxiliary sub-ADC 612 and the respective signals on the respective paths of the respective sub-ADCs 610 to facilitate determining and applying calibrations or adjustments that can be made or applied to the respective sub-ADCs of the set 610 and/or their respective sub-ADC paths (and/or respective signals) to correct or mitigate path differences (e.g., path difference errors) between the respective paths of the respective sub-ADCs. This can facilitate mitigating distortions that would otherwise have been caused as a result of the uncorrected or unmitigated path differences. In accordance with various aspects, the calibration component 614 can comprise, for example, a calibration management component 616, a monitor component 618, an analyzer component 620, an alignment component 622, a phase interpolator component 624 (PHASE INTER. COMPONENT), a calculator component 626, a path difference determination component 628 (PATH DIF. DETERMIN. COMPONENT), a channel estimator component 630, an offset component 632, and a filter component 634.

[0084] The calibration management component 616 can control or manage operations of the various components (e.g., monitor component 618, analyzer component 620, an alignment component 622, etc.) of the calibration management component 616, data flow between the various components of the calibration management component 616, data between the calibration management component 616 and other components (e.g., the ADC component 608, the combiner component 636, the processor component 640, the data store 642, etc.), and/or other operations of or associated with the calibration management component 616. Employing the various components of the calibration management component 616, the calibration management component 616 also can respectively calibrate or adjust the respective sub-ADCs of the ADC component 608 and/or information or paths (e.g., sub-ADC paths) associated with the respective sub-ADCs to facilitate correcting or mitigating the respective sub-ADC path differences between paths (e.g., correcting, mitigating, equalizing or substantially equalizing path differences between the sub-ADC paths) associated with the respective sub-ADCs.

[0085] The monitor component 618 can monitor, sense, or detect information, such as information relating to auxiliary samples on the auxiliary path, samples on the respective sub-ADC paths, path differences between paths, communication conditions, information relating to transfer characteristics, etc., associated with the transceiver component 600. For instance, the monitor component 618 can monitor, sense, or detect information relating to auxiliary samples on the auxiliary path and samples on the respective sub-ADC paths, wherein such information can facilitate determining path differences between paths of the respective sub-ADCs of the ADC component 608.

[0086] The analyzer component 620 can analyze, evaluate, or compare data associated with the transceiver component 600 to facilitate calibrating or adjusting the respective sub-ADCs of the ADC component 308 and/or information or paths (e.g., sub-ADC paths) associated with the respective sub-ADCs to facilitate correcting or mitigating the respective sub-ADC path differences (e.g., equalizing or substantially equalizing the respective sub-ADC paths) associated with the respective sub-ADCs. The data that can be analyzed by the analyzer component 620 can relate to, for example, analog or digital samples associated with the respective sub-ADCs of the set 610, digital samples associated with the auxiliary sub-ADC 612, recovered data (e.g., digital data) associated with (e.g., obtained from) a received analog signal, various types of transfer characteristics that can be associated with the respective sub-ADCs, information relating to channel estimation or channel responses, information resulting from calculations performed by the calculator component 626, information relating to respective transfer functions associated with respective sub-ADCs, information relating to respective path differences between respective sub-ADCs, and/or other information relating to calibration of the sub-ADCs. Based at least in part on the data analysis, the analyzer component 620 can generate analysis results that can be used by the calibration management component 616 to facilitate making determinations relating to calibration or adjustment of the respective sub-ADCs of the ADC component 608 and/or information or paths associated with the respective sub-ADCs to facilitate correcting or mitigating the respective sub-ADC path differences between paths associated with the respective sub-ADCs.

[0087] The alignment component 622 can align or calibrate (e.g., initially align or calibrate, re-align or re-calibrate) the auxiliary sub-ADC 612 with or to a

sub-ADC of the set 610, in accordance with a defined alignment algorithm. In some implementations, the calibration component 614 can comprise or be associated with the phase interpolator component 624, which can be associated with the auxiliary sub-ADC 612 to facilitate adjusting a phase or time difference between the auxiliary sub-ADC 612 and the sub-ADCs of the set 610 to facilitate aligning or calibrating the auxiliary sub-ADC 612 with or to a sub-ADC of the set 610.

[0088] For instance, the phase interpolator component 624 can enable the auxiliary sub-ADC 612 to be lined up to any one of the sampling instants of a sub-ADC of the set 610. The alignment component 622 also can employ analog delay lines that can be applied to the auxiliary path (and associated auxiliary signal) associated with the auxiliary sub-ADC 612 or a path (and associated signal) associated with a sub-ADC of the set 610 to facilitate delaying an auxiliary signal or signal, respectively, to facilitate aligning or calibrating the auxiliary sub-ADC 612 with or to the sub-ADC. An auxiliary path sampling rate, a phase interpolator of the phase interpolator component 624, and analog delay lines can be suitably designed or controlled (e.g., by the alignment component 622 and/or the calibration management component 616) to facilitate establishing an initial match (or at least substantial match) between sampling instants of the auxiliary sub-ADC 612 and a sub-ADC of the set 610.

[0089] In some implementations, the alignment component 622 and/or the calibration management component 616 can control the phase interpolator component 624 to adjust the phase of the auxiliary sub-ADC 612 in connection with the auxiliary path and/or can facilitate adjusting or selecting an analog delay line that can be applied to the auxiliary path (and associated auxiliary signal) to facilitate performing an alignment (e.g., initial alignment) of the auxiliary sub-ADC 612 and auxiliary path with a sub-ADC of the set 610 and the associated sub-ADC path. For each phase interpolator delay and analog delay line delay, the alignment component 622 can examine (e.g., analyze, evaluate) the samples of all of the sub-ADCs of the set 610 for each one of their analog delay lines or paths to determine whether the auxiliary sub-ADC 612 is aligned with a sub-ADC of the set 610. When alignment of the auxiliary sub-ADC 612 is determined to be achieved, the alignment component 622 can end the alignment process and can transmit an alignment indicator to the calibration management component 616, wherein the alignment indicator can indicate that

the desired alignment of the auxiliary sub-ADC 612 with a sub-ADC of the set 610 has been achieved.

[0090] The calculator component 626 can perform calculations (e.g., mathematical calculations) on data values using equations, including the equations disclosed herein, and/or matrices, to generate calculation results. For example, the calculator component 626 can calculate the squared difference error or average (or median or trend) squared difference error between an auxiliary sample (or average, median, or trend value of auxiliary samples) for the auxiliary sub-ADC 612 and a corresponding sample (or average, median, or trend value of corresponding samples) associated with a sub-ADC of the set 610. The calibration management component 616 can use the calculation results to facilitate calibrating or adjusting the respective sub-ADCs of the ADC component 608 and/or information or paths (e.g., sub-ADC paths) associated with the respective arrays to facilitate correcting or mitigating the respective sub-ADC path differences associated with the respective sub-ADCs of the set 610.

[0091] The path difference determination component 628 can be employed to determine differences between the respective paths of the sub-ADCs of the set 610 as well as between the auxiliary path of the auxiliary sub-ADC 612 and the paths of the sub-ADCs of the set 610, based at least in part on analysis results from the analyzer component 620, calculation results (e.g., squared difference error results or other results) from the calculator component 626, or other information. For example, the path difference determination component 628 can determine differences between the respective paths of the sub-ADCs of the set 610 and/or between the auxiliary path of the auxiliary sub-ADC 612 and the paths of the sub-ADCs of the set 610, based at least in part on the results (e.g., analysis or calculation results) relating to the comparison of the auxiliary signal associated with the auxiliary sub-ADC 612 and the respective signals associated with the respective sub-ADCs of the set 610.

[0092] The channel estimator component 630 can perform channel estimations or determinations to facilitate determining respective transfer functions associated with, and/or a transfer function difference between, the respective paths of the respective sub-ADCs of the ADC component 608, for example, using a desired channel estimation technique. The channel estimator component 630 can employ any of a number of channel estimation techniques

to facilitate determining such transfer functions. For example, the channel estimator component 630 can use a least-squares channel estimation technique, a data cross-correlation technique, an iterative channel estimation technique (e.g., LMS channel estimation, RLS channel estimation, blind channel estimation, etc.), or another desired channel estimation technique, to facilitate determining such transfer functions or transfer function differences.

[0093] The offset component 632 can be used by the calibration management component 616, for example, to facilitate adjusting an offset(s), such as a timing offset(s), associated with a sub-ADC path(s) to facilitate reducing or minimizing a path difference(s) (e.g., based on a squared difference error metric) between the respective paths of the respective sub-ADCs of the set 610 and/or between the paths of the sub-ADCs of the set 610 and the auxiliary path associated with the auxiliary sub-ADC 612. For example, based at least in part on the results of the analysis of the sample-related information, the calibration management component 616 or offset component 632 can determine a timing offset that can be applied to a sub-ADC(s) of a sub-ADC array that can reduce or minimize a squared difference error metric associated with the sub-ADC(s) with respect to the auxiliary sub-ADC 612. The calibration management component 616 or offset component 632 can adjust one or more of the sub-ADC paths associated with one or more of the sub-ADCs of the ADC component 608 by the timing offset(s) to reduce or minimize the squared difference error metric determined with respect to the paths of the sub-ADCs with respect to the auxiliary sub-ADC 122. In this way, it can be known that all of the sub-ADC path delays are equalized without the calibration component 120 (or other component) having to perform additional computations.

[0094] In some implementations, the offset component 632 can be employed to implement or introduce one or more timing offsets to facilitate measuring, determining, or estimating respective channel responses (e.g., by the channel estimator component 630) of respective sub-ADC paths at the one or more offsets, and/or to facilitate correcting or mitigating path differences between sub-ADCs of the set 610. In other implementations, the offset component 632 can be used by the calibration management component 616 to facilitate adjusting a timing offset(s) associated with a sub-ADC path(s) to facilitate adjusting respective transfer functions of respective sub-ADCs of the

set 610 until the respective transfer functions of the respective sub-ADCs are the same or at least substantially the same.

[0095] The filter component 634 can comprise one or more analog or digital filters that can filter or process information, such as analog signals (e.g., analog data samples) or digital signals (e.g., digital data samples), to facilitate correcting, mitigating, or equalizing (or at least substantially equalizing) sub-ADC path differences between respective paths of the sub-ADCs of the ADC component 608. The filter component 634 can facilitate configuring a filter(s) (e.g., an analog correction filter or a digital correction filter) based at least in part on information relating to estimated or determined channel responses of each ADC sub-component of the ADC component 608. The filter component 634 can use the configured filter(s) to facilitate processing (e.g., filtering) respective sub-ADC signals of the respective sub-ADCs to facilitate correcting, mitigating, or equalizing path differences between the respective sub-ADCs of the ADC component 608. In accordance with implementations, the filter component 634 can configure a filter (e.g., a sub-ADC path correction digital filter) using iterative or adaptive techniques (e.g., LMS or RLS techniques), or using direct computation (e.g., as facilitated by the calculator component 626). In certain implementations, the filter component 634 can employ a correction filter that can be an analog filter, wherein the calibration management component 616 can facilitate controlling or configuring the analog correction filter, based at least in part on the information of the estimated or determined channel responses of the respective ADC sub-components, to facilitate processing the respective sub-ADC signals to facilitate equalizing or at least substantially equalizing path differences between the respective ADC sub-components of the ADC component 608.

[0096] The transceiver component 600 also can comprise a combiner component 636 that can combine, integrate, or deinterleave the respective digital data substreams of the respective sub-ADCs of the ADC component 608 to generate a digital data stream that can accurately represent the data contained in the received analog signal. The combiner component 636 can be associated with (e.g., communicatively connected to) the ADC component 608 to facilitate receiving the digital data substreams from the sub-ADCs of the ADC component 608. The combiner component 636 also can be associated with the calibration component 614 to facilitate providing the respective digital data

substreams (e.g., respective digital data samples) to the calibration component 614 for analysis by the calibration component 614 to facilitate calibrating or adjusting the respective sub-ADCs of the ADC component 608 and/or information or paths associated with the respective sub-ADCs to facilitate correcting or mitigating the respective sub-ADC path differences (e.g., equalizing or substantially equalizing the respective sub-ADC paths) associated with the respective sub-ADCs of the ADC component 608.

[0097] The transceiver component 600 also can comprise a decoder component 638 that can decode and/or error correct the digital data stream, comprising the combined or integrated digital data samples of digital data substreams output from the sub-ADCs of the ADC component 608, to facilitate determining or recovering the data (e.g., determining the data values of data) that was sent in the analog signal to the transceiver component 600, in accordance with a desired decoding and/or error correction techniques. The decoder component 638 can employ, for example, a Reed-Solomon algorithm, a Hamming code, a Bose, Ray-Chaudhuri, Hocquenghem (BCH) algorithm, a forward error correction (FEC) algorithm, or other decoding algorithm or error correction algorithm, etc., to facilitate decoding and/or correcting errors associated with the respective digital data samples of the digital data substreams to facilitate determining or recovering the data of the analog signal.

[0098] The transceiver component 600 also can comprise a processor component 640 that can operate in conjunction with the other components (e.g., transmitter component 602, receiver component 604, interleaver component 606, ADC component 608, calibration component 614, etc.) to facilitate performing the various functions of the transceiver component 600, such as disclosed herein. The processor component 640 can employ one or more processors (e.g., central processing units (CPUs), graphical processing units (GPUs), field-programmable gate arrays (FPGAs), etc.), microprocessors, or controllers that can process data, such as information (e.g., voice or data information) relating to operations performed by the transceiver component 600, etc., to facilitate transmitting signals, receiving signals, generating auxiliary signals, calibrating or adjusting the set of sub-ADCs 610 and the auxiliary sub-ADC 612, calibrating or adjusting information or paths associated with sub-ADCs in the set 610 and the auxiliary sub-ADC 612, performing channel estimation, performing calculations, configuring filters, filtering signals, and/or

performing other operations; and can control data flow between the transceiver component 600 and other components associated with (e.g., connected to) the transceiver component 600 and can control data flow between various components of the transceiver component 600.

[0099] In another aspect, the transceiver component 600 also can include a data store 642 that can store data structures (e.g., voice information, data, metadata); code structure(s) (e.g., modules, objects, classes, procedures), commands, or instructions; information relating to transmitting signals, receiving signals, generating auxiliary signals, calibrating or adjusting the set of sub-ADCs 610 and the auxiliary sub-ADC 612, calibrating or adjusting information or paths associated with the set of sub-ADCs 610 and the auxiliary sub-ADC 612, performing channel estimation, performing calculations, configuring filters, filtering signals, and/or performing other operations; parameter data; information relating to algorithms (e.g., algorithm(s) relating to calibrating sub-ADCs, algorithm(s) relating to configuring an analog or digital filter, algorithm(s) (e.g., the defined alignment algorithm) relating to aligning the auxiliary sub-ADC 612 with a sub-ADC of the set 610, algorithm(s) relating to channel estimation, etc.); defined path correction criterion(s); and so on. In an aspect, the processor component 640 can be functionally coupled (e.g., through a memory bus) to the data store 642 in order to store and retrieve information desired to operate and/or confer functionality, at least in part, to the transmitter component 602, receiver component 604, interleaver component 606, ADC component 608, calibration component 614, etc., and/or substantially any other operational aspects of the transceiver component 600. The various components of the transceiver component 600 can communicate information between each other and/or between other components associated with the transceiver component 600 as desired to carry out operations of the transceiver component 600. Respective components (e.g., transmitter component 602, receiver component 604, interleaver component 606, ADC component 608, calibration component 614, etc.) of the transceiver component 600 each can be a stand-alone unit, can be included within the transceiver component 600 (as depicted), can be incorporated within another component of the transceiver component 600 or a component separate from the transceiver component 600, and/or virtually any suitable combination thereof, as desired.

[00100] Methods may be better appreciated with reference to the flow charts of **FIGs. 7-9**. For simplicity, while the methods are shown as a series of blocks, the claimed subject matter is not limited by the order of the blocks, as some blocks may occur in different orders and/or concurrently with other blocks from what is depicted and described herein. Moreover, not all illustrated blocks may be required to implement the methods described hereinafter.

[00101] **FIG. 7** illustrates a flow diagram of an example method 700 that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences. The method 700 can be implemented by a communication device, such as a transceiver component, which can comprise a calibration component and an ADC component, for example.

[00102] At block 702, path differences between respective sub-ADCs of a sub-ADC array can be determined based at least in part on results of an analysis of respective signals associated with the respective sub-ADCs and an auxiliary signal associated with an auxiliary sub-ADC. The communication device can receive an analog signal, comprising data, from another communication device. The sub-ADCs of the ADC component, which can be interleaved, can sample and digitize the analog signal, wherein the respective sub-ADCs can receive the analog signal with respective time-delays. The data (e.g., digital data) can be recovered from the digitized data samples (e.g., after the digitized data samples are decoded by a decoder component).

[00103] In addition to the sub-ADCs that can convert analog data signals to digital data signals, the ADC component can comprise the auxiliary sub-ADC, wherein an auxiliary signal can be routed via an auxiliary path associated with the auxiliary sub-ADC. The calibration component can analyze (e.g., evaluate, compare) the respective signals associated with the respective sub-ADCs and the auxiliary signal associated with the auxiliary sub-ADC. Based at least in part on the analysis results, the calibration component can determine the path differences between the respective sub-ADCs of the sub-ADC array, for example. The path differences can relate to, example, timing skews between respective paths of the sub-ADCs, path channel or bandwidth mismatches between respective sub-ADC paths, or other types of path differences or errors between respective sub-ADC paths that can cause distortion in the recovered

digital data stream generated by the ADC component in response to the received analog signal.

[00104] At block 704, the respective sub-ADCs of the sub-ADC array can be calibrated, based at least in part on the path differences between the respective sub-ADCs, to facilitate reducing or minimizing path differences between the respective sub-ADCs of the sub-ADC array. The calibration component can determine one or more calibrations or adjustments that can be applied to one or more of the respective sub-ADCs of the sub-ADC array, based at least in part on the determined path differences between the respective sub-ADCs of the sub-ADC array, to facilitate reducing, minimizing, correcting, or mitigating path differences between the respective sub-ADCs of the sub-ADC array. For instance, the calibration component can determine a timing adjustment, a bandwidth adjustment, a transfer function, or other type of calibration that can be applied to one or more of the respective sub-ADCs, based at least in part on the determined path differences between the respective sub-ADCs, to calibrate the respective sub-ADCs. The calibration of the sub-ADCs can facilitate reducing or mitigating distortions in the digital data stream that otherwise may have been caused as a result of the uncorrected or unmitigated path differences.

[00105] The communication device also can comprise a combiner component that can combine or integrate the respective digital data substreams from the respective sub-ADCs to generate a digital data stream that can correspond to the data from the received analog signal. As desired, the digital data stream can be further processed (e.g., using an equalizer component and/or decoder component) or can be provided (e.g., presented or displayed) as an output.

[00106] FIG. 8 depicts a flow diagram of another example method 800 that can facilitate calibrating sub-ADCs of an array of sub-ADCs of a transceiver component to facilitate correcting or mitigating sub-ADC path differences. The method 800 can be implemented by a communication device, such as a transceiver component, which can comprise an interleaver component, an ADC component comprising an auxiliary sub-ADC and a set of sub-ADCs, a calibration component, a decoder component, and a combiner component, for example.

[00107] At block 802, the auxiliary sub-ADC can be aligned with a sub-ADC of the set of sub-ADCs. The calibration component can align or calibrate (e.g., initially align or calibrate, or re-align or re-calibrate) the auxiliary sub-ADC with a sub-ADC of the set of sub-ADCs. The calibration component can align or calibrate the auxiliary sub-ADC with a sub-ADC of the set of sub-ADCs to enable the sampling of the auxiliary sub-ADC to be aligned with the sub-ADC. The calibration component can comprise or be associated with a phase interpolator component and/or can employ a delay line(s) (e.g., analog delay line(s)) that can be used to facilitate aligning or calibrating the auxiliary sub-ADC with the sub-ADC. For instance, the calibration component can select an auxiliary sampling rate, and can align the auxiliary sampling time associated with the auxiliary sub-ADC with a sampling time associated with a sub-ADC, to enable the sampling of the auxiliary signal associated with the auxiliary path of the auxiliary sub-ADC to occur at the same or at least substantially the same time as a subset of the sampling times associated with the sub-ADC.

[00108] At block 804, an analog signal, comprising data, can be received. The communication device can receive the analog signal from another communication device via a wireline or wireless communication channel or medium.

[00109] At block 806, the analog signal can be interleaved across respective interleaved sub-ADCs of a set (e.g., an array) of sub-ADCs. An interleaver component can facilitate interleaving the analog signal across the respective sub-ADCs, wherein the respective sub-ADCs can receive the analog signal with respective time-delays from the interleaver component.

[00110] At block 808, the respective time-delayed analog signals associated with the respective sub-ADCs and an auxiliary signal associated with the auxiliary sub-ADC can be sampled to generate respective analog data samples associated with the respective sub-ADCs and auxiliary samples associated with the auxiliary sub-ADC to facilitate digitizing the respective time-delayed analog signals and to facilitate determining path differences between the respective sub-ADCs. The respective sub-ADCs (or a sampler component associated with the sub-ADCs) can sample the respective time-delayed analog signals to generate the respective analog data samples, wherein the respective sub-ADCs can be sampled at respective sampling times (e.g., a first sub-ADC can be sampled at times 0 , $2t$, $4t$, $6t$, and so on, whereas a second sub-ADC

can be sampled at times $1t$, $3t$, $5t$, $7t$, and so on). The auxiliary sub-ADC (or an auxiliary sampler associated with the auxiliary sub-ADC) can be sampled at a sampling rate that can enable the auxiliary sub-ADC to sample the auxiliary signal at times that can correspond to one or more respective sampling times of each of the sub-ADCs of the set of sub-ADCs over a defined period of time.

[00111] In some implementations, the sampling rate associated with the auxiliary sub-ADC can be a lower rate than the sampling rate associated with the sub-ADCs. For example, if the set of sub-ADCs comprises the first sub-ADC and the second sub-ADC that are sampled at respective times, as indicated above, the calibration component (or another component) can set the sampling rate associated with the auxiliary path (and auxiliary sub-ADC) to sample at a slower rate, such as every $5t$, wherein the auxiliary signal can be sampled by the auxiliary sub-ADC or sampler at $5t$, $10t$, $15t$, $20t$, and so on.

[00112] At block 810, the respective analog data samples and the auxiliary sample can be converted to respective digital data samples and a digital auxiliary samples. The respective sub-ADCs can analyze the respective analog data samples and can digitize or convert the analog data samples to the respective digital data samples, wherein the respective digital data samples can correspond to the respective analog data samples. The auxiliary sub-ADC can analyze the analog auxiliary samples and can digitize or convert the analog auxiliary samples to a corresponding digital auxiliary samples.

[00113] At block 812, respective signals (e.g., analog or digital data samples) associated with the sub-ADCs and the auxiliary signal (e.g., analog or digital auxiliary samples) associated with the auxiliary sub-ADC can be analyzed. The calibration component can analyze (e.g., evaluate, compare) the respective signals associated with the sub-ADCs and the auxiliary signal associated with the auxiliary sub-ADC to facilitate determining path differences between respective sub-ADCs of the set of sub-ADCs. For example, the calibration component can evaluate or compare characteristics associated with the auxiliary signal in relation to respective characteristics associated with the respective signals associated with the sub-ADCs to facilitate determining the path differences between respective sub-ADCs.

[00114] At block 814, path differences between respective sub-ADCs of the set of sub-ADCs can be determined based at least in part on results of the analysis of the respective signals associated with the respective sub-ADCs and

an auxiliary signal associated with an auxiliary sub-ADC. The calibration component can determine the path differences between respective sub-ADCs based at least in part on the results of analyzing (e.g., evaluating, comparing) characteristics associated with the auxiliary signal and the respective characteristics associated with the respective signals associated with the sub-ADCs.

[00115] At block 816, the respective sub-ADCs of the set of sub-ADCs can be calibrated, based at least in part on the path differences between the respective sub-ADCs, to facilitate reducing or minimizing path differences between the respective sub-ADCs. The calibration component can determine one or more calibrations or adjustments that can be applied to one or more of the respective sub-ADCs of the set of sub-ADCs, based at least in part on the determined path differences (e.g., timing skew(s), bandwidth difference(s), other path difference(s)) between the respective sub-ADCs, to facilitate reducing, minimizing, correcting, or mitigating path differences between the respective sub-ADCs of the sub-ADC array.

[00116] With the sub-ADCs of the set of sub-ADCs calibrated by the calibration component, the respective sub-ADCs can operate to produce respective digital data substreams comprising respective digital data samples, wherein distortion or error for a digital data substream can be reduced or minimized when the respective digital data substreams are combined to generate the digital data stream. Thus, the calibration component and the method 800 can facilitate mitigating distortions that would otherwise have been caused as a result of uncorrected or unmitigated path differences.

[00117] At block 818, the respective data (e.g., data values) of the respective digital data samples can be determined. In some implementations, the combiner component can combine or integrate the respective digital data substreams (e.g., the respective digital data samples) of the respective sub-ADCs to generate a digital data stream, wherein the digital data stream can comprise data that can correspond to the data (e.g., in analog form) contained in the received analog signal. The decoder component can decode the digital data stream, comprising the digital data samples, to facilitate recovering (e.g., determining) the respective data from (of) the respective digital data samples. As desired, the respective data can be further processed or can be provided (e.g., presented or displayed) as an output.

[00118] FIG. 9 is a flow diagram of an example method 900 that can align or calibrate an auxiliary sub-ADC (and associated auxiliary path) with a sub-ADC (and associated sub-ADC path) of a set (e.g., an array) of sub-ADCs. The method 900 can be implemented by a communication device, such as a transceiver component, which can comprise an ADC component and a calibration component, for example. The ADC component can comprise an auxiliary sub-ADC and a set of sub-ADCs, wherein the set of sub-ADCs can be employed to convert analog signals to digital signals, and the auxiliary sub-ADC can be employed to facilitate calibrating the set of sub-ADCs. The auxiliary sub-ADC can comprise or be associated with, and can employ, a phase interpolator component and/or can employ delay lines (e.g., analog delay lines) to facilitate aligning or calibrating the auxiliary sub-ADC with a sub-ADC of the set of sub-ADCs.

[00119] At block 902, one or more respective sampling times can be determined for one or more respective sub-ADCs of the set of sub-ADCs. At block 904, an auxiliary sampling time can be determined for the auxiliary sub-ADC. The calibration component can determine the respective sampling times associated with the respective sub-ADCs and the auxiliary sampling time associated with the auxiliary sub-ADC.

[00120] At block 906, the respective sampling times associated with the respective sub-ADCs can be compared with the auxiliary sampling time associated with the auxiliary sub-ADC. The calibration component can analyze the respective sampling times and the auxiliary sampling time. As part of the analysis, the calibration component can compare the respective sampling times with the auxiliary sampling time.

[00121] At block 908, a determination can be made regarding whether the auxiliary sampling time is aligned (or at least substantially aligned) with any one of the respective sampling times associated with the respective sub-ADCs. Based at least in part on the results of the comparison of the respective sampling times with the auxiliary sampling time, the calibration component can determine whether the auxiliary sampling time is aligned (or at least substantially aligned) with any one of the respective sampling times.

[00122] If it is determined that the auxiliary sampling time is not aligned (or is not at least substantially aligned) with any one of the respective sampling times associated with the respective sub-ADCs, at block 910, the auxiliary

sampling time can be adjusted by a defined amount of time to facilitate aligning the auxiliary sub-ADC with a sub-ADC of the set of sub-ADCs. For example, if the auxiliary sampling time starts with a sampling error or offset of $0.2t$, instead of sampling at time 0, and a sub-ADC of the set is associated with a sampling time that starts with a sampling error or offset of $0.1t$, the calibration component can determine that the auxiliary sampling time is not aligned (or is not at least substantially aligned) with the sampling time associated with the sub-ADC. The calibration component can determine a time adjustment amount, or can use a defined (e.g., predefined) time adjustment amount (e.g., $-0.1t$, $+0.1t$, or some other desired time adjustment amount), to apply to the auxiliary sampling time to facilitate adjusting the auxiliary sampling time to facilitate aligning (or substantially aligning) the auxiliary sub-ADC with a sub-ADC of the set. The calibration component can employ the phase interpolator component and/or analog delay lines to facilitate adjusting the auxiliary sampling time of the auxiliary sub-ADC by the desired time adjustment amount. At this point, as the auxiliary sub-ADC is not aligned (or substantially aligned) with a sub-ADC of the set, the method 900 can return to block 902 and can proceed from that point.

[00123] Referring to block 908, if, at block 908, it is determined that the auxiliary sampling time is aligned (or at least substantially aligned) with one of the respective sampling times associated with a sub-ADC of the set of sub-ADCs, at block 912, it can be determined that the auxiliary sub-ADC is aligned (e.g., suitably or acceptably aligned) with a sub-ADC of the set of sub-ADCs. If, based at least in part on the comparison results, the calibration component determines that the auxiliary sampling time is aligned (or at least substantially aligned) with one of the respective sampling times associated with a sub-ADC of the set, the calibration component can determine that the auxiliary sub-ADC is aligned (e.g., suitably or acceptably aligned) with a sub-ADC of the set. The alignment of the auxiliary sub-ADC with the sub-ADC can enable the auxiliary sub-ADC to be used by the calibration component to facilitate determining path differences between paths associated with respective sub-ADCs and calibrating the respective sub-ADCs to correct, mitigate, or reduce those path differences.

[00124] As an example of method 900, if a first analog signal of a first sub-ADC of the set of sub-ADCs is set to be sampled at times 0, $2t$, $4t$, $6t$, $8t$, $10t$, ..., $18t$, $20t$, $22t$, and so on, the calibration component can select the auxiliary sampling rate (e.g., every $5t$), and can align the sampling times (e.g., $10t$, $20t$,

30t, and so on) associated with the auxiliary sub-ADC with certain sampling times associated with the first sub-ADC, to enable the sampling of the auxiliary signal associated with the auxiliary path of the auxiliary sub-ADC to occur at the same or at least substantially the same time as a subset of the sampling times (e.g., 10t, 20t, 30t, and so on) associated with the first sub-ADC. As another example, if, instead, a first analog signal of a first sub-ADC of the set of sub-ADCs is set or determined to be sampled at times $(0+0.1)t$, $(2+0.1)t$, $(4+0.1)t$, $(6+0.1)t$, $(8+0.1)t$, $(10+0.1)t$, ..., $(18+0.1)t$, $(20+0.1)t$, $(22+0.1)t$, and so on, the calibration component can select the auxiliary sampling rate (e.g., every 5t), and can align the sampling times (e.g., $(10+0.1)t$, $(20+0.1)t$, $(30+0.1)t$, and so on) associated with the auxiliary sub-ADC with the sampling time associated with the first sub-ADC, to enable the sampling of the auxiliary signal associated with the auxiliary path of the auxiliary sub-ADC to occur at the same or at least substantially the same time as a subset of the sampling times (e.g., $(10+0.1)t$, $(20+0.1)t$, $(30+0.1)t$, and so on) associated with the first sub-ADC.

[00125] The techniques described herein can be applied to any device and/or network where calibration of ADC sub-components of an ADC component is desirable in a system comprising a communication device (e.g., transceiver component). Handheld, portable and other computing devices and computing objects of all kinds are contemplated for use in connection with the various non-limiting embodiments, e.g., anywhere that it can be desirable for a device to implement calibration of ADC sub-components of an ADC component associated with a system that is associated with a communication device. Accordingly, the below general purpose remote computer described below in **FIG. 10** is one example, and the disclosed subject matter can be implemented with any client having network/bus interoperability and interaction. Thus, the disclosed subject matter can be implemented in an environment of networked hosted services in which very little or minimal client resources are implicated, e.g., a networked environment in which the client device serves merely as an interface to the network/bus, such as an object placed in an appliance.

[00126] **FIG. 10** illustrates an example of a computing system environment 1000 in which some aspects of the disclosed subject matter can be implemented, although the computing system environment 1000 is only one example of a computing environment for a device.

[00127] FIG. 10 is an exemplary device for implementing the disclosed subject matter includes a general-purpose computing device in the form of a computer 1010. Components of computer 1010 may include a processing unit 1020, a system memory 1030, and a system bus 1021 that couples various system components including the system memory to the processing unit 1020.

[00128] Computer 1010 typically includes a variety of computer readable media. The system memory 1030 may include computer storage media in the form of volatile and/or nonvolatile memory such as read only memory (ROM) and/or random access memory (RAM).

[00129] The computer 1010 can operate in a networked or distributed environment using logical connections to one or more other remote computer(s), such as remote computer 1070, which can in turn have media capabilities different from device 1010. The logical connections depicted in FIG. 10 include a network 1071, such local area network (LAN) or a wide area network (WAN), but can also include other networks/buses, either wired or wireless. When used in a LAN networking environment, the computer 1010 can be connected to the LAN 1071 through a network interface or adapter.

[00130] FIG. 11 is a schematic diagram of an exemplary networked or distributed computing environment 1100. The distributed computing environment comprises computing objects 1110, 1112, etc. and computing objects or devices 1120, 1122, 1124, 1126, 1128, etc., which may include programs, methods, data stores, programmable logic, etc., as represented by applications 1130, 1132, 1134, 1136, 1138 and data store(s) 1140.

[00131] Each computing object 1110, 1112, etc. and computing objects or devices 1120, 1122, 1124, 1126, 1128, etc. can communicate with one or more other computing objects 1110, 1112, etc. and computing objects or devices 1120, 1122, 1124, 1126, 1128, etc. by way of the communications network 1142, either directly or indirectly. In FIG. 11, as an example, computing objects or devices 1120, 1122, 1124, 1126, 1128, etc. can be thought of as clients and computing objects 1110, 1112, etc. can be thought of as servers where computing objects 1110, 1112, etc., acting as servers provide data services, such as receiving data from client computing objects or devices 1120, 1122, 1124, 1126, 1128, etc., storing of data, processing of data, transmitting data to client computing objects or devices 1120, 1122, 1124, 1126, 1128, etc.,

although any computer can be considered a client, a server, or both, depending on the circumstances.

[00132] In a network environment in which the communications network 1142 or bus is the Internet, for example, the computing objects 1110, 1112, etc. can be Web servers with which other computing objects or devices 1120, 1122, 1124, 1126, 1128, etc. communicate via any of a number of known protocols, such as the hypertext transfer protocol (HTTP).

[00133] The disclosed subject matter can be implemented as a method, apparatus, or article of manufacture using typical manufacturing, programming or engineering techniques to produce hardware, firmware, software, or any suitable combination thereof to control an electronic device to implement the disclosed subject matter. Computer-readable media can include hardware media, software media, non-transitory media, or transport media.

CLAIMS

What is claimed is:

1. A communication system, comprising:

a converter component comprising a set of converter sub-components for converting respective time-delayed analog signals to respective digital data samples, and an auxiliary converter sub-component associated with an auxiliary path, wherein respective converter sub-components of the set of converter sub-components are associated with respective paths, wherein the respective time-delayed analog signals are generated based at least in part on processing of an analog signal received from a remote communication component; and

a calibration component for determining path differences between the respective paths of the respective converter sub-components, based at least in part on a result of an analysis of an auxiliary signal associated with the auxiliary path and respective signals associated with the respective paths of the respective converter sub-components, and calibrating the respective converter sub-components to reduce the path differences, wherein the respective signals comprise the respective digital data samples,

wherein the respective converter sub-components comprise a converter sub-component, and the respective paths comprise a path associated with the converter-sub-component, and

wherein, prior to, and to enable, the determining of the path differences and the calibrating of the respective converter sub-components to reduce the path differences, the calibration component controls a phase interpolator component to adjust a phase of the auxiliary converter sub-component associated with the auxiliary path to respectively initially align the auxiliary converter sub-component and the auxiliary path with the converter sub-component and the path.

2. The system of claim 1, wherein a set of auxiliary samples is generated based at least in part on the auxiliary signal, and wherein, to facilitate the analysis, the calibration component compares information relating to the set of auxiliary samples with other information relating to respective sets of the digital data samples, based at least in part on the respective signals, and determines the path differences between the respective paths based at least in part on respective differences between the information relating to the set of auxiliary samples and the other information relating to the respective sets of digital data samples.

3. The system of claim 2, wherein, to facilitate the determining of the path differences, the calibration component determines a squared difference error metric based at least in part on the respective differences between the information relating to the set of auxiliary samples and the other information relating to the respective sets of digital data samples.

4. The system of claim 3, wherein the calibration component calculates the squared difference error metric based at least in part on a difference between auxiliary-sample-related information relating to a first auxiliary sample of the set of auxiliary samples and sample-related information relating to a first digital data sample of a first set of the respective sets of digital data samples that is associated with a first converter sub-component of the set of converter sub-components, wherein an auxiliary sampling time of the first auxiliary sample coincides with a sampling time of the first digital data sample.

5. The system of claim 4, wherein the calibration component calculates the squared difference error metric based at least in part on a second difference between second auxiliary-sample-related information relating to a second auxiliary sample of the set of auxiliary samples and sample-related information relating to a second digital data sample of a second set of the respective sets of digital data samples that is associated with a second converter sub-component of the set of converter sub-components, wherein a second auxiliary sampling time of the second auxiliary sample coincides with a second sampling time of the second digital data sample.

6. The system of claim 3, wherein the squared difference error metric is at least one of an average squared difference error metric or a median squared difference error metric, and the calibration component calculates at least one of the average squared difference error metric or the median squared difference error metric based at least in part on a difference between auxiliary-sample-related information relating to an average value or a median value associated with multiple auxiliary samples of the set of auxiliary samples and sample-related information relating to another average value or another median value associated with multiple digital data samples of a first set of the respective sets of digital data samples that is associated with a first converter sub-component of the set of converter sub-components, the respective auxiliary

sampling times of the multiple auxiliary samples coincide with respective sampling times of the multiple digital data samples.

7. The system of claim 1, wherein the calibration component aligns the auxiliary path associated with the auxiliary converter sub-component with the path associated with the converter sub-component to facilitate enabling sampling of the auxiliary signal by the auxiliary converter sub-component to coincide with a portion of sampling of a signal by the converter sub-component.

8. A signal processing method, comprising:

determining path differences between respective paths of respective converter sub-components of a set of converter sub-components, based at least in part on a result of analyzing an auxiliary signal associated with an auxiliary path that is associated with an auxiliary sub-component and respective signals associated with the respective paths of the respective converter sub-components, to facilitate calibrating the respective converter sub-components to mitigate the path differences, wherein the respective converter sub-components comprise a converter sub-component, and the respective paths comprise a path associated with the converter-sub-component;

adjusting the respective converter sub-components or the respective paths to facilitate mitigating the path differences between the respective converter sub-components or the respective paths; and

prior to the determining of the path differences and the adjusting of the respective converter sub-components or the respective paths to mitigate the path differences, controlling a phase interpolator component to adjust a phase of the auxiliary converter sub-component associated with the auxiliary path to respectively initially align the auxiliary converter sub-component and the auxiliary path with the converter sub-component and the path.

9. The method of claim 8 further comprising:

determining a squared difference error based at least in part on respective differences between information relating to a set of auxiliary samples associated with the auxiliary signal and other information relating to respective sets of samples associated with the respective signals to facilitate the determining of the path differences,

wherein the analyzing further comprises:

comparing the information relating to the set of auxiliary samples with the other information relating to the respective sets of samples, wherein the determining of the path differences further comprises determining the path differences between the respective paths based at least in part on the respective differences between the information relating to the set of auxiliary samples and the other information relating to the respective sets of samples.

10. A transceiver, comprising:

means for determining path differences between respective paths of respective converter sub-components of a set of converter sub-components, based at least in part on a result of comparing an auxiliary signal associated with an auxiliary path that is associated with an auxiliary sub-component with respective signals associated with the respective paths of the respective converter sub-components of the set of converter sub-components, to facilitate calibrating the respective converter sub-components to reduce the path differences, wherein the respective converter sub-components comprise a converter sub-component, and the respective paths comprise a path associated with the converter sub-component;

means for calibrating the respective converter sub-components or the respective paths to facilitate the reducing of the path differences between the respective converter sub-components or the respective paths; and

means for controlling a phase interpolator component, wherein, before the determining of the path differences and the calibrating of the respective converter sub-components or the respective paths to facilitate the reducing of the path differences, the means for controlling the phase interpolator component controls the phase interpolator component to modify a phase of the auxiliary converter sub-component associated with the auxiliary path to respectively initially align the auxiliary converter sub-component and the auxiliary path with the converter sub-component and the path.

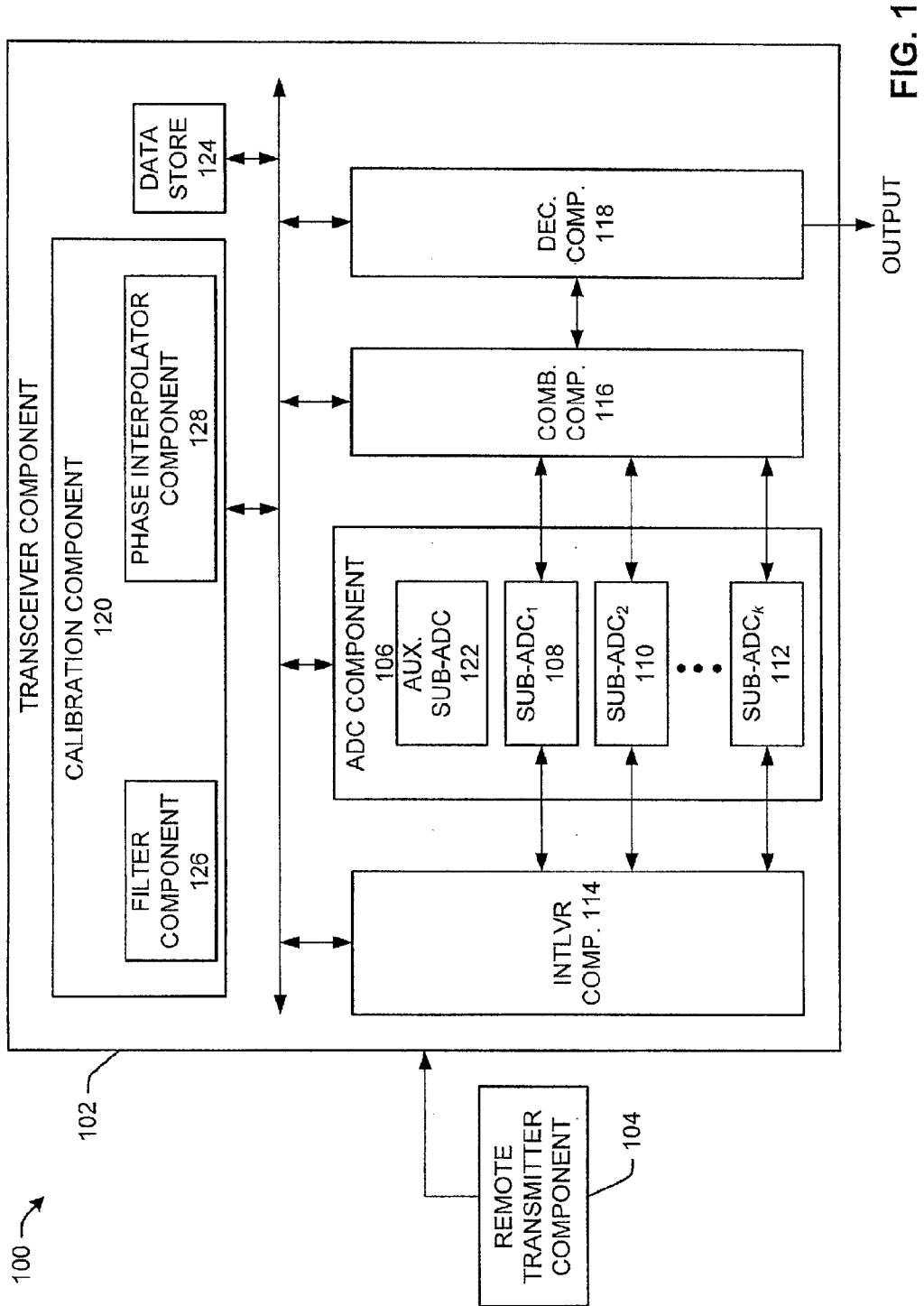


FIG. 1

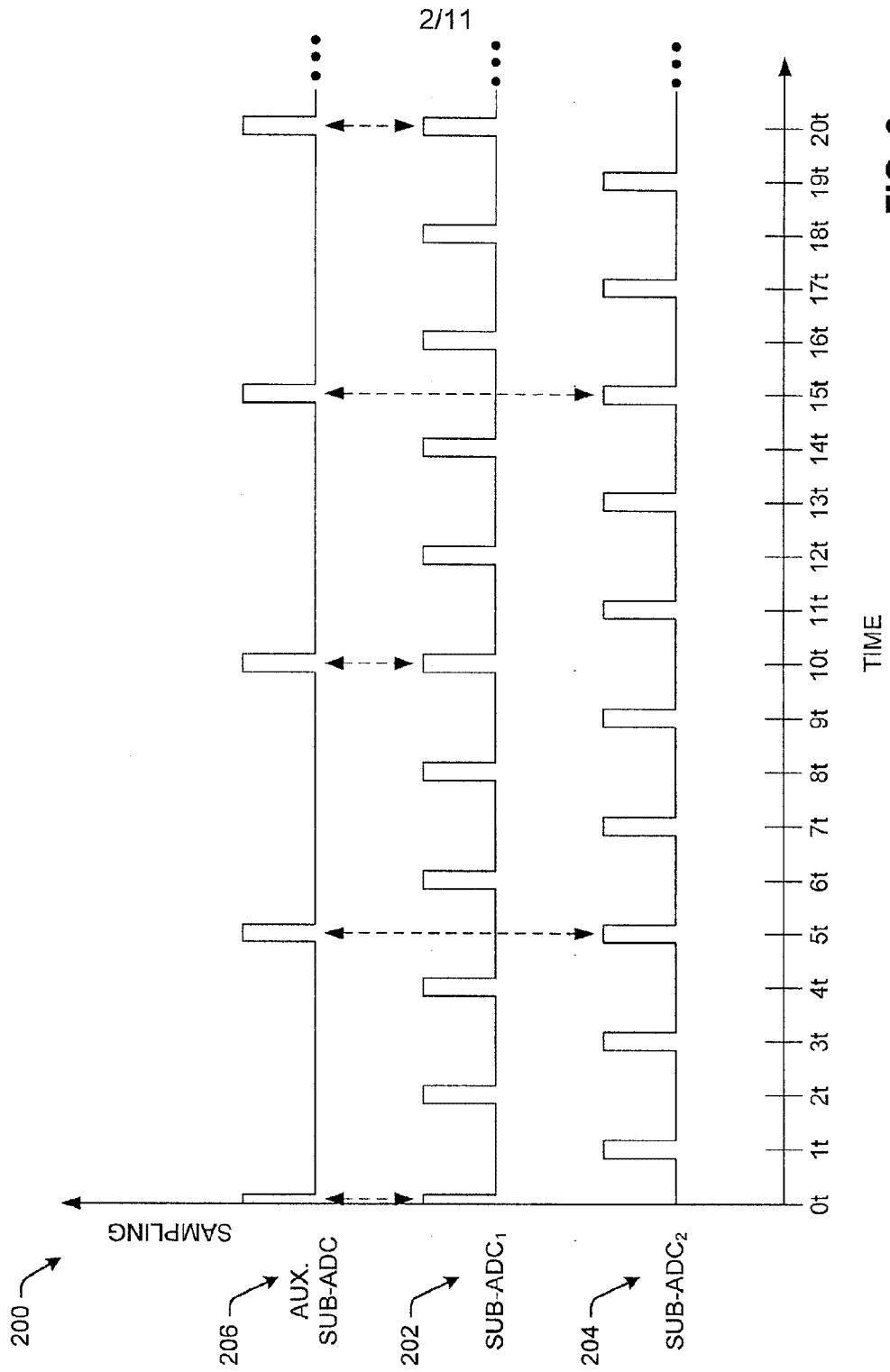


FIG. 2

3/11

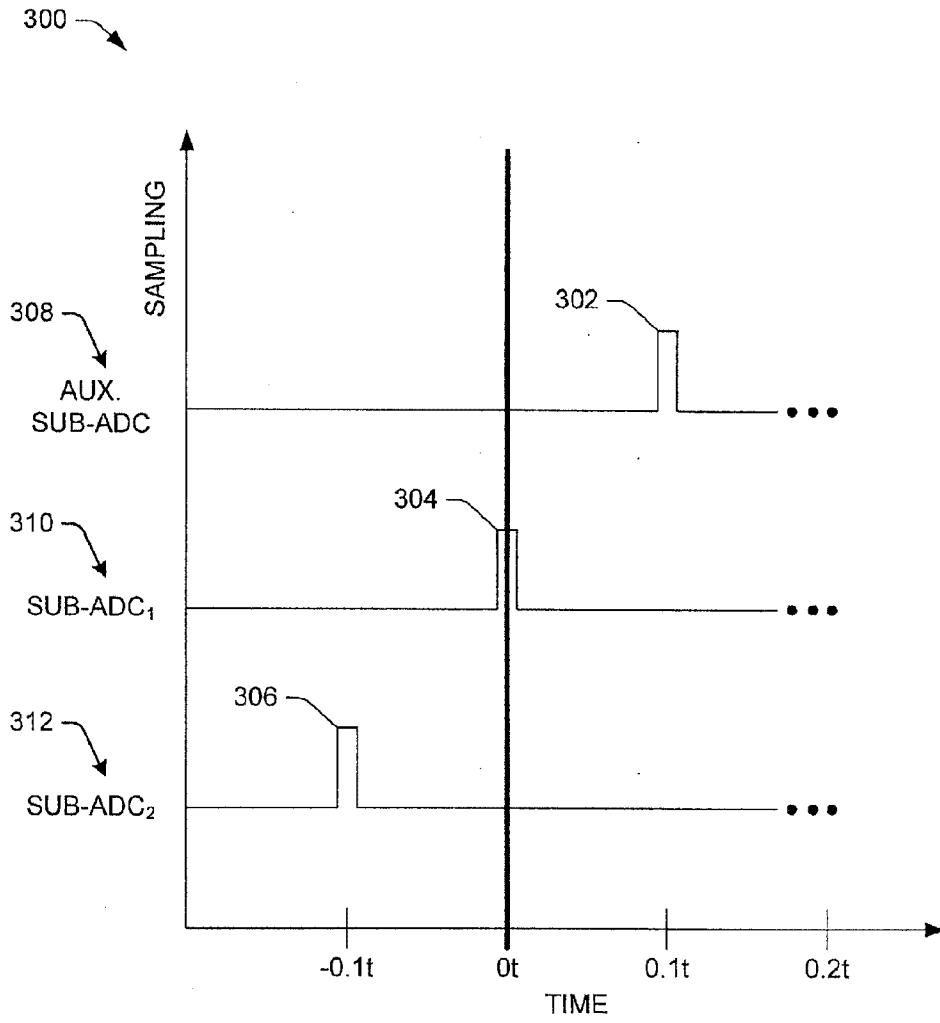


FIG. 3

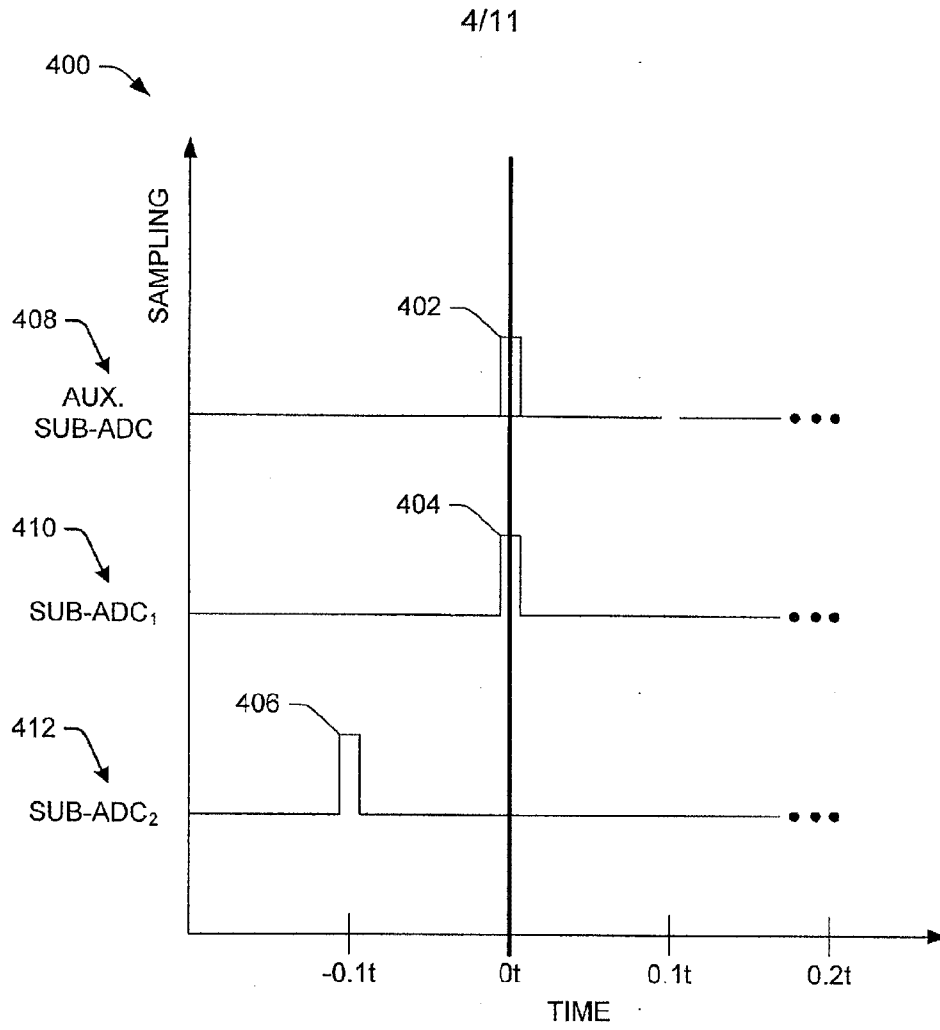


FIG. 4

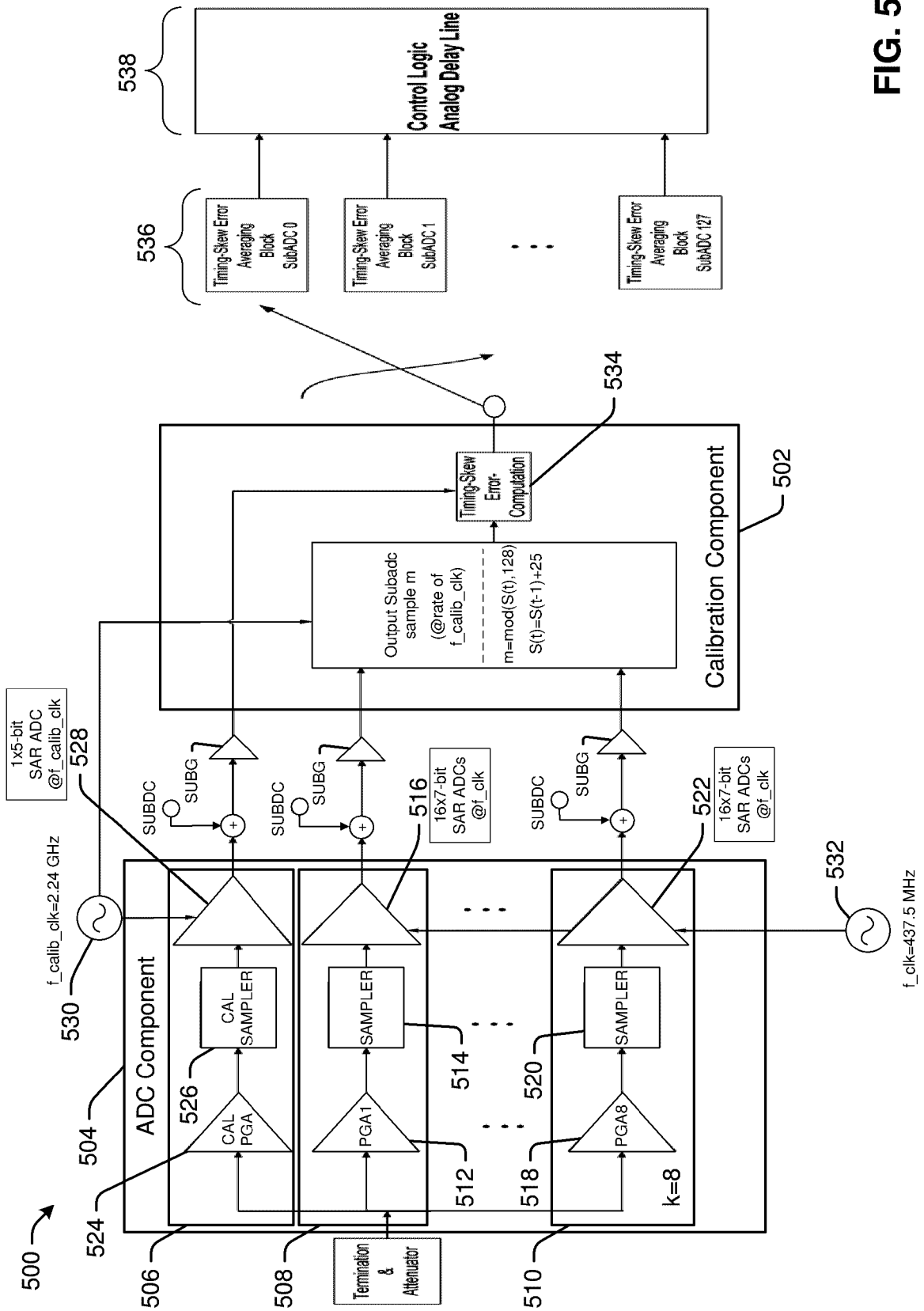


FIG. 5

6/11

600

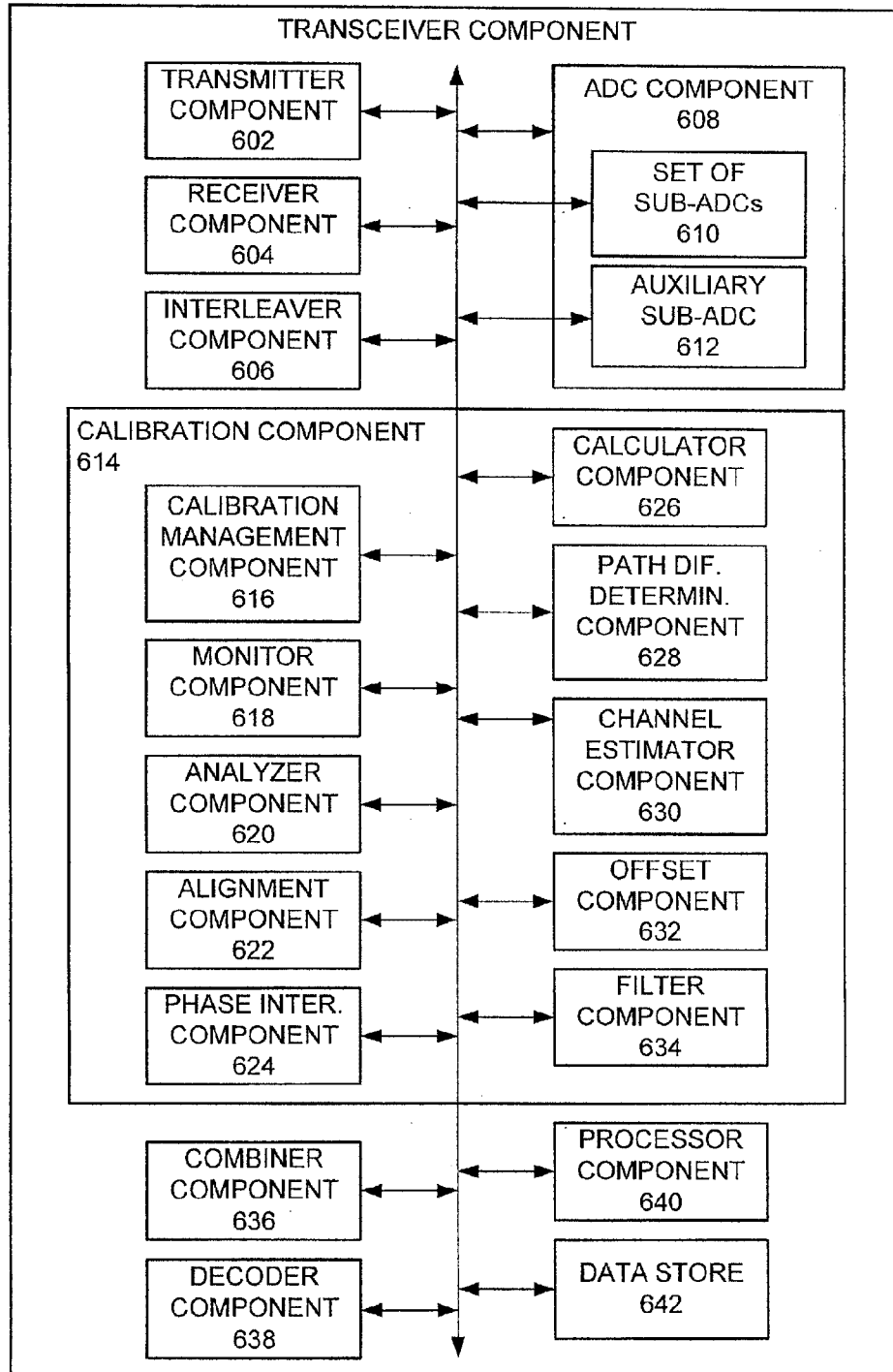


FIG. 6

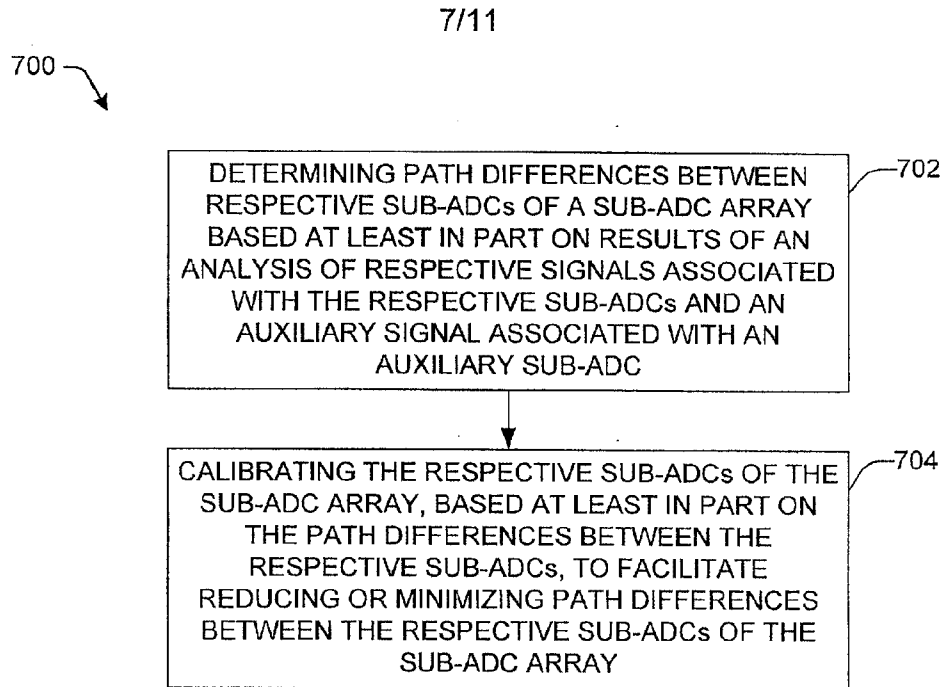


FIG. 7

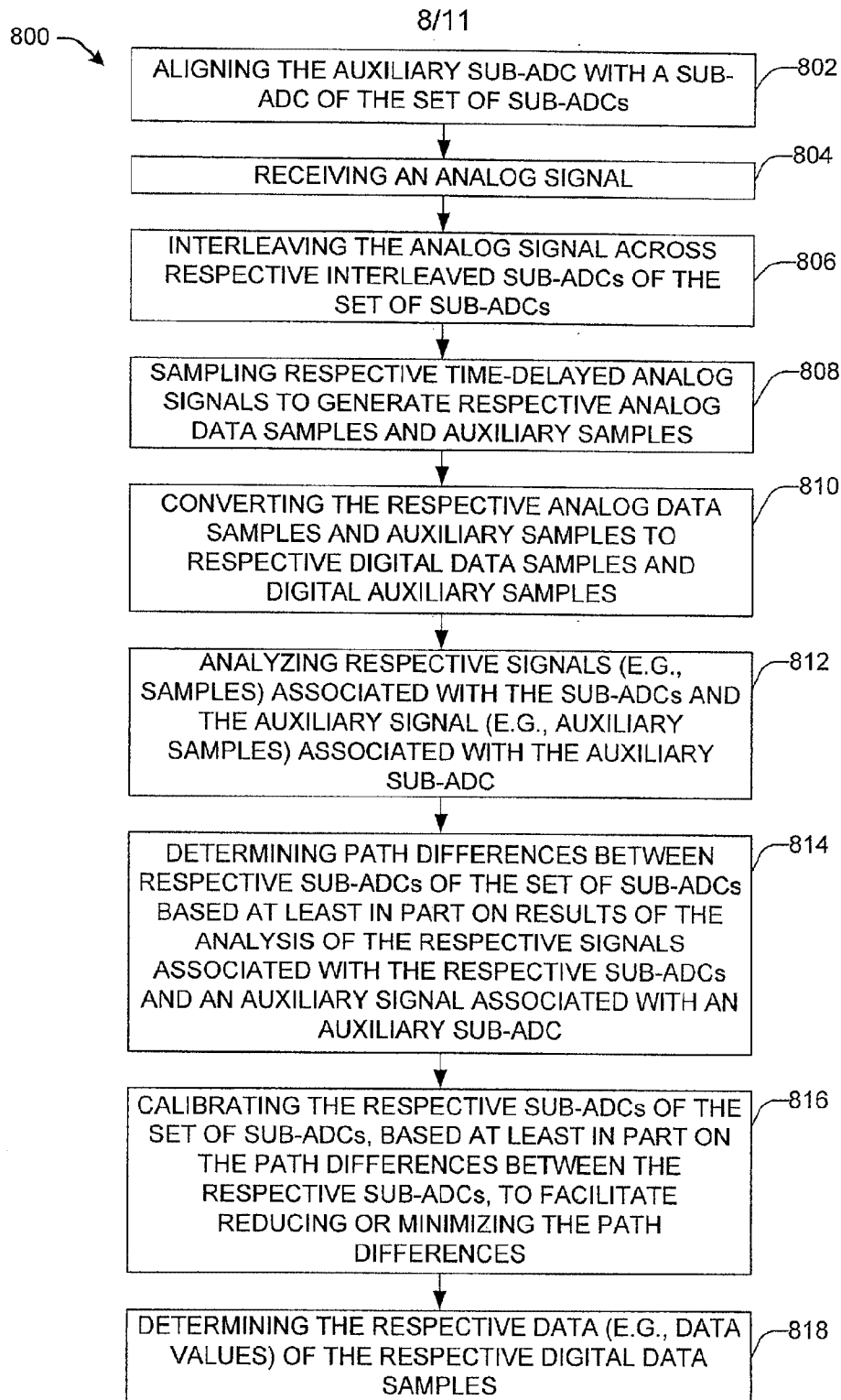


FIG. 8

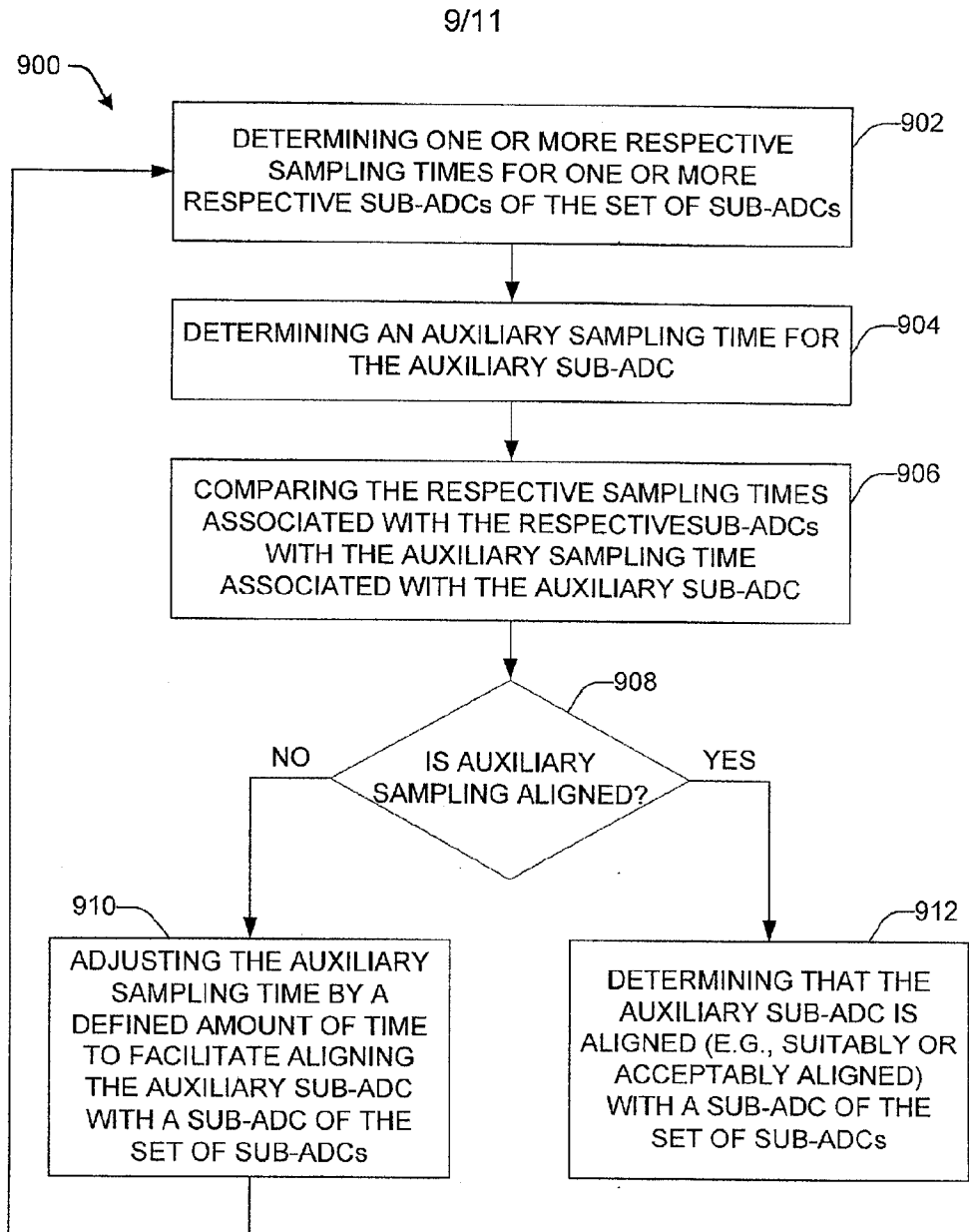


FIG. 9

10/11

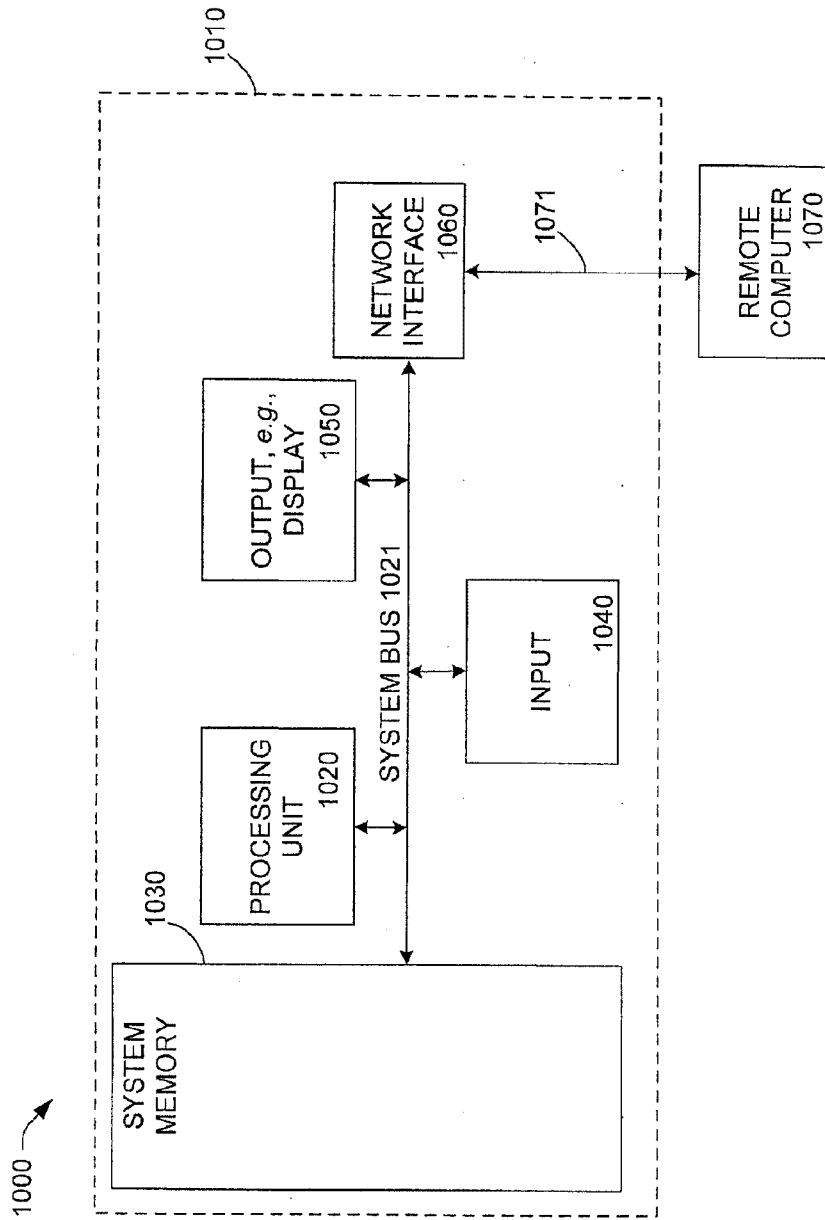


FIG. 10

11/11

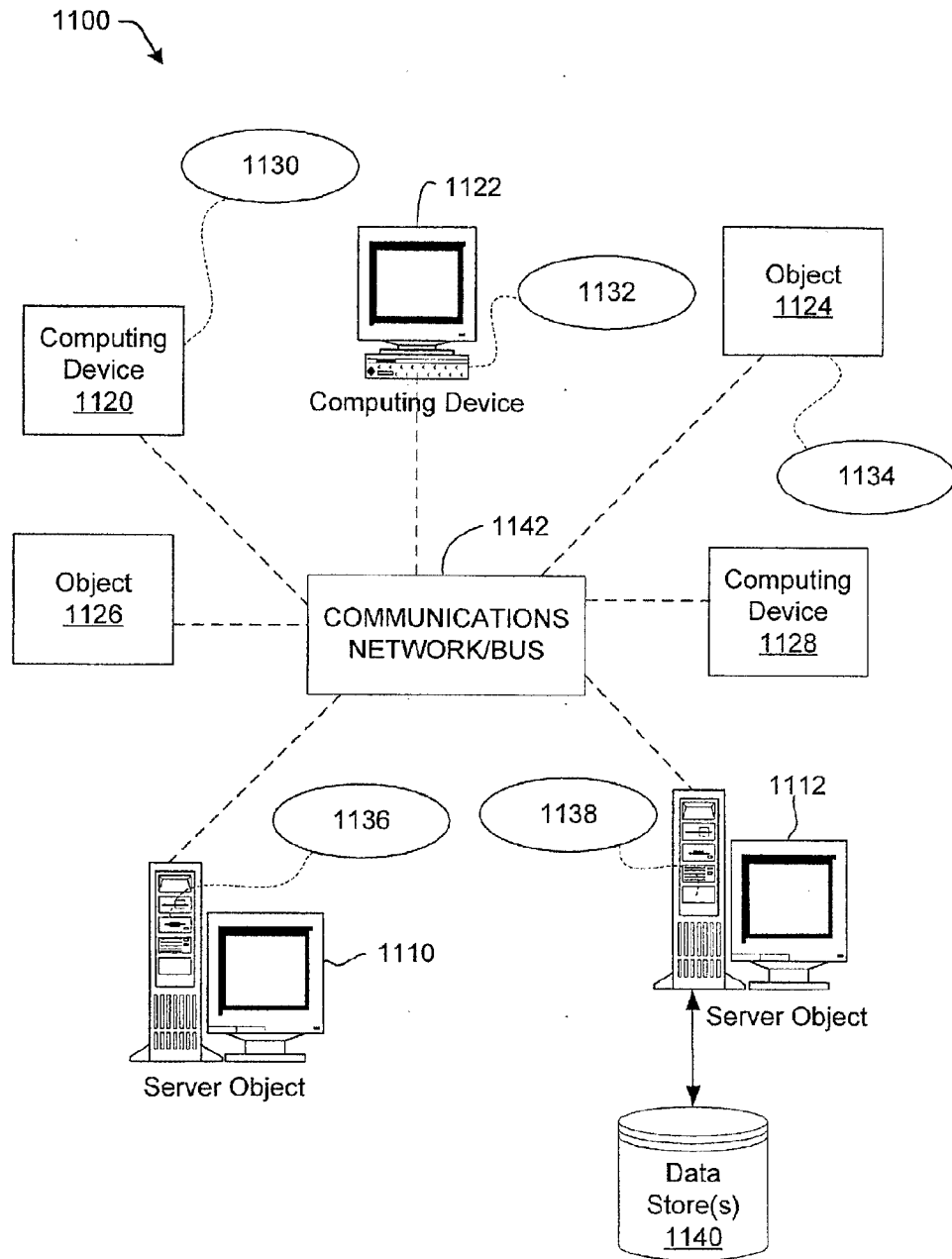


FIG. 11

