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- (54) Title: FABRICATION OF PIEZOELECTRIC DEVICE WITH PMNPT LAYER
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- FIG. 2
- (57) Abstract: A piezoelectric device includes a substrate, a thermal oxide layer on the substrate, a metal or metal oxide adhesion layer on the thermal oxide layer, a lower electrode on the metal oxide adhesion layer, a seed layer on the lower electrode, a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer on the seed layer, and an upper electrode on the PMNPT piezoelectric layer.
- [Continued on next page]

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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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FABRICATION OF PIEZOELECTRIC DEVICE WITH PMNPT LAYER

TECHNICAL FIELD

This invention relates to fabrication of piezoelectric devices, and more particularly to piezoelectric devices that include PMNPT as the piezoelectric layer.

BACKGROUND

Piezoelectric materials have been used for several decades in a variety of technologies, e.g., ink jet printing, medical ultrasound and gyroscopes. Conventionally, piezoelectric layers are fabricated by producing a piezoelectric material in a bulk crystalline form and then machining the material to a desired thickness, or by using sol-gel techniques to deposit the layer. Lead zirconate titanate (PZT), typically of the form $\text{Pb}[\text{Zr}_x\text{Ti}_{1-x}]\text{O}_3$, is a commonly used piezoelectric material. Sputtering of PZT has been proposed.

More recently relaxor-lead titanate (relaxor-PT) materials, such as lead magnesium niobate-lead titanate (PMNPT), typically $(1-x)[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]-x[\text{PbTiO}_3]$, as well as lead yttrium niobate-lead titanate (PYN-PT) such as $(1-X)[\text{Pb}(\text{Y}_{1/3}\text{Nb}_{2/3})\text{O}_3]-X[\text{PbTiO}_3]$, lead zirconium niobate-lead titanate (PZN-PT) such as $(1-X)[\text{Pb}(\text{Zr}_{1/3}\text{Nb}_{2/3})\text{O}_3]-X[\text{PbTiO}_3]$, and lead indium niobate-lead titanate (PIN-PT) such as $(1-X)[\text{Pb}(\text{In}_{1/3}\text{Nb}_{2/3})\text{O}_3]-X[\text{PbTiO}_3]$, have been proposed as piezoelectric materials. PMNPT can offer improved piezoelectric properties over the more commonly used PZT material. However, large area thin film deposition of a PMNPT layer in a commercially viable manner has been not yet been demonstrated.

SUMMARY

In one aspect, a piezoelectric device includes a substrate, a thermal oxide layer on the substrate, a metal or metal oxide adhesion layer on the thermal oxide layer, a lower electrode on the metal oxide adhesion layer, a seed layer on the lower electrode, a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer on the seed layer, and an upper electrode on the PMNPT piezoelectric layer.

In another aspect, a method of fabricating a piezoelectric device includes forming an adhesion layer on a thermal layer of a substrate, depositing a lower electrode on the adhesion layer, forming a seed layer on the lower electrode,

depositing a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer on the seed layer by physical vapor deposition, and depositing an upper electrode on the PMNPT piezoelectric layer.

Implementations may have, but are not limited to, one or more of the following advantages.

A device that includes a layer of PMNPT can be fabricated in a commercially viable process. The layer stack on which the PMNPT layer is fabricated permits good adhesion to an underlying semiconductor wafer. The layer of PMNPT can be deposited by physical vapor deposition, which can provide high purity, good throughput and low costs. The layer stack permits the PMNPT material to be fabricated with highly (001) oriented columnar grains, which can provide a superior d33 coefficient. The process can also limit the presence of parasitic phases such as PbOx and pyrochlore, which can be detrimental to the piezoelectric properties.

The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features, objects, and advantages will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic cross-sectional view of a physical vapor deposition processing chamber.

FIG. 2 illustrates a cross-section of a portion of a device that includes a piezoelectric layer of PMNPT.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Machining a piezoelectric layer from a bulk crystal and depositing a piezoelectric layer using sol-gel techniques are slow processes that are not conducive to being performed in a semiconductor fabrication plant. Bulk crystals need to be machined in conventional machine shops. This is not only expensive but also limits the ability of the piezoelectric layer to be integrated into devices. Sol-gel processes require multiple rounds of deposition and curing, thus making it time-consuming. Thus, deposition of a piezoelectric material by a physical vapor deposition process, e.g., sputtering, would be desirable.

As noted above, PMNPT can provide improved piezoelectric properties over the conventional PZT-based solutions. However, fabrication of thin films of PMNPT by physical vapor deposition over large area semiconductor wafers, e.g., silicon wafers, has been challenging. The films of PMNPT can be difficult to provide a uniform crystalline structure with the desired phase with the desired texture.

A technique that may address these issues is to deposit a layer stack on the semiconductor wafer that includes silicon oxide, a metal oxide, a platinum layer, and a thin seed layer. The PMNPT layer is deposited on this layer stack. The layer stack can provide good adhesion to the silicon wafer, while also promoting proper crystalline orientation of the PMNPT.

FIG. 1 depicts a schematic representation of a chamber 100 of an integrated processing system, e.g., an ENDURA system, suitable for practicing the physical vapor deposition process discussed below. The processing system can include multiple chambers, which can be adapted for PVD or CVD processes. For example, the processing system can include a cluster of interconnected process chambers, for example, a CVD chamber and a PVD chamber.

The chamber 100 includes chamber walls 101 that surround a vacuum chamber 102, a gas source 104, a pumping system 106 and a target power source 108. Inside the vacuum chamber 102 is a target 110 and a pedestal 112 to support the substrate 10. A shield can be placed inside the chamber to enclose a reaction zone. The pedestal can be vertically movable, and a lift mechanism 116 can be coupled to the pedestal 112 to position the pedestal 112 relative to the target 110. A heater or chiller 136, e.g., a resistive heater or a thermoelectric chiller, can be embedded in the pedestal 112 to maintain the substrate 10 at a desired process temperature.

The target 110 is composed of the material to be deposited, e.g., lead magnesium niobate-lead titanate for PMNPT. However, the target can have an excess of PbO_x relative to the desired stoichiometry for the layer to be deposited to account for the loss of lead due to its volatile nature during either deposition or post-processing, such as annealing step. For example, the target can have an excess of PbO of 1-20 mol% to account for the loss of volatile Pb and PbO_x from the deposited material. The target itself should be of homogenous composition. The target 110 can be platinum (Pt) or Titanium (Ti) for deposition of other layers.

The gas source 104 can introduce an inert gas, e.g., argon (Ar) or xenon (Xe), or a mixture of an inert gas with a processing gas, e.g., oxygen, into the vacuum

chamber 102. The chamber pressure is controlled by the pumping system 106. The target power source 108 may include a DC source, a radio frequency (RF) source, or a DC-pulsed source.

5 In operation, the substrate 10 is supported within the chamber 102 by the pedestal 112, gas from the source 104 flows into the chamber 102, and the target power source 108 applies power to the target 110 at a frequency and voltage to generate a plasma in the chamber 102. The target materials are sputtered from the target 110 by the plasma, and deposited on the substrate 10.

10 If the target power source 108 is DC or DC-pulsed, then the target 110 acts as a negatively biased cathode and the shield is a grounded anode. For example, a plasma is generated from the inert gas by applying a DC bias to the sputtering target 210 sufficient to generate a power density of about 1 to 350 Watts per square inch, e.g., 100-38,000 W for a 13 inch diameter target, and more typically about 100-10,000 W. If the target power source 108 is an RF source, then the shield is typically
15 grounded and the voltage at the target 110 varies relative to the shield at a radio frequency, typically 13.56 MHz. In this case, electrons in the plasma accumulate at the target 110 to create a self-bias voltage that negatively biases the target 110.

The chamber 100 may include additional components for improving the sputtering deposition process. For example, a power source 124 may be coupled to
20 the pedestal 112 for biasing the substrate 10, in order to control the deposition of the film on the substrate 10. The power source 124 is typically an AC source having a frequency of, for example, between about 350 to about 450 kHz. When the bias is applied by the power source 124, a negative DC offset is created (due to electron accumulation) at the substrate 10 and the pedestal 112. The negative bias at the
25 substrate 10 attracts sputtered target material that becomes ionized. The target material is generally attracted to the substrate 10 in a direction that is substantially orthogonal to the substrate 10. As such, the bias power source 124 improves the step coverage of deposited material compared to an unbiased substrate 10.

The chamber 100 may also have a magnet 126 or magnetic sub-assembly
30 positioned behind the target 110 for creating a magnetic field proximate to the target 1210. In some implementations, the magnet rotates during the deposition process.

The operation of the chamber can be controlled by a controller 150, e.g., a dedicated microprocessor, e.g., an ASIC, or a conventional computer system executing a computer program stored in a non-volatile computer readable medium.

The controller 150 can include a central processor unit (CPU) and memory containing the associated control software.

FIG. 2 illustrates a cross-section of a portion of a substrate 10 for fabrication of a device that includes a piezoelectric layer 16 of PMNPT formed on a semiconductor wafer 12. In particular, the substrate 10 includes a layer stack 14 between the semiconductor wafer 12 and the piezoelectric layer 16. The layer stack 14 can both improve adhesion of the piezoelectric material to the semiconductor wafer 12, and promote proper crystalline orientation of the PMNPT material in the piezoelectric layer 16.

The semiconductor wafer can be a silicon wafer or another semiconductor such as germanium (Ge). The silicon wafer can be a single crystal silicon wafer, and can have a $\langle 001 \rangle$ crystallographic orientation, although other orientations can work.

The layer stack 14 includes, in order, a silicon oxide (SiO_x) layer 20, an adhesion layer 22, a first conductive layer 24, and a first seed layer 26 that provides a seed layer for the PMNPT layer. The adhesion layer 22 can be a metal oxide, e.g., titanium oxide, and the seed layer can also be metal oxide, e.g., titanium oxide or niobium oxide.

The silicon oxide layer 20 can include SiO_2 , SiO , or a combination thereof. The silicon oxide layer 20 can be a thermal oxide, and can have a thickness of about 50-1000 nm. The silicon oxide layer 20 can be an amorphous layer.

The adhesion layer 22 can be a metal oxide layer. The stoichiometry of the metal oxide layer can MO_2 , M_2O_3 , or MO (with M representing the metal element), or another suitable stoichiometry of the metal and oxygen. In particular, the adhesion layer 22 can be formed of titanium oxide, e.g., TiO_2 , Ti_2O_3 , TiO , or another stoichiometry of titanium and oxygen. In some implementations, rather than a metal oxide layer, the adhesion is a pure metal or a metal alloy. Examples for the metal (either for the metal of the metal oxide, or for the pure metal or component of the metal alloy) include titanium, chromium, chromium-nickel, and nickel. The adhesion layer 22 can be thinner than the silicon oxide layer 20. For example, a titanium oxide adhesion layer 22 can have a thickness of 25-40 nm. The adhesion layer 22 can have a crystallographic orientation for facilitating a desired crystallographic orientation of the conductive layer 24. For example, a TiO_2 layer can have a $\langle 001 \rangle$ orientation to facilitate a $\text{Pt}\langle 111 \rangle$ orientation.

The first conductive layer 24 is formed of a conductive material such as platinum, gold, iridium, molybdenum, SrRuO₃. The first conductive layer 24 can be thicker than the adhesion layer 22, and can be thicker than the silicon oxide layer 20. For example, the first conductive layer 24 can have a thickness of 50-300 nm. The first conductive layer 24 can have a crystallographic orientation for facilitating a desired crystallographic orientation of the seed layer 26. For example, a platinum layer can have a <111> crystallographic orientation to facilitate a <111> orientation in a titanium oxide seed layer.

The seed layer 26 can be metal oxide. In particular, the seed layer 24 can be an oxide of titanium or niobium. For example, the seed layer 26 can be TiO₂, Ti₂O₃, TiO, or another stoichiometry of titanium and oxygen. The seed layer 26 should have a uniform stoichiometry across the surface of the substrate 10. The seed layer 26 can have a crystallographic orientation for facilitating a desired crystallographic orientation of the piezoelectric layer 28. For example, a titanium oxide layer can have a <001> crystallographic orientation to facilitate a <001> orientation in a PMNPT piezoelectric layer. The seed layer 26 is thinner than the adhesion layer 22. For example, first seed layer 26 can be about 1-5 nm, thick, e.g., 2 nm.

The piezoelectric layer 16 is formed on the seed layer 26. Examples of material for the piezoelectric layer 16 include PZT and relaxor-PT materials. In particular, the material can be $(1-x)[\text{Pb}(\text{Mg}_{(1-y)}\text{Nb}_y)\text{O}_3]-x[\text{PbTiO}_3]$, where x is about .2 to .8, and y is about .8 to .2, e.g., about 2/3. Due to the presence of the metal oxide seed layer, the PMNPT material can be predominantly, e.g., substantially entirely, a <001> crystallographic orientation. The piezoelectric layer can have a thickness of 50 nm to 10 microns.

A second conductive layer 30 is formed on the piezoelectric layer 16. The second conductive layer 30 can be the same material composition as the first conductive layer 24, and can be the same thickness as the first conductive layer 24. For example, the second conductive layer 30 can be platinum, and can have a thickness of 50- 300 nm.

A voltage can be applied between the first and second conductive layers, 24 and 30, in order to actuate the piezoelectric layer 16. Thus, the first conductive layer provides 24 a lower electrode and the second conductive layer 30 provides an upper electrode with the piezoelectric layer 16 sandwiched therebetween.

To fabricate the layer stack 14, an oxide of SiO_2 can be grown on a Si $\langle 001 \rangle$ single crystal wafer by thermal processing in an oxygen-containing atmosphere. The thermal oxide can be grown to a thickness of 50-1000 nm, e.g., 100 nm. The thermal oxide can be formed on both sides of the silicon wafer.

5 Thereafter, a metal layer which will provide the metal of the adhesion layer is deposited by PVD. For example, a titanium layer can be deposited. For example, the metal layer can be deposited with the substrate between room temperature and 600 °C and a power density of 1 to 350 Watts per square inch, e.g., about 1.5 Watts per square inch, applied to the target. Deposition of the metal layer can be followed by
10 annealing in a rapid thermal processing chamber or furnace in the presence of oxygen or air to form the adhesion layer in the form of the metal oxide layer, e.g., TiO_x . The annealing can be at a temperature of 500-800 °C, e.g., for 2-30 minutes. The resulting adhesion layer can have a thickness of 5-400 nm.

 Then the first conductive layer, e.g., the highly oriented platinum $\langle 111 \rangle$ film,
15 is deposited by PVD on the adhesion layer, e.g., on the titanium oxide layer. For example, a platinum layer can be deposited at a substrate temperature of room temperature to 500 °C, with a power density of 0.5 to 20 Watts per square inch, e.g., 4-5 Watts per square inch, applied to the target. Deposition of the bottom metallic layer can proceed until the layer has a thickness of 50-300 nm. The adhesion layer
20 provides improved adhesion between the metallic electrode and the silicon oxide, in addition to helping in uniform texturing of the metallic layer.

 Next, a thin metal layer e.g., titanium, is deposited on the lower electrode, e.g., the platinum layer, by a PVD (e.g., DC sputtering) or a CVD (e.g., ALD) technique. In particular, a titanium layer can be deposited, e.g., by DC sputtering. For example,
25 the titanium seed layer can be deposited with the substrate at room temperature to 500 C and a power density of 0.5 to 4 Watts per square inch, e.g., 1 Watt per square inch, applied to the target. The thin metal layer can have a thickness of 1-5 nm. The thin metal layer can then be oxidized, e.g., heated in an oxidizing atmosphere to convert the metal layer to a metal oxide, e.g., convert Ti to TiO_x , to provide the seed layer.
30 Additionally, the oxidized seed layer can also be deposited directly by a PVD or CVD technique, e.g., TiO_x deposition by RF sputtering or ALD.

 The PMNPT layer is then deposited on the seed layer by 22 by PVD. For example, the PMNPT layer can be deposited at a substrate temperature of up to 800 °C, e.g., up to 800 °C, with a power density of 4 to 40 Watts per square inch.

Finally, a second conductive layer, e.g., a platinum film, is deposited by PVD on the PMNPT layer. For example, the second platinum film can be deposited under the same conditions as the first platinum film.

Thus, the final device includes a stack that consists of 1) a wafer, e.g., a single
5 crystal silicon wafer of $\langle 001 \rangle$ crystallographic orientation, 2) a layer of thermal oxide, e.g., silicon oxide, 3) an adhesion layer, e.g., of titanium oxide, 4) a first conductive layer, e.g., Pt $\langle 111 \rangle$ of crystallographic orientation, that provides a bottom electrode, 5) a seed layer, e.g., an titanium oxide seed layer, 6) a PMNPT layer of $\langle 001 \rangle$ crystallographic orientation, and 7) a second conductive layer, e.g., a
10 platinum layer, that provides a top electrode.

Without being limited to any particular theory, the favorable lattice match between adhesion layer, e.g., TiO_x $\langle 001 \rangle$ and bottom electrode, e.g., Pt permits the growth of highly oriented bottom metallic electrode, e.g., Pt $\langle 111 \rangle$ grains. And the highly oriented bottom metallic electrode, e.g., platinum $\langle 111 \rangle$ film permits the
15 formation of a piezoelectric layer having highly oriented PMNPT $\langle 001 \rangle$ grains. This stack can also limit the presence of parasitic phases such as PbO_x and pyrochlore, which are detrimental to the piezoelectric properties.

A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit
20 and scope of the disclosure. For example,

- The system 100 illustrated in FIG. 1 is suitable for processing a planar substrate 10, such as a semiconductor substrate, e.g., a silicon wafer, but the techniques discussed below could be adapted to non-planar substrate.
- The PVD process can use a self-ionized plasma (SIP). In the SIP
25 process, a plasma is initially ignited using an inert gas such as argon. After plasma ignition, the inert gas flow is terminated, and the deposition plasma is maintained by ions generated from the sputtering target.
- The upper electrode could be a different conductive material than the lower electrode, e.g., a conductive material other than platinum.

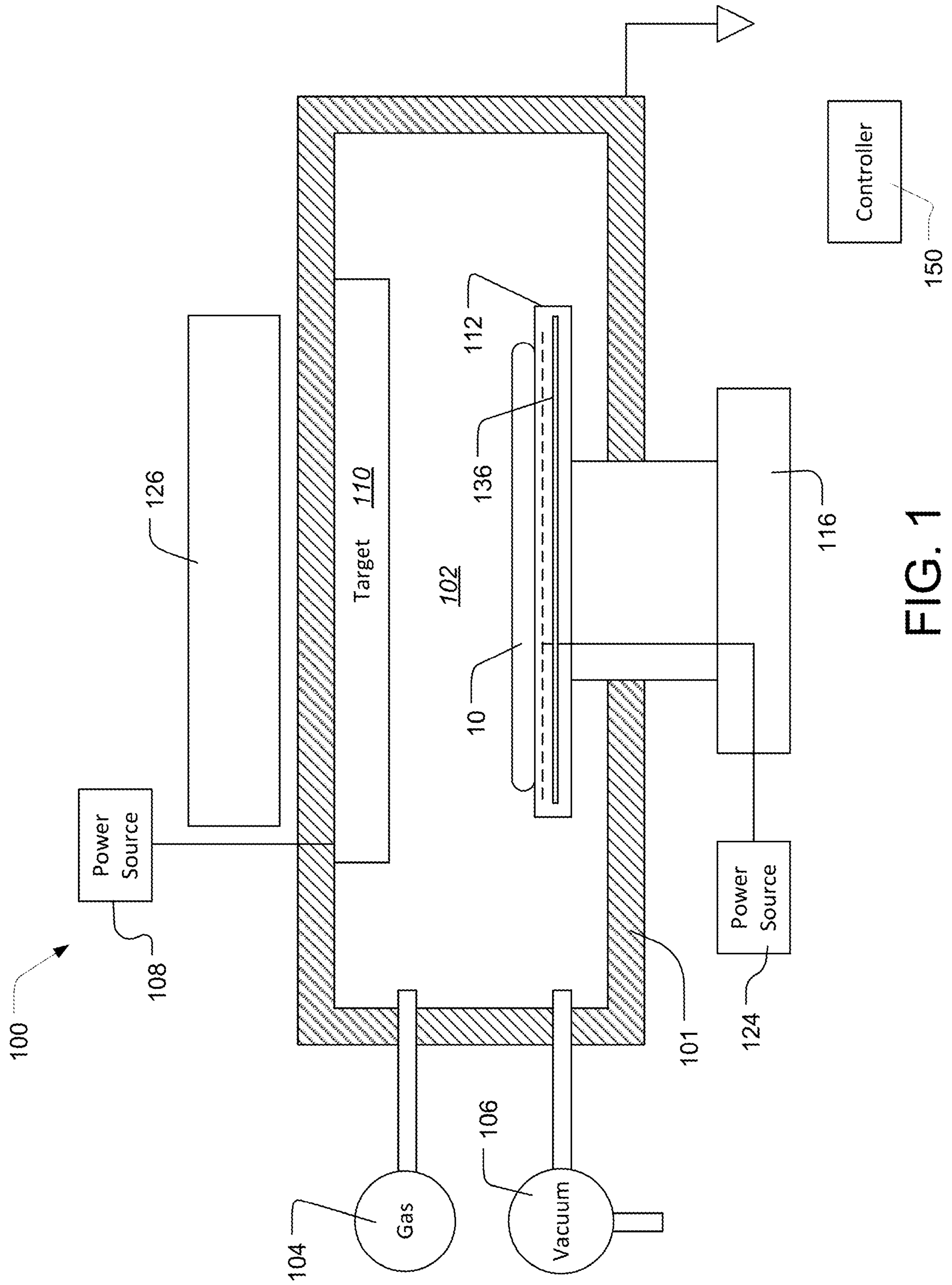
30 Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A piezoelectric device, comprising:
 - a substrate;
 - a thermal oxide layer on wafer;
 - a metal or metal oxide adhesion layer on the thermal oxide layer;
 - a lower electrode on the metal oxide adhesion layer;
 - a seed layer on the lower electrode;
 - a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer on the seed layer; and
 - an upper electrode on the PMNPT piezoelectric layer.
2. The device of claim 1, wherein the wafer comprises a silicon substrate and the thermal oxide is silicon oxide.
3. The device of claim 2, wherein the metal or metal oxide adhesion layer includes one or more of titanium, nickel, chromium.
4. The device of claim 3, wherein the metal or metal oxide adhesion layer is composed of titanium oxide.
5. The device of claim 3, wherein the metal or metal oxide layer adhesion layer is composed of metallic chromium, nickel or an alloy thereof.
6. The device of claim 3, wherein the metal oxide adhesion layer comprises niobium oxide or titanium oxide.
7. The device of claim 1, wherein the lower electrode is composed of platinum.
8. The device of claim 1, wherein the PMNPT material is composed of $(1-x)[\text{Pb}(\text{Mg}_{(1-y)}\text{Nb}_y)\text{O}_3]-x[\text{PbTiO}_3]$, where x is about .2 to 0.8, and y is about .8 to 0.2
9. The device of claim 1, wherein the PMNPT piezoelectric layer has a $\langle 001 \rangle$ crystallographic orientation.

10. The device of claim 1, wherein the upper electrode has a same composition as the platinum lower electrode.
11. A method of fabricating a piezoelectric device, comprising:
 - forming an adhesion layer on a thermal layer of a substrate;
 - depositing a lower electrode on the adhesion layer;
 - forming a seed layer on the lower electrode;
 - depositing a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer on the seed layer by physical vapor deposition; and
 - depositing an upper electrode on the PMNPT piezoelectric layer.
12. The method of claim 11, wherein forming the adhesion layer includes depositing a first metal layer and annealing the substrate to convert at least a portion of the first metal layer to a metal oxide adhesion layer.
13. The method of claim 12, comprising depositing the first metal layer with the substrate at 20-25 °C.
14. The method of claim 13, comprising annealing the first metal layer at a temperature of 700-800 °C.
15. The method of claim 12, wherein forming the seed layer includes depositing a second metal layer and annealing the substrate to convert at least a portion of the second metal to a metal oxide seed layer.
16. The method of claim 15, wherein forming the adhesion layer, depositing the lower electrode and forming the seed layer comprise physical vapor depositions.
17. The method of claim 11, wherein forming the adhesion layer comprises forming a metal or metal oxide layer.
18. The method of claim 15, wherein forming the adhesion layer comprises depositing metallic titanium, chromium, nickel or a combination thereof.

19. The method of claim 11, wherein the PMNPT piezoelectric layer has a $\langle 001 \rangle$ crystallographic orientation.
20. A piezoelectric device, comprising:
- a single crystal silicon wafer having a $\langle 001 \rangle$ crystallographic orientation;
 - a silicon oxide layer on the silicon wafer;
 - a titanium oxide adhesion layer on the silicon oxide layer, the titanium oxide adhesion layer having a thickness of 25-40 nm;
 - a platinum lower electrode having a $\langle 111 \rangle$ crystallographic orientation on the metal oxide adhesion layer;
 - a titanium oxide seed layer on the platinum lower electrode, the titanium oxide seed layer having a thickness of 1-5 nm;
 - a lead magnesium niobate-lead titanate (PMNPT) piezoelectric layer having a $\langle 001 \rangle$ crystallographic orientation on the titanium oxide seed layer; and
 - a platinum upper electrode on the PMNPT piezoelectric layer.



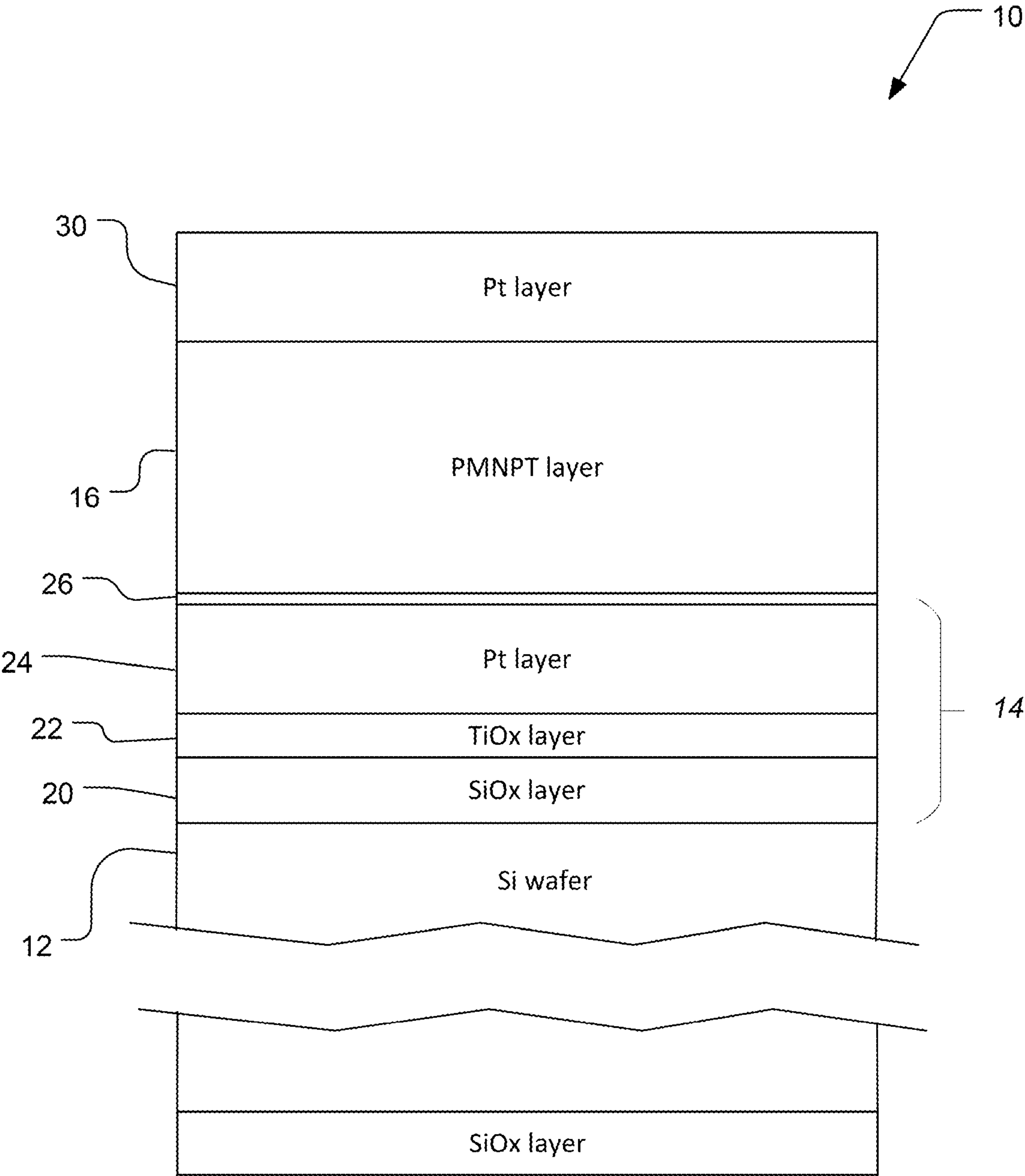


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2020/059881

A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 41/18(2006.01); B41J 2/045(2006.01); G02F 1/35(2006.01); G02F 1/39(2006.01); H01L 41/02(2006.01); H01L 41/047(2006.01); H01L 41/083(2006.01); H01L 41/187(2006.01); H01L 41/27(2013.01); H03H 9/02(2006.01); H03H 9/17(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: piezoelectric, oxide, adhesion, layer, electrode, seed, orientation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2008-0062228 A1 (TAKESHI SAITO) 13 March 2008 (2008-03-13) paragraphs [0045]-[0083], claim 1 and figures 4A-7C	1-19 20
A	US 2019-0214541 A1 (FUJIFILM CORPORATION) 11 July 2019 (2019-07-11) paragraphs [0067]-[0071] and figure 1	1-20
A	US 2018-0275485 A1 (DROR HURWITZ) 27 September 2018 (2018-09-27) paragraphs [0196]-[0209] and figure 1	1-20
A	US 2019-0245509 A1 (ZHUHAI CRYSTAL RESONANCE TECHNOLOGIES CO., LTD.) 08 August 2019 (2019-08-08) claim 1 and figure 1	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “D” document cited by the applicant in the international application “E” earlier application or patent but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family
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Date of the actual completion of the international search

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Date of mailing of the international search report

26 February 2021

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015-0084486 A1 (KONICA MINOLTA, INC.) 26 March 2015 (2015-03-26) paragraphs [0029]-[0037] and figure 1	1-20

INTERNATIONAL SEARCH REPORT
Information on patent family members

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Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
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