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(71) **Applicant**: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard MS: RNB-4-150, Santa Clara, California 95054 (US).

(72) **Inventor; and**
(71) **Applicant** : **EBERLEIN, Matthias** [DE/DE]; Eschenstr. 5, 83607 Holzkirchen (DE).

(74) **Agents**: **MUGHAL, Usman A.** et al.; Blakely, Sokoloff, Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).

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(54) **Title**: CURRENT-MODE DIGITAL TEMPERATURE SENSOR APPARATUS

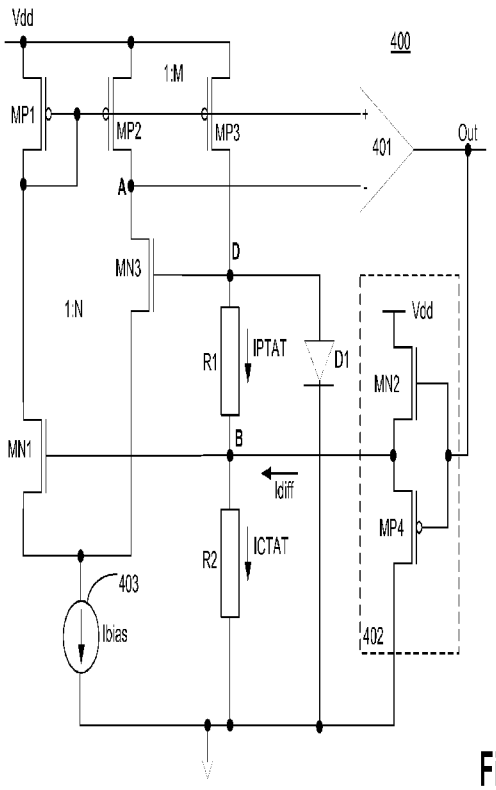

Fig. 4

(57) **Abstract**: Described is a current-mode thermal sensor apparatus which comprises: a first transistor with a gate terminal coupled to a first node; a second transistor with a gate terminal coupled to a second node; a first resistor coupled to the first and second nodes; a second resistor coupled to the first node and a supply node; and a diode coupled to the second node and the supply node.

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CURRENT-MODE DIGITAL TEMPERATURE SENSOR APPARATUS

BACKGROUND

[0001] Accurate sensors to monitor temperature are used for thermal management of micro-processors. Most System-on-Chip (SoC) solutions use some kind of temperature tracking, in order to optimize or control the performance of certain functions. At times, where phones merge with mobile computers, relevant applications of thermal sensors include also mixed-signal functions, like RF (radio frequency) or audio power amplifiers.

[0002] Most integrated solutions for accurate sensors are based on the temperature characteristic of bipolar junctions, namely the base-emitter voltage of parasitic bipolar junction transistors (BJTs). They include an analog-to-digital-converter (ADC) and a reference (e.g., bandgap), typically together with techniques for error correction. **Fig. 1** is a conventional BJT based thermal sensor 100. Thermal sensor 100 includes a first PNP BJT Q1 with base and collector terminals connected to ground (Vss), and emitter terminal connected to a first current source Ic (which is coupled to power supply Vdd). Thermal sensor 100 further includes a second PNP BJT Q2 with base and collector terminals connected to ground (Vss), and emitter terminal connected to a second current source to provide current which is multiple of current Ic i.e., Ic x m, where 'm' is a multiple. The emitters of both Q1 and Q2 have voltages V_{BE1} and V_{BE2} respectively, which are provided to the ADC.

[0003] A conventional approach for a temperature measurement uses a voltage which increases linearly with temperature. This so-called PTAT (proportional-to-absolute-temperature) voltage is typically generated from the difference of two base-emitter voltages (i.e., ΔV_{BE}) of PNP BJTs Q1 and Q2, which are biased with different current densities (e.g. ratio 1:m). An actual temperature value can be extracted by comparing the PTAT voltage (= "ΔVbe") to a temperature independent reference (e.g., a bandgap). In practice, this is achieved by measuring the PTAT voltage (or a multiple of it) directly with an ADC, which in turn includes (or is controlled by) such reference. These circuits may achieve high precision after trimming, but the solution is very complex. Multi-placement is therefore costly.

[0004] Multiple hot-spot sensing using conventional thermal sensors can be performed in deep-submicron technologies and may achieve a significantly smaller size e.g., by using remote diodes away from the core thermal sensor. However, the absence of error compensation results in reduced accuracy, with still average power consumption. Some alternative (non-BJT) concepts yield more "digital-alike" circuits, e.g., by using frequency of ring oscillators as thermal reference. But the assumed advantage towards technology scaling manifests actually as a handicap, because the characteristics of MOS (metal-oxide semiconductor) devices vary

strongly with process. Poor linearity and spread is discouraging for using such concepts in volume production.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0006] **Fig. 1** is a conventional BJT based thermal sensor.

[0007] **Fig. 2** is a high level circuit architecture of a sensor with SAR (successive approximation algorithm) type ADC and resistive digital-to-analog converter (DAC), according to one embodiment.

[0008] **Fig. 3** is a thermal sensor with PTAT generation loop, according to one embodiment.

[0009] **Fig. 4** is a MOS (metal oxide semiconductor) based current-mode thermal sensor, according to one embodiment of the disclosure.

[0010] **Fig. 5** is a plot showing operation of the MOS based current-mode thermal sensor, according to one embodiment of the disclosure.

[0011] **Fig. 6** is a MOS based current-mode thermal sensor, according to another embodiment of the disclosure.

[0012] **Fig. 7** shows architecture of a system with the thermal sensors of the embodiments.

[0013] **Fig. 8** is a smart device or a computer system or an SoC (system-on-chip) with apparatus current-mode thermal sensor, according to one embodiment of the disclosure.

DETAILED DESCRIPTION

[0014] The embodiments describe an apparatus to measure temperature of a silicon die by simple means, but with high accuracy. In one embodiment, the apparatus provides a digital interface and with low silicon area, trimming effort, or power consumption. In one embodiment, the apparatus (which is a thermal sensor) generates a PTAT (proportional-to-absolute temperature) current and a CTAT (complementary-to-absolute temperature) current, and uses their difference as a measure for actual temperature. In one embodiment, the thermal sensor comprises a nonlinear feedback loop which provides inherently the function of a current comparator, and a digital output. In the embodiments, compatibility to dual-well process is

achieved by generating the PTAT signal through MOS devices operated in weak inversion, and the CTAT signal through a bipolar junction (i.e., diode).

[0015] In one embodiment, a successive approximation algorithm (SAR) type analog-to-digital converter (ADC) is realized by sequentially adjusting the temperature threshold, as a function of the digital output. The thermal sensor of the embodiments is less sensitive to process variations and especially MOS mismatch compared to traditional thermal sensors (e.g., **Fig. 1**). The embodiments may also achieve high linearity/precision without costly techniques for error compensation.

[0016] There are many technical effects of the embodiments. Some non-limiting technical effects include lower complexity of a thermal sensor design compared to traditional thermal sensors i.e., smaller silicon area is used. The thermal sensor of the embodiments may also exhibit higher accuracy and linearity compared to traditional thermal sensors because the thermal sensor of the embodiments is inherently insensitive to MOSFET mismatch. The thermal sensor of the embodiments may also exhibit higher power supply rejection compared to traditional thermal sensors. In contrast to traditional thermal sensor circuits, the PTAT signal, reference, and analog-to-digital conversion is generated within one feedback loop which makes the thermal sensor of the embodiments insensitive to external distortion. The sensor of the embodiments may allow low voltage operation e.g., power supply voltages of less then 1.0V. The thermal sensor of the embodiments provides higher dynamic range compared to traditional thermal sensors, and so allows for higher resolution and precision. The thermal sensor of the embodiments is also compatible with future technology scaling and FinFet process.

[0017] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0018] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0019] Throughout the specification, and in the claims, the term "connected" means a direct electrical connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0020] The term "scaling" generally refers to converting a design (schematic and layout) from one process technology to another process technology. The term "scaling" generally also refers to downsizing layout and devices within the same technology node. The term "scaling" may also refer to adjusting (e.g., slow down) of a signal frequency relative to another parameter, for example, power supply level. The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 20% of a target value.

[0021] Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0022] For purposes of the embodiments, the transistors are metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors also include Tri-Gate and FinFet transistors, Gate All Around Cylindrical Transistors or other devices implementing transistor functionality like carbon nano tubes or spintronic devices. Source and drain terminals may be identical terminals and are interchangeably used herein. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure. The term "MN" indicates an n-type transistor (e.g., NMOS, NPN BJT, etc.) and the term "MP" indicates a p-type transistor (e.g., PMOS, PNP BJT, etc.).

[0023] **Fig. 2** is a high level circuit architecture 200 of a thermal sensor with SAR type ADC and resistive digital-to-analog converter (DAC), according to one embodiment. In one embodiment, architecture 200 comprises a first current source 201, a second current source realized as a DAC based resistor R2, current comparator 202, SAR type ADC logic 203, and transistor Q1.

[0024] In one embodiment, first current source 201 is coupled to supply Vdd and node B. In one embodiment, resistor R2 is coupled to node B and ground (i.e., Vss). In one embodiment, the base terminal of Q1 is coupled to node B, the emitter terminal of Q1 is coupled to Vss, and

the collector terminal is coupled to another current source (not shown). In one embodiment, current comparator 202 has an input coupled to node B and a one-bit output "Out" which is received by SAR type ADC logic 203. In one embodiment, SAR type ADC logic 203 generates a Control signal (e.g., n-bit signal where 'n' is an integer greater than one) to control resistance of resistor R2. In one embodiment, the Control signal also indicates the temperature "Temp."

[0025] The operating principle of architecture 200 is based on a current-mode technique which avoids errors introduced by device mismatch, according to one embodiment. The current-mode technique of architecture 200 is in contrast to traditional thermal sensor solutions, which mostly use voltages, either by direct measurement or through conversion to frequency. In one embodiment, temperature sensing is performed by subtracting two currents at node B with opposite temperature coefficients—a precise PTAT current (IPTAT) provided by first current source 201 having positive temperature coefficient and a CTAT current (ICTAT) which is generated by resistor R2 across a V_{BE} voltage of bipolar NPN transistor Q1. Here, V_{BE} voltage of bipolar NPN transistor Q1 has a negative temperature coefficient.

[0026] In one embodiment, at a certain threshold temperature, which can be adjusted by adjusting resistance of R2, the current-difference equals zero. In one embodiment, current comparator 202 transforms the analog signal (i.e., the current difference signal) into a 1-bit output "Out." In one embodiment, this result can be further processed with SAR, by means of controlling resistance of R2 implemented as resistive DAC. In one embodiment, after 'n' steps, the resulting SAR output corresponds to the temperature value in digital format.

[0027] While architecture 200 illustrates a current source 201 coupled to Vdd and node B, in one embodiment, architecture 200 can be modified so that current source 201 is coupled to Vss and node B while resistor R2 is coupled to node B and Vdd. In such an embodiment, Q1 is replaced with a PNP BJT transistor with its emitter terminal coupled to Vdd and its collector terminal coupled to a current source which is further coupled to ground.

[0028] **Fig. 3** is a thermal sensor 300 with PTAT generation loop, according to one embodiment. It is pointed out that those elements of **Fig. 3** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0029] In one embodiment, thermal sensor 300 comprises first resistor R1, second resistor R2, third resistor R0, NPN BJT transistors Q1 and Q2, comparator 301, buffer 302, startup circuit 303, and p-type transistors MP1, MP2, and MP3. In one embodiment, third resistor R0 is optional.

[0030] In one embodiment, first resistor R1 is coupled to node B and a current source. In this embodiment, the current source is realized by MP3 with its drain terminal coupled to first

resistor R1 and its source terminal coupled to Vdd, and its gate terminal biased by some bias voltage. In one embodiment, second resistor R2 is coupled to node B and ground (same as shown in **Fig. 2**). In one embodiment, transistor Q1 is coupled as shown in **Fig. 2**, where the collector terminal is coupled to the drain terminal of MP1.

[0031] In one embodiment, MP1 and MP2 form a current mirror, where MP1 is diode connected (i.e., its gate terminal coupled to its drain terminal). In such an embodiment, MP1 generates a reference current which is mirrored on MP2 which is biased by the same voltage as MP1 because their respective gate terminals are coupled together. In one embodiment, MP2 is sized 'N' times larger than MP1 to up-scale current through MP2 by N times compared to current through MP1. In one embodiment, MP3 is also biased by the same gate voltage as gate voltage of MP1. In other embodiments, MP3 is a standalone current source decoupled from current mirror formed of MP1 and MP2. In one embodiment, current through MP3 may be same or different than the currents through MP1 and/or MP2.

[0032] In one embodiment, a second PNP transistor Q2 is coupled to MP2. In such an embodiment, the collector terminal (node A) of Q2 is coupled to drain terminal of MP2, the emitter terminal of Q2 is coupled to ground, and the base terminal of Q2 is coupled to first resistor R1 directly or via third resistor R0. In one embodiment, transistors Q1 and Q2 form a pseudo-differential pair with intentional asymmetry defined by a size (or current-) ratio of 1:N. In one embodiment, comparator 301 is coupled to drain terminal of MP1 and drain terminal of MP2 (i.e., node A). In one embodiment, output "Out" of comparator 301 is coupled to input of buffer 302.

[0033] In one embodiment, buffer 302 comprises devices that coupled together provide a non-linear characteristic. In one embodiment, buffer 302 comprises an n-type transistor MN2 coupled in series to a p-type transistor MP4. In this embodiment, drain terminal of MN2 is coupled to Vdd and source terminal of MN2 is coupled to node B. In one embodiment, source terminal of MP4 is coupled to node B and drain terminal of MP4 is coupled to ground.

[0034] In one embodiment, start-up circuit 303 comprises a p-type transistor MP5 coupled in series to an NPN transistor Q3 as shown. In one embodiment, start-up circuit 303 comprises an n-type transistor MN1 with its gate terminal coupled to common terminal of MP5 and Q3, its source terminal coupled to ground, and its drain terminal coupled to drain terminal of MP1. In one embodiment, gate terminal of MP5 and base terminal of Q3 are biased by a voltage on node C.

[0035] In one embodiment, the pseudo-differential pair Q1 and Q2, with intentional asymmetry defined by a size (or current-) ratio of 1:N, cause PTAT current (IPTAT) to be generated such that the base-emitter voltage (V_{BE}) difference of Q1 and Q2 appears across

resistor R1 within a (positive) feedback loop. In such an embodiment, the accuracy of IPTAT is not degraded by variations of size or gain in MP3, or even offset of amplifier/comparator 301 because IPTAT may not depend on matching of MP3 (e.g., W, L or Vth) versus MP1/MP2.

[0036] In one embodiment, resistor R2 is coupled in series to resistor R1 so that reference current (ICTAT) is provided for comparison function, without the need for additional current mirrors. In this embodiment, ICTAT is well defined by base-emitter voltage V_{BE} of Q1, and the negative temperature coefficient (TC) allows larger sensitivity than a conventional zero TC reference. Assuming Idiff=0 and neglecting base current Ib1 of Q1, there is one certain operating condition (respectively temperature), where IPTAT matches ICTAT to fulfill Kirchhoff's current law.

[0037] In one embodiment, architecture 300 is stabilized by providing a second (negative) feedback which delivers current Idiff to the summing node B. In this embodiment, the second feedback includes amplifier 301 with buffer 302. In one embodiment, buffer 302 is a class-AB driver. In one embodiment, amplifier 301 is a differential pair (not shown). In other embodiments, other implementations for amplifier 301 may be used. In one embodiment, amplifier 301 performs the function of decoupling node A from node B. In this embodiment, the differential operation of amplifier 301 has benefits for symmetry and PSRR (power supply rejection ratio), because collectors of NPN transistors Q1 and Q2 are now forced to same potential. In one embodiment, amplifier 301 has a current source which is a replica of MP3. In such an embodiment, architecture 300 is self-biased.

[0038] Base current Ib1 of NPN transistor Q1 may create an error (offset) voltage across R1, which also varies with process. In one embodiment, the offset is corrected by choosing IPTAT to be much larger than the current through NPN transistor Q1. In such an embodiment, Ib1 is negligible. In another embodiment, resistor R0 is added in series to NPN transistor Q2, which effectively compensates the error, even for low β.

[0039] **Fig. 4** is a MOS based current-mode thermal sensor 400, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 4** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. So as not to obscure the embodiments, discussion of same elements discussed previously with reference to other embodiments are not repeated again.

[0040] In one embodiment, MOS based current-mode thermal sensor 400 comprises p-type transistors MP1, MP2, and MP3 which are similar to the p-type transistors MP1, MP2, and MP3 of **Fig. 3**. As discussed with reference to **Fig. 3**, in one embodiment, MP3 may be a standalone current source decoupled from current mirror formed by transistors MP1 and MP2.

Referring back to **Fig. 4**, in one embodiment, amplifier 401 is same as amplifier 301. In one embodiment, amplifier 401 can be a general amplifier (e.g., multi-stage amplifier). In one embodiment, amplifier 401 can also be a single stage amplifier with single input from node A. In one embodiment, output signal "Out" of amplifier 402 may be provided to a digital input for further processing directly or via a comparator, a logic gate, or a Schmitt trigger. In one embodiment, resistors R1 and R2 of MOS based current-mode thermal sensor 400 are same as resistors R1 and R2 of **Fig. 3**, and coupled together in series with MP3.

[0041] In one embodiment, buffer 402 is same as buffer 301. In one embodiment, buffer 402 introduces a non-linearity into the transfer curve of the voltage provided to the input of buffer 402 and the current provided at its output to the summing node B. The non-linearity has the effect that the ratio between a given output current swing provided by buffer 402 and the input voltage swing to provide the output current swing is not linear over the input voltage range of buffer 402.

[0042] In one embodiment, buffer 402 is configured such that this ratio has its minimum at the point where the polarity of the current changes polarity i.e., around the zero point of the output current, larger input voltage swings are needed to produce a given output current swing than from higher output current values. In one embodiment, there may be a voltage threshold in the control of buffer 402. In such an embodiment, around the zero point of the output current, the input voltage of buffer 402 corresponding to the output voltage "Out" of amplifier 401 has to overcome this voltage threshold before it can cause a change in the output current. In this embodiment, the input voltage of buffer 402 behaves likes a digital signal since all voltages below the threshold voltage no longer occur since they have no effect on the output current and only higher voltage value about the threshold voltage occur.

[0043] In one embodiment, MOS based current-mode thermal sensor 400 comprises an asymmetric differential amplifier using MOS transistors MN1 and MN3 together with current mirror loads MP1 and MP2. In one embodiment, drain terminal of MN1 is coupled to drain terminal of MP1 and source terminal of MN1 is coupled to current source 403. In one embodiment, drain terminal of MN3 is coupled to drain terminal of MP2 and source terminal of MN3 is coupled to current source 403. In one embodiment, current through current source 403 is Ibias. In one embodiment, gate terminal of MN3 is coupled to node D. In one embodiment, gate terminal of MN1 is coupled to node B. In one embodiment, a diode D1 is coupled in parallel to resistors R1 and R2 i.e., diode D1 is in parallel to node D. For example, anode of diode D1 is coupled to node D and cathode of diode D1 is coupled to ground (Vss).

[0044] In this embodiment, IPTAT is not generated by V_{BE} of NPN transistor Q2, but is generated by MOS transistor MN3 operating in weak inversion mode. In one embodiment, MN1

also operates in weak inversion mode. In one embodiment, MN1 and MN3 operate in weak inversion mode by making MN1 and MN3 large devices (i.e., their W/Ls are substantially larger than W/Ls of other transistors of sensor 400). In one embodiment, MN1 and MN3 are operated in weak inversion mode by keeping current density of these devices low enough so that exponential current law, instead of square current law, is valid for these devices.

[0045] In one embodiment, the core function is generated by MOS transistors MN1 and MN3, which operate in weak-inversion and at different current densities (ratio 1:N). In one embodiment, weak-inversion in devices MN1 and MN3 is achieved by specific device ratio, or by forcing a different current ratio, or both. In one embodiment, MP3 provides a current to diode D1 and also resistor R1 such that the voltage drop over resistor R1 keeps the differential pair in equilibrium. Compared to the embodiment of **Fig. 3**, there is no positive feedback loop (through MP3) in the embodiment of **Fig. 4** i.e., all feedback happens through buffer 402 only, which stabilizes IPTAT.

[0046] In one embodiment, resistor R1 is coupled between the gates of 'N' ratio-ed transistors MN1 and MN3, the corresponding delta-Vgate-voltage is PTAT and results in a strictly temperature-proportional current, IPTAT, which can be expressed as:

$$IPTAT = \frac{Vg1 - Vg3}{R1} = \eta \cdot Vt \cdot \frac{ln(N)}{R1} \quad \ldots (1)$$

where Vt = thermal voltage (= k*T/q), η = sub threshold slope factor, and Vg1 and Vg3 are the gate voltages of MN1 and MN3, respectively. This method of PTAT generation is useful for FinFet technologies, where η equals to 1. Normally factor η varies slightly with process, but it is virtually constant (i.e. equal to 1) for FinFets, which show no "bulk-effect." In one embodiment, higher overall precision is achieved when FinFets are used in weak inversion to generate IPTAT.

[0047] In one embodiment, diode D1 which is coupled in parallel to the PTAT branch, effectively clamps node D to a fixed voltage Vg3 with CTAT behaviour. In one embodiment, diode D1 defines a common mode level. In one embodiment, MP3 provides just a bias current to diode D1 and resistor R1. In one embodiment, MP3 is not involved in feedback control. In one embodiment, the value of tail current Ibias, which in one embodiment is a replica of current through MP3 may be created by a simple PTAT current source to get a predictable temperature slope. In one embodiment, Ibias is generated by a self-biased loop. In one embodiment, when Ibias is provided by current source 403, sensor 400 achieves startup and can operate for its normal function. In such an embodiment, a special startup circuit (e.g., 303 of **Fig. 3**) may not be used.

[0048] In one embodiment, diode D1 may be realized by a diode-connected bipolar device (e.g. "substrate-PNP"), a device which produces a voltage drop with negative temperature

coefficient, Schottky-contact diode, a discrete diode, a lateral bipolar diode, a diode formed from an MOS transistor, or a BJT based diode. The above list of diodes is not meant to be an exclusive list. Other forms of diode or diode behaving elements can be used for realizing diode D1.

[0049] In one embodiment, biasing current for D1 is provided by, or by other means. In one embodiment, due to the feedback loop, the voltage at node B (Vg1) is also "CTAT," and equals the voltage-drop of a diode with 'N' times smaller current density than diode D1. In one embodiment, since resistor R2 is coupled in parallel to such "virtual diode," it carries a current ICTAT with negative temperature coefficient which can be expressed as:

$$ICTAT = \frac{Vg1}{R2} \quad \ldots (2)$$

where Vg1 is the virtual diode D2 voltage which has negative temperature coefficient.

[0050] In one embodiment, the "threshold" value of temperature can be adjusted by modifying resistance of resistor R2. In one embodiment, resistance of resistor R2 is modified by digitally controlled switches (e.g., resistor DAC).

[0051] Continuing with the above explanation, by adding amplifier 401 and buffer 402 as illustrated in sensor 400, a current Idiff is inserted at node B, according to one embodiment. In one embodiment, current Idiff generated by buffer 402 is used to regulate IPTAT, which also stabilizes Vg1 to have CTAT behaviour. In such an embodiment, negative feedback is added, and a stable operating condition is achieved, with:

$$Idiff = IPTAT - ICTAT = \frac{Vt}{R1} \cdot \eta \cdot \ln(N) - \frac{Vg1}{R2} \quad \ldots (3)$$

[0052] In this embodiment, Idiff of equation 3 has a much larger (absolute) temperature coefficient than temperature coefficients of traditional thermal sensors, and so more precise evaluation of temperature is achieved by sensor 400. In one embodiment, Idiff takes on both polarities (i.e., positive and negative) and crosses zero when the temperature matches with the predefined threshold (through resistance of resistor R2).

[0053] In one embodiment, a strongly non-linear transfer function is provided between nodes A and B, so that the loop gain reduces drastically at Idiff=0. In one embodiment, this is accomplished by specific coupling of NMOS/PMOS devices, driving Idiff in class AB-type. In such an embodiment, the voltage at OUT switches between two distinctive values and therefore outputs the function of a highly sensitive current comparator.

[0054] In one embodiment, all relevant functions of sensor 400 are established with little sensitivity to MOSFET matching. In such an embodiment, sensor 400 achieves high precision without extra circuits for error correction, like increased area, chopping or auto-zero techniques. In one embodiment, the most sensitive PTAT signal is regulated through main feedback loop and

does not depend on matching of MP3. In one embodiment, overall linearity of sensor 400 is hardly affected by mismatch of current mirror MP1 and MP2 due to the large g_m of MN1 and MN3.

[0055] In contrast to traditional thermal sensors, the embodiments process currents instead of voltages for thermal measurement and evaluation. This enables high (e.g., unlimited) dynamic range and avoids limitations with voltage headroom. In one embodiment, MOS based current-mode thermal sensor 400 does not include any open loop control, with subsequent provision for error correction. For example, different tasks of generating a temperature dependent signal, providing a reference and comparison, are all accomplished at once within a feedback loop. The above features account for low sensitivity to mismatch errors, and therefore higher accuracy.

[0056] Depending on the comparison result, MOS based current-mode thermal sensor 400 flips between two operating states, therefore comprising a bi-stable behavior. In one embodiment, MOS based current-mode thermal sensor 400 allows analog-to-digital conversion by applying a simple successive approximation algorithm ("SAR"). For example, a single comparator output is provided which compares the temperature signal against a threshold value. This threshold can be adjusted by digital numbers, which inherently represents the main ADC functionality.

[0057] In one embodiment, a processor can have multiple sensors like sensor 400 dispersed through out the processor for sensing temperatures at various parts of the processor. In one embodiment, outputs of each sensor can be processed by a power management unit (PCU) to control various features of the processor e.g., power supply level, operating frequency, external thermal control (e.g., fan speed control), etc. In one embodiment, sensor 400 is implemented as an on-die thermal sensor. In other embodiments, sensor 400 is implemented as an off-die thermal sensor.

[0058] **Fig. 5** is a plot 500 showing operation of the MOS based current-mode thermal sensor, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 5** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0059] The x-axis is temperature in Celsius (C), the y-axis on the left side is current (μA), and the y-axis on the right side is voltage (V). Plot 500 indicates IPTAT and ICTAT as a function of temperature. In one embodiment, when IPTAT and ICTAT are substantially equal (or identical), Idiff is sensed as zero (or substantially zero). In one embodiment, node "OUT" acts like a digital signal, switching sharply between positive and negative MOS threshold when Idiff changes polarity. In one embodiment, the DAC settings for resistor R2 (which determine

the temperature threshold) indicate the sensed temperature. Idiff at zero-crossing point can be expressed as:

$$Idiff = IPTAT - ICTAT = \frac{1}{R1} \cdot \frac{kT}{e} \ln(N) - \frac{Vg1}{R2} = 0; \Rightarrow \quad T = \frac{Vgo}{\frac{R2}{R1} \cdot \frac{k \cdot \ln(N)}{e}} - tc \qquad \ldots (4)$$

where, Vgo is a constant of approximately 1.2V and related to the silicon bandgap extrapolated to 0 K), "tc" is the temperature coefficient of diode D1 and is approximately 2mV/K.

[0060] In one embodiment, if the negative feedback (node A towards B) has a strong nonlinear transfer characteristic exactly at Idiff=0, then it includes effectively the function of a current comparator. This behavior is accomplished by transistors MP2 and MP3 in the specific configuration, working similar like two anti-parallel diodes.

[0061] **Fig. 6** a MOS based current-mode thermal sensor 600, according to another embodiment of the disclosure. It is pointed out that those elements of **Fig. 6** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0062] The embodiment of MOS based current-mode thermal sensor 600 is similar to the embodiment of MOS based current-mode thermal sensor 400 except that the design is a complementary design using n-type current mirror, p-type differential pair, and n-type current source to generate Ibias. MOS based current-mode thermal sensor 600 is functionally equivalent to MOS based current-mode thermal sensor 400. So as not to obscure the embodiments, functional details of each device/component of sensor 600 are not discussed because they are similar to that of sensor 400.

[0063] In one embodiment, current-mode thermal sensor 600 comprises amplifier 601 (functions similar to amplifier 401), buffer 602 (which functions similar to buffer 402), current source 603 to generate Ibias (which functions similar to current source 403), differential p-type transistors MP1 and MP3 (which function similar to differential n-type transistors MN1 and MN3), n-type current mirror loads MN1 and MN2 (which function similar to p-type current mirror loads MP1 and MP2), n-type current source MN3 (which functions similar to p-type current source MP3), resistor R1 (same as resistor R1 of **Fig. 4**), resistor R2 (which is same as resistor R2 of **Fig. 4**), and diode D1 which is same as diode D1 of **Fig. 4**.

[0064] In this embodiment, anode of diode D1 is coupled to Vdd and cathode of diode D1 is coupled to node D. In this embodiment, resistor R2 is coupled between Vdd and node B and resistor R1 is coupled between nodes B and D. In this embodiment, MN4 of buffer 602 has its drain terminal coupled to Vdd and source terminal coupled to node B. In this embodiment, source terminal of MP2 is coupled to node B while drain terminal of MP2 is coupled to ground.

In this embodiment, current source 603 is coupled between Vdd and common node of MP1 and MP3.

[0065] **Fig. 7** shows architecture 700 of a system 710 with the thermal sensors of the embodiments. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0066] In one embodiment, system 710 may be a system on chip (SoC) or in general any semiconductor circuit using an indication of temperature. In one embodiment, system 710 may have a system block 716, a first temperature sensor 711, 712, a second temperature sensor 713,714 and a third temperature sensor 715. In one embodiment, system 710 may have only one temperature sensor or any other number of temperature sensors. In one embodiment, system block 716 may be of any type and may be for example a communication circuit and may have a digital section.

[0067] In one embodiment, first temperature sensor 711, 712 may have an analog section 711 and a digital section 712. In one embodiment, second temperature sensor 713, 714 may also have an analog section 713 and a digital section 714. In one embodiment, third temperature sensor 715 may have only an analog section 715. In one embodiment, analog sections 711, 713 and 715 of the first, second and third temperature sensors may the circuit arrangement of **Fig. 4** and/or **Fig. 6**. In one embodiment, digital sections 712, 714 of the first and second temperature sensors may have control circuit for adjusting resistance of R2. In one embodiment, for third temperature sensor 715 the control circuit (not shown) may be formed by elements within the system block 716. In one embodiment, these elements may be dedicated digital circuit components or a program for performing the required functions.

[0068] In one embodiment, the three temperature sensors 711 – 715 allow to sense the temperature within the system 710 at three different places. Different temperature sensors may also be used to provide both a temperature reading indicating the absolute temperature and a binary temperature information indicating only whether the temperature exceeds a threshold.

[0069] **Fig. 8** is a smart device or a computer system or an SoC (system-on-chip) with apparatus of current-mode thermal sensor, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 8** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0070] **Fig. 8** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In one embodiment, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-

phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0071] In one embodiment, computing device 1600 includes a first processor 1610 with apparatus of current-mode thermal sensor described with reference to embodiments discussed. Other blocks of the computing device 1600 may also include apparatus of current-mode thermal sensor described with reference to embodiments discussed. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0072] In one embodiment, processor 1610 (and processor 1690) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0073] In one embodiment, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0074] Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0075] I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of

audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0076] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0077] In one embodiment, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0078] In one embodiment, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0079] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g.,

BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0080] Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0081] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0082] Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[0083] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0084] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or

characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0085] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0086] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. For example, other memory architectures e.g., Dynamic RAM (DRAM) may use the embodiments discussed. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0087] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0088] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0089] For example, in one embodiment, apparatus comprises: a first transistor with a gate terminal coupled to a first node; a second transistor with a gate terminal coupled to a second node; a first resistor coupled to the first and second nodes; a second resistor coupled to the first node and a supply node; and a diode coupled to the second node and the supply node. In one embodiment, the first and second transistors to operate in weak inversion mode.

[0090] In one embodiment, the first and second transistors are configured to form a differential pair. In one embodiment, the first and second transistors provide a PTAT signal. In one embodiment, the diode provides a CTAT signal on the first and second nodes. In one embodiment, the supply node is a ground node. In one embodiment, the apparatus further comprises a current source coupled to a common node of the first and second transistors.

[0091] In one embodiment, the apparatus further comprises a current mirror to provide: a first current through the first transistor, and a second current through the second transistor. In one embodiment, the current mirror to cause the second current to be a multiple of the first current. In one embodiment, the apparatus further comprises: an amplifier including inputs coupled to nodes of the current mirror, and an output; and a buffer including an input coupled to the output of the amplifier, and an output coupled to the first node. In one embodiment, the buffer comprises devices that coupled together provide a non-linear characteristic.

[0092] In one embodiment, the apparatus further comprises a current source to provide a third current through a third transistor, wherein the third transistor is coupled to the second node. In one embodiment, the apparatus further comprises a circuit to adjust resistance of the second resistor. In one embodiment, the circuit comprises a digital-to-analog converter (DAC). In one embodiment, the diode is one of: a device which produces a voltage drop with negative temperature coefficient; Schottky-contact diode; a discrete diode; a lateral bipolar diode; a diode formed from a MOS transistor; or a BJT based diode. In one embodiment, the first and second resistors are coupled together in series.

[0093] In another example, an apparatus comprises: a first transistor with a gate terminal coupled to a first node; a second transistor with a gate terminal coupled to a second node; a first resistor coupled to the first and second nodes; a second resistor coupled to the first node and a ground node; a third transistor coupled in series with the first and second resistors; a current mirror to provide a first current through the first transistor, a second current through the second transistor, and a third current through a third transistor; and a diode coupled to the second node and the ground node, the diode to receive a part of the third current.

[0094] In one embodiment, the first and second transistors to operate in weak inversion mode. In one embodiment, the apparatus further comprises a circuit to adjust resistance of the

second resistor. In one embodiment, the first and second transistors provide a PTAT signal. In one embodiment, the diode provides a CTAT signal on the first and second nodes.

[0095] In another example, a system comprises a memory unit; a processor coupled to the memory unit, the processor having a temperature sensor according to apparatus discussed above; and a wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit for displaying content processed by the processor.

[0096] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
   a first transistor with a gate terminal coupled to a first node;
   a second transistor with a gate terminal coupled to a second node;
   a first resistor coupled to the first and second nodes;
   a second resistor coupled to the first node and a supply node; and
   a diode coupled to the second node and the supply node.

2. The apparatus of claim 1, wherein the first and second transistors to operate in weak inversion mode.

3. The apparatus of claim 1, wherein the first and second transistors are configured to form a differential pair.

4. The apparatus of claim 1, wherein the first and second transistors to provide a PTAT signal.

5. The apparatus of claim 1, wherein the diode to provide a CTAT signal on the first and second nodes.

6. The apparatus of claim 1, wherein the supply node is a ground node.

7. The apparatus of claim 1 further comprises a current source coupled to a common node of the first and second transistors.

8. The apparatus of claim 1 further comprises a current mirror to provide:
   a first current through the first transistor, and
   a second current through the second transistor.

9. The apparatus of claim 8, wherein the current mirror to cause the second current to be a multiple of the first current.

10. The apparatus of claim 8 further comprises:

an amplifier including inputs coupled to nodes of the current mirror, and an output; and

a buffer including an input coupled to the output of the amplifier, and an output coupled to the first node.

11. The apparatus of claim 10, wherein the buffer comprises devices that coupled together provide a non-linear characteristic.

12. The apparatus of claim 1 further comprises a current source to provide a third current through a third transistor, wherein the third transistor is coupled to the second node.

13. The apparatus of claim 1 further comprises a circuit to adjust resistance of the second resistor.

14. The apparatus of claim 13, wherein the circuit comprises a digital-to-analog converter (DAC).

15. The apparatus of claim 1, wherein the diode is one of:

a device which produces a voltage drop with negative temperature coefficient;

Schottky-contact diode;

a discrete diode;

a lateral bipolar diode;

a diode formed from a MOS transistor; or

a BJT based diode.

16. The apparatus of claim 1, wherein the first and second resistors are coupled together in series.

17. An apparatus comprising:

a first transistor with a gate terminal coupled to a first node;

a second transistor with a gate terminal coupled to a second node;

a first resistor coupled to the first and second nodes;

a second resistor coupled to the first node and a ground node;

a third transistor coupled in series with the first and second resistors;

a current mirror to provide a first current through the first transistor, a second current through the second transistor, and a third current through a third transistor; and

a diode coupled to the second node and the ground node, the diode to receive a part of the third current.

18. The apparatus of claim 17, wherein the first and second transistors to operate in weak inversion mode.

19. The apparatus of claim 17 further comprises a circuit to adjust resistance of the second resistor.

20. The apparatus of claim 17, wherein the first and second transistors to provide a PTAT signal.

21. The apparatus of claim 17, wherein the diode to provide a CTAT signal on the first and second nodes.

22. A system comprising:

a memory unit;

a processor coupled to the memory unit, the processor having a temperature sensor according to any one of apparatus claims 1 to 16; and

a wireless interface for allowing the processor to communicate with another device.

23. The system of claim 22 further comprises a display unit for displaying content processed by the processor.

24. A system comprising:

a memory unit;

a processor coupled to the memory unit, the processor having a temperature sensor according to any one of apparatus claims 17 to 21; and

a wireless interface for allowing the processor to communicate with another device.

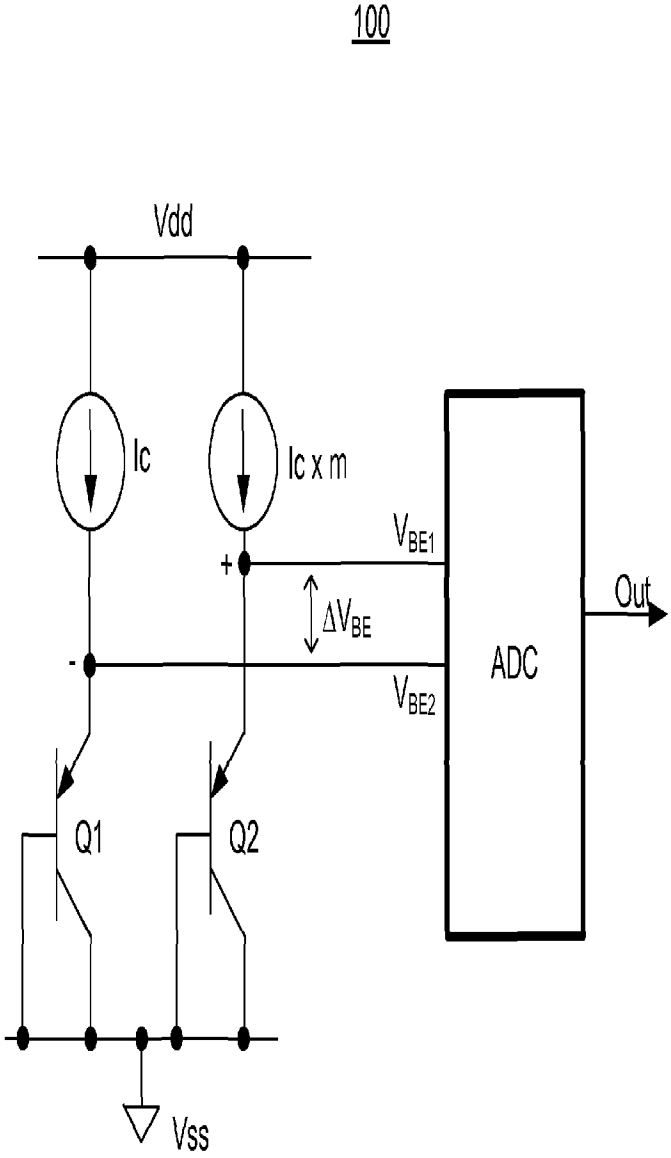
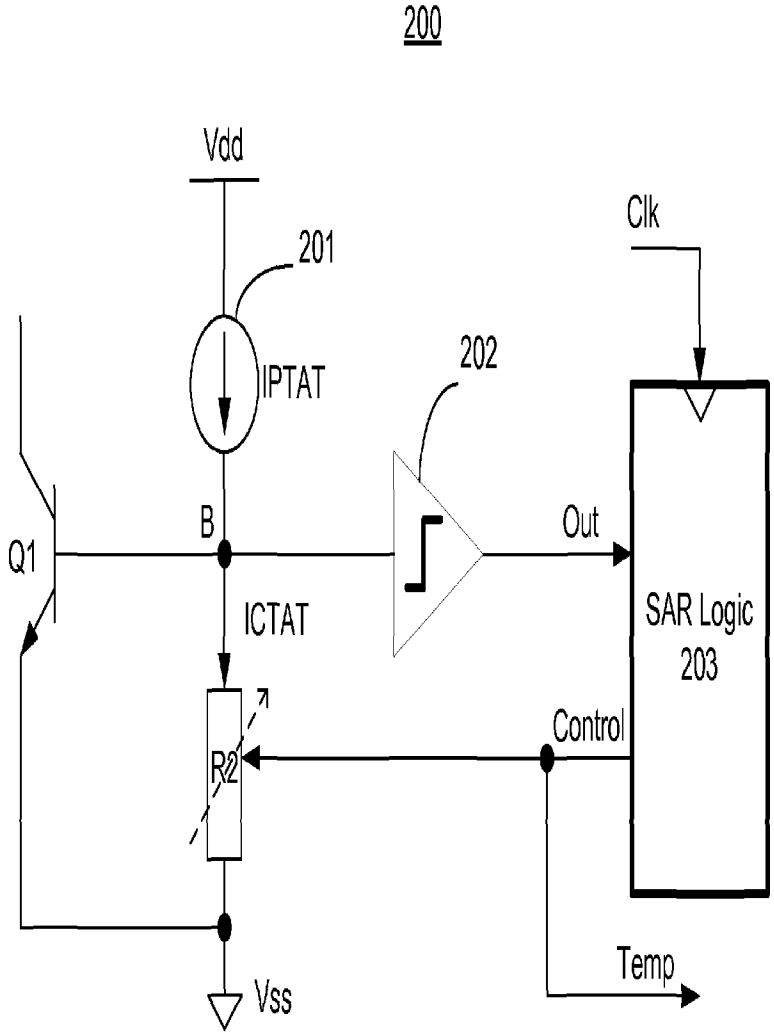


Fig. 1
(prior Art)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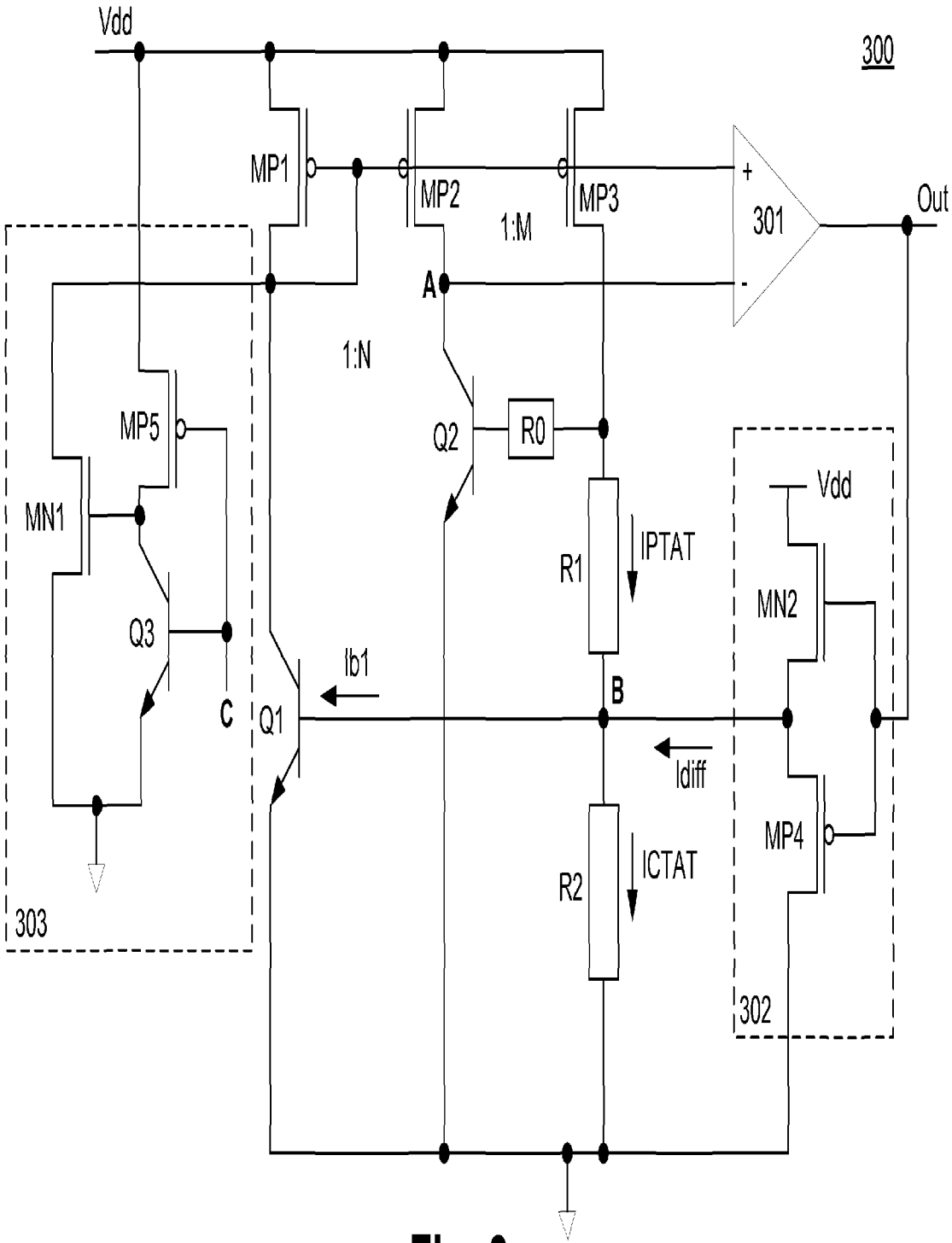
202
Clk
Q1
B
Out
SAR Logic
203
ICTAT
Control
R2
Temp
Vss

Fig. 2


Vdd
300
MP1
MP2
MP3
1:M
+
301
-
Out
A
1:N
MP5
Q2
R0
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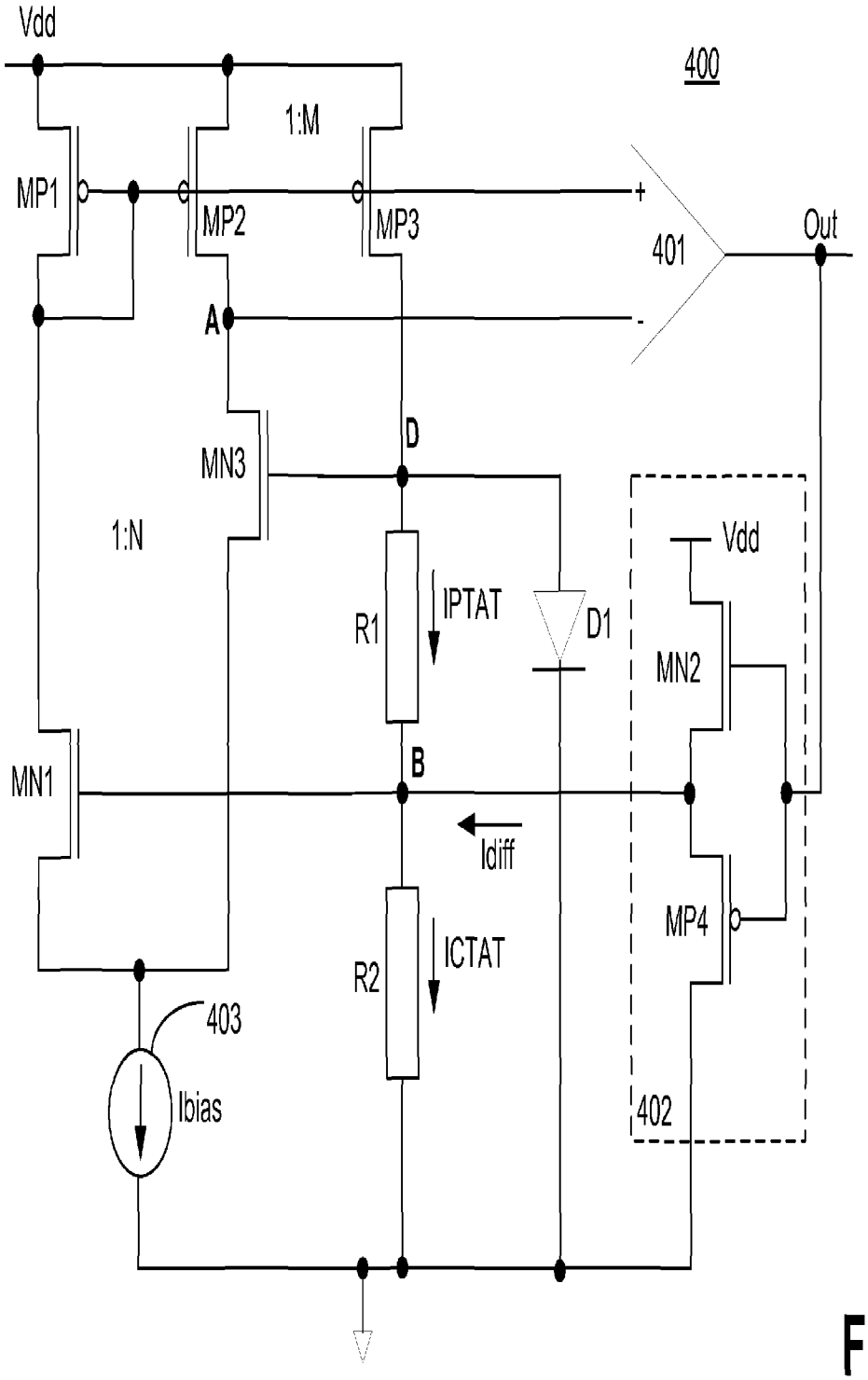
Ib1
B
C
Q1
Idiff
MP4
R2
ICTAT
303
302

Fig. 3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MP1
MP2
MP3
+
401
Out
-
A
D
MN3
1:N
Vdd
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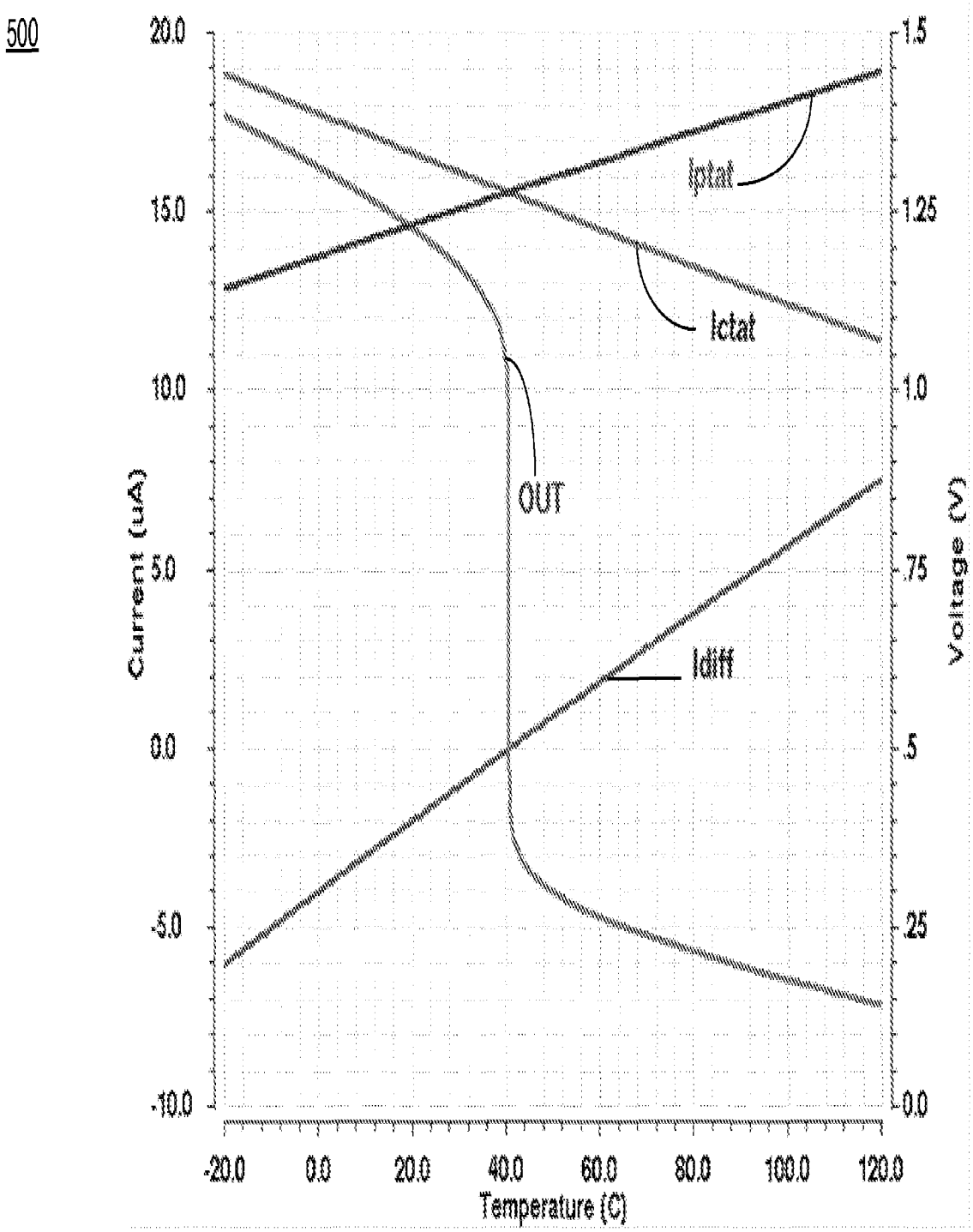
IPTAT
D1
MN2
MN1
B
Idiff
MP4
R2
ICTAT
403
Ibias
402

Fig. 4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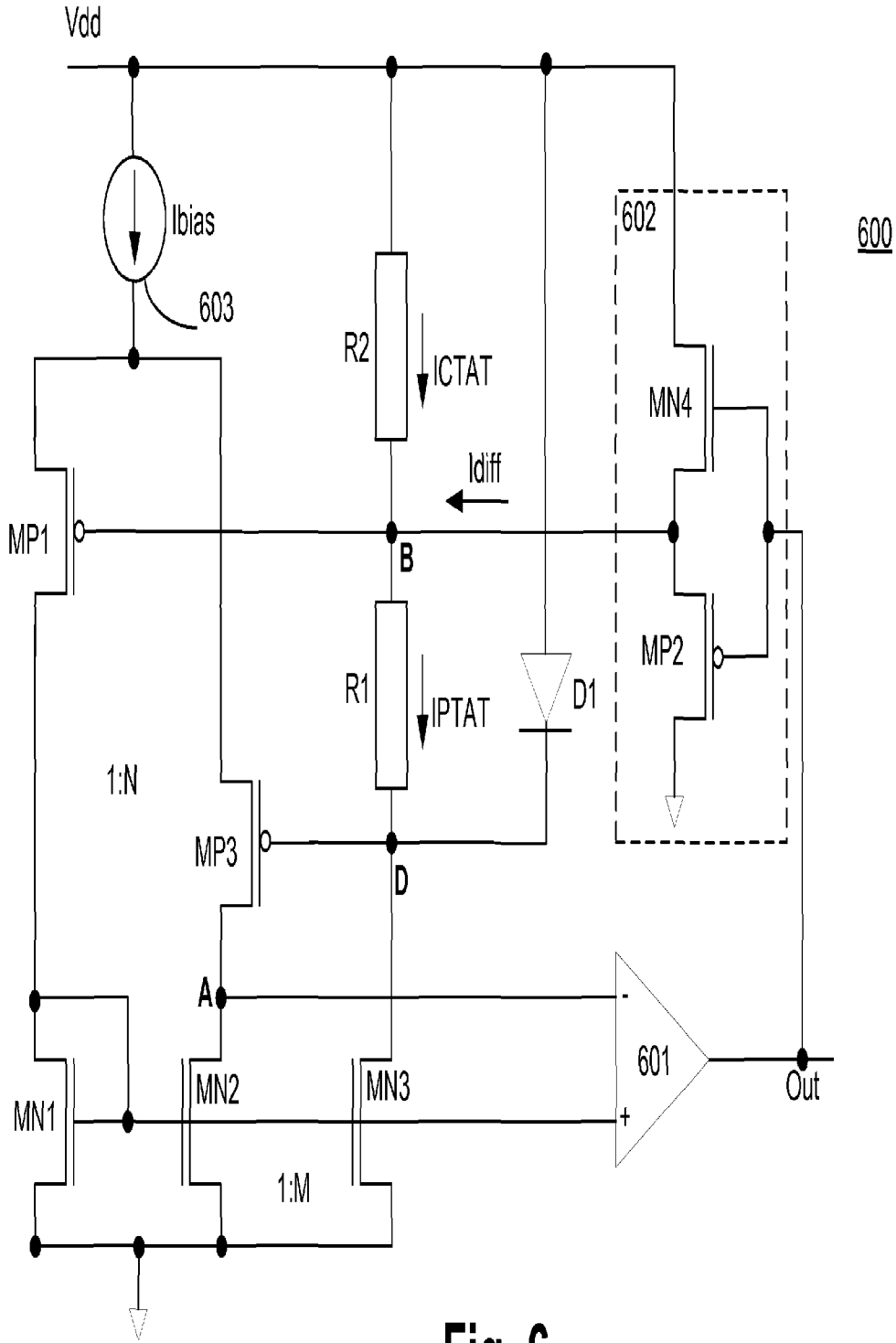
15.0
10.0
5.0
0.0
-5.0
-10.0
Current (uA)
1.5
1.25
1.0
.75
.5
.25
0.0
Voltage (V)
Iptat
Ictat
OUT
Idiff
-20.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
Temperature (C)

Fig. 5


Vdd
Ibias
603
R2
ICTAT
Idiff
602
600
MN4
MP1
B
MP2
R1
IPTAT
D1
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MP3
D
A
-
601
Out
MN1
MN2
MN3
+
1:M

Fig. 6

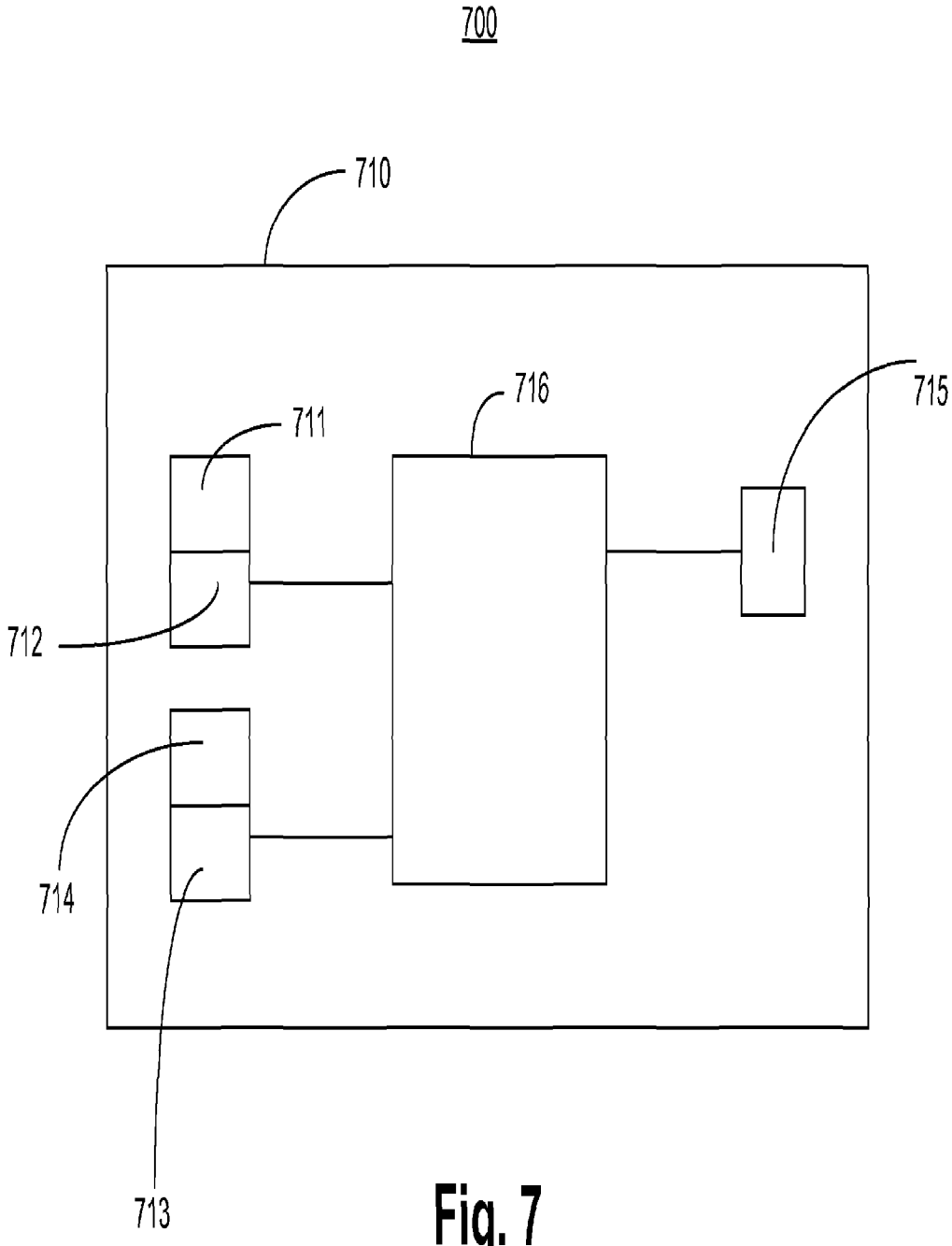

Fig. 7

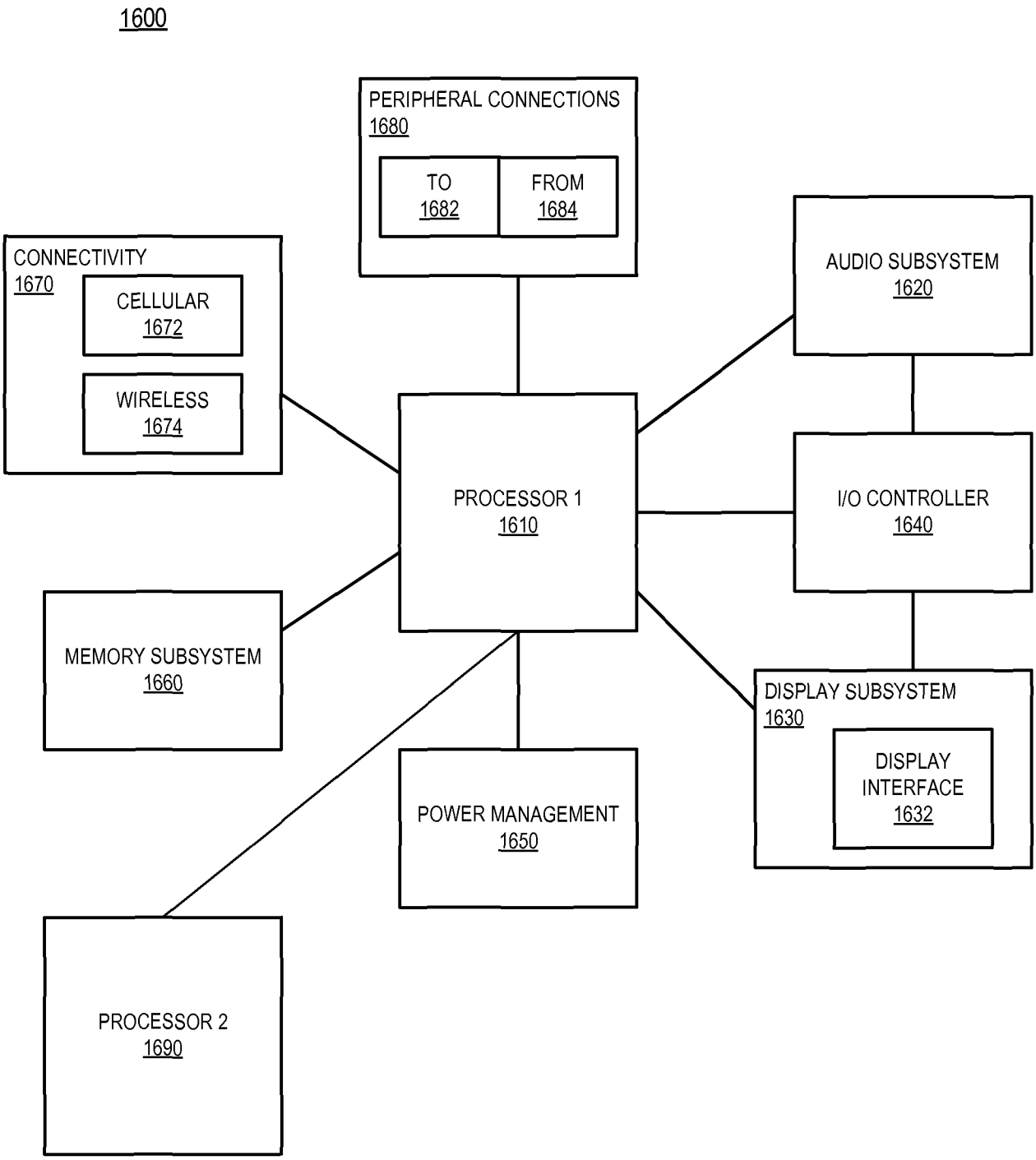
1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1620
PROCESSOR 1
1610
I/O CONTROLLER
1640
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650
PROCESSOR 2
1690

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2013/051526

A. CLASSIFICATION OF SUBJECT MATTER

G01K 7/01 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01K 7/00, 7/01, 7/16-7/25, G05F 3/24-3/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2425419 A (WOLFSON MICROELECTRONICS PLC) 25.10.2006	1-24
A	US 2009/0279584 A1 (JY-DER DAVID TAI) 12.11.2009	1-24
A	US 2004/0095187 A1 (INTERSIL AMERICAS INC.) 20.05.2004	1-24
A	US 4224537 A (MOTOROLA, INC.) 23.09.1980	1-24

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/ FIPS Russia, 123995, Moscow, G-59, GSP-5, Berezhkovskaya nab., 30-1 Facsimile No. +7 (499) 243-33-37	Authorized officer A. Grigoryan Telephone No. 499-240-25-91

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