(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 March 2014 (06.03.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/036291 A1

(51) International Patent Classification:
H01L 23/48 (2006.01)

(21) International Application Number:
PCT/US2013/057337

(22) International Filing Date:
29 August 2013 (29.08.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/601,394 31 August 2012 (31.08.2012) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: LATCH-UP SUPPRESSION AND SUBSTRATE NOISE COUPLING REDUCTION THROUGH A SUBSTRATE BACK-TIE FOR 3D INTEGRATED CIRCUITS

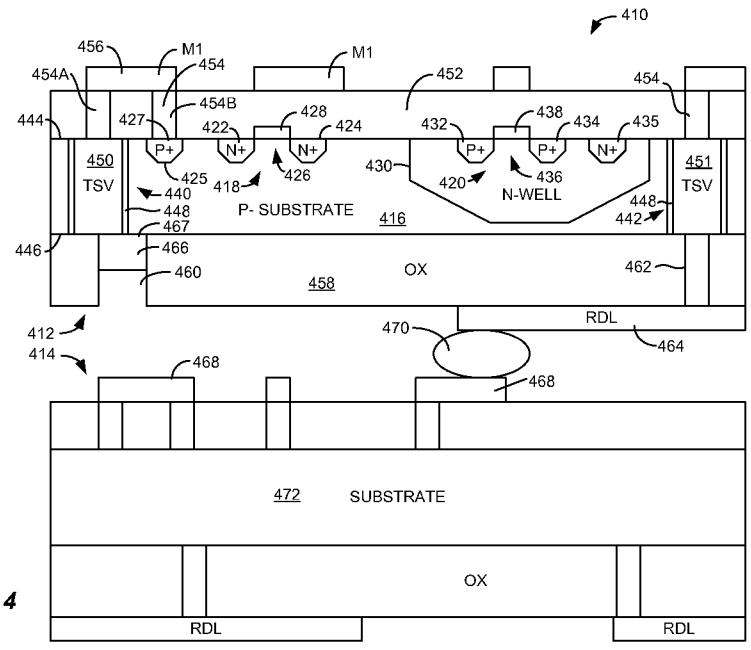

FIG. 4

(57) **Abstract**: Roughly described, an integrated circuit device has a conductor extending entirely through the substrate, connected on one end to the substrate topside surface and on the other end to the substrate backside surface. In various embodiments the conductor is insulated from all RDL conductors on the backside of the substrate, and/or is insulated from all conductors and device features on any below-adjacent chip in a 3D integrated circuit structure. Methods of fabrication are also described.

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LATCH-UP SUPPRESSION AND SUBSTRATE NOISE COUPLING REDUCTION THROUGH A SUBSTRATE BACK-TIE FOR 3D INTEGRATED CIRCUITS

BACKGROUND

[0001] The invention relates to 3D integrated circuits, and more particularly to structures and methods for suppressing latch-up and noise coupling.

[0002] A typical CMOS circuit includes N- and P-type regions arranged to form planar or multi-gate MOS transistors. Regions of opposite conductivity types which are adjacent each other typically form parasitic pn junctions and bipolar transistor structures. While usually reverse-biased, conditions can occur in which these structures become forward biased. When this occurs, a positive feedback loop ensues which provides a low resistance current path from the positive supply voltage to ground, thereby interfering with proper functioning of the circuit and, in serious cases, destroying the chip through heat damage.

[0003] Fig. 1 is a schematic diagram showing a typical CMOS arrangement including a PMOS transistor 110 adjacent to an NMOS transistor 112. Such proximity is common in CMOS devices. The PMOS transistor 110 includes two heavily doped P+ diffusion regions 116 and 118 separated laterally by a channel region 120. A gate stack 122 overlies the channel region 120. The two P+ diffusion regions 116 and 118 are formed inside an N-well 124, which is itself an N-doped region formed inside a lightly doped P- substrate 114. Also formed within the N-well 124 is a heavily doped N+ diffusion 125, also called a well tie or a contact pad, for connecting the N-Well 124 to VDD.

[0004] The NMOS transistor 112 includes two heavily doped N+ type diffusion regions 126 and 128 separated laterally by a channel region 130. A gate stack 132 overlies the channel region 130. The two N+ diffusion regions 126 and 128 are formed directly in the P- substrate 114. Also formed in the substrate in close proximity to one of the N+ diffusion regions 126 and 128, is a heavily doped P+ diffusion region 135, also called a substrate tie or a contact pad, for connecting the P- substrate 114 to ground.

[0005] Other CMOS arrangements are common as well, including those that also include a lightly doped P--well in which the NMOS transistor 112 is formed. The arrangement of Fig. 1

will be illustrative of the latch-up problem, but it will be understood that many other arrangements also suffer from the same problem.

[0006] Superimposed on the CMOS diagram of Fig. 1 is a circuit schematic illustrating the bipolar transistors that are formed by the various PN junctions formed by the CMOS arrangement. In particular, a PNP transistor Q1 is formed by one of the P+ diffusions 116 or 118 acting as the emitter E1, the N-well 124 acting as the base B1, and the P- substrate 114 acting as the collector C1. At the same time, the N-well 124 acts as the collector C2 of an NPN transistor Q2, with the P- substrate 114 acting as the base B2, and one of the N+ regions 126 or 128 acting as the emitter E2. The base B1 of the PNP transistor Q1 is connected to the collector C2 of the NPN transistor Q2, and the base of NPN transistor Q2 is connected to the collector C1 of PNP transistor Q1. The base B1 of transistor Q1 is connected to N+ diffusion 125 through the resistance Rw of the N-well 124, and the base B2 of transistor Q2 is connected to P+ diffusion 135 through the substrate resistance Rs.

[0007] Fig. 2 is schematic circuit diagram of Fig. 1 rearranged to show it vertically. It can be seen that as long as the two bipolar transistors Q1 and Q2 are not forward biased, current will not flow through the circuit. A number of conditions can trigger latch-up however, including noise, which sometimes can induce sufficient current at the base of one of the transistors for long enough to forward bias the other transistor, thereby starting a feedback loop. Several techniques have been devised for reducing or eliminating latch-up susceptibility, some of which are discussed in Wolf, Silicon Processing for the VLSI Era, Vol. II, Process Integration, pp. 400-419 (1990), incorporated herein by reference.

[0008] One common technique for reducing or eliminating latch-up susceptibility is to connect the backside of the substrate to ground. Referring to Fig. 1, if the substrate tie 135 is also connected to ground, it can be seen that this technique provides a low resistance current path in parallel with the substrate resistance Rs, effectively short circuiting it. The base B2 of NPN transistor Q2 therefore is effectively connected to its emitter E2 and the transistor cannot conduct.

[0009] Fig. 3 (consisting of Fig. 3A and 3B) illustrates how the short circuiting of Rs is often accomplished in a typical lead frame package. Fig. 3A is a cross-sectional view of the package showing a die 310, and Fig. 3B is an enlarged topside view of a corner 322 of the structure of Fig. 3A. As shown in Fig. 3A, the die 310 is attached on its back side using an electrically conductive die attach adhesive 312, to a metal lead frame pad 314. The lead frame also includes a number of metal leads 316 that extend out through the epoxy molded packaging material 318 for external electrical connection. Some of the leads 316, for example lead 316A, are connected

to the lead frame pad 314 to ground externally of the package, and thereby connect the back side of the die 310 to ground. Others of the leads 316 are connected to various I/O and power pads (324 in Fig. 3B) on the top side of the chip. In addition, Fig. 3B also illustrates that some of the bonding pads 324, for example 324A, are connected ("down-bonded") directly to the lead frame pad 314 using corresponding bonding wires 320A. These bonding pads 324A are formed on and connect to heavily doped P+ contact pads such as 135 (Fig. 1). Since as previously mentioned the backside of the die is also connected to the lead frame pad 314 through conductive die attach material 312, it can be seen that a very low resistance conductive path is formed electrically connecting the P+ contact pads 135 to the backside of the substrate die 310, thereby short circuiting the substrate resistance Rs (Fig. 1). With Rs short circuited, it becomes much less likely that transient current flow through PNP transistor Q1 can increase the base-collector voltage on NPN transistor Q2 sufficiently to turn it on. As a result, latch-up conditions are less likely.

[0010] Recently, as integrated circuit densities have increased, manufacturers have begun developing packaging structures in which two or more dies are stacked on top of each other. Signal and power supply lines from the top surface of one chip are passed through the body of the chip to the one below using through-silicon vias (TSVs). A TSV is a conductive post that extends all the way through the chip, from the topside surface to the backside surface, where it can connect through metal bump contacts to conductors on the topside surface of the below-adjacent chip. The conductor in the TSV is typically copper or another metal such as TiW, and it is typically isolated from the substrate along its entire length by a dielectric or other barrier material. On the topside, ordinary metal interconnects connect the top ends of the TSV conductors to circuit components. The backside surface of the chip is coated with an insulator, such as an oxide, and holes are opened to expose the bottom ends of the TSV conductors. One or more layers of metal interconnects (called RDL (redistribution layer) conductors) are formed on the backside to electrically route signals and power from the bottom ends of the TSV conductors to the positions required for mating with the appropriate bump contacts on the below-adjacent chip. The bottom chip in the stack is connected to external circuitry usually by TSVs connected on the backside to a ball grid array (BGA). The overall stack of chips is sometimes referred to herein as a three-dimensional integrated circuit (3DIC).

[0011] 3DIC technology poses a number of problems for known techniques for suppressing latch-up. First, because of the difficulties in fabricating very deep TSVs, chip substrates used in 3DICs typically are considerably thinned, from the backside, to a thickness of only around 50

microns. Referring to Fig. 1, it can be seen that a much thinner substrate considerably narrows the current path through the substrate to the P+ substrate contact pads 135, thereby significantly increasing the substrate resistance Rs. Moreover, down-bonding is no longer available to short circuit this current path, since the substrate backside is not connected by die attach adhesive to a below-adjacent lead frame pad. Thus Rs is not short circuited, and the potential for latch-up conditions is significantly higher. Second, in 3DIC's, it is common for TSVs to be used to carry power and signals through a particular chip, from the below-adjacent chip to the above-adjacent chip and vice-versa, without ever having to connect to the chip or chips stacked between them. This is common where, for example, some chips are designed to operate at 1 volt while the chips above and below are operating at 3.3 volts. In this case the TSV might carry a 3.3 volt signal through a 1 volt chip, which can easily induce sufficient currents by capacitive coupling to trigger latch-up in the more sensitive 1 volt chip.

[0012] Accordingly, an opportunity arises to create robust solutions to the problem of latch-up susceptibility in 3D integrated circuits. Better chip yields, and denser, and more powerful circuits, components and systems may result.

SUMMARY

[0013] Roughly described, an integrated circuit device has a conductor extending entirely through the substrate, connected on one end to the substrate topside surface and on the other end to the substrate backside surface. In various embodiments the conductor is insulated from all RDL conductors on the backside of the substrate, and/or is insulated from all conductors and device features on any below-adjacent chip in a 3D integrated circuit structure.

[0014] The above summary of the invention is provided in order to provide a basic understanding of some aspects of the invention. This summary is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later. Particular aspects of the invention are described in the claims, specification and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0015] The invention will be described with respect to specific embodiments thereof, and reference will be made to the drawings, in which:

[0016] Fig. 1 is a schematic diagram showing a typical CMOS structure in cross-section. Bipolar parasitic transistor circuitry is superimposed on the cross-section.

[0017] Fig. 2 is schematic circuit diagram of the bipolar circuitry of Fig. 1 rearranged to show it vertically.

[0018] Fig. 3 consists of Fig. 3A and 3B.

[0019] Fig. 3A a cross-sectional view of a package showing a die.

[0020] Fig. 3B is an enlarged topside view of a corner 322 of the structure of Fig. 3A.

[0021] Fig. 4 is a cross-sectional view illustrating pertinent features of a 3D integrated circuit structure incorporating aspects of the invention.

[0022] Fig. 5 (consisting of Figs. 5A through 5I) illustrates an example process flow that can be used to fabricate a 3D integrated circuit such as that shown in Fig. 4.

[0023] Fig. 6 shows a simplified representation of an illustrative digital integrated circuit design flow incorporating features of the invention.

[0024] Fig. 7 is a simplified block diagram of a computer system 710 that can be used to implement software incorporating aspects of the present invention.

DETAILED DESCRIPTION

[0025] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[0026] Fig. 4 is a cross-sectional view illustrating pertinent features of a 3D integrated circuit structure 410 incorporating aspects of the invention. The drawing, as with all drawings herein, is not to scale. Only a small part of the structure is shown, and it will be understood that typically each chip is much larger (laterally) and includes many more features. Additionally, Fig. 4 shows only two vertically-adjacent chips of the 3D structure 410: chip 412 and below-adjacent chip 414. A typical 3D IC might include additional chips further above and/or below, all oriented parallel to each other in a fixed structure. Pertinent features of chip 412 are described herein, and only some features of chip 414 are described herein. It will be understood that chip 414 may be structured similarly to chip 412 in some embodiments, but need not be.

[0027] Chip 412 includes a lightly doped P- substrate 416 on which all features are formed. As used herein, no distinction is made between the formation of features "in" or "on" a substrate,

and both terms are used interchangeably herein. The chip 412, which is only about 50 microns thick in the illustrated embodiment, includes an NMOS transistor 418 and a PMOS transistor 420. The NMOS transistor 418 includes two N+ diffusions 422 and 424 separated laterally by a channel region 426. A gate stack 428 is formed above the channel region 426. The PMOS transistor 420 is formed within an N-well diffusion 430, and includes two P+ diffusions 432 and 434 separated laterally by a channel region 436. A gate stack 438 is formed above the channel region 436. The chip also includes a heavily doped N+ contact pad 435 formed in N-well 430, as well as a heavily doped P+ contact pad 425 formed directly in the P- substrate 416.

[0028] In the illustration of Fig. 4 the chip 412 also includes two through-silicon vias (TSVs) 440 and 442. These vias extend entirely through the chip 416, from the topside surface 444 through the backside surface 446. As used herein, a "topside" surface and a "backside" surface are the two opposite major surfaces of the chip, and it will be understood that if the chip is turned upside down, the surface labeled the topside surface remains the topside surface and the surface labeled the backside surface remains the backside surface. In addition, the terms topside and backside also indicate directions relative to the wafer. That is, a layer said to be located "on the backside" of a wafer need not necessarily be disposed immediately adjacent to the backside surface, so long as it is disposed beyond the backside surface, in a direction away from the wafer body. For example, in the illustration of Fig. 4 both the oxide layer 458 and the RDL conductor 464 each can be described as being "on the backside" of the wafer, and the RDL conductor 464 also can be described as being "on the backside" of the oxide layer 458.

[0029] The TSVs 440 and 442 in Fig. 4 are filled with an electrically conductive material such as copper or TiW to form conductors 450 and 451 respectively, and lined with an insulating material such as SiO2 448 to isolate the conductors from the substrate. The topside surface 444 of the substrate 416, and above the gate stacks 428, 438, there is formed a dielectric layer 452, made for example of an oxide. Vias (holes) are formed in the dielectric layer 452. The vias are filled with a conductive material 454, such as aluminum, and first metal layer M1 conductors are formed on top. Note that whereas the illustration of Fig. 4 shows only one metal layer M1, it will be appreciated that a typical chip may also have several more metal layers formed above M1, each isolated from the below-adjacent layer by a dielectric similar to dielectric layer 452.

[0030] It can be seen in Fig. 4 that one of the M1 conductive segments is electrically connected to the topside end of the TSV conductor 451 through via 454C. Another one of the M1 conductive segments 456 electrically connect the substrate topside end of the TSV conductor 450 to the P+ contact pad 425, through respective vias 454A and 454B. In another embodiment, the

connection of the substrate topside end of the TSV conductor 450 to the P+ contact pad 425 can be made in a different metal layer instead, or in some embodiments through a conductive path traversing more than one layer of metal.

[0031] On the backside surface 446 the chip 412 includes a dielectric layer 458 (such as an oxide), and on the backside of the dielectric layer 458 are RDL (redistribution layer) conductors for routing power and signals to desired lateral positions for making contact with a below-adjacent chip. One RDL conductor 464 is shown, it being understood that typically there are many more in addition. RDL 464 is connected to the backside-end of TSV conductor 451 through conductive material in a via 462 passing through the dielectric layer 458. As is typical, the conductive material in via 462 is considerably narrower than the conductor 451 in TSV 442, and at the backside surface 446 it makes electrical contact only with the conductor 451.

[0032] It can also be seen in Fig. 4 that no RDL conductor is connected to the backside end of TSV conductor 450. Instead, via 460 is offset relative to the TSV 440 such that the conductive material 466 inside it makes electrical contact with both the backside end of TSV conductor 450 and the backside surface 446 of the substrate 416 itself. Because of this connection, as well as the connection on the topside of substrate 416 through metal layer conductive segment 456, it can be seen that in the structure of Fig. 4 the P+ contact pad 425 on the topside surface 444 is connected to the backside surface 446 of the substrate 416, thereby bypassing the substrate resistance Rs with a low resistance path and effectively suppressing lockup conditions. More particularly, the TSV conductor 450 has a topside end connected to a point on the substrate 416 topside surface 444, and has a backside end connected to a point on the substrate 416 backside surface 446.

[0033] The TSV conductor 450 topside end is actually connected to an entire surface region 427 on the substrate 416 topside surface 444, but as used herein, that does not alter the fact that it is connected to at least one point. Similarly, the TSV conductor backside end is actually connected to an entire surface region 467 on the substrate 416 backside surface 446, but as used herein, that does not alter the fact that it is connected to at least one such point. Also, whereas the portion of chip 412 illustrated in Fig. 4 shows only one TSV conductor 450 that is connected in this way, it will be appreciated that preferably a chip would contain numerous such conductors, spread throughout the lateral area of the chip.

[0034] The chip 414 of Fig. 4, as mentioned, is below-adjacent to the chip 412 in the 3D IC 410. Chip 414 includes upper layer conductors 468 which are connected to circuit or device features below through vias in various dielectric layers. The upper layer conductors 468 are connected to

circuitry on the above-adjacent chip 412 by bump contacts such as 470. An electrically conductive path is formed from a device feature (not shown) on chip 414 to a device feature on chip 412 by conductors passing through vias on the topside of the substrate 472 of chip 414 and routed along various metal layers, through bump contacts such as 470, along RDL conductive segments such as 464 on the backside of the above-adjacent chip 412, through vias such as 462 and TSV conductors such as 451 to the topside of chip 412, and then through conductors passing through vias on the topside of the substrate 416 and routed along metal layers to the device feature on the chip 412.

[0035] Below-adjacent chip 414 is mechanically attached to the chip 412 by any of a variety of mechanisms, such as by dielectric adhesive, or by a separate scaffolding structure, or even by the mechanical and adhesive properties of the bump contacts 470. Other mechanisms will be apparent to the reader.

[0036] The TSV conductor 450 is not connected to any (insulated from all) conductors and device features on the below-adjacent chip 414. Preferably but not essentially, this is accomplished by not connecting the backside end of TSV conductor 450 to any RDL conductive segment (insulating the backside end of TSV conductor 450 from all RDL conductive segments). In the embodiment of Fig. 4, connection to any RDL conductive segment is avoided by not completely filling the via 460 with the conductive material 466. The remaining depth of via 460 may be filled with a dielectric, or with passivation material, or air. In other embodiments the conductive material 466 may fill via 460, in the same way as does the conductive material in via 462, but any RDL material is simply etched in such a pattern that avoids the lateral position of TSV 460. Many other mechanisms will be apparent to the reader for insulating TSV conductor 450 from any device feature on the below-adjacent chip 414.

[0037] Fig. 5 (consisting of Figs. 5A through 5I) illustrates an example process flow that can be used to fabricate a 3D integrated circuit such as 410. It will be understood that many of the steps can be combined, performed partially or completely simultaneously with other steps, or performed in a different sequence without deviating from the invention. In some cases, as the reader will appreciate, a re-arrangement of steps will achieve the same results only if certain other changes are made as well. In other cases, as the reader will appreciate, a re-arrangement of steps will achieve the same results only if certain conditions are satisfied. Furthermore, it will be appreciated that the fabrication flow described herein mentions only steps that are pertinent to an understanding of the invention, and it will be understood that numerous additional fabrication steps, well known to the reader, may be needed to develop a working device.

[0038] Referring to Fig. 5A, initially, a lightly doped P-type wafer including substrate 416 is provided. This wafer may be, for example, on the order of 500 microns thick. Wafers typically are manufactured with the light P-type doping throughout, and arrive that way to the chip maker. After devices and interconnects are formed on a wafer the wafer is usually sliced ("diced") into individual dies, or chips. As used herein, the terms wafer and substrate are similar except that whereas "wafer" refers to the entire slice provided to the fab, "substrate" need not. "Substrate" applies equally well to an entire wafer or to a chip cut from the wafer.

[0039] Next, referring to Fig. 5B, N-well 430 is formed by known techniques such as ion implantation or dopant diffusion. Note that though the diffusion regions shown in the drawings are referred to herein as "diffusion" regions, it will be understood that this is only for convenience and that in many embodiments they may actually be formed by other methods such as ion implantation.

[0040] After the N-well 430 is formed, the gate stacks 428 and 438 are formed by known techniques. Known self-aligned techniques are then used to form the N+ diffusions 422 and 424 for NMOS transistor 418 and the P+ diffusions 432 and 434 for PMOS transistor 420. The contact pads 425 and 435 are also formed at this time. Next, trenches 540 and 542 are etched into the wafer, such as by forming and patterning a photoresist layer, and using the patterned photoresist as an etch mask for etching the trenches. The photoresist can then be removed by, for example, a plasma etch. The trenches 540 and 542 extend more than about 50 microns in depth, but do not pass through the entire substrate 416.

[0041] Next, the insulating material 448 is formed inside the trenches 540 and 542 and lining the walls thereof. For example, SiO2 or another dielectric can be grown or deposited over the trench sidewalls. Other insulating materials can be used as well, as can a combination of materials which together act as an insulator or dielectric.

[0042] Referring to Fig. 5C, the TSV trenches 540 and 542 are filled with a conductive material such as copper, to form TSV conductors 450 and 451. This step can be accomplished for example by depositing a thin film seed metal layer on the inside surfaces of the trench sidewall material, and applying the conductive material by electroplating. Next, oxide layer 452 is formed by oxidation and vias such as 554 are etched in the oxide by applying and patterning a photoresist, then etching the oxide through exposed regions of the photoresist.

[0043] Referring to Fig. 5D, the vias 554 are then filled for example with aluminum, to thereby form conductors 454A, 454B, as well as other conductors 454. The M1 metal layer is then applied above the dielectric layer 452 and patterned to form metal interconnects including

conductive segment 456. Conductive segment 456 completes the connection of the topside end of TSV conductor 450 to the topside surface of the substrate 416 at the contact pad 425. Other dielectric and conductive layers (not shown) are formed above the M1 layer.

[0044] Referring to Fig. 5E, after all the topside processing is complete, the wafer is ground from the backside until its thickness is reduced sufficiently to expose the backside ends of TSV conductors 450 and 451. The wafer is then inverted and backside processing begins. Referring to Fig. 5F, a dielectric layer such as oxide 458 is grown on the entire backside surface 446 of the substrate 416. Referring to Fig. 5G, vias 460 and 460 are formed in the oxide 458 by etching the oxide through a patterned photoresist. The via 462 is much narrower than the diameter of TSV 542, and is roughly centered laterally across the backside end of TSV conductor 451. The via 460, on the other hand, is either wider or laterally offset from the center of the backside end of TSV 540, or both, so that it exposes both the backside end of TSV conductor 450 and the region 467 on the backside surface 446 of the substrate 416. If desired to improve the connectivity to the substrate 416 backside surface, at this time an additional P+ contact pad (not shown) can be formed in the substrate 416 at region 467 by ion implantation through the backside vias. As used herein, an insulator such as 458 is said to have an opening "exposing" a region even though the opening might be filled with another material, such as a conductor. The term does not necessarily mean that the "exposed" region is visible through the opening. The term indicates that the "exposed" region is exposed at least so far as the insulator is concerned.

[0045] Referring to Fig. 5H, a metal layer is applied to the backside of the dielectric layer 458, which also fills the vias 460 and 462. This metal may be the same as that used to fill the TSVs 540 and 542. The metal 466 in via 460 connects to both the backside end of TSV conductor 450 and the region 467 on the backside surface 446 of the substrate 416. A conductive path is thereby completed from the contact pad 425 on the topside surface 444 of the substrate 416, through the TSV conductor 450, to the backside surface 446 of the substrate 416. The metal layer is then etched back so that it only partially fills via 460, as shown in the figure. A patterned photoresist mask is used to protect the metal in via 462 from this etch-back. An additional dielectric or passivation layer (not shown) is then formed in the via 460 to protect the metal 466 and to insulate it from contact with any other conductor on the chip 412 or on the below-adjacent chip 414. Referring to Fig. 5I, a metallization layer is then formed on the backside of dielectric layer 458 and patterned to form the RDL conductors 464. The metal used for the RDL conductors again may be the same as that used to fill the TSVs 540 and 542. As shown in Fig. 4I the RDL conductors connect to TSV conductor 451 (through via 462) but do not connect to (remain

insulated from) TSV conductor 450. Additional RDL levels (not shown) may also be formed on the backside of the substrate 416 in various embodiments. The below-adjacent chip 414 is then attached as illustrated in Fig. 4.

[0046] Note that alternative embodiments exist in which some or all of the chips in a three-dimensional chip stack do not use RDL conductors at all. Such embodiments can still include TSV conductors like 450 solely for the purpose of the back-tie to the substrate 416 backside as described herein.

Overall Design Process Flow

[0047] Fig. 6 shows a simplified representation of an illustrative digital integrated circuit design flow, applicable for each of the chips 412 and 414 in the 3DIC. At a high level, the process starts with the product idea (step 600) and is realized in an EDA (Electronic Design Automation) software design process (step 610). When the design is finalized, it can be taped-out (step 627). At some point after tape out, the fabrication process (step 650) and packaging and assembly processes (step 660) occur resulting, ultimately, in finished integrated circuit chips (result 670).

[0048] The EDA software design process (step 610) is itself composed of a number of steps 612 -630, shown in linear fashion for simplicity. In an actual integrated circuit design process, the particular design might have to go back through steps until certain tests are passed. Similarly, in any actual design process, these steps may occur in different orders and combinations. This description is therefore provided by way of context and general explanation rather than as a specific, or recommended, design flow for a particular integrated circuit.

[0049] A brief description of the component steps of the EDA software design process (step 610) will now be provided.

[0050] System design (step 612): The designers describe the functionality that they want to implement, they can perform what-if planning to refine functionality, check costs, etc. Hardware-software architecture partitioning can occur at this stage. Example EDA software products from Synopsys, Inc. that can be used at this step include Model Architect, Saber, System Studio, and DesignWare® products.

[0051] Logic design and functional verification (step 614): At this stage, the VHDL or Verilog code for modules in the system is written and the design is checked for functional accuracy. More specifically, the design is checked to ensure that it produces correct outputs in response to

particular input stimuli. Example EDA software products from Synopsys, Inc. that can be used at this step include VCS, VERA, DesignWare®, Magellan, Formality, ESP and LEDA products.

[0052] Synthesis and design for test (step 616): Here, the VHDL/Verilog is translated to a netlist. The netlist can be optimized for the target technology. Additionally, the design and implementation of tests to permit checking of the finished chip occurs. Example EDA software products from Synopsys, Inc. that can be used at this step include Design Compiler®, Physical Compiler, DFT Compiler, Power Compiler, FPGA Compiler, TetraMAX, and DesignWare® products.

[0053] Netlist verification (step 618): At this step, the netlist is checked for compliance with timing constraints and for correspondence with the VHDL/Verilog source code. Example EDA software products from Synopsys, Inc. that can be used at this step include Formality, PrimeTime, and VCS products.

[0054] Design planning (step 620): Here, an overall floor plan for the chip is constructed and analyzed for timing and top-level routing. Example EDA software products from Synopsys, Inc. that can be used at this step include Astro and Custom Designer products.

[0055] Physical implementation (step 622): The placement (positioning of circuit elements) and routing (connection of the same) occurs at this step, as can selection of library cells to perform specified logic functions. Example EDA software products from Synopsys, Inc. that can be used at this step include the Astro, IC Compiler, and Custom Designer products. The TSVs such as 450 can be defined in this step or in step 620 in various embodiments.

[0056] Analysis and extraction (step 624): At this step, the circuit function is verified at a transistor level, this in turn permits what-if refinement. Example EDA software products from Synopsys, Inc. that can be used at this step include AstroRail, PrimeRail, PrimeTime, and Star-RCXT products.

[0057] Physical verification (step 626): At this step various checking functions are performed to ensure correctness for: manufacturing, electrical issues, lithographic issues, and circuitry. Example EDA software products from Synopsys, Inc. that can be used at this step include the Hercules product.

[0058] Tape-out (step 627): This step provides the “tape-out” data to be used (after lithographic enhancements are applied if appropriate) for production of masks for lithographic use to produce finished chips. Example EDA software products from Synopsys, Inc. that can be used at this step include the IC Compiler and Custom Designer families of products.

[0059] Resolution enhancement (step 628): This step involves geometric manipulations of the layout to improve manufacturability of the design. Example EDA software products from Synopsys, Inc. that can be used at this step include Proteus, ProteusAF, and PSMGen products.

[0060] Mask data preparation (step 630): This step provides mask-making-ready "tape-out" data for production of masks for lithographic use to produce finished chips. Example EDA software products from Synopsys, Inc. that can be used at this step include the CATS(R) family of products.

[0061] In the layout process performed in steps 620 and 622, the locations of all the TSVs typically are defined before other cells are placed. TSVs 540 in one embodiment are placed in a regular pattern across the chip. In another embodiment, TSVs 540 are placed close to the N+ and P+ regions of I/O areas, rather than those of core areas. In either case the placement may be performed automatically by a computer system under the control of place-and-route software.

[0062] The layout defines a number of masks for the fabrication process. Among these masks is a TSV layer mask, which identifies the lateral size, shape and position of each of the TSVs. This mask is used to pattern a photoresist on the substrate topside surface, with openings through which the TSV trenches will be etched. The layout also defines several metal layer masks, each used to pattern a respective one of the metal interconnect layers. It is in the layout for one of these masks that an interconnect is defined for electrically connecting the topside end of TSV conductor 450 to the heavily doped P+ contact pad 425. The layout also defines a mask to pattern the vias 460 and 462 in the backside dielectric 458. It is in the layout for this mask that the via 460 is defined such that it is either wider or laterally offset from the center of the backside end of TSV 540, or both, so that it exposes both the backside end of TSV conductor 450 and the region 467 on the backside surface 446 of the substrate 416. The layout also defines a mask to pattern a photoresist for etching back the metal 446 deposited in via 460 while protecting the metal in via 462 from this etch-back.

[0063] Thus among other things, the layout identifies mask features (e.g. the locations of the photoresist openings) for etching a TSV 540 which, after electroplating and thinning, will form a TSV conductor 450 extending entirely through the chip. It also identifies mask features (e.g. the location of interconnect 456) for forming a conductive path electrically connecting the topside end of the TSV conductor 450 to P+ contact pad 425 on topside surface of the chip, as well as mask features (e.g. the size, shape and position of via 460 in the backside dielectric 458) for electrically interconnecting the backside end of the TSV conductor 450 to region 467 on the

backside surface 446 of the chip. The layout of course also defines many other masks for fabrication of the chip 412.

Computer System

[0064] Fig. 7 is a simplified block diagram of a computer system 710 that can be used to implement software incorporating aspects of the present invention. In particular, the layout process described above is implemented using such a computer system, under control of layout software. The software implementing the layout process and the other process steps identified in Fig. 6 causes the computer system 710 to operate in the specified manner.

[0065] Computer system 710 typically includes a processor subsystem 714 which communicates with a number of peripheral devices via bus subsystem 712. These peripheral devices may include a storage subsystem 724, comprising a memory subsystem 726 and a file storage subsystem 728, user interface input devices 722, user interface output devices 720, and a network interface subsystem 716. The input and output devices allow user interaction with computer system 710. Network interface subsystem 716 provides an interface to outside networks, including an interface to communication network 718, and is coupled via communication network 718 to corresponding interface devices in other computer systems. Communication network 718 may comprise many interconnected computer systems and communication links. These communication links may be wireline links, optical links, wireless links, or any other mechanisms for communication of information, but typically it is an IP-based communication network. While in one embodiment, communication network 718 is the Internet, in other embodiments, communication network 718 may be any suitable computer network.

[0066] The physical hardware component of network interfaces are sometimes referred to as network interface cards (NICs), although they need not be in the form of cards: for instance they could be in the form of integrated circuits (ICs) and connectors fitted directly onto a motherboard, or in the form of macrocells fabricated on a single integrated circuit chip with other components of the computer system.

[0067] User interface input devices 722 may include a keyboard, pointing devices such as a mouse, trackball, touchpad, or graphics tablet, a scanner, a touch screen incorporated into the display, audio input devices such as voice recognition systems, microphones, and other types of input devices. In general, use of the term "input device" is intended to include all possible types

of devices and ways to input information into computer system 710 or onto computer network 718.

[0068] User interface output devices 720 may include a display subsystem, a printer, a fax machine, or non visual displays such as audio output devices. The display subsystem may include a cathode ray tube (CRT), a flat panel device such as a liquid crystal display (LCD), a projection device, or some other mechanism for creating a visible image. The display subsystem may also provide non visual display such as via audio output devices. In general, use of the term "output device" is intended to include all possible types of devices and ways to output information from computer system 710 to the user or to another machine or computer system.

[0069] Storage subsystem 724 stores the basic programming and data constructs that provide the functionality of certain embodiments of the present invention. For example, the various modules implementing the functionality of certain embodiments of the invention may be stored in storage subsystem 724. These software modules are generally executed by processor subsystem 714.

[0070] Memory subsystem 726 typically includes a number of memories including a main random access memory (RAM) 730 for storage of instructions and data during program execution and a read only memory (ROM) 732 in which fixed instructions are stored. File storage subsystem 728 provides persistent storage for program and data files, and may include a hard disk drive, a floppy disk drive along with associated removable media, a CD ROM drive, an optical drive, or removable media cartridges. The databases and modules implementing the functionality of certain embodiments of the invention may have been provided on a computer readable medium such as one or more CD-ROMs, and may be stored by file storage subsystem 728. The host memory 726 contains, among other things, computer instructions which, when executed by the processor subsystem 714, cause the computer system to operate or perform functions as described herein. As used herein, processes and software that are said to run in or on "the host" or "the computer", execute on the processor subsystem 714 in response to computer instructions and data in the host memory subsystem 726 including any other local or remote storage for such instructions and data.

[0071] Bus subsystem 712 provides a mechanism for letting the various components and subsystems of computer system 710 communicate with each other as intended. Although bus subsystem 712 is shown schematically as a single bus, alternative embodiments of the bus subsystem may use multiple busses.

[0072] Computer system 710 itself can be of varying types including a personal computer, a portable computer, a workstation, a computer terminal, a network computer, a television, a

mainframe, a server farm, or any other data processing system or user device. Due to the ever changing nature of computers and networks, the description of computer system 710 depicted in Fig. 7 is intended only as a specific example for purposes of illustrating the preferred embodiments of the present invention. Many other configurations of computer system 710 are possible having more or less components than the computer system depicted in Fig. 7.

[0073] As used herein, the "identification" of an item of information does not necessarily require the direct specification of that item of information. Information can be "identified" in a field by simply *referring* to the actual information through one or more layers of indirection, or by identifying one or more items of different information which are together sufficient to determine the actual item of information. In addition, the term "indicate" is used herein to mean the same as "identify".

[0074] The following references are incorporated herein for their teachings: U.S. Patent Pre-grant Publication Nos. 2010-0244179 and 2011-0195546, and U.S. Patent Nos. 5,428,247, 7,262,109, 7,691,748 and 7,956,442.

[0075] The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that aspects of the present invention may consist of any such feature or combination of features. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

[0076] The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. For example, whereas "TSV early" processing is described above with respect to Fig. 5, other embodiments can use other variants such as "TSV first" processing. Also, in some embodiments, the contact to the backside surface can be connected for example to the ground of the below-adjacent chip through an RDL routing conductor. In particular, and without limitation, any and all variations described, suggested or incorporated by reference in this patent application are specifically incorporated by reference into the description herein of embodiments of the invention. In addition, any and all variations

described, suggested or incorporated by reference herein with respect to any one embodiment are also to be considered taught with respect to all other embodiments. The embodiments described herein were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

[0077] What is claimed is:

CLAIMS

1. An integrated circuit device comprising:

a first semiconductor substrate having opposite topside and backside surfaces; and

a first conductor extending entirely through the first substrate, the first conductor being electrically connected on a first end to a first point on the first substrate topside surface and on a second end to a second point on the first substrate backside surface.

2. A device according to claim 1, wherein the first substrate comprises a p-type lightly doped substrate and a p-type heavily doped contact pad at the first substrate topside surface,

wherein the first point is on the p-type heavily doped contact pad.

3. A device according to any preceding claim, further comprising:

an insulating layer on the backside surface of the first substrate, the insulating layer having an opening which exposes both the second end of the first conductor and a particular region of the first substrate on the backside thereof; and

a conductive material in the opening electrically connecting the second end of the first conductor with the particular region.

4. A device according to any preceding claim, further comprising:

an additional TSV passing through the first substrate;

an insulating layer on the backside surface of the first substrate; and

a plurality of RDL conductors on the backside of the insulating layer,

wherein the additional TSV is electrically connected to one of the RDL conductors through a via in the insulating layer, and

the first conductor is not connected to any RDL conductors on the backside of the first substrate.

5. A device according to any preceding claim, further comprising:

a further TSV passing through the first substrate; and

an additional integrated circuit chip located on the backside of the insulating layer,

wherein the further TSV is electrically connected to a conductor on the additional integrated circuit chip; and

the first conductor is insulated from all conductors on the additional integrated circuit chip.

6. A device according to any preceding claim, wherein the first conductor is insulated along its entire length from the first substrate.

7. A method for making an integrated circuit device, comprising the steps of:

providing a first semiconductor substrate having opposite topside and backside surfaces; and

forming a first conductor extending entirely through the first substrate, the first conductor being electrically connected on a first end to a first point on the first substrate topside surface and on a second end to a second point on the first substrate backside surface.

8. A method according to claim 7, wherein the step of forming a first conductor comprises the steps of:

forming an insulating layer on the backside surface of the first substrate;

opening a via which exposes both the second end of the first conductor and a particular region of the first substrate on the backside thereof; and

forming a conductive material in the via which electrically connects the second end of the first conductor with the particular region.

9. A method according to any of claims 7-8, further comprising the steps of:

forming an additional TSV passing through the first substrate;

forming a plurality of RDL conductors on the backside of the first substrate;

electrically connecting the additional TSV to one of the RDL conductors; and

insulating the first conductor from all RDL conductors on the backside of the first substrate.

10. A method according to any of claims 7-9, further comprising the steps of:

forming a further TSV passing through the first substrate; and

providing an additional semiconductor substrate located on the backside of the first semiconductor substrate,

electrically connecting the further TSV to a conductor on the additional substrate; and

insulating the first conductor from all conductors on the additional substrate.

11. A method according to any of claims 7-10, further comprising insulating the first conductor along its entire length from the first substrate.

12. A method for making an integrated circuit device, comprising the steps of:

providing a first semiconductor substrate having opposite topside and backside surfaces; and

forming a first conductor extending entirely through the first substrate, the first conductor being electrically connected on a first end to a first point on the first substrate topside surface; and

forming a plurality of RDL conductors on the backside of the insulating layer; and

insulating the first conductor from all RDL conductors on the backside of the first substrate.

13. A method according to claim 12, further comprising the step of:

forming an additional TSV passing through the first substrate; and

electrically connecting the additional TSV to one of the RDL conductors.

14. A method for making an integrated circuit device, comprising the steps of:

providing a first semiconductor substrate having opposite topside and backside surfaces;

forming a first conductor extending entirely through the first substrate;

electrically connecting a first end of the first conductor to a first point on the first substrate topside surface;

providing an additional integrated circuit chip on the backside of the first substrate; and

insulating the first conductor from all conductors on the additional integrated circuit chip.

15. A method according to claim 14, further comprising the steps of:

forming an additional TSV passing through the first substrate; and

electrically connecting the additional TSV to a conductor on the additional integrated circuit chip.

16. A three-dimensional integrated circuit comprising:

a plurality of integrated circuit chips stacked vertically in a fixed structure, the plurality of chips including a first chip having opposite topside and backside surfaces; and

a first conductor extending entirely through the first chip, the first conductor being electrically connected on a first end to a first point on the first chip topside surface and on a second end to a second point on the first chip backside surface.

17. A three-dimensional integrated circuit according to claim 16, wherein the first chip has no RDL conductors on the backside of the first chip.

18. An A three-dimensional integrated circuit comprising:

a plurality of integrated circuit chips stacked vertically in a fixed structure, the plurality of chips including a first chip having opposite topside and backside surfaces;

a first conductor extending entirely through the first chip, the first conductor being electrically connected on a first end to a first point on the first chip topside surface; and

a plurality of RDL conductors on the backside of the first chip;

wherein the first conductor is insulated from all RDL conductors on the backside of the first chip.

19. An A three-dimensional integrated circuit comprising:

a plurality of integrated circuit chips stacked vertically in a fixed structure, the plurality of chips including a first chip having opposite topside and backside surfaces and an additional chip stacked adjacent to the backside of the first chip; and

a first conductor extending entirely through the first chip, the first conductor being electrically connected on a first end to a first point on the first chip topside surface,

wherein the first conductor is insulated from all conductors on the additional chip.

20. A method for designing a three-dimensional integrated circuit, comprising the steps of:

using a computer system, developing a layout for a first chip of the three-dimensional integrated circuit in dependence upon a provided an integrated circuit design for the first chip, the first chip having opposite topside and backside surfaces; and

providing the layout for fabricating the first chip, wherein the layout identifies mask features for:

forming a first conductor extending entirely through the first chip; and

forming a conductive path electrically connecting a first end of the first conductor to a first point on the first chip topside surface and a second end of the first conductor to a second point on the first chip backside surface.

21. A non-transitory computer-readable storage medium storing instructions that, when executed by a processor, cause a computer system to perform a method for designing a three-dimensional integrated circuit, the method comprising:

defining a plurality of integrated circuit chips stacked vertically in a fixed structure, the plurality of integrated circuit chips including a first chip having opposite topside and backside surfaces; and defining a first conductor extending entirely through the first chip, the first conductor being electrically connected on a first end to a first point on the first chip topside surface and on a second end to a second point on the first chip backside surface.

22. An integrated circuit device comprising:

a first semiconductor substrate having opposite topside and backside surfaces;

a first conductor extending entirely through the first substrate, the first conductor being electrically connected on a first end to a first point on the first substrate topside surface;

a plurality of RDL conductors on the backside of the first substrate,

wherein the first conductor is insulated from all RDL conductors on the backside of the first substrate.

23. A device according to claim 22, further comprising:

an additional TSV passing through the first substrate,

wherein the additional TSV is electrically connected to one of the RDL conductors.

24. An integrated circuit device comprising:

a first semiconductor substrate having opposite topside and backside surfaces;

a first conductor extending entirely through the first substrate, the first conductor being electrically connected on a first end to a first point on the first substrate topside surface; and

an additional integrated circuit chip located on the backside of the first substrate,

wherein the first conductor is insulated from all conductors on the additional substrate.

25. A device according to claim 24, further comprising:

an additional TSV passing through the first substrate,

wherein the additional TSV is electrically connected to a conductor on the additional integrated circuit chip.

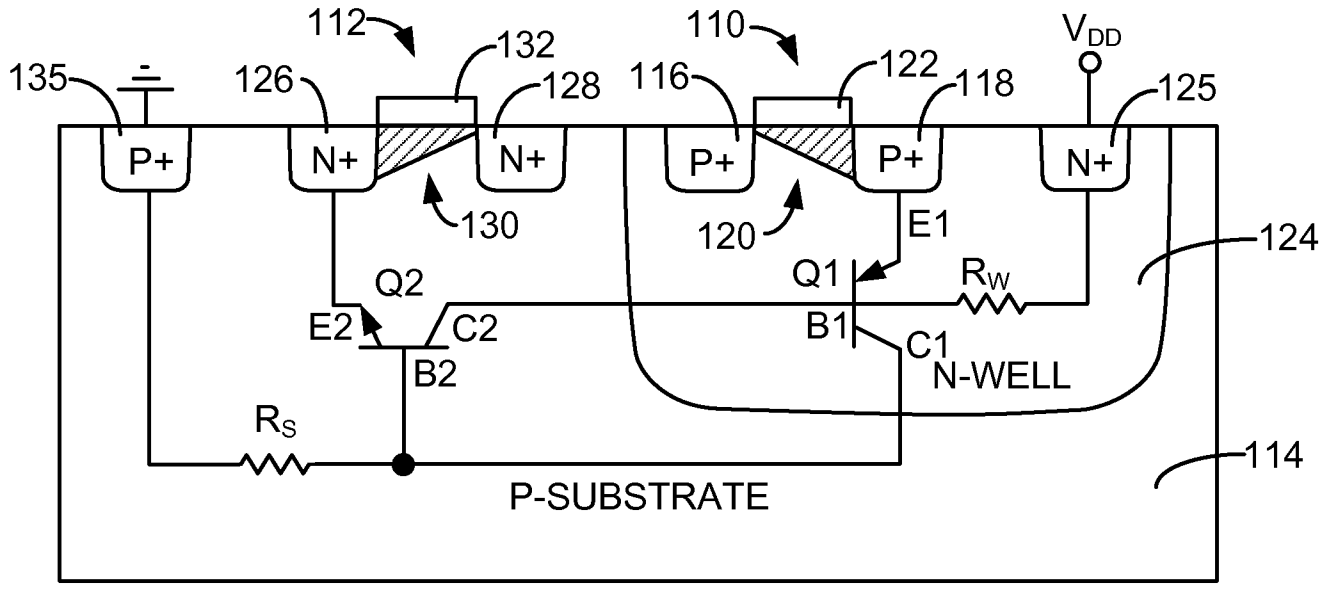


FIG. 1
(Prior Art)

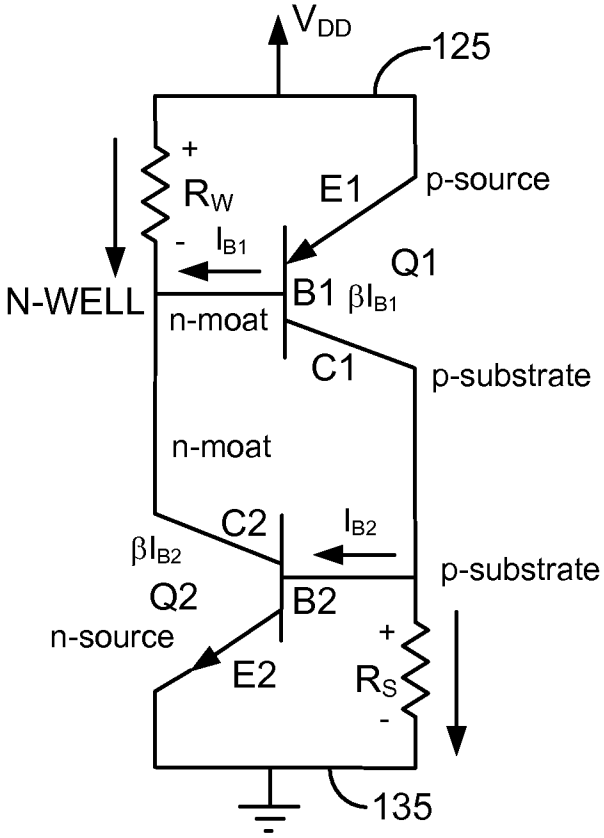


FIG. 2
(Prior Art)

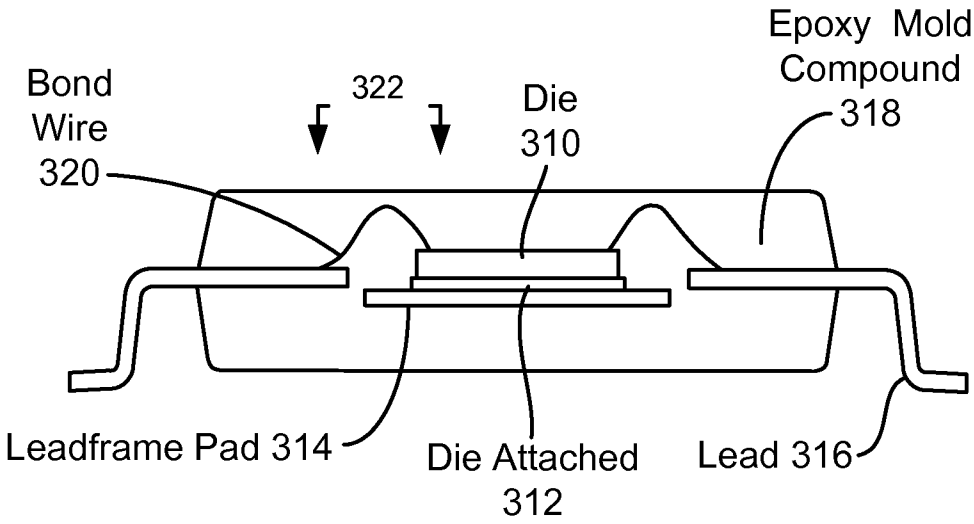


FIG. 3A
(Prior Art)

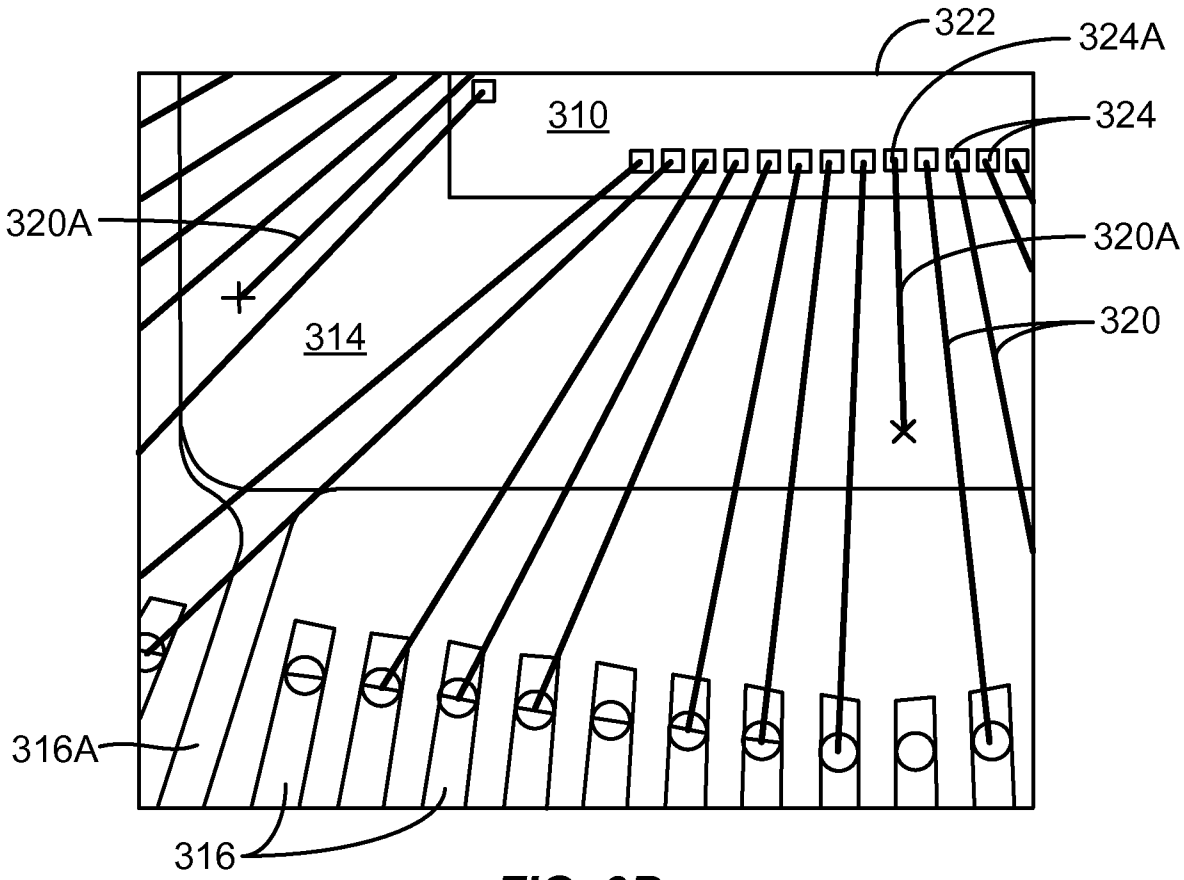
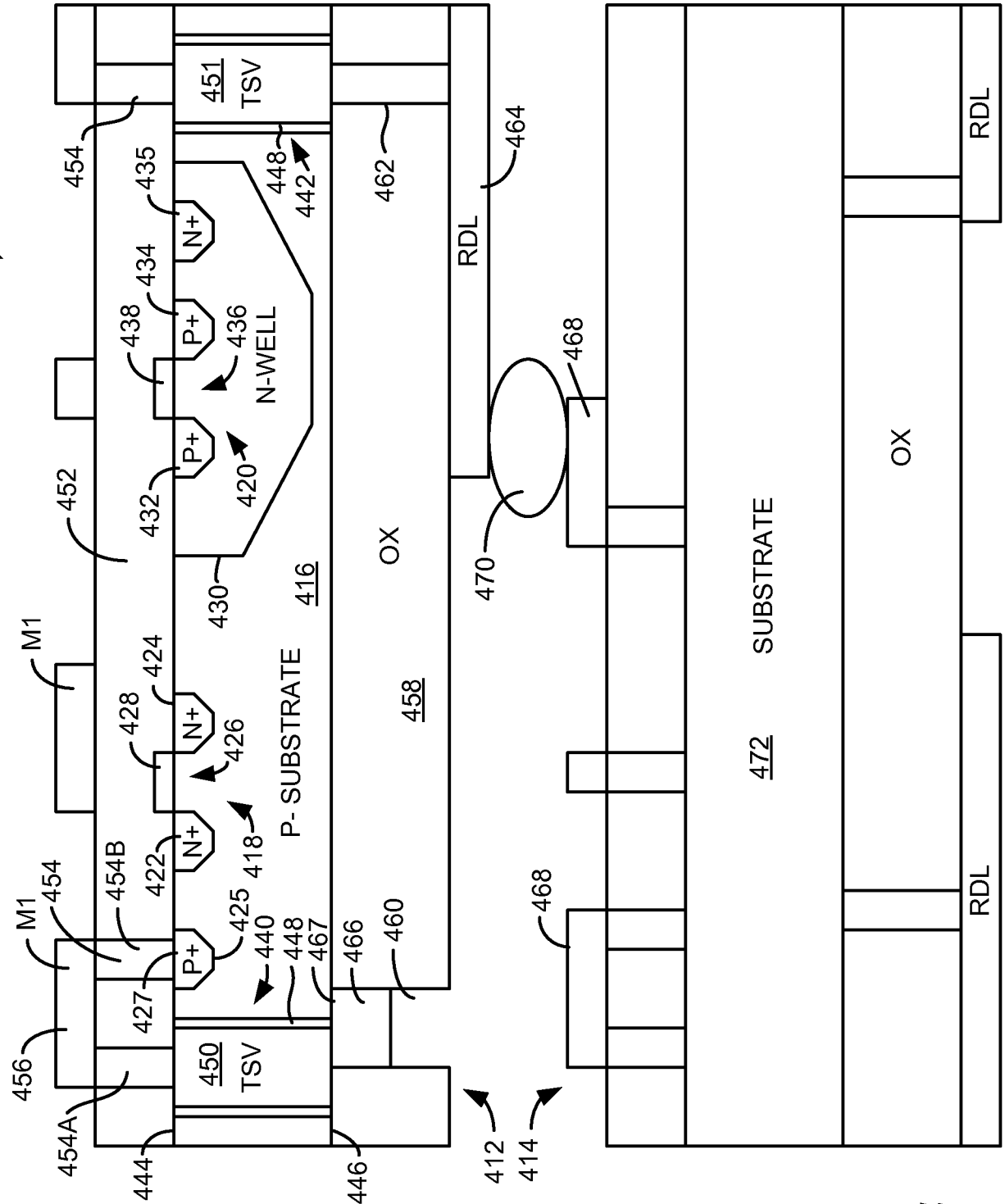


FIG. 3B
(Prior Art)


410
451
TSV
450
TSV
N+
P+
N-WELL
P- SUBSTRATE
416
458
OX
RDL
SUBSTRATE
472
M1
454
454A
454B
456
452
444
446
412
414
418
420
422
424
425
426
427
428
430
432
434
435
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466
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468
470

FIG. 4

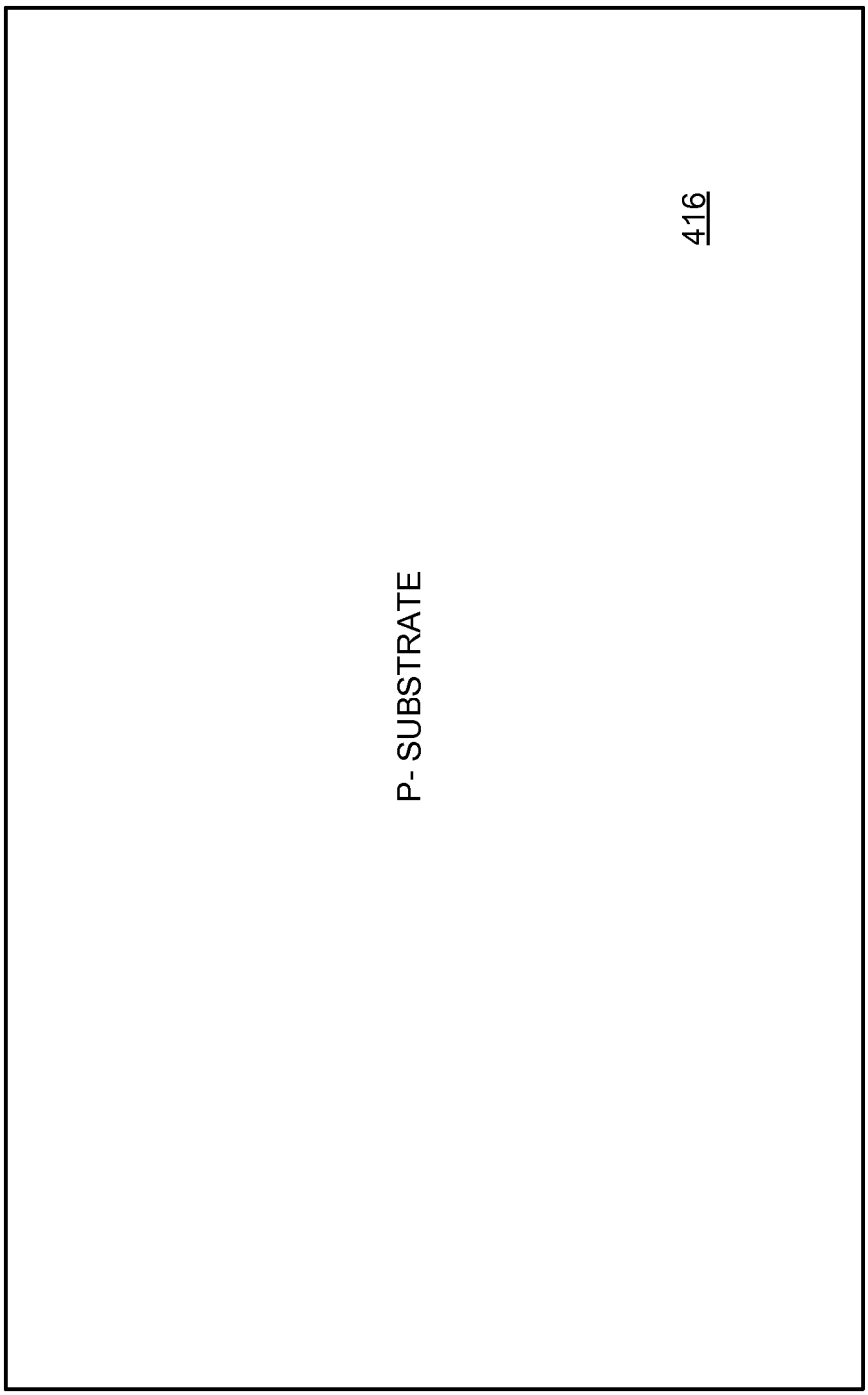
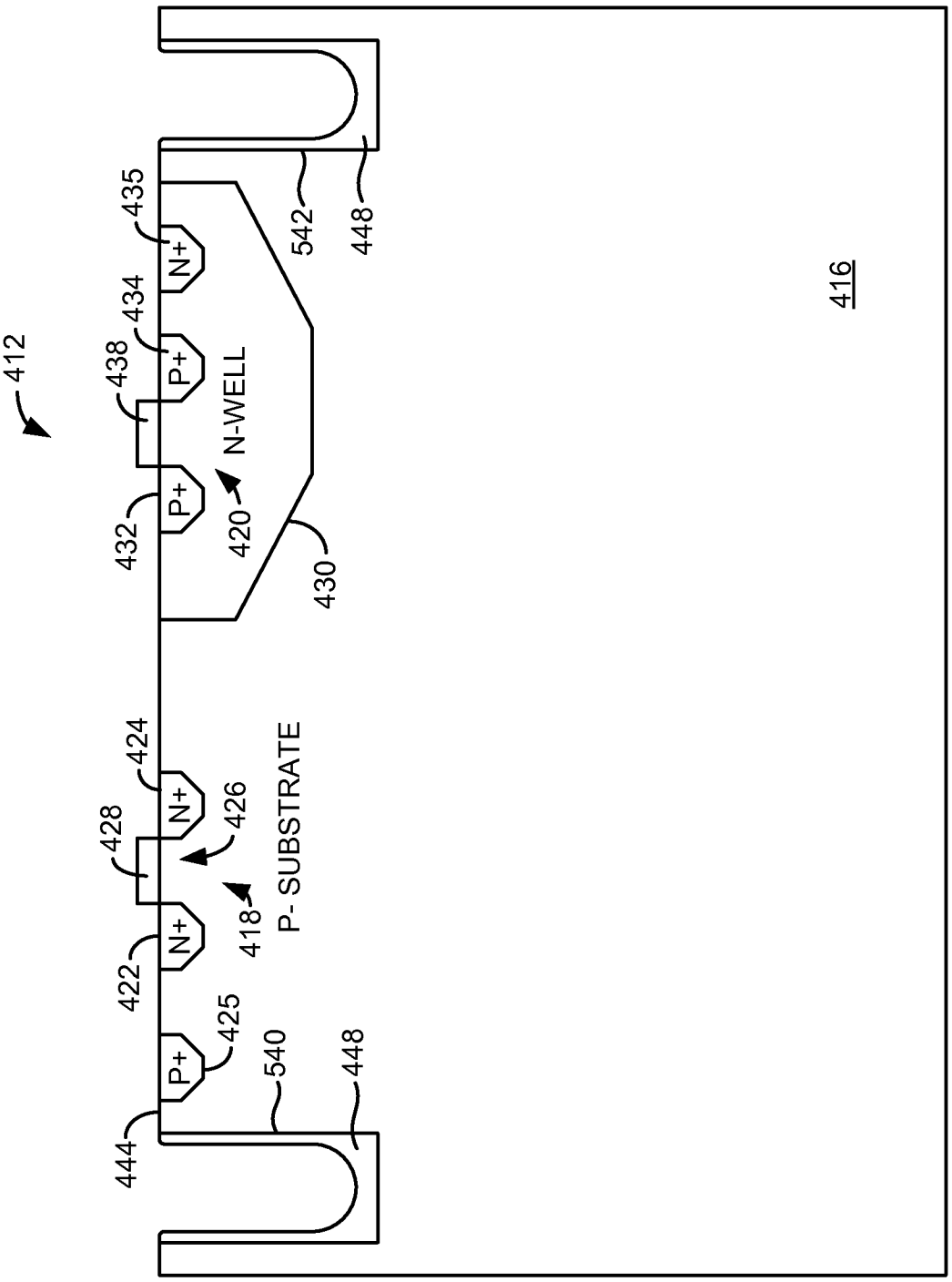


FIG. 5A


412
435
N+
434
P+
438
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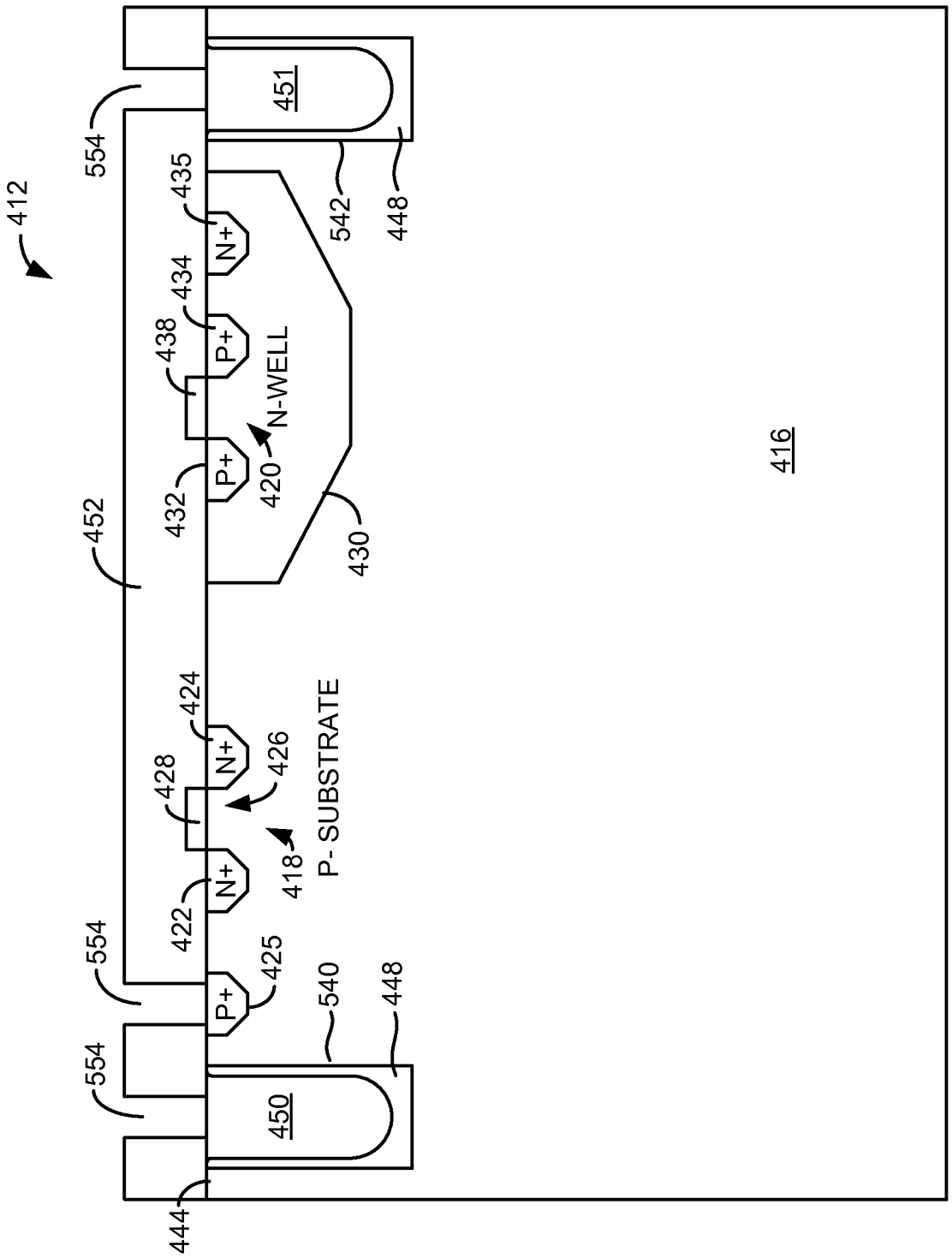
432
P+
420
430
542
448
416
424
N+
426
428
P- SUBSTRATE
418
N+
422
425
P+
540
448
444

FIG. 5B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554
451
435
N+
542
448
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P+
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420
P+
432
452
430
416
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N+
426
428
P- SUBSTRATE
418
N+
422
554
425
P+
540
448
554
450
444

FIG. 5C

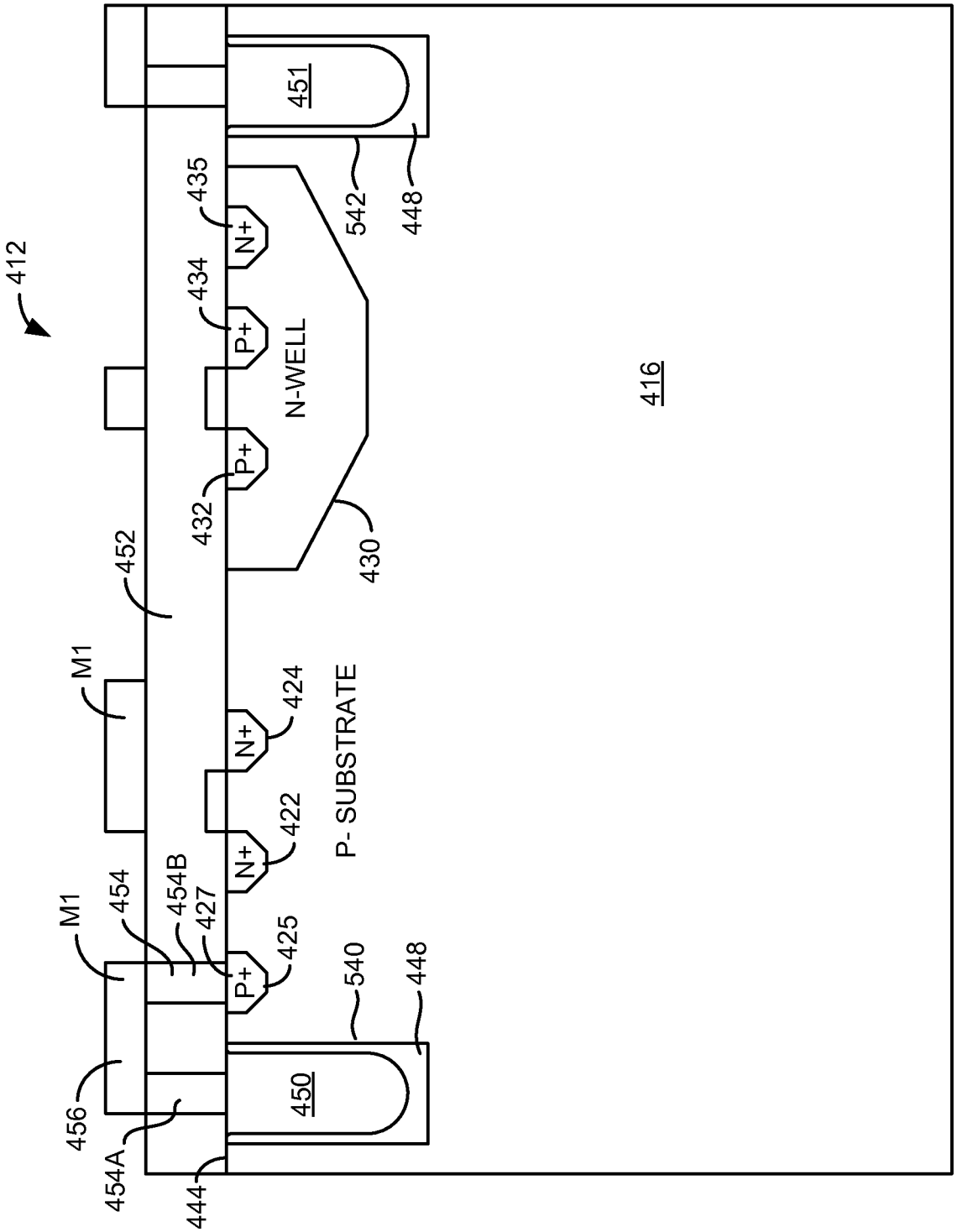

412
451
542
448
435
N+
434
P+
N-WELL
P+
432
430
416
452
M1
424
N+
P- SUBSTRATE
422
N+
M1
454
454B
427
425
P+
540
448
456
450
454A
444

FIG. 5D

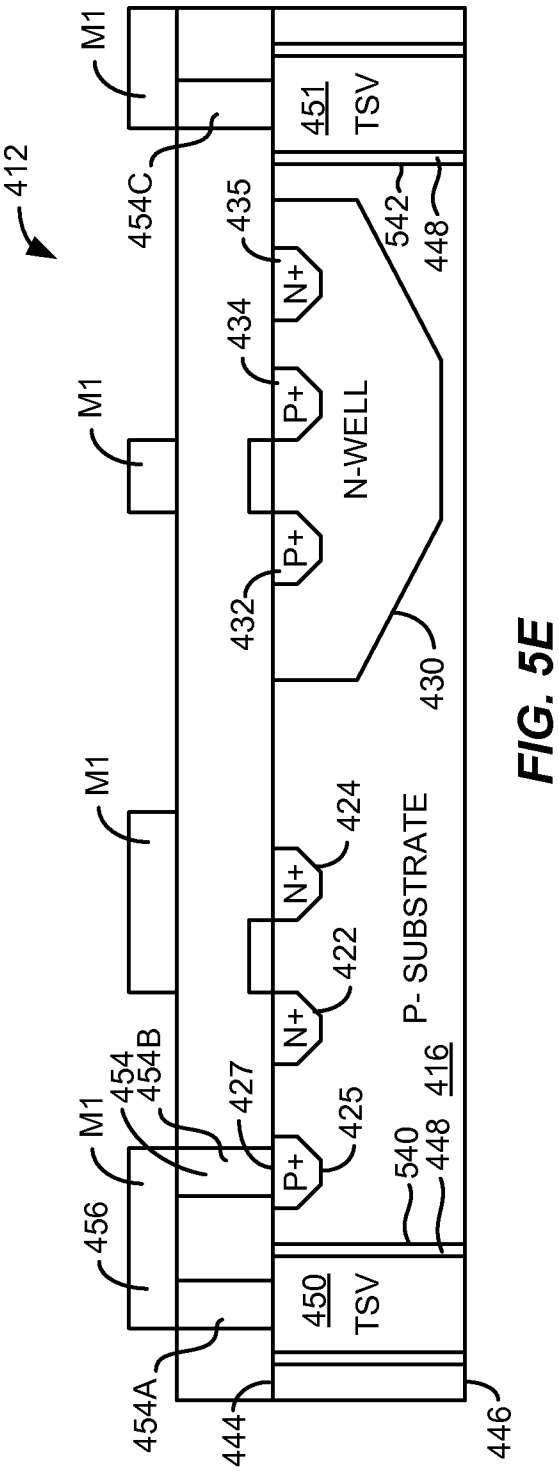

412
M1
454C
451
TSV
435
N+
542
448
434
P+
N-WELL
M1
432
P+
430
M1
424
N+
422
N+
P- SUBSTRATE
416
M1
454
454B
427
425
P+
540
448
456
450
TSV
454A
444
446

FIG. 5E

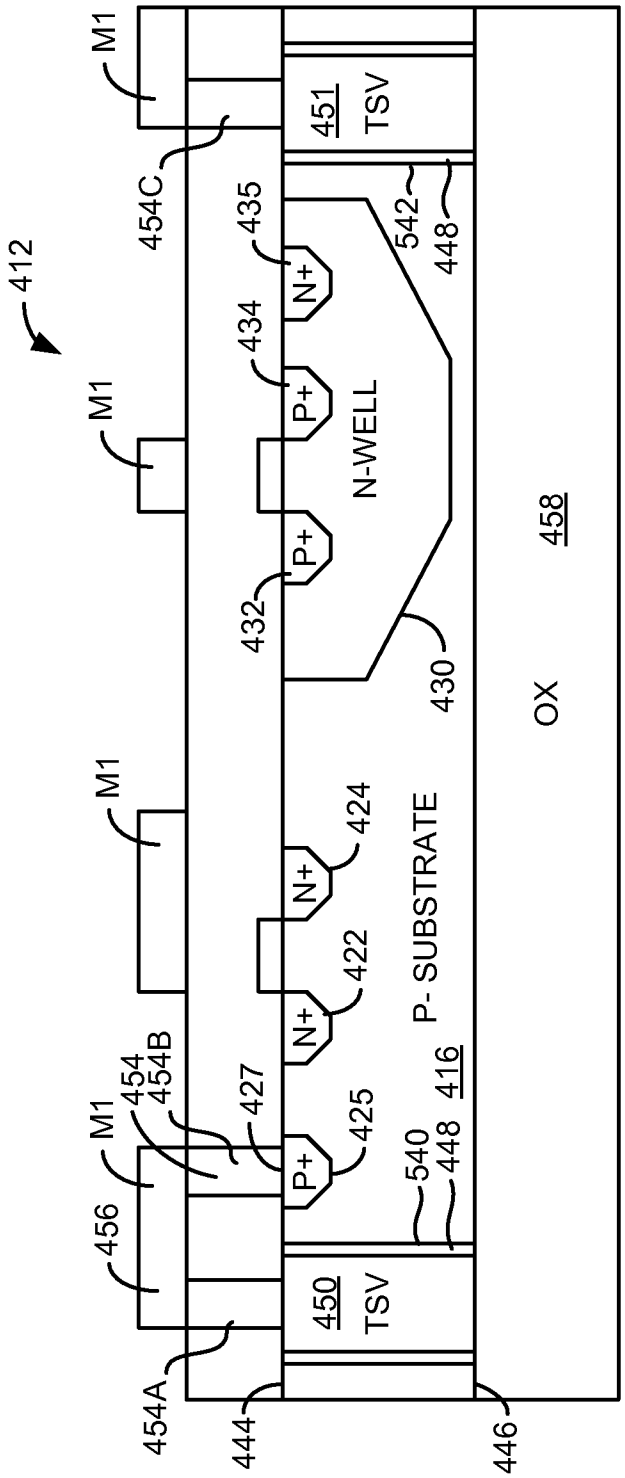

412
M1
454C
451
TSV
435
N+
542
448
434
P+
N-WELL
M1
432
P+
430
458
OX
M1
424
N+
422
N+
P- SUBSTRATE
416
M1
454
454B
427
425
P+
540
448
456
450
TSV
454A
444
446

FIG. 5F

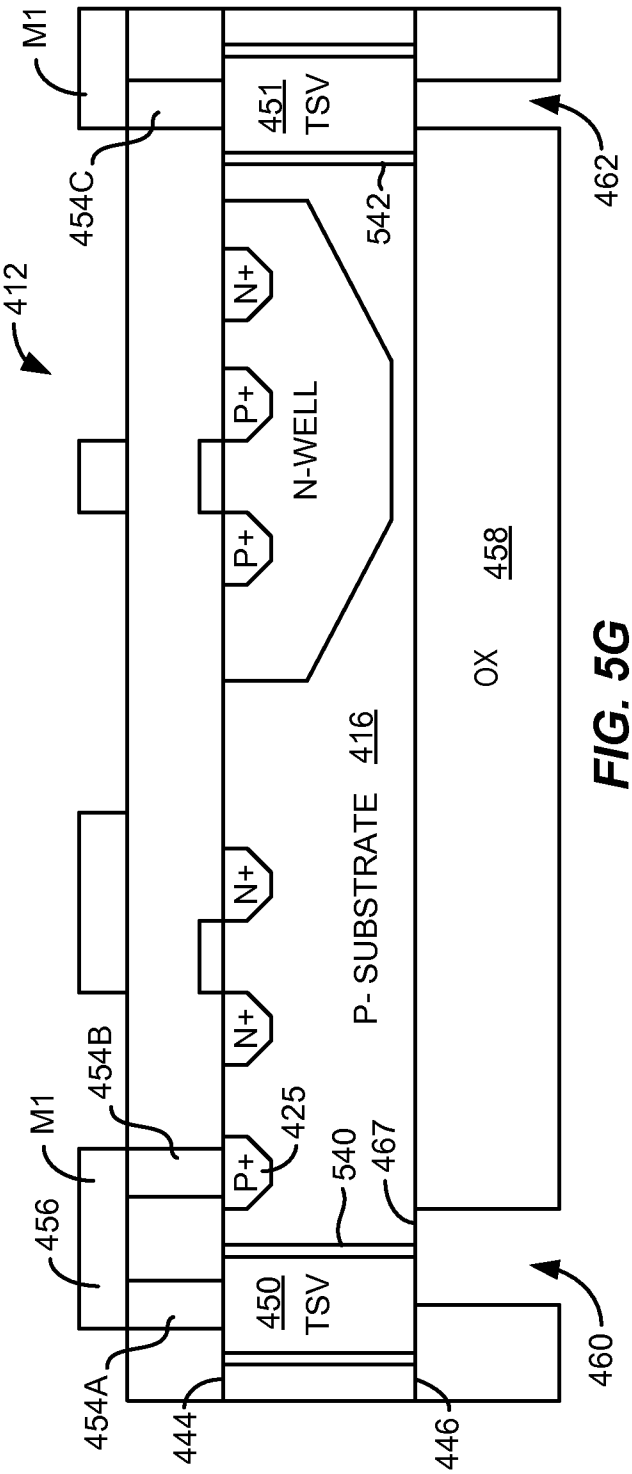

M1
454C
451
TSV
462
542
412
N+
P+
P+
N-WELL
N+
N+
P- SUBSTRATE 416
OX 458
M1
454B
456
425
540
467
P+
450
TSV
454A
444
446
460

FIG. 5G

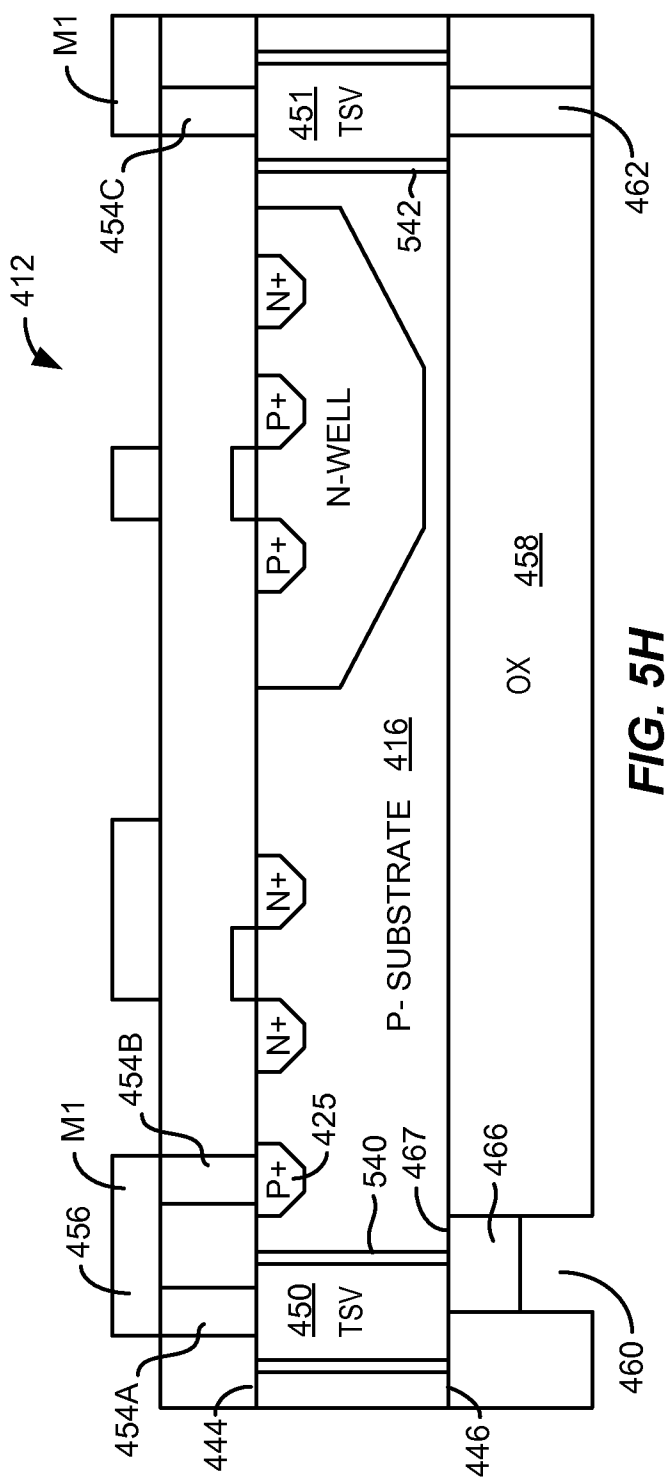
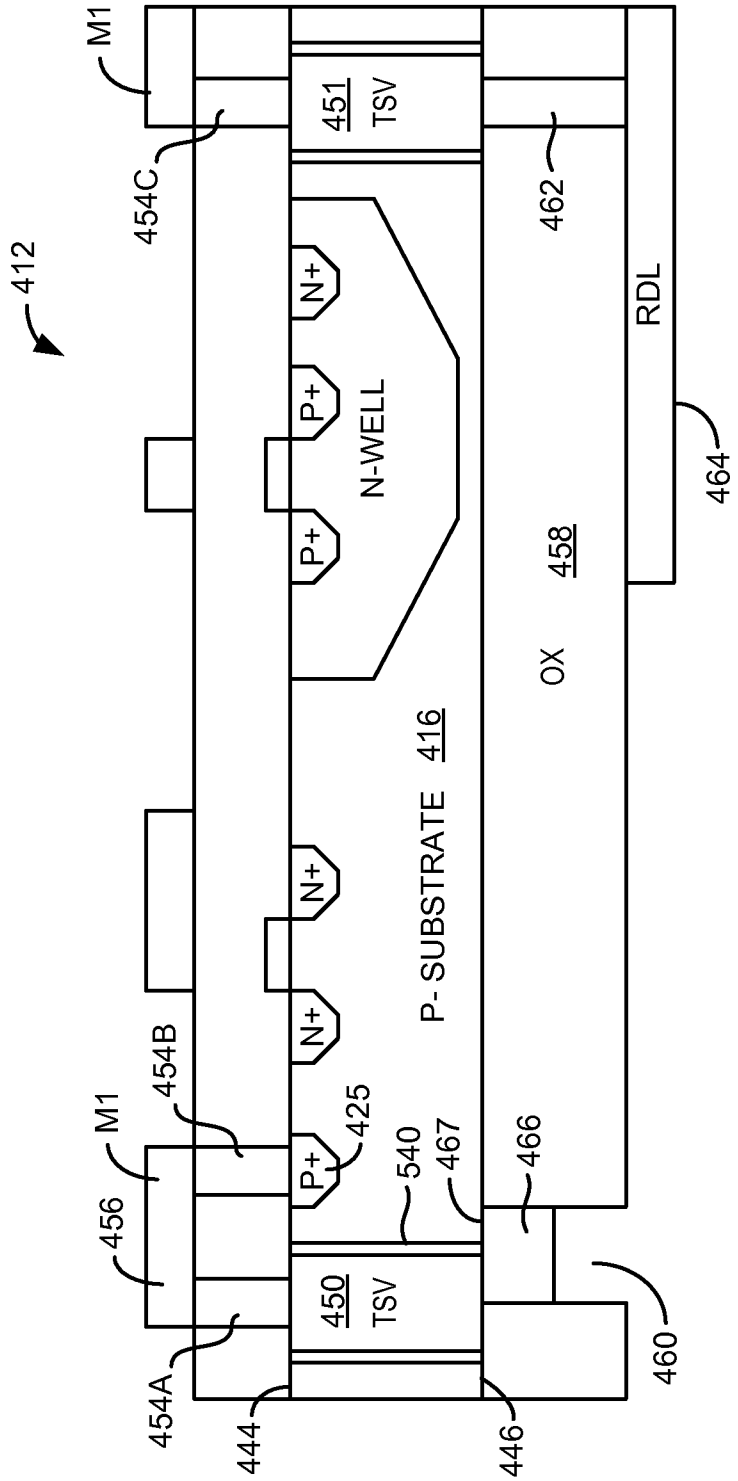

M1
454C
451
TSV
462
542
412
N+
P+
P+
N-WELL
N+
N+
P- SUBSTRATE 416
OX 458
M1
454B
456
425
540
467
466
P+
450
TSV
454A
444
446
460

FIG. 5H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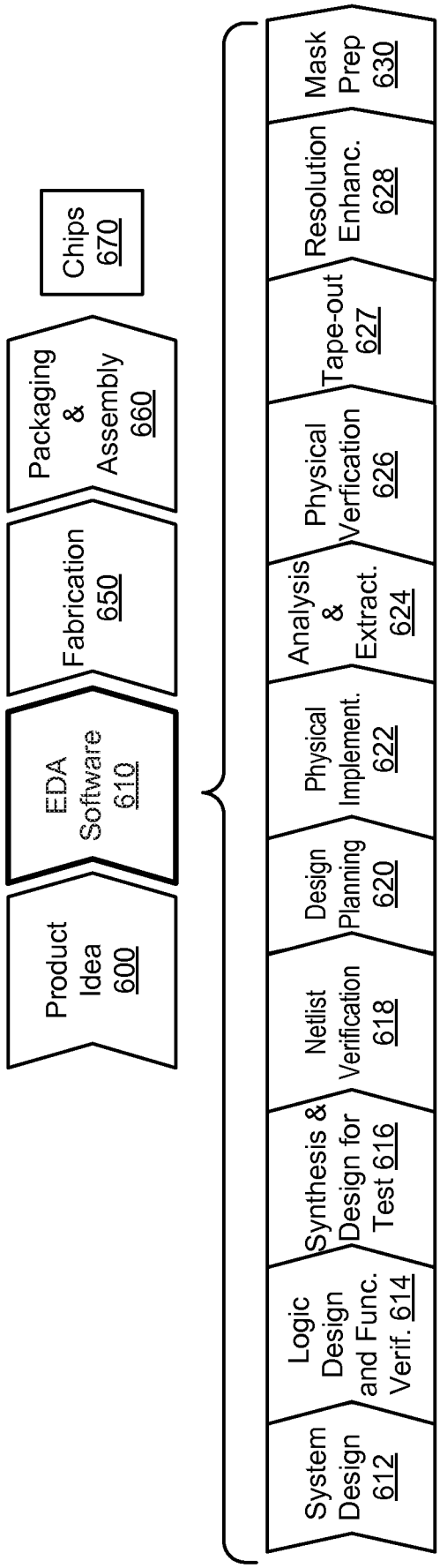
M1
454C
451
TSV
462
RDL
464
N+
P+
P+
N-WELL
458
OX
416
P- SUBSTRATE
N+
N+
454B
M1
425
P+
540
467
466
456
450
TSV
460
454A
444
446

FIG. 5I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Fabrication 650
Packaging & Assembly 660
Chips 670
System Design 612
Logic Design and Func. Verif. 614
Synthesis & Design for Test 616
Netlist Verification 618
Design Planning 620
Physical Implement. 622
Analysis & Extract. 624
Physical Verfication 626
Tape-out 627
Resolution Enhanc. 628
Mask Prep 630

FIG. 6

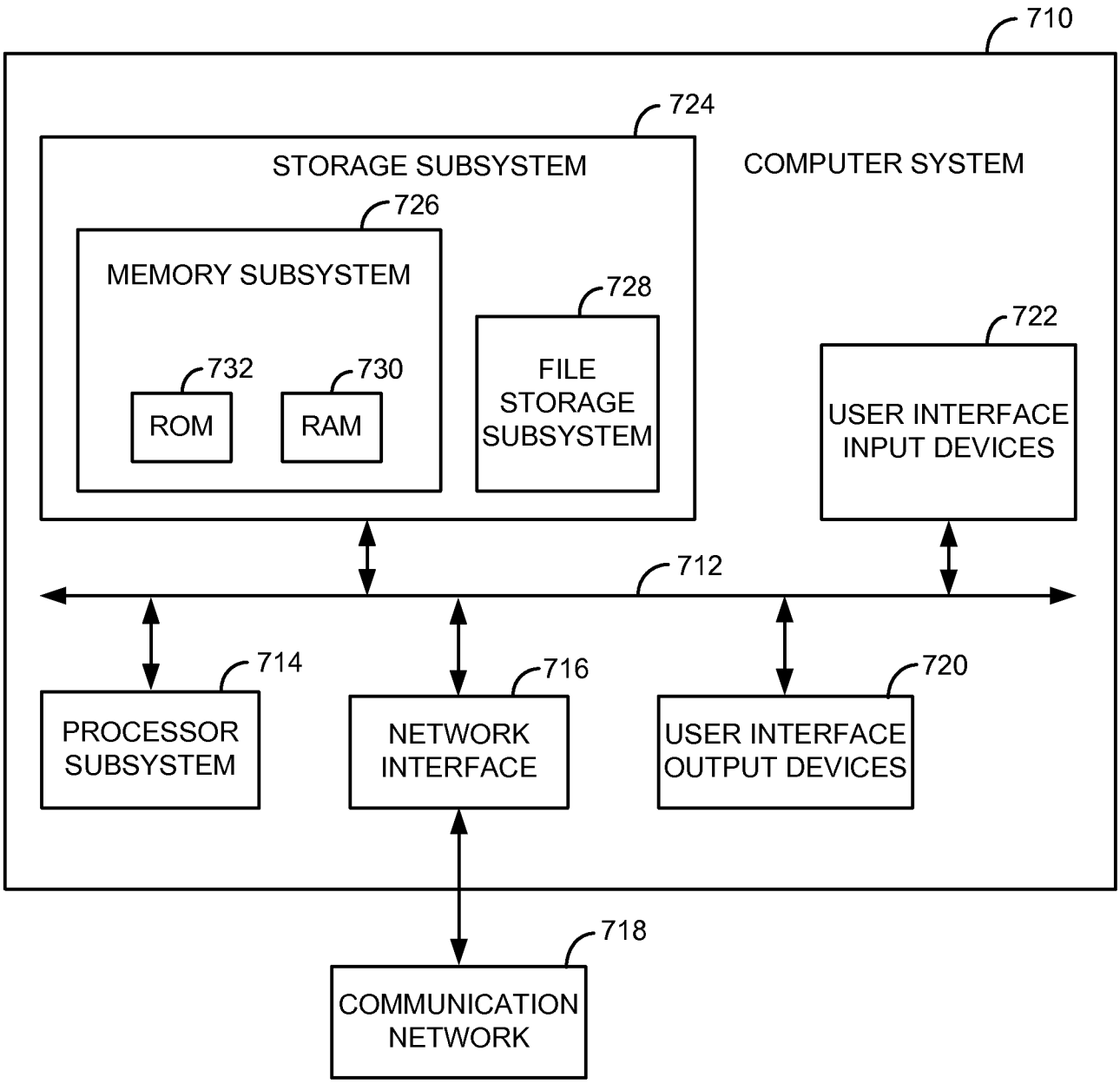
710
724
STORAGE SUBSYSTEM
COMPUTER SYSTEM
726
MEMORY SUBSYSTEM
728
722
732
730
ROM
RAM
FILE STORAGE SUBSYSTEM
USER INTERFACE INPUT DEVICES
712
714
716
720
PROCESSOR SUBSYSTEM
NETWORK INTERFACE
USER INTERFACE OUTPUT DEVICES
718
COMMUNICATION NETWORK

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057337

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/48(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/48; H01L 21/768; G06F 17/50; H01L 21/30; H01L 23/60; H01L 23/055

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: TSV, substrate, 3D integrated circuit, latch-up, noise coupling

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0304010 A1 (ZHE-WEI JIANG et al.) 15 December 2011 See paragraphs [0007], [0027]-[0030], [0040]-[0049], claims 1-5 and figure 3.	1-2,7,16-17,21
Y		20
A		3,8-9,12-15,18-19,22-25
Y	US 2011-0314437 A1 (LISA G. MCLLRATH) 22 December 2011 See abstract, paragraphs [0048]-[0049] and claim 1.	20
A	US 2010-0225002 A1 (OSCAR M.K. LAW et al.) 09 September 2010 See abstract, paragraphs [0036]-[0041], claim 1 and figure 5.	1-3,7-9,12-25
A	US 2009-0160050 A1 (NOBUAKI MIYAKAWA et al.) 25 June 2009 See abstract, paragraphs [0053]-[0074] and figures 11-18.	1-3,7-9,12-25
A	KR 10-2011-0039183 A (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 15 April 2011 See abstract, paragraphs [0014]-[0021], [0028]-[0031] and figures 1, 4a-4c.	1-3,7-9,12-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 December 2013 (24.12.2013)	**27 December 2013 (27.12.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057337

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 4-6, 10-11
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/057337

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0304010 A1	15/12/2011	TW 201145495 A	16/12/2011
US 2011-0314437 A1	22/12/2011	US 2009-055789 A1	26/02/2009
		US 2009-064058 A1	05/03/2009
		US 2010-005437 A1	07/01/2010
		US 2012-317528 A1	13/12/2012
		US 7526739 B2	28/04/2009
		US 8032857 B2	04/10/2011
		US 8209649 B2	26/06/2012
		US 8266560 B2	11/09/2012
		WO 2007-014300 A2	01/02/2007
		WO 2007-014300 A3	30/04/2009
US 2010-0225002 A1	09/09/2010	CN 101840912 A	22/09/2010
		JP 2010-219526 A	30/09/2010
		KR 10-2010-0100629 A	15/09/2010
		TW 201034157 A	16/09/2010
		US 2013-230985 A1	05/09/2013
		US 8487444 B2	16/07/2013
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		TW I388050 B	01/03/2013
		TW I388050 I	01/03/2013
		US 2010-0164055 A1	01/07/2010
		US 2010-0167495 A1	01/07/2010
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		US 8048763 B2	01/11/2011
		US 8049296 B2	01/11/2011
		WO 2007-024022 A1	01/03/2007
KR 10-2011-0039183 A	15/04/2011	CN 102044512 A	04/05/2011
		JP 2011-082524 A	21/04/2011
		TW 201133762 A	01/10/2011
		US 2011-0084365 A1	14/04/2011
		US 8264067 B2	11/09/2012