

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
24 January 2008 (24.01.2008)

PCT

(10) International Publication Number
WO 2008/010017 A1

- (51) International Patent Classification:
G03F 1/00 (2006.01) **G03F 1/14** (2006.01)
- (21) International Application Number:
PCT/IB2006/003431
- (22) International Filing Date: 19 July 2006 (19.07.2006)
- (25) Filing Language: English
- (26) Publication Language: English
- (71) Applicants (for all designated States except US):
FREESCALE SEMICONDUCTOR, INC. [US/US];
6501 William Cannon Drive West, Austin, Texas 78735
(US). **KONINKLIJKE PHILIPS ELECTRONICS N.V.**
[NL/NL]; Groenewoudseweg 1, NL-5621 Ba Eindhoven
(NL).

Tweed Court, Austin, TX 78727 (US). **VASEK, James Edward** [US/US]; 3902 John Simpson TR, Austin, TX 78732 (US). **WILKINSON, William Louis** [US/US]; 2313 Brookhollow Ter, Georgetown, TX 78626 (US). **COUDERC, Christophe** [FR/FR]; Philips Intellectual Property & Standards, P O Box 220, NL-5600 AE Eindhoven (NL).

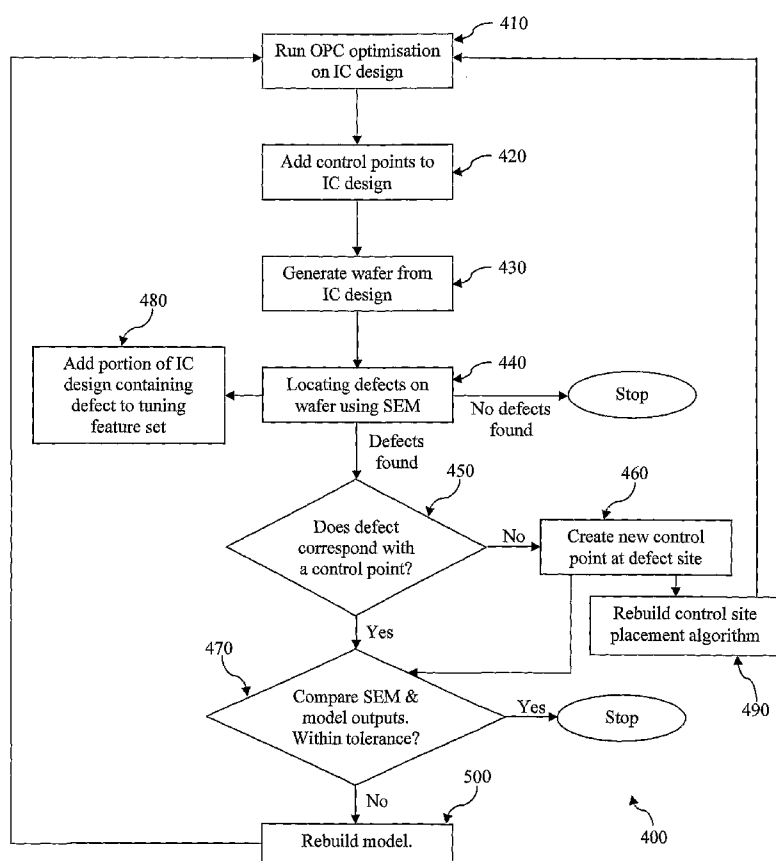
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **LUCAS, Kevin Dean** [US/FR]; 29B Avenue de Chamrousse, F-38240 Meylan (FR). **BOONE, Robert Elliott** [US/US]; 12104

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR DESIGNING AN INTEGRATED CIRCUIT



(57) Abstract: Method and apparatus for designing an integrated circuit by adding a plurality of control points (40, 204) to an integrated circuit wafer design. Each control point has at least one attribute. Then, an integrated circuit wafer is manufactured (430) using the integrated circuit wafer design. A defect on the integrated circuit wafer is then located (440). The control points are adjusted (470) such that they correspond with the defect.



European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Published:

— *with international search report*

METHOD AND APPARATUS FOR DESIGNING AN INTEGRATED CIRCUIT**Field of the Invention**

5 The present invention relates to a method and apparatus for designing an integrated circuit.

Background of the Invention

10 When making an integrated circuit (which may also be referred to as an IC, chip or device), a design layout of the IC is made using, for example, CAD tools. A reticle or mask is then produced for the IC design layout and then photolithography is used to transfer features from the
15 reticle or mask to a die (integrated circuit semiconductor wafer).

 Various techniques are used to reduce the level of defects in the resultant die. For instance, prior to the production of the reticle, the design layout may be
20 optimised using optical proximity correction (OPC) to create a reticle layout. This optimisation process amends the physical design layout in order to avoid optical or process distortions also known as patterning defects when features are transferred from the reticle or mask that may cause
25 failures of the device. The OPC optimisation process discretizes the design layout into moveable segments and adds control points to the design where it is determined that patterning defects may occur. The segmented features of the IC design are then amended using a model of the
30 patterning process to calculate patterning error information at these control points until it is determined that the

patterning defects are fixed. Once the patterning defects are fixed there is no further use for the control points.

Once the reticle is produced and wafer dies have been manufactured, features on these wafer dies may be measured
5 or micrographed by scanning electron microscope (SEM) techniques to evaluate if there are patterning defects which were not adequately fixed during OPC. Obviously, individually measuring or micrographing each feature on a multi-million gate device is unfeasible. Therefore, certain
10 representative features are chosen. These representative features can be determined by rule-based guidelines or by lithographic simulation predictions.

Where wafer patterning defects are found that would result in an unacceptable failure rate for the IC, the
15 reticle layout must be adjusted to avoid these critical defects. This results in further iterations of OPC, build and test of the die until no critical defects are found or the die meets other success criteria. This is a costly and labour intensive process and may result in many time
20 consuming iterations until a successful reticle layout is found.

Summary of the Invention

25 The present invention provides a method and apparatus for designing an integrated circuit as described in the accompanying claims.

Brief description of the Figures

30 The present invention may be put into practice in a number of ways and an embodiment will now be described by

way of example only and with reference to the accompanying drawings, in which:

FIG. 1 shows a schematic diagram of a layout of a
5 portion of an integrated circuit according to an embodiment of the present invention, including control points at particular locations, given by way of example;

FIG. 2 shows a SEM image of a portion of the integrated
10 circuit corresponding to the portion shown in FIG. 1, given by way of example;

FIG. 3 shows a schematic diagram of the layout of the
15 portion of the integrated circuit shown in FIG. 1 but with control points in different locations, given by way of example;

FIG. 4 shows a SEM image of a portion of the integrated
20 circuit corresponding to the portion shown in FIG. 3, given by way of example; and

FIG. 5 shows a flowchart of a method for designing an
integrated circuit according to an embodiment of the present
25 invention, given by way of example.

It should be noted that the figures are illustrated for simplicity and are not necessarily drawn to scale.

Detailed description of an embodiment

30

FIG. 1 shows a schematic diagram of the layout 10 of several features forming part of an integrated circuit (IC).

The IC layout is designed using known CAD tools and may be optimised using an optical proximity correction (OPC) technique. OPC may be used to reduce the adverse effects of optical and process distortions occurring during fabrication of a wafer.

During the OPC process certain feature locations may be identified as potential areas for causing defects in the wafer leading to failure of the IC. For instance, the areas around bends in a track may be produced too thin to the extent that they cannot conduct a high enough electrical current leading to burn-out at this point. These potentially problematic feature locations may be tagged by the addition of control points to the design. These control points are used to reference particular feature locations and are not fabricated on the final wafer. The control points are used during the OPC optimisation process to amend particular features.

In the method in accordance with the present invention, the control points are also used during wafer patterning defect evaluation. The use of control points during wafer patterning defect evaluation is not known from previous techniques. In one embodiment, instead of discarding the control points after the OPC optimisation process is completed, the control points are instead stored for use during wafer patterning defect evaluation. In another embodiment, an algorithm for determining placement of the control points may be stored for use during wafer patterning defect evaluation. In yet another embodiment, the control points may be regenerated on a subset of the original layout for use during wafer patterning defect evaluation.

Control points are locations for calculation of edge position (EP), edge position error (EPE), or critical

dimension (CD) for wafer features. The CD of a feature indicates the width at a specific location on that particular feature or the space at a specific location between two features. The EP, EPE or CD for any particular location may be estimated during the OPC optimisation step. During a step in the OPC optimisation process the EPs, EPEs or CDs for potentially problematic features are calculated at the control points. Therefore, each control point will have certain attributes that may be recorded for later retrieval. These attributes include location, tolerance, critical dimension, EP, EPE, CD, size and accuracy. The attributes for the control points may be stored in a database or other suitable computer file format.

Control points are generated during the OPC procedure before the movement of the design segments by the OPC software. Control points are generated by an algorithm for determining where OPC segment movements will be required in a design. To place control points, the algorithm may use geometrical rules such as distance from a design corner, or the results of patterning simulations such as light intensity minima or both.

FIG. 1 and FIG. 2 illustrate an example situation, where control points are not located correctly. This may be due, for example, to deficiencies in the algorithm used to generate control points. For example, if geometric rules are used to determine the placement of control points near design corners, the results of the geometric rules may not provide for optimum control point placement when there are many design corners in close proximity to each other on a given feature. In this example OPC optimisation has not effectively optimised the design layout due to the misplaced control points.

FIG. 1 contains a simulation of a particular problematic feature 20 that has a pinch point indicated by arrow 30. Three pairs of control points 40 surround the pinch point but none line up precisely with it. These
5 control points 40 were added during an OPC optimisation process.

Once a wafer has been fabricated wafer patterning defect evaluation may be used to analyze potentially problematic features. These checks may involve measuring
10 the actual minimum wafer CD of problematic features and comparing this measurement to a predetermined CD tolerance threshold. If the actual CD measured is less than the CD tolerance threshold, a patterning defect may be highlighted. These checks may also involve measuring the distance between
15 the detected patterning defect location and the nearest control point. If this measured distance is greater than a predetermined threshold distance, a control point placement error may be highlighted.

FIG. 2 shows a SEM micrograph of a portion 110 of the
20 IC wafer corresponding to the portion of IC design shown in FIG. 1. Corresponding SEM feature 20 is shown with control points 40 highlighted. SEM CD measurements taken at control points 40 in FIG. 2 may be compared to the patterning model's prediction of feature 20 CDs at the control points
25 in FIG. 1. The predicted vs. measured CD comparison shows that the patterning model has sufficient accuracy, as can be seen by comparing the model predicted feature 20 in FIG. 1 to the SEM image of feature 20 in FIG. 2. Dotted lines 50 indicate the measured CD of the pinch point on feature 20.
30 However, none of the control points 40 are placed at the narrowest point in feature 20. Thus, although the patterning model had sufficient accuracy, the OPC

optimisation failed to identify the most critical portion of feature 20 (i.e. the pinch point 30). Furthermore, none of the CDs of the feature 20 measured at each of the control points 40 are below the predetermined CD tolerance

5 threshold. This portion of the wafer will therefore, pass this particular validation test when looking at control points 40 without the most critical feature being measured. Nevertheless, the IC manufactured according to the design may fail at this point. Further measurements may be made
10 using the SEM and these measurements will not necessarily use control points 40 but instead are used to look for features that may potentially cause failures.

FIG. 3 and FIG. 4 illustrate an example situation, where control points are placed correctly, i.e. the minimum
15 distance between the control points 40 and the patterning defect location 30 is less than a predetermined threshold value. In this example although OPC optimisation occurred at the correct location the layout of the feature was not compensated to a sufficient degree to avoid failures. The
20 failure in this example to compensate the feature adequately is due to a limitation of the patterning model accuracy. Because of this model inaccuracy, simulated CD, EP or EPE measurements made at the control points may not effectively test the suitability of the IC design. Again, the control
25 points 40 were positioned during an OPC optimisation process.

FIG. 3 shows a similar schematic diagram to that of FIG. 1. However, the portion of the IC design 210 contains only a single pair of control points 240. The control
30 points are located at the correct position, i.e. at the narrowest point of the feature 20. However, the measured CD at the control points 240 is less than an acceptable CD.

FIG. 4 shows a SEM micrograph of a portion 310 of the IC wafer corresponding to the portion of IC design 210 shown in FIG. 3. Again, the pair of control points 240 are overlaid on this micrograph portion 310. The patterning model predicted CD of the feature 20 at control points 240 is greater than the minimum acceptable CD, and so the validation test using the control points will pass but as the actual minimum wafer CD of feature 20 measured by the SEM at the control points 240 is narrower than the minimum acceptable CD the feature 20 may still cause a failure once the IC is in use.

Since the attributes of the control points and the accuracy of the patterning model both affect the success of OPC optimisation it may therefore, be necessary to optimize these attributes and/or the model accuracy before subsequent OPC optimisation processes commence.

FIG. 5 shows a flowchart showing the steps for designing an IC. FIG. 5 is an embodiment of the method according to the invention. Flowchart 400 starts after an initial IC design has been completed. Implementation of flowchart 400 reduces the risk of encountering similar situations to those described with respect to FIGS. 1 to 4.

OPC optimisation is run on the initial IC layout design 410. During OPC optimisation control points may be added at a suitable step, to identify potentially problematic features 420. Control points may be added by an algorithm for determining where OPC segment movements will be required in a design. To place control points, the algorithm may use geometrical rules or alternatively, the results of patterning simulations or both. In one embodiment, the control points and their associated attributes may be stored for later retrieval. In another embodiment, the placement

algorithm may be stored for later regeneration of the control points and their associated attributes.

Once an OPC optimisation process has been run, an IC wafer may be fabricated using the optimised IC design 430.

5 Then, the IC wafer may be examined using a SEM or other suitable imaging or scanning technique in order to locate defects 440. The potential defect locations to examine with the SEM may be determined using simulation analysis of the OPC optimised design, using a wafer based defect detection
10 method such as die-die optical wafer inspection, by a review of programmed potential defective structures such as structures drawn at design rule limits, or other suitable detection method. If no defects are found the process may stop and the wafer may go into full production in the usual
15 way.

 The portion of the IC layout design containing a defect found in step 440 may be added to a tuning feature set 480 and used to find similar defects during subsequent optimisation of previous IC designs, of this IC design or of
20 future IC designs. For example, a portion of a layout containing a defect found in step 440 may be compared against other designs using pattern matching algorithms in order to determine if these designs will contain the same defect. In another example, the portion of the layout
25 containing a defect found in step 440 can be placed into a feature set used for training empirical process models. In yet another example, the portion of the layout containing a defect found in step 440 can be placed into a feature set for optimizing or verifying OPC characteristics such as
30 control point placement. If defects are found it may be determined whether or not they correspond to control points or pairs of control points 450. If the defects do not

correspond to existing control points this indicates that the OPC process may have misplaced the control points. For instance, the control points may be in the wrong locations (see FIGS. 1 and 2 and the corresponding description). In this case control points may be moved or added to the defective feature 460 to ensure that control points correspond to the defective feature. In a further embodiment of the method of the invention step 480 may be left out.

The algorithm for placing control sites may be rebuilt 490 using the layout portion containing a defect found in step 440. In a further embodiment of the method of the invention step 490 may be left out.

After it is known that control points correspond to the defective feature, simulated measurements of CD, EP or EPE can be taken at the defect location using the process model. The simulated results can be compared to the SEM measurements at the defective location 470. If the difference between the SEM measured and process model predicted results 470 is less than a predetermined threshold value, the process may stop. If the difference between the SEM measured and process model predicted results 470 is greater than a predetermined threshold value, then this indicates the process model has insufficient accuracy and should be amended or rebuilt 500. The process model may be rebuilt using the feature set used for training empirical process models. The process model uses an empirical model or function which is used to transform or analyze an approximate physically based simulation of light intensity and to predict CD, EP, EPE or other OPC parameters. Some process model parameters may be empirically fit to match experimental SEM CD, EP or EPE data using a set of model

training layout structures. Possible reasons for discrepancies in measured vs. process model predicted values include insufficient training layout structure coverage, poor empirical parameter values, and poor physical approximations in simulated light intensities.

If the process model is amended or rebuilt, the stored attributes associated with the incorrect control points will require updating. Once the process model is improved, the OPC process may be re-run and the process repeated until all significant defects have been removed. It may be possible to carry out a partial OPC optimisation rather than to optimise the entire IC design. For repeated structures, updates to one instance may be duplicated for all instances.

In this way the information used to generate control points during OPC optimisation may be re-used and tuned to further optimise the OPC process. This results in a more efficient design process and a final design may be found using fewer OPC, build and test cycles.

The method described above may be carried out in an automated manner using suitable apparatus or a computer programmed to perform each of the method steps.

As will be appreciated by the skilled person, details of the above embodiment may be varied without departing from the scope of the present invention, as defined by the appended claims.

For example, the control points may be added to the design at another stage in the design process rather than during OPC optimisation.

The defects that may be detected include tracks that are too narrow to allow sufficient current to flow, tracks that are too close together, tracks that are too short or weak connections.

Defects may be found on the wafer using various techniques including scanning electron microscope measurements.

The separation of a pair of control points may be used
5 to define an estimated CD for a particular feature.

Control points may be used to assist with the location of defects on the wafer as they may be located in proximity to parts of features susceptible to defects.

CLAIMS:

1. A method (400) of designing an integrated circuit comprising the steps of:

5 adding (420) a plurality of control points (40, 240) to an integrated circuit wafer design, wherein each control point has at least one attribute;

manufacturing (430) an integrated circuit wafer using the integrated circuit wafer design;

10 locating (440) a defect on the integrated circuit wafer; characterised by

adjusting (470) the plurality of control points (40, 240) such that they correspond with the defect.

15 2. The method of claim 1, wherein the adjusting step further comprises changing the at least one attribute.

3. The method of claim 1 or claim 2, wherein the at least one attribute is selected from the group consisting of

20 location, tolerance, critical dimension, CD, edge position, EP, edge position error, EPE, and size.

4. The method of claims 1, 2 or 3, wherein the adjusting step further comprises adding a control point (40, 240).

25 5. The method of any previous claim further comprising the step of recording a portion of the integrated circuit design containing the defect, in a tuning feature set.

30 6. The method of any previous claim, wherein the plurality of control points (40, 240) are added during an optical proximity correction, OPC, optimisation process (410).

7. The method of any previous claim further comprising the step of storing the plurality of control points (40, 240).

5 8. The method of any previous claim, further comprising the step of determining an error between a process model prediction of the at least one attribute and a physical measurement of the at least one attribute.

10 9. The method of claim 8, wherein the determining the error step further comprises comparing the error within a predetermined threshold error value to determine if the process model should be amended.

15 10. The method of claim 8 of claim 9, wherein the physical measurement is a scanning electron microscope, SEM, measurement.

20 11. The method of any previous claim, wherein the locating step (440) is performed using a SEM.

25 12. A computer program comprising program instructions that, when executed on a computer cause the computer to perform the method of any of the previous claims.

13. A computer-readable medium carrying a computer program according to claim 12.

30 14. A computer programmed to perform the method of any of claims 1 to 11.

15. An integrated circuit manufactured according to the method of any of claims 1 to 11.

16. Apparatus for designing an integrated circuit

5 comprising:

means for adding a plurality of control points (40, 240) to an integrated circuit wafer design, wherein each control point has at least one attribute;

10 means for locating a defect on the integrated circuit wafer manufactured using the integrated circuit wafer design; characterised by

means for adjusting the plurality of control points such that they correspond with the defect.

15 17. The apparatus of claim 16, wherein the means for locating an error is a SEM.

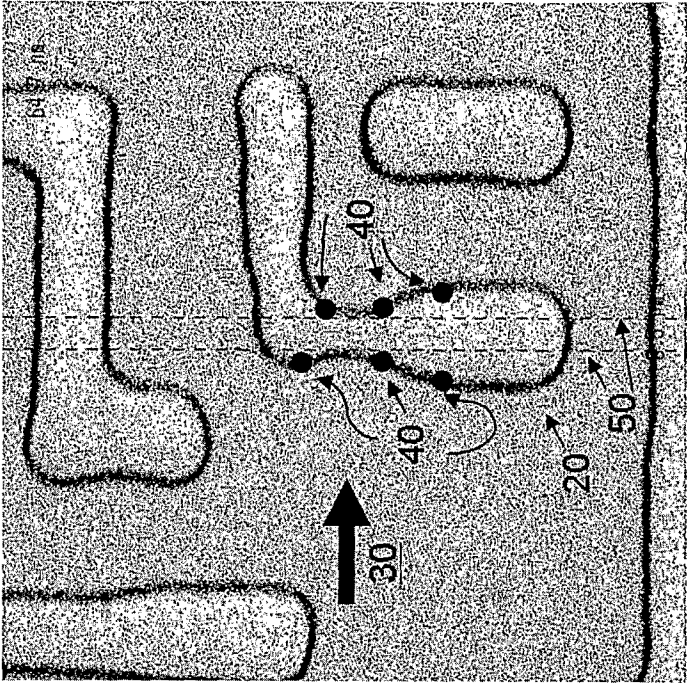


FIG. 2

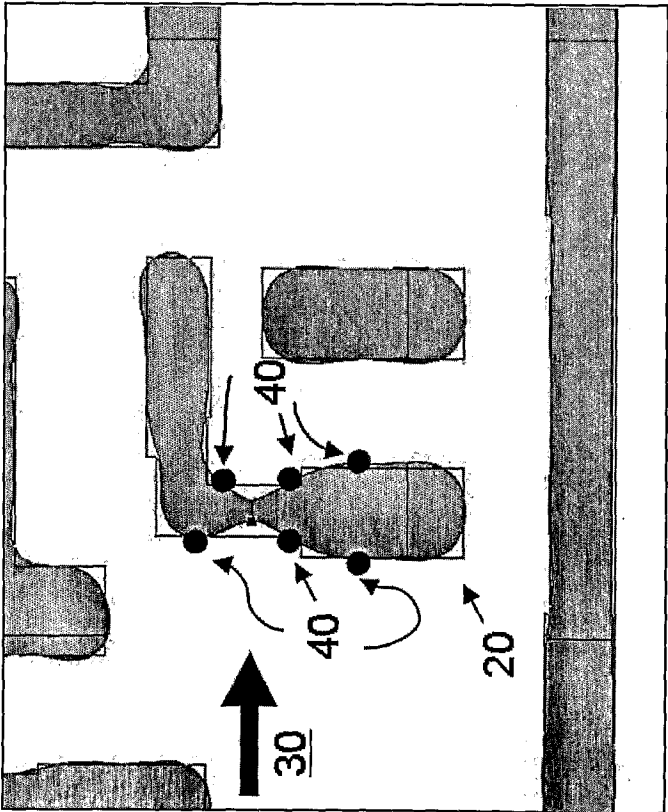


FIG. 1

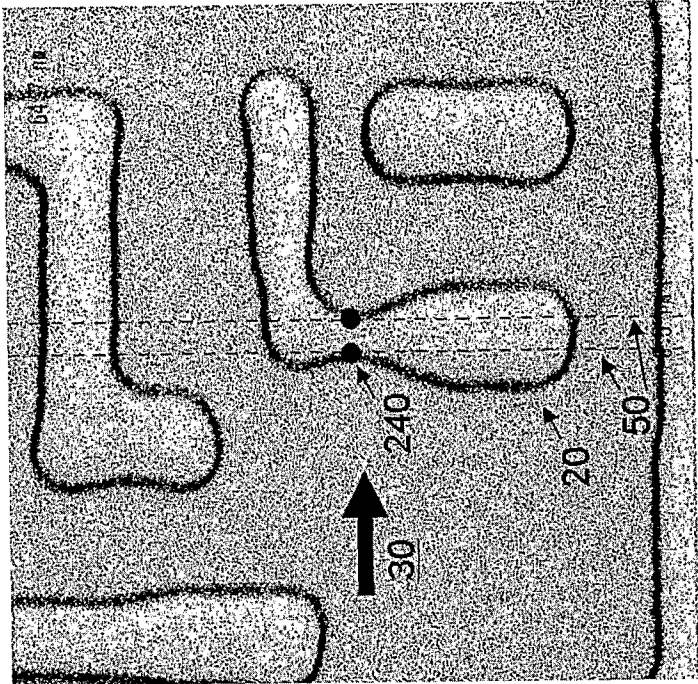


FIG. 4

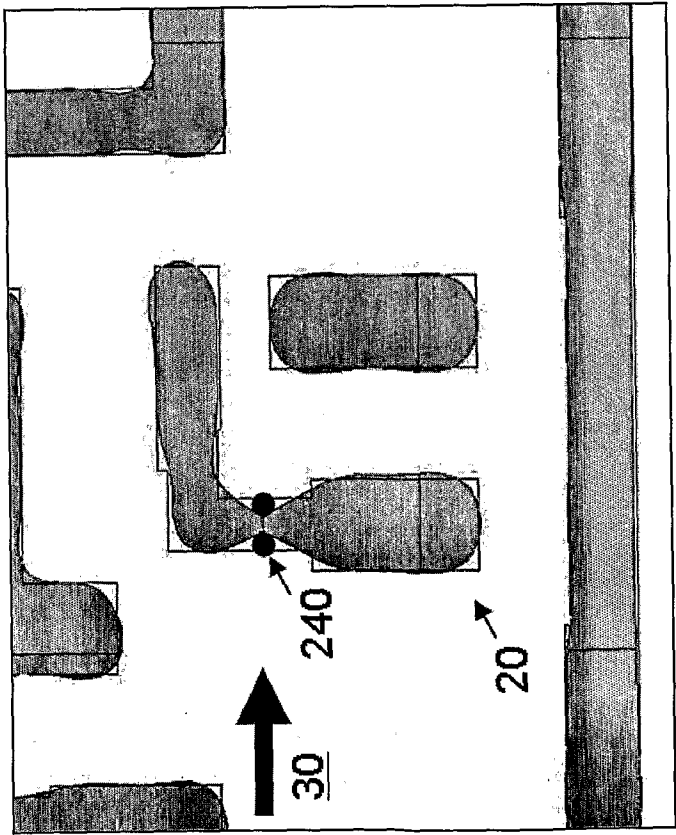
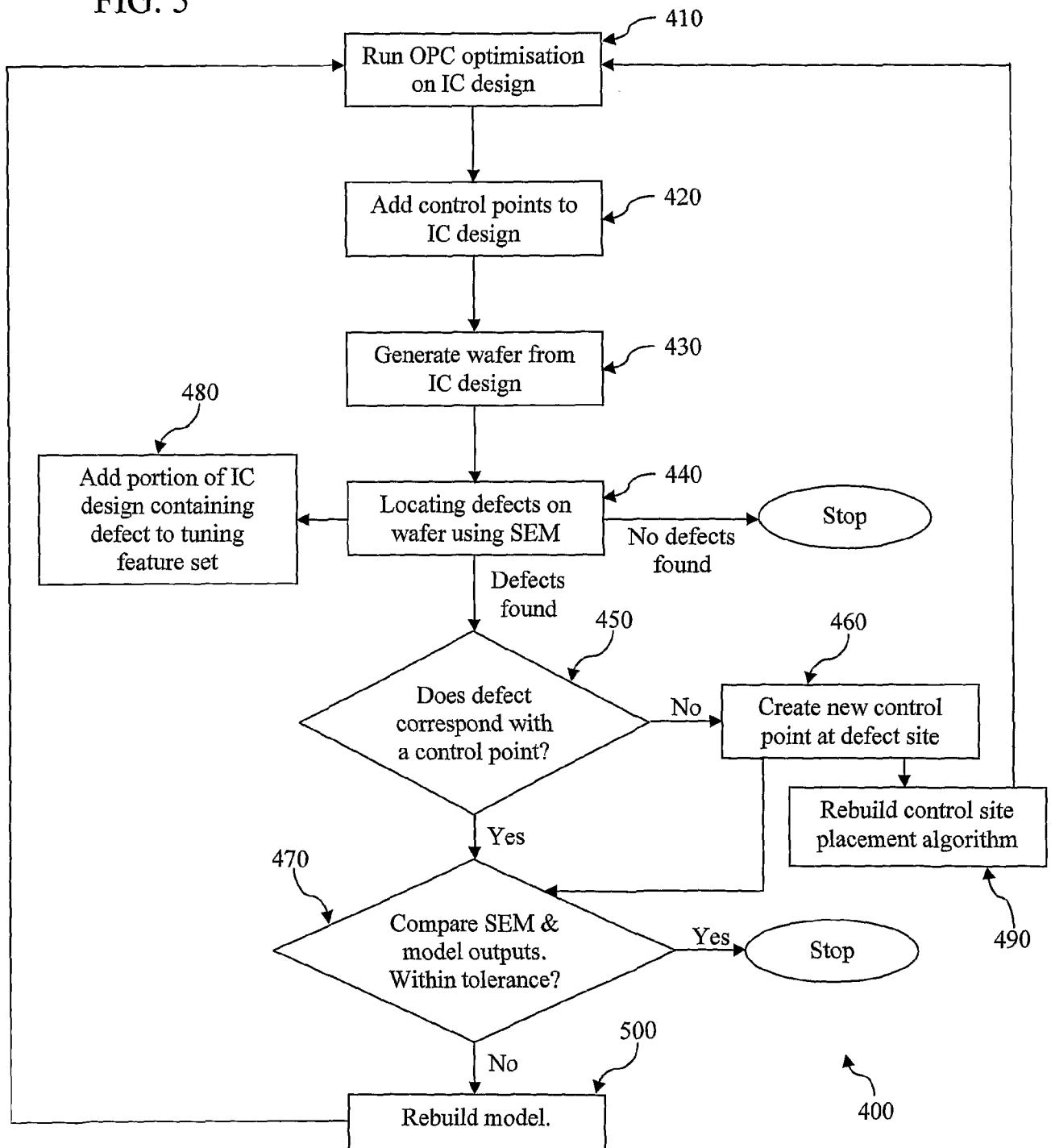


FIG. 3

FIG. 5



INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2006/003431

A. CLASSIFICATION OF SUBJECT MATTER
 INV. G03F1/00 G03F1/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G03F G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/121021 A1 (LIU HUA-YU [US] ET AL) 26 June 2003 (2003-06-26)	1,3,4,6, 7,11-17
X	paragraphs [0027], [0028]	6
X	paragraphs [0039], [0040]	
Y	paragraph [0030]	3
	-----	2,5,8-10
X	US 7 080 349 B1 (BABCOCK CARL [US] ET AL) 18 July 2006 (2006-07-18)	1,3,4, 12-16
	column 6, line 63 - column 7, line 7 column 8, line 13 - column 9, line 5 column 11, line 10 - column 12, line 33	

A	US 2003/015674 A1 (BROERMANN OLIVER [DE]) 23 January 2003 (2003-01-23)	11,17
	paragraphs [0005], [0006], [0040], [0041]	

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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

28 March 2007

Date of mailing of the international search report

13/04/2007

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Müller-Kirsch, Lutz

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/003431

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2006/063268 A (KLA TENCOR TECH CORP [US]; WU KENONG [US]; RANDALL DAVID [US]; NAFISI) 15 June 2006 (2006-06-15) paragraph [0090] -----	5
Y	EP 1 424 595 A (LSI LOGIC CORP [US]) 2 June 2004 (2004-06-02) paragraphs [0021] - [0024]; figure 2 -----	8-10
Y	US 2003/115034 A1 (TSAI CHI-MING [US] ET AL) 19 June 2003 (2003-06-19) paragraphs [0026] - [0030] -----	2
A	WO 2004/008245 A (CADENCE DESIGN SYSTEMS INC [US]) 22 January 2004 (2004-01-22) page 19, lines 14-33 -----	2
A	US 2003/110465 A1 (ZHANG YOUPIING [US]) 12 June 2003 (2003-06-12) paragraphs [0039] - [0057] -----	1,12-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2006/003431

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2003121021	A1	26-06-2003	NONE	
US 7080349	B1	18-07-2006	NONE	
US 2003015674	A1	23-01-2003	DE 10134755 A1	06-02-2003
WO 2006063268	A	15-06-2006	US 2006291714 A1	28-12-2006
EP 1424595	A	02-06-2004	JP 2004177961 A	24-06-2004
			US 2004102912 A1	27-05-2004
			US 2004199349 A1	07-10-2004
US 2003115034	A1	19-06-2003	NONE	
WO 2004008245	A	22-01-2004	AU 2003256530 A1	02-02-2004
			EP 1579274 A2	28-09-2005
			JP 2006502422 T	19-01-2006
US 2003110465	A1	12-06-2003	US 2004181770 A1	16-09-2004