A circuit for driving a plasma display panel in a time division manner applies pulses of an opposite polarity to an electrode pair disposed on opposite sides of a gas discharge cell to be made to glow, and applies pulses of the same polarity to the electrodes disposed in registration with a gas discharge cell that should not be made to glow.
FIG. 1
(a) 1st. ROW ELECTRODE
(b) 2nd. ROW ELECTRODE
(c) m-th COLUMN ELECTRODE
(d) 1st. ROW m-th COLUMN CELL
(e) 2nd. ROW m-th COLUMN CELL

FIG. 2
(a) 1st. ROW ELECTRODE
(b) 2nd. ROW ELECTRODE
(c) m-th COLUMN ELECTRODE
(d) 1st. ROW m-th COLUMN CELL
(e) 2nd. ROW m-th COLUMN CELL

FIG. 4
(a) 1st. ROW ELECTRODE
(b) 2nd. ROW ELECTRODE
(c) m-th COLUMN ELECTRODE
(d) 1st. ROW m-th COLUMN CELL
(e) 2nd. ROW m-th COLUMN CELL
FIG. 3

BRIGHTNESS OF THE CELL

VOLTAGE APPLIED ACROSS A CELL

FIG. 5

(a) 1st ROW ELECTRODE $V_1$
(b) 2nd ROW ELECTRODE $V_1$
(c) m-th COLUMN ELECTRODE $V_2$
(d) 1st ROW m-th COLUMN CELL $V_1, V_2$
(e) 2nd ROW m-th COLUMN CELL $V_1, V_2$
FIG. 6
FIG. 8
PULSES OF THE SAME OR AN OPPOSITE POLARITY TO ELECTRODES OF A PLASMA DISPLAY PANEL

BACKGROUND OF THE INVENTION

This invention relates to display driving circuitry and, more specifically, to a circuit for driving an external electrode discharge display panel in a time division manner.

External electrode discharge display panels or plasma display panels of various types are described in a first prior patent application Ser. No. 291,700 filed Sept. 25, 1972, by Tsunekatyo Iwakawa and Togo Miyazaki. Like panels are described in a second prior patent application Ser. No. 306,843 filed Nov. 15, 1972, by Tsunekatyo Iwakawa and Akira Yano. Similar panels are further described in a third prior patent application Ser. No. 328,055 filed Jan. 30, 1973, by Tsunekatyo Iwakawa and Akira Yano. Conventional driving circuits for such plasma display panels are described in the above-referenced prior patent applications.

One of the conventional driving circuits described in the second and the third prior patent applications comprises structure for cyclically applying a pulse train of a predetermined duration to the electrodes of a first group, such as the row electrodes, of a plasma display panel and structure for selectively supplying another pulse train of the opposite polarity to the electrodes of a second group, such as the column electrodes. A gas discharge occurs in a gas discharge cell interposed between the opposing electrodes simultaneously supplied with the pulse trains. The gas discharge produced is selected one or the cells of the display is observed as a display of a numeral, a letter, a symbol, and/or a combination of these.

Although it is not necessary to selectively supply pulse voltages of the same amplitude or pulse height to the respective electrode groups, it is assumed that each pulse voltage has the same amplitude V for simplicity of description. Let the voltage at which the discharge occurs in the cell as a result of rises in the respective pulse voltages and the voltage at which the discharge disappears as a result of decreases in the respective pulse voltages be represented by $V_d$ and $V_n$, respectively. Normal time division drive of the plasma display panel is possible when the pulse height V satisfies the following inequalities:

$$2V > 2V_d \quad (1)$$

and

$$V < 2V_n \quad (2)$$

among which the inequality (1) provides a condition for the discharge to occur when both row and column electrodes are selected simultaneously and the inequality (2) provides another condition for the discharge not to occur when only a row or a column electrode is selected. The inequality (2) imposes an upper limit to the pulse voltage V. This makes it impossible to achieve higher brightness by raising the pulse voltages. From the inequalities (1) and (2), the relationship

$$V > 2(V_d - V_n) \quad (3)$$

follows, in which the right side is dependent for the most part on the characteristics of the discharge cells.

The inequality (3) imposes a lower limit to the pulse height V. This prohibits the use of a plasma display panel with integrated circuits and the use of driving circuit switching elements characterized by a low breakdown voltage.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a circuit for driving an external electrode discharge display panel in a time division manner, Operable with pulse voltages of a variety of amplitudes.

It is another object of this invention to provide a circuit for driving an external electrode discharge display panel in a time division manner, said circuit being capable of avoiding several factors which impose restrictions on the amplitudes of the pulse voltages supplied to the external electrodes.

It is still another object of this invention to provide a circuit for driving an external electrode discharge display panel in a time division manner, said circuit being operable with integrated circuits.

It is yet another object of this invention to provide a circuit for driving an external electrode discharge display panel in a time division manner, said circuit comprising switching elements of low withstand voltage.

According to this invention, there is provided a circuit for driving an external electrode discharge display panel having a plurality of gas discharge cells, a first and a second group of electrodes disposed on opposite sides of said cells, and first means for cyclically applying a first pulse train of a predetermined duration to the electrodes of said first group, wherein the improvement comprises second means for supplying a second pulse train to each electrode of said second group, said second pulse train comprising pulses of a polarity opposite to the pulses of said first pulse train for the duration of time in which the electrode of said first group is energized for second group electrodes associated with cells which are to glow and otherwise comprising pulses of the same polarity as the pulses of said first pulse train.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features, objects and advantages will become more clear from the discussion here-inbelow regarding plural display driving circuit embodiments of the present invention, presented below in conjunction with the drawing, in which

FIG. 1 depicts wave forms of pulse trains supplied to electrodes of a plasma display panel by a first conventional driving circuit;

FIG. 2 shows wave forms of pulse trains supplied to electrodes of a plasma display panel by another conventional driving circuit;

FIG. 3 illustrates the relationship between the pulse voltage supplied across a gas discharge cell of a plasma display panel and the brightness of the glow of the cell;

FIG. 4 depicts wave forms of pulse trains supplied to electrodes of a plasma display panel in accordance with one aspect of the instant invention;
FIG. 5 shows wave forms of pulse trains supplied to electrodes of a plasma display panel in accordance with another aspect of this invention; FIG. 6 is a schematic circuit diagram of a fundamental embodiment of this invention; FIG. 7 is a schematic circuit diagram of a first embodiment of the present invention; and FIG. 8 is a schematic circuit diagram of a second embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

For convenience of description, let it be assumed for the following that an external electrode discharge display panel comprises a plurality of row electrodes, \( n \) in number, and a plurality of column electrodes.

Before describing several preferred embodiments of the instant invention, operation of a conventional driving circuit for a plasma display panel will be analyzed with reference to FIGS. 1 and 2 in order to facilitate an understanding of the principles on which this invention is based.

Referring specifically to FIG. 1 which is a substantial reproduction of FIG. 2 of the third prior patent application referred to hereinabove, a conventional driving circuit comprises structure (not shown) for cyclically supplying pulsed voltages to the first, the second, . . . , and the \( n \)-th row electrodes (not shown). The pulsed voltages comprise pulse trains of a common duration \( T \) shifted by a common interval \( T \) as typified in FIGS. 1(a) and 1(b) for the first and the second row electrodes. The pulse trains of each pulsed voltage comprises plural pulses each characterized by an amplitude \( V \), and the train and is refreshed at a period \( nT \). The driving circuit further comprises structure (not shown) for selectively supplying a similar pulsed voltage to each of the column electrodes (not shown) across the row electrodes at those gas discharge cells interposed therebetween wherein a discharge should be made to occur. As shown in FIG. 1 (C) for the \( m \)-th column electrode, the voltage pulses supplied to a column electrode have a polarity opposite to the pulses supplied to the row electrodes and appear in coincident timed relation to the latter pulses. With the illustrated pulses supplied to the row and column electrodes, an alternating voltage of necessary and sufficient amplitude is supplied across the first row \( m \)-th column cell as shown in FIG. 1(d) to make the cell glow during the duration of period \( T \). The second row \( m \)-th column cell is supplied with the voltage depicted in FIG. 1(e) and is made to glow for only a very short transient time by the first pulse applied thereacross.

Referring to FIG. 2 wherein the pulse voltages supplied to the row and column electrodes have different amplitudes, let it be assumed for mere convenience of description that the pulses supplied to the row electrodes have a pulse height \( V_f \) that is larger than a pulse height \( V_v \) of the pulses for the column electrodes as exemplified at FIGS. 2(a), (b), and (c) for the first and second row electrodes and for the \( m \)-th column electrode. In order that the first row \( m \)-th column cell glow during the period allotted to the first row cells when the \( m \)-th column electrode is selected,

\[
V_1 + V_2 > 2V_f
\]

must hold as illustrated in FIG. 2(d). In order to prevent the second row \( m \)-th column cell from glowing during the period for the second row column even when the \( m \)-th column electrode is selected,

\[
V_1 < 2V_f
\]

must hold as shown in FIG. 2(e).

Referring now to FIG. 3, the abscissa represents the pulse height \( V \) of the voltage supplied to each electrode when the pulse heights \( V_1 \) and \( V_2 \) are equal to each other and the ordinate shows the brightness of the glow of the cell actually measured for two pulse repetition frequencies 20 kHz and 10 kHz. As shown, the brightness increases with an increase in the pulse amplitude. The inequality (2), however, imposes a limitation on the maximum brightness available with the conventional driving circuit. On the other hand, the inequality (3) imposes a limitation on the lowest pulse height applicable to the conventional driving circuit. For example, the difference \( V_f - V_v \) amounts to as high as about 20 volts due to the deviation in the cell characteristics of a plasma display panel so that the pulse height of the voltage supplied to one of the electrode pair should be 40 volts or more. This results in the high breakdown voltage required for the switching elements used in the driving circuit and, accordingly, the high selling price of a driving circuit set.

Referring to FIG. 4, a circuit for driving a plasma display panel in accordance with the principles of the present invention comprises first means (not shown) for cyclically supplying a first pulse train of a pulse height \( V_1 \) and of a predetermined duration \( T \) to the first through the \( n \)-th row electrodes in a manner similar to the cyclic application of a pulse train described with reference to FIG. 1 or 2. The pulse trains supplied to the first and the second row electrodes are exemplified in FIGS. 4(a) and (b). The driving circuit further comprises second means (not shown) for simultaneously supplying second pulse trains to the respective column electrodes (not shown). When it is desired to make the first row \( m \)-th column cell glow and to cause the second row \( m \)-th column cell not to glow, the second pulse train supplied to the \( m \)-th column electrode comprises pulses of a pulse height \( V_2 \) and of the polarity opposite to the pulses supplied to the row electrodes during the period when the first row electrode is supplied with the first pulse train, and pulses of the pulse height \( V_2 \) and of the same polarity as the pulses supplied to the row electrodes during the period when the second row electrode is supplied with the first pulse train, as illustrated in FIG. 4(c). The voltages applied across the first row and the second row \( m \)-th column cells become as shown in FIGS. 4(d) and (e), respectively. It is necessary that the amplitudes \( V_1 + V_2 \) and \( V_2 \) of the pulses applied across the first row \( m \)-th column cell satisfy the inequalities,

\[
V_1 + V_2 > 2V_f
\]

and that the amplitudes \( V_2 \) and \( V_1 - V_2 \) of the pulses applied across the second row \( m \)-th column cell should satisfy the inequalities

\[
V_2 < 2V_f
\]

and

\[
V_1 - V_2 < 2V_f
\]

It follows therefore that the pulse heights \( V_1 \) and \( V_2 \) should satisfy
and

\[ (V_I - V_c) < V < (V_I + V_c) \]

from which it is seen that the upper limit for the larger pulse height \( V_c \) and the lower limit for the smaller pulse height \( V_s \) are extended to \( 2(V_I + V_c) \) and to \( V_I - V_c \) in contrast to the corresponding limits \( 2V_c \) and \( 2(V_I - V_c) \) for the conventional driving circuit. It is thus possible with a driving circuit according to this invention to provide a brighter display and to reduce the voltage that the switching elements must be capable of withstanding for pulses of the pulse height \( V_s \) to about a half of that required for the corresponding switching elements used in the conventional driving circuit.

Turning to FIG. 5, negative going pulses may be supplied to the row electrodes as illustrated in FIGS. 5 (a) and (b) for the first and the second row electrodes. In accordance therewith, the pulses supplied to each column electrode go positive when it is desired to make a discharge occur in the cell interposed between the column electrode and the particular row electrode simultaneously supplied with the pulse train, and go negative in other cases as depicted in FIG. 5 (c) for the \( m \)-th column electrode. The pulses applied across the first row and the second row \( m \)-th column cells under the illustrated condition are illustrated in FIG. 5 (d) and (e). This aspect of the present invention is preferable in that the discharge quickly occurs upon selection of a cell due to the stronger electric field present in the cell while the cell is not selected than the corresponding field produced by the pulse trains illustrated with reference to FIG. 4. In this connection, it should be noted that the first and second pulse trains cooperate to supply a direct-current component voltage approximately equal to \( V_I - V_c \) while the first pulse train is not supplied to the row electrodes disposed in registration with the last-mentioned cells.

Referring now to FIG. 6, there is shown a fundamental embodiment of this invention for driving a plasma display panel comprising row electrodes 11, 12, 13, ..., and column electrodes 21, 22, 23, ..., Pulse trains illustrated with reference to FIG. 5 are supplied to the electrode via a row driver 26 and a column driver 27 supplied with a clock pulse train from a clock generator 28 and with control pulses from a control signal generator 29. The control pulses for the row driver rise to the logic "1" level cyclically. The control pulses for the column driver 27 are selectively set to the logic 1 level in timed relation to the control pulses for the row electrodes or in accordance with the particular cell or cells that are to be made to glow.

The row driver 26 comprises two-input NAND gates 31, 32, 33, ..., supplied with the clock pulses and the respective row control pulses, and row switching elements 41, 42, 43, ..., driven by the respective outputs of the NAND gates 31, 32, 33, ..., for supplying the row electrodes 11, 12, 13, ..., with the pulse trains exemplified in FIG. 5 (a) and (b). The column driver 27 comprises an inverter 50 for inverting the clock pulses, two-input first AND gates 51, 52, 55, ..., supplied with the clock pulses and the respective control column pulses to be enabled when the associated column electrodes are selected; control signal inverters 61, 62, 63, ..., for inverting the respective column control pulses; two-input second AND gates 71, 72, 73, ..., supplied with the inverted clock pulses and the respective inverted column control pulses to be enabled when the associated column electrodes are not selected; NOR gates 81, 82, 83, ..., supplied with the outputs of the first and second AND gates 51 and 71, 72 and 73, 74, ..., and column switching elements 91, 92, 93, ..., driven by the respective outputs of the NOR gates 81, 82, 83, ..., for supplying the respective column electrodes 21, 22, 23, ..., with the pulse trains exemplified in illustrated FIG. 5 at (c).

Referring to FIG. 7, elements of a first embodiment of this invention which are similar to those illustrated in conjunction with the fundamental embodiment depicted in FIG. 6 are designated with like reference numerals. The row switching circuits 41, 42, 43, ..., comprise NPN transistors 101, 102, 103, ..., and their collector resistors 111, 112, 113, ..., supplied with a D.C. voltage \( V_s \) by a D.C. source 110. The outputs of the AND gates 31', 32', 33', ..., used herein instead of the NAND gates 31, 32, 33, ..., of the fundamental embodiment are supplied to the base electrodes of the NPN transistors 101, 102, 103, .... The row electrodes 11, 12, 13, ... are supplied from the collector electrodes of the NPN transistors 101, 102, 103, .... The column switching circuits 91, 92, 93, ..., comprise PNP transistors 121, 122, 123, ..., supplied with another D.C. voltage \( V_s' \) by another D.C. source 130 and their collector resistors 131, 132, 133, .... The outputs of the NOR gates 81, 82, 83, ..., are supplied to the base electrodes of the PNP transistors 121, 122, 123, .... and the column electrodes 21, 22, 23, ..., are supplied from the collector electrodes of the PNP transistors 121, 122, 123, .... Further referring to FIG. 7, let it be assumed that the voltages \( V_I \) and \( V_c \) are 120 volts and 100 volts, respectively, for a particular plasma display panel to be driven by the driving circuit depicted therein. The D.C. voltages \( V_s \) and \( V_s' \) may be set at 220 volts and 24 volts, respectively. The driving circuit supplies the row electrodes 11, 12, 13, ..., with pulse trains whose amplitude is 220 volts and whose phase is opposite to the phase of the clock pulses. The column electrode or electrodes selected by the column selection pulses are supplied with driving pulses 24 volts in amplitude and the same phase as the clock pulses. The unselected column electrodes are supplied with pulse trains 24 volts in amplitude and a phase, opposite to the phase of the clock pulses. The possibility of using MOS integrated circuit inverters for the PNP transistors 121, 122, 123, ..., has been confirmed. By contrast, it has been found impossible to make the conventional driving circuit shown in FIG. 2 drive the particular plasma display panel without misoperation with the pulse amplitude \( V_c \) reduced below \( 2(V_I - V_s) = 40 \) volts.

Referring finally to FIG. 8, a circuit for supplying the pulse trains depicted in FIG. 5 to row electrodes 11, 12, 13, ..., and column electrodes 21, 22, 23, ..., of a plasma display panel according to a second embodiment of this invention comprises a row driver 26 and a column driver 27 supplied from a control signal generator 29 and a D.C. and clock pulse source 150. The row driver 26 comprises first NPN transistors 151, 152, 153, ..., whose emitter electrodes are supplied with inverted clock pulses \( \phi \) from the source 150. The collector electrodes of these transistors are supplied with a first D.C. voltage \( V_s \) from the source 150, through collector resistors 161, 162, 163, ..., and the transistor base electrodes are supplied with the cyclic control signals from the control signal generator 29 through resis-
The row electrodes 11, 12, 13, ... are energized from the collector electrodes of the first NPN transistors 151, 152, 153, ... with the pulse trains of amplitude $V_A$ and of a phase opposite to the clock pulses while the row control signals cyclically assume the higher level.

The column driver 27 comprises second NPN transistors 181, 182, 183, ... having emitter electrodes supplied from the source 150 with first inverted clock pulses $\phi$. The collector electrodes are supplied with a second D.C. voltage $V_C$ from the source 150 through collector resistors 191, 192, 193, ... Second inverted clock pulses $\phi_2$ supplied from the source 150 through first diodes 201, 202, 203, ... and column selection signals supplied from the control signal generator 29 through resistors 211, 212, 213, ... are combined and supplied to the base electrodes of the second NPN transistors 181, 182, 183, ... through capacitors 221, 222, 223, ... The base electrodes are supplied with zero potential through resistors 231, 232, 233, ... and with a third D.C. voltage $V_{ee}$ through resistors 241, 242, 243, ... to be held at a predetermined potential while the column selection signals assume the lower level. Second diodes 251, 252, 253, ... prevent the base potentials going below zero potential when the column selection signals take the higher level. By rendering the amplitude of the second inverted clock pulses $\phi_2$ greater than that of the first inverted clock pulses $\phi_1$, it is possible to supply the column electrodes 21, 22, 23, ... with pulse trains which are in phase with the clock pulses during presence of the column selection signals and are phase opposite to the clock pulses while the column selection signals take the lower level.

While the present invention has thus far been described in specific connection with plasma display panels having row and column electrodes, it will be appreciated that the invention is equally well applicable to driving circuits for plasma display panels having external electrode pairs of other types.

What is claimed is:

1. A circuit for driving an external electrode discharge display panel having a plurality of gas discharge cells, a first and a second group of electrodes disposed on opposite sides of said cells, and means for cyclically supplying a first pulse train of a predetermined duration to the electrodes of said first group, wherein the improvement comprises means for supplying a second pulse train to each electrode of said second group, said second pulse train supplying means comprising means for supplying pulses of a polarity opposite to the pulses of said first pulse train and substantially coincident with said first pulse train when the display discharge cell associated with the first and second group electrodes respectively receiving said first and second pulse trains is to glow, and means for otherwise supplying pulses of the same polarity as the pulses of said first pulse train wherein said first and second pulse train supplying means supply a direct-current voltage component to the cells while said first pulse train is not supplied to the electrodes of said first pulse train is not supplied to the electrodes of said first electrode group disposed on one side of said cells.

2. A combination as in claim 1, wherein said discharge cells are characterized by a firing potential $V_F$ and a glow abating potential $V_{gb}$ and wherein said first and second pulse train supplying means supply pulses of a voltage amplitude $V_1$ and $V_2$ where $V_1$, $V_2$, $V_F$ and $V_{gb}$ are real numbers wherein $2(V_F+V_{gb}) = V_1 = V_2 = V_F - V_{gb}$.

3. A circuit for driving an external electrode discharge display panel having a plurality of gas discharge cells, a first and a second group of electrodes disposed on opposite sides of said cells, and means for cyclically supplying a first pulse train of a predetermined duration to the electrodes of said first group, wherein the improvement comprises means for supplying a second pulse train to each electrode of said second group, said second pulse train supplying means comprising means for supplying pulses of a polarity opposite to the pulses of said first pulse train to each electrode of said second group, said second pulse train supplying means comprising means for supplying pulses of a polarity opposite to the pulses of said first pulse train to each electrode of said second group, said second pulse train supplying means comprising means for supplying pulses of a polarity opposite to the pulses of said first pulse train to each electrode of said second group.

* * * * *
UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,869,644 Dated March 4, 1975
Inventor(s) Yano; Sato and Iwakawa

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Claim 1, column 8, line 12, "pulse train is not supplied to the" should be deleted;

line 13, "electrodes of said first" should be deleted.

Claim 2, column 8, line 17, "whereins aid" should be --wherein said--.

Claim 3, column 8, line 30, "oppostie to the pulse" should be --opposite to the pulses--;

line 31, "traiin" should be deleted and the following substituted therefor --of said first pulse train and substantially coincident with said first pulse train when--;

line 37, after "means" insert --and a control signal generator for supplying first and second control signals to said first and second pulse train supplying means--;

line 46, "AND" should be --AND--.

Signed and sealed this 15th day of July 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks