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KATOU et al.(10) **Pub. No.: US 2017/0047316 A1**(43) **Pub. Date: Feb. 16, 2017**(54) **SEMICONDUCTOR DEVICE****H01L 29/78** (2006.01)**H01L 29/10** (2006.01)(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**,
Tokyo (JP)(52) **U.S. Cl.**CPC **H01L 27/0211** (2013.01); **H01L 29/7813**
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Kanazawa Ishikawa (JP)(21) Appl. No.: **15/057,046**(22) Filed: **Feb. 29, 2016**(30) **Foreign Application Priority Data**

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A semiconductor device includes a first semiconductor region of a first conductivity type, a plurality of second semiconductor regions of a second conductivity type, each comprising a first part, on the first semiconductor region, wherein the second semiconductor regions are spaced apart in a first direction, a third semiconductor region of the first conductivity type on each of the second semiconductor regions, an insulation portion between two of the second semiconductor regions, the insulation portion having one side in contact with one of the first parts and the other side in contact with one of the third semiconductor regions, a first electrode within the insulation portion, a gate electrode spaced apart from the first electrode and within the insulation portion, and a second electrode on the third semiconductor region and electrically connected to the first electrode and the third semiconductor region.

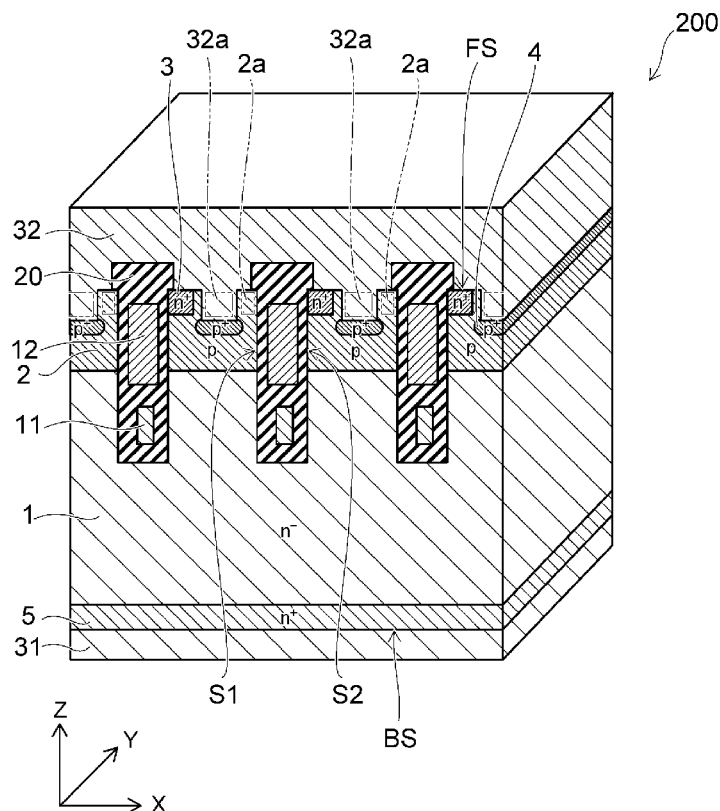


FIG. 1

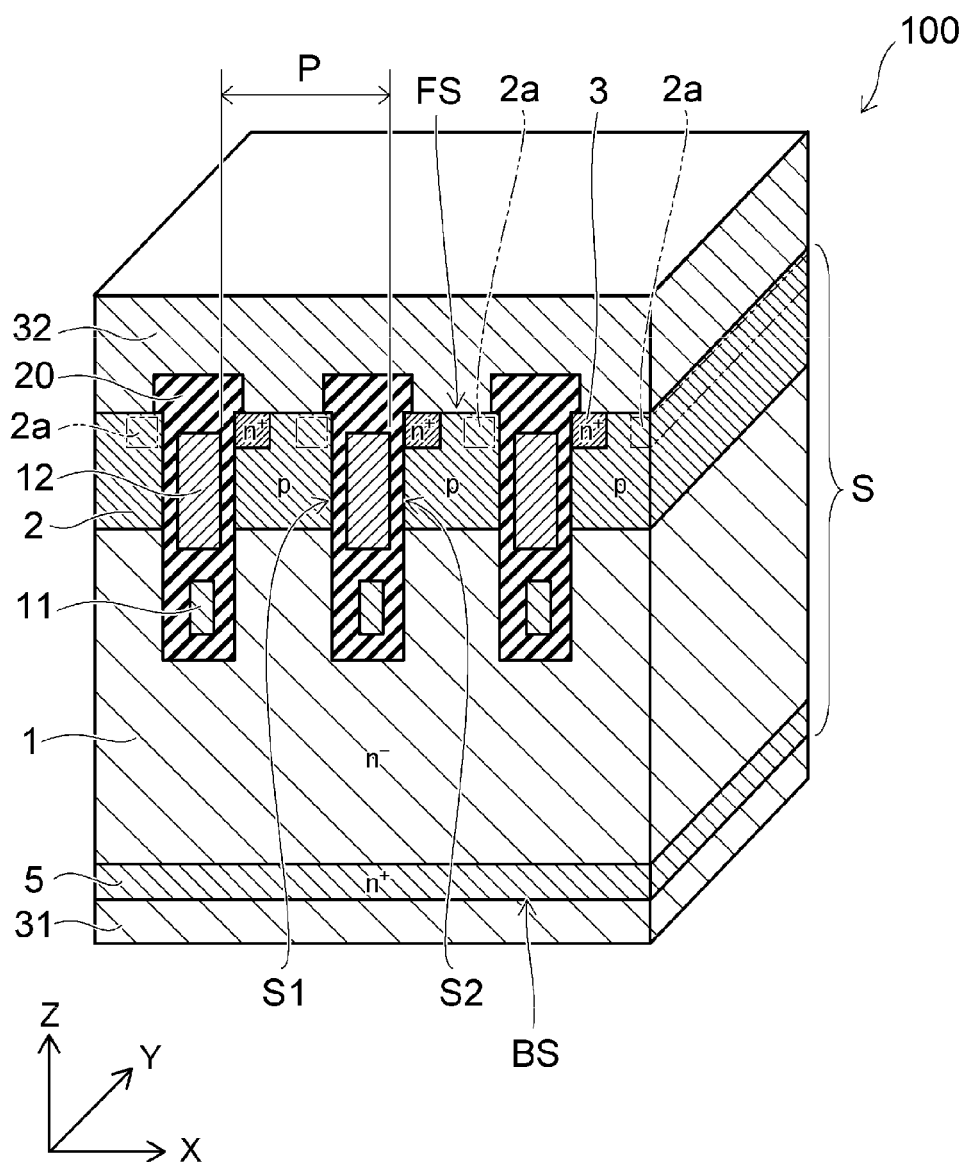


FIG. 2A

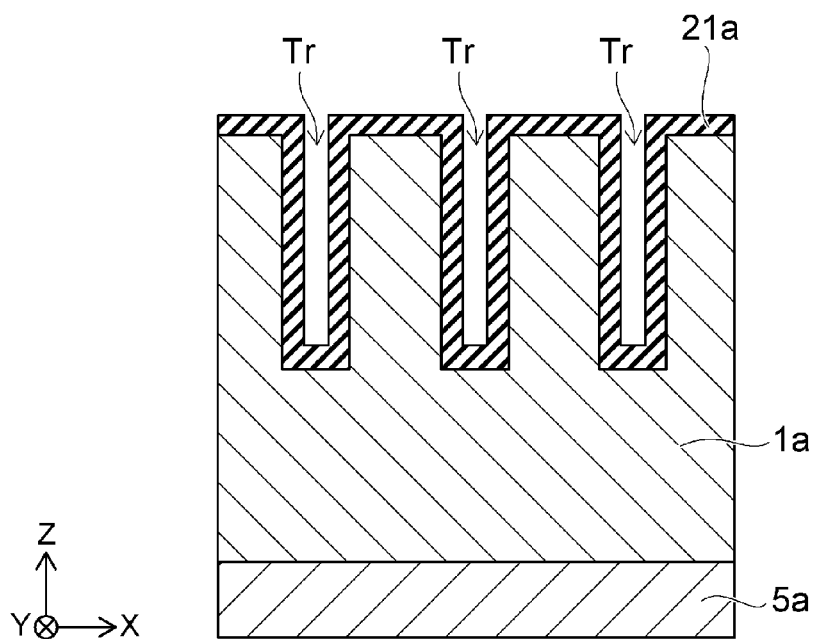


FIG. 2B

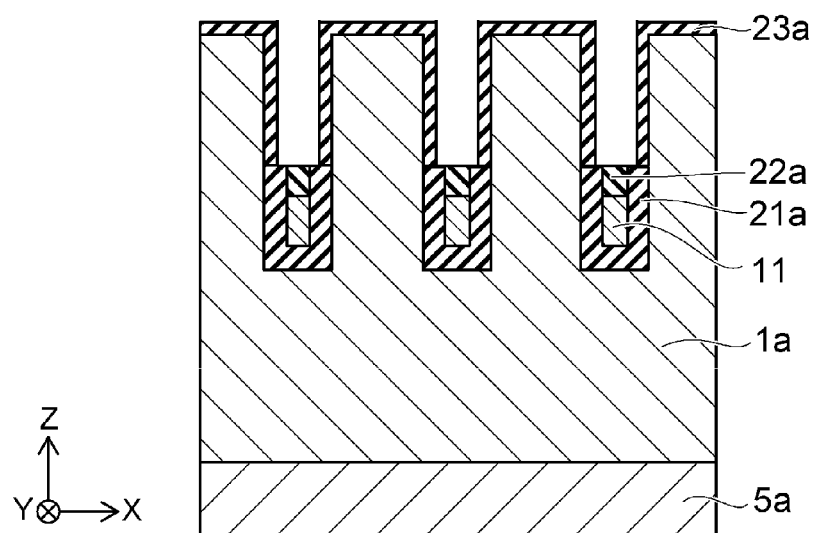


FIG. 3A

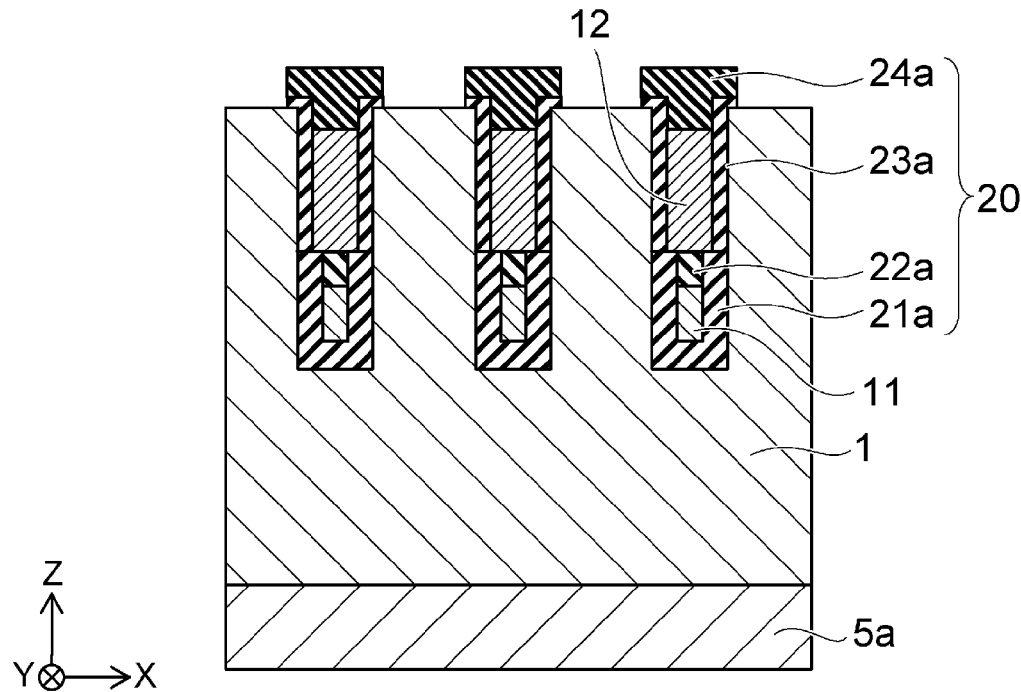


FIG. 3B

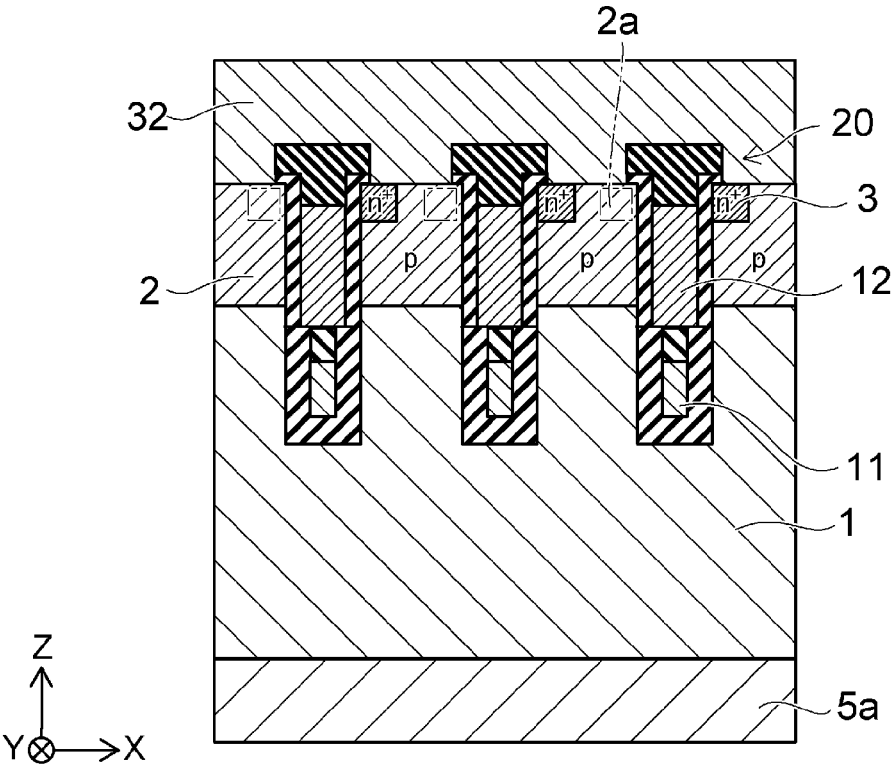
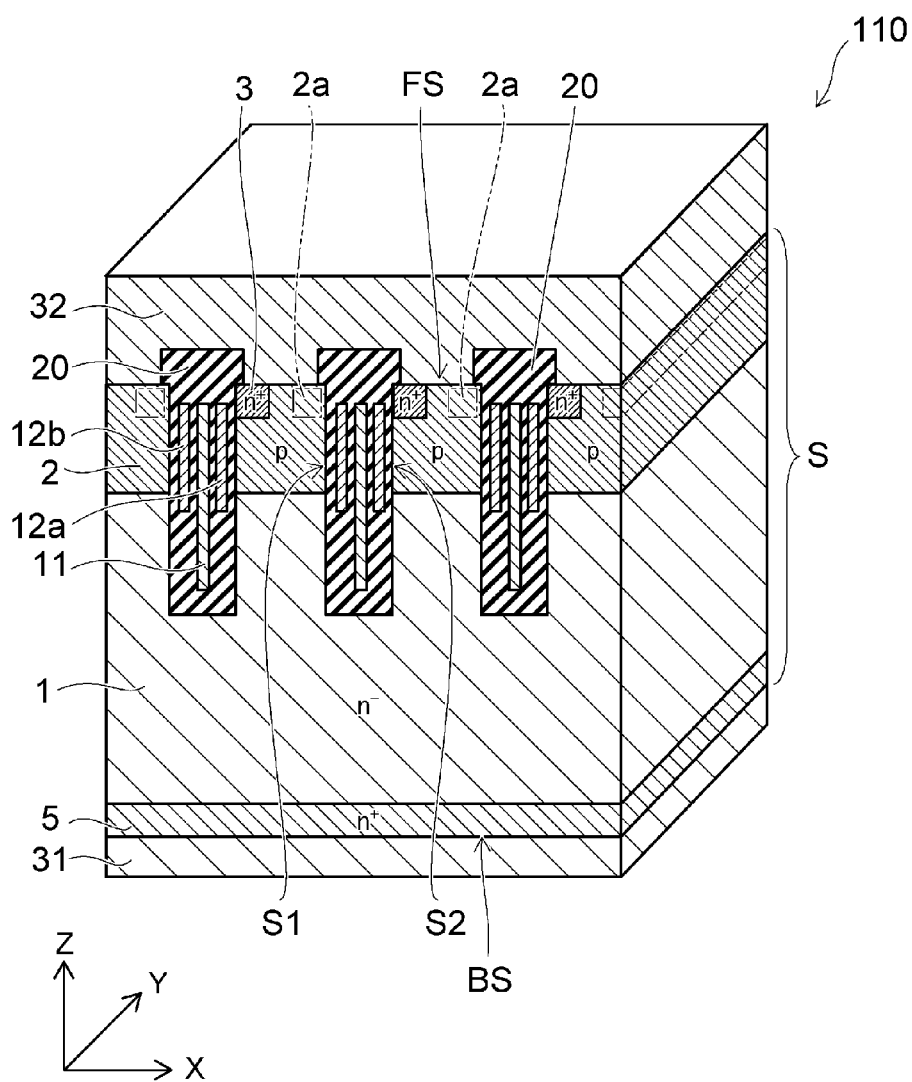


FIG. 4



SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-158364, filed Aug. 10, 2015, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

[0003] A semiconductor device such as a metal oxide semiconductor field effect transistor (MOSFET) is used to control electric power, for example. Such a semiconductor device is used for various purposes, including uses under a high temperature environment.

[0004] However, there is a concern that the semiconductor device might break as a result of stresses caused by heat, when the semiconductor device is used under the high temperature environment.

DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a perspective sectional view illustrating a part of a semiconductor device according to a first embodiment.

[0006] FIGS. 2A and 2B are cross-sectional views illustrating results of the manufacturing process of the semiconductor device according to the first embodiment.

[0007] FIGS. 3A and 3B are cross-sectional views illustrating results of the manufacturing process of the semiconductor device according to the first embodiment.

[0008] FIG. 4 is a perspective sectional view illustrating a part of the semiconductor device according to a modified example of the first embodiment.

[0009] FIG. 5 is a perspective sectional view illustrating a part of the semiconductor device according to a second embodiment.

DETAILED DESCRIPTION

[0010] Embodiments provide a semiconductor device capable of suppressing heat-caused breakage.

[0011] In general, according to one embodiment, a semiconductor device includes a first semiconductor region of a first conductivity type, a plurality of second semiconductor regions of a second conductivity type, each comprising a first part, on the first semiconductor region, wherein the second semiconductor regions are spaced apart in a first direction and extend in a second direction crossing the first direction, a third semiconductor region of the first conductivity type on each of the second semiconductor regions, the third semiconductor regions extending in the second direction parallel to the first parts, an insulation portion between two of the second semiconductor regions, the insulation portion having one side in contact with one of the first parts and the other side in contact with one of the third semiconductor regions, a first electrode separated from the first semiconductor region in the first direction by the insulation portion, a gate electrode spaced apart from the first electrode, and separated from the second semiconductor region

in the first direction by the insulation portion, and a second electrode on the third semiconductor region, and electrically connected to the first electrode and the third semiconductor region.

[0012] Hereinafter, the embodiments will be described with reference to drawings.

[0013] Moreover, the drawings are schematic or conceptual, a relationship between a thickness and a width of each part, and a ratio in size between the parts are not always the same as those in an actual semiconductor device. Also, even when the same two parts are described, one part may be illustrated in different size or ratio from the other part.

[0014] In addition, in this specification and each drawing, the same components as illustrated in the previous drawings are given the same reference numbers and a detailed description thereof will not be repeated.

[0015] Each of the embodiments will be described with reference to an XYZ orthogonal coordinate system. Two directions intersecting with each other in a direction parallel to a surface of the semiconductor layer S are respectively set to an X-direction (second direction) and a Y-direction (third direction), and a direction perpendicular to both of the X-direction and the Y-direction is set to a Z-direction (first direction).

[0016] In a description hereinafter, n^+ , n^- , and p^+ , p^- indicate relative high and low levels of an impurity concentration in each of conductivity types. That is, the n^+ indicates an n-type impurity concentration relatively higher than the n^- . In addition, the p^+ indicates a p-type impurity concentration relatively higher than the p^- .

[0017] In each of the embodiments described hereinafter, a p-type and an n-type of each of semiconductor regions may be reversed, and this may be applied to each of the embodiments.

First Embodiment

[0018] An example of a semiconductor device according to a first embodiment will be described with reference to FIG. 1. FIG. 1 is a perspective sectional view illustrating a part of a semiconductor device 100 according to the first embodiment.

[0019] The semiconductor device 100 is, for example, a MOSFET. The semiconductor device 100 includes an n^+ type (first conductivity type) drain region 5, an n^- type semiconductor region 1 (first semiconductor region), a p type (second conductivity type) base region 2 (second semiconductor region), an n^+ type source region 3 (third semiconductor region), an insulation portion 20, a field plate electrode 11 (first electrode), a gate electrode 12, a drain electrode 31, and a source electrode 32 (second electrode).

[0020] The source electrode 32 is provided on a front surface FS of a semiconductor layer S. The drain electrode 31 is formed on a back surface BS of the semiconductor layer S.

[0021] The n^+ type drain region 5 is provided on the back surface BS side of the semiconductor layer S. The n^+ type drain region 5 is electrically connected to the drain electrode 31.

[0022] The n^- type semiconductor region 1 is provided on the n^+ type drain region 5.

[0023] The p^- type base region 2 is selectively provided on the n^- type semiconductor region 1. A plurality of p^- type

base regions **2** are formed spaced apart in the X-direction, and each of the p⁻ type base regions **2** extends in a Y-direction.

[0024] The p⁻ type base region **2** includes a first part **2a** provided on the front surface FS side. A p-type impurity concentration of the first part **2a** may be equal to or higher than the p-type impurity concentration of the other part of the p⁻ type base region **2**.

[0025] The n⁺ type source region **3** is selectively provided on the p⁻ type base region **2**. A plurality of n⁺ type source regions **3** are provided spaced apart in the X-direction, and each of the n⁺ type source regions **3** extends in the Y-direction.

[0026] The n⁺ type source region **3** and the first part **2a** of the p⁻ type base region **2** are arranged in the X-direction and extend in the Y direction parallel with each other. The first part **2a** and the n⁺ type source region **3** are alternately arranged in the X-direction.

[0027] The field plate electrode (hereinafter, refer to as FP electrode) **11** and the gate electrode **12** are surrounded by the insulation portion **20** in an X-Z plane direction.

[0028] The FP electrode **11** is surrounded by the n⁻ type semiconductor region **1** through the insulation portion **20** in an X-Z plane direction.

[0029] The gate electrode **12** is provided over the FP electrode **11**, and faces the p⁻ type base region **2** through the insulation portion **20** in the X-direction. The gate electrode **12** is spaced from the FP electrode **11** in a Z-direction (direction from n⁻ type semiconductor region **1** toward p⁻ type base region **2**).

[0030] The FP electrode **11**, the gate electrode **12**, and the insulation portion **20** are provided in multiple in the X-direction, and each of these electrodes extends in the Y-direction.

[0031] The insulation portion **20** includes a first surface S1 and a second surface S2 opposite the first surface S1. The first surface S1 and the second surface S2 are respectively along the Y-direction and the Z-direction. A part of the first surface S1 comes into contact with the first part **2a**, and a part of the second surface S2 comes into contact with the n⁺ type source region **3**.

[0032] On the p⁻ type base region **2**, the n⁺ type source region **3**, and the insulation portion **20**, a source electrode **32** is provided. The source electrode **32** is electrically connected to the p⁻ type base region **2**, the n⁺ type source region **3**, and the FP electrode **11**.

[0033] In a state in which a positive voltage with respect to the source electrode **32** is applied to the drain electrode **31**, a MOSFET is turned on by applying a voltage equal to or more a threshold to the gate electrode **12**. At this time, a channel (reverse layer) is formed on a region near the insulation portion **20** of the p⁻ type base region **2**.

[0034] When the MOSFET is turned off and a negative potential is applied to the drain electrode **31** with respect to a potential of the source electrode **32**, a depletion layer broadens from an interfacial surface between the insulation portion **20** and the n⁻ type semiconductor region **1** toward the n⁻ type semiconductor region **1**. This is because of the FP electrode **11** connected to the source electrode **32** is provided under the gate electrode **12**. The broadening of the depletion layer from the interfacial surface of the insulation portion **20** and the n⁻ type semiconductor region **1** causes an increase in the breakdown voltage increased.

[0035] Next, an example of a manufacturing method of the semiconductor device **100** according to the first embodiment will be described with reference to FIG. 2A to FIG. 3B.

[0036] FIG. 2A to FIG. 3B are cross-sectional views illustrating the results of steps of a manufacturing process of the semiconductor device **100** according to the first embodiment.

[0037] First, a semiconductor substrate in which the n⁻ type semiconductor layer **1a** is provided on the n⁺ type semiconductor layer **5a** is prepared. A main component of the n⁺ type semiconductor layer **5a** and the n⁻ type semiconductor layer **1a** is silicon, silicon carbide, gallium arsenide, or gallium nitride.

[0038] Hereinafter, a case in which the main component of the n⁺ type semiconductor layer **5a** and the n⁻ type semiconductor layer **1a** is silicon will be described.

[0039] Next, a plurality of trenches Tr are formed on the n⁻ type semiconductor layer **1a**. Subsequently, as illustrated in FIG. 2A, an upper surface of the n⁻ type semiconductor layer **1a** and an inner wall of the trench Tr are thermally oxidized, and thus, the insulation layer **21a** including silicon oxide is formed. A layer including silicon nitride may be further formed on the insulation layer **21a**.

[0040] Next, a conductive layer including polysilicon is formed on the insulation layer **21a**. By etching back the conductive layer, the FP electrode **11** which is provided inside of each of the trenches Tr is formed. Subsequently, an upper surface of the FP electrode **11** is thermally oxidized, and thus the insulation layer **22a** is formed.

[0041] Next, the insulation layer **21a** which is located higher than the insulation layer **22a** is removed, and the upper surface of the n⁻ type semiconductor layer **1a** and a part of the inner wall of the trench Tr are exposed. The exposed surfaces are thermally oxidized, and thus, the insulation layer **23a** is formed as illustrated in FIG. 2B. A film thickness of the insulation layer **23a** is thinner than, for example, a film thickness of the insulation layer **21a**.

[0042] Next, the conductive layer is formed on the insulation layer **22a** and on the insulation layer **23a**. By etching back the conductive layer, the gate electrode **12** which is provided inside each of the trenches Tr is formed. Subsequently, an insulation layer **24a** covering the n⁻ type semiconductor layer **1a**, the insulation layer **23a** and the gate electrode **12** is formed. By patterning the insulation layers **23a** and **24a**, the insulation portion **20** including the insulation layers **21a** to **24a** is formed as illustrated in FIG. 3A.

[0043] Next, a p-type impurity and an n-type impurity are sequentially ion-implanted in the front surface FS of the n⁻ type semiconductor layer **1a**, and the p⁻ type base region **2** and the n⁺ type source region **3** are formed. At this time, the p⁻ type base region **2** and the n⁺ type source region **3** are formed so that the n⁺ type source region **3** is positioned at one side of the insulation portion **20**, and the first part **2a** is positioned at the other side thereof. That is, the n⁺ type source region **3** is formed on only one side of the insulation portion **20**. In the n⁻ type semiconductor layer **1a**, a region other than the p⁻ type base region **2** and the n⁺ type source region **3** corresponds to the n⁻ type semiconductor region **1**.

[0044] Next, a metal layer covering the semiconductor region and the insulation portion **20** is formed. By patterning the metal layer, the source electrode **32** is formed as illustrated in FIG. 3B.

[0045] Next, the back surface BS of the n⁺ type semiconductor layer **5a** is ground until the n⁺ type semiconductor

layer 5a achieves a predetermined thickness. The n⁺ type drain region 5 is formed by a process described above.

[0046] After that, the drain electrode 31 is formed under the n⁺ type drain region 5, thereby obtaining the semiconductor device 100 as illustrated in FIG. 1.

[0047] Here, an action and an effect according to the embodiment will be described.

[0048] According to the embodiment, heat-caused breakage of the semiconductor device can be suppressed while reducing the on-resistance of the semiconductor device.

[0049] Means for solving the above problems are as follows.

[0050] The semiconductor device includes the FP electrode 11, thereby making it possible to increase the breakdown voltage of the semiconductor device. For this reason, the impurity concentration in the n⁻ type semiconductor region 1 is increased as much as the breakdown voltage is increased by the FP electrode 11, and thus the on-resistance of the semiconductor device can be reduced.

[0051] At this time, as an interval between the FP electrodes 11 becomes narrower, the impurity concentration in the n⁻ type semiconductor region 1 can be increased.

[0052] Meanwhile, when making the interval between the FP electrodes 11 narrow, an interval between the gate electrodes 12 also becomes narrow. That is, an interval between the channels formed by the gate electrode 12 also becomes narrow. When making the interval between the channels narrow, overlapping of paths of current which flows in the n⁻ type semiconductor region 1 through the channel becomes significant. When overlapping of current paths becomes significant, an amount of heat generation in the n⁻ type semiconductor region 1 increases, and a possibility that heat-caused breakage of the semiconductor device also increases.

[0053] However, in the semiconductor device according to the embodiment, the first part 2a, which is arranged in the n⁺ type source region 3 in the X-direction and comes into contact with the insulation portion 20, is provided. In other words, the n⁺ type source region 3 is provided on only one side of the insulation portion 20.

[0054] By adopting such a configuration, the interval between the channels formed at the time of applying the voltage to the gate electrode 12 can be broadened. For this reason, overlapping of paths of the current, which flows in the n⁻ type semiconductor region 1 through each of the channels, is reduced, and the heat generation in the n⁻ type semiconductor region 1 is suppressed. As a result, the heat-caused breakage of the semiconductor device can be suppressed.

[0055] The heat generation by overlapping of the current paths can be a problem, for example, particularly, when a pitch between the gate electrodes 12 is 2.0 μm or less, and the impurity concentration in the n⁻ type semiconductor region 1 is 1.0×10¹⁶ atm/cm³ or more. This is because, at the pitch between the gate electrodes 12 of 2 μm or less, the overlapping width of the current paths becomes significant, and, when the impurity concentration in the n⁻ type semiconductor region 1 is high, the current path in the n⁻ type semiconductor region 1 is likely to widen, and overlapping between the current paths becomes significant.

[0056] Accordingly, the embodiment is particularly effective in a semiconductor device which has the pitch between the gate electrodes 12 and the impurity concentration in the n⁻ type semiconductor region 1 as described above.

[0057] Meanwhile, between the insulation portions 20, in order to easily form the first part 2a and the n⁺ type source region 3, the pitch between the gate electrodes 12 is preferably 0.8 μm or more. Also, when the pitch between the gate electrodes 12 is 0.8 μm or more, from a point of the breakdown voltage of the semiconductor device, the impurity concentration in the n⁻ type semiconductor region 1 is preferably 8.0×10¹⁶ atm/cm³ or less.

[0058] As used herein, “pitch” means an interval between the gate electrodes 12 which are arranged side by side. In an example illustrated in FIG. 1, the pitch is equal to a distance P between end portions of each of the gate electrodes 12 in the X-direction.

[0059] The n⁺ type source region 3 is provided on only one side of the insulation portion 20, and two first parts 2a and two n⁺ type source regions 3 can also be arranged alternatively in the X-direction. That is, two n⁺ type source regions 3 are provided on either side of a gate electrode 12 on a part of the p⁻ type base region 2, and the two first parts 2a can also be provided on either side of a gate electrode 12 on the other part of the p⁻ type base region 2.

[0060] However, as illustrated in FIG. 1, overlapping of the current paths can be further reduced, and the heat generation in the n⁻ type semiconductor region 1 can be further suppressed in a case in which the first part 2a and the n⁺ type source region 3 are arranged alternatively in the X-direction compared to a case in which the two first parts 2a and the two n⁺ type source regions 3 are arranged alternatively in the X-direction.

Modified Example

[0061] With reference to FIG. 4, a part of the semiconductor device according to a modified example of the first embodiment will be described.

[0062] FIG. 4 is a sectional view illustrating a part of the semiconductor device 110 according to the modified example of the first embodiment.

[0063] The semiconductor device 110 according to the modified example has a different configuration of the FP electrode 11 and the gate electrode 12 compared to the semiconductor device 100.

[0064] Specifically, as illustrated FIG. 4, the semiconductor device 110 includes the FP electrode 11, the gate electrodes 12a and 12b which are separated from each other and arranged on either side of the FP electrode 11 in the X-direction in parallel with each other. The gate electrodes 12a and 12b are thus provided between the FP electrode 11 and each of the p⁻ type base regions 2.

[0065] Also in the embodiment, in the same manner in the embodiment illustrated in FIG. 1, since the n⁺ type source region 3 is provided on only one side of the insulation portion 20, on-resistance thereof can be reduced, and heat-caused breakage of the semiconductor device can be suppressed.

[0066] However, it is possible to further reduce areas of facing surfaces of the FP electrode 11 and the gate electrode 12 in a case in which the FP electrode 11 and the gate electrode 12 are spaced apart in the Z-direction, compared to a case in which the FP electrode 11 and the gate electrode 12 are spaced apart in the X-direction. When facing areas of the FP electrode 11 and the gate electrode 12 are reduced, a capacity between the FP electrode 11 (source electrode 32) and the gate electrode 12 can be reduced.

[0067] That is, according to the semiconductor device 100 illustrated in FIG. 1, compared to the semiconductor device 110 according to the modified example, when a voltage is applied to the gate electrode 12 until a voltage equal to or more than a threshold is applied to the gate electrode 12, a time during the semiconductor device is turned on can be reduced.

[0068] In addition, a length of the insulation portion 20 in the X-direction becomes greater in a case in which the FP electrode 11 and the gate electrode 12 are spaced in the Z-direction compared to a case in which the FP electrode 11 and the gate electrode 12 are spaced in the X-direction. For this reason, according to the semiconductor device 100 illustrated in FIG. 1, compared to the semiconductor device 110 according to the modified example, channel density increases, and thus the on-resistance can be reduced.

[0069] Meanwhile, when the channel density increases, as described above, heat generation amount due to overlapping of the current paths increases. Accordingly, suppressing the heat generation amount of the semiconductor device by providing the first part 2a is further effective in the semiconductor device 100 in which the FP electrode 11 and the gate electrode 12 are arranged in the Z-direction.

[0070] As illustrated in FIG. 4, when the FP electrode 11 and the gate electrode 12 are spaced apart in the X-direction, the heat generation due to overlapping of the current paths causes a problem particularly, for example, when the pitch between the gate electrodes 12 is equal to or less than 4.5 μm , and the impurity concentration in the n^- type semiconductor region 1 is equal to or more than $0.5 \times 10^{16} \text{ atm/cm}^3$.

[0071] Accordingly, the modified example is effective particularly in the semiconductor device having the pitch between the gate electrodes 12 and the impurity concentration in the n^- type semiconductor region 1 as described above.

[0072] Meanwhile, in order to easily form the first part 2a and the n^+ type source region 3 between the insulation portions 20, the pitch between the gate electrodes 12 is preferably 2.5 μm or more. In addition, when the pitch between the gate electrodes 12 is 2.5 μm or more, in terms of the breakdown voltage of the semiconductor device, the impurity concentration in the n^- type semiconductor region 1 is preferably $2.5 \times 10^{16} \text{ atm/cm}^3$ or less.

Second Embodiment

[0073] An example of the semiconductor device according to a second embodiment will be described with reference to FIG. 5.

[0074] FIG. 5 is a sectional view illustrating a part of a semiconductor device 200 according to a second embodiment.

[0075] In the semiconductor device 200 according to a second embodiment, it is different in that the source electrode 32 includes a first electrode part 32a, and a p^+ type contact region (fourth semiconductor region) is further included when compared to the semiconductor device 100.

[0076] As illustrated in FIG. 5, the source electrode 32 includes the first electrode part 32a provided between the first part 2a and the n^+ type source region 3. The first electrode part 32a is positioned between the adjacent insulation portions 20 in the X-direction.

[0077] Alternatively, the first part 2a is not only provided between the first electrode part 32a and the insulation

portion 20, but the first electrode part 32a also comes into contact with the insulation portion 20.

[0078] The p^+ type contact region 4 is provided between the first electrode part 32a and the p^- type base region 2. As illustrated in FIG. 5, a lower end of the first electrode part 32a may be surrounded by a part of the p^+ type contact region 4 along the X-Y plane.

[0079] The semiconductor device 200 can be manufactured by, for example, a method as follows.

[0080] First, processes same as the processes illustrated in FIG. 2A to FIG. 3A are performed. Subsequently, the p^- type base region 2 and the n^+ type source region 3 are formed. Subsequently, apart of a region where the n^+ type source region 3 is not provided in the p^- type base region 2 is removed, and a trench is formed.

[0081] When the p-type impurity is ion-implanted into a part of the p^- type base region 2 through the formed trench, the p^+ type contact region 4 is formed. Subsequently, the metal layer is formed so as to embed the trench, and the source electrode 32 is formed. After that, in the same manner as a manufacturing method of the semiconductor device 100, a rear surface of the n^+ type semiconductor layer 5a is ground and the drain electrode 31 is formed, thereby obtaining the semiconductor device 200.

[0082] Here, actions and effects of the embodiment will be described.

[0083] When the semiconductor device 200 is turned off, a surge voltage is applied to the drain electrode 31 by an inductance of the semiconductor device 200. When a potential of the p^- type base region 2 increases by the surge voltage, there is a case where a parasitic bipolar transistor included in the semiconductor device 200 enters a latch-up state. When the semiconductor device is used under a high temperature, current flowing when the parasitic bipolar transistor is in the latch-up state is also great, and the semiconductor device further generates heat by the current, whereby a possibility of the heat-caused breakage of the semiconductor device is likely to be increased.

[0084] In the embodiment, the semiconductor device includes the first electrode part 32a and p^+ type contact region 4, and thus an electric resistance between the p^- type base region 2 and the source electrode 32 can be reduced. When the electric resistance between the p^- type base region 2 and the source electrode 32 is reduced, the increase of the potential of the p^- type base region 2 at the time of applying the surge voltage to the drain electrode 31 can be suppressed. For this reason, the latch-up state of the parasitic bipolar transistor is suppressed, and the heat-caused breakage of the semiconductor device is also suppressed.

[0085] Further, in the semiconductor device according to the embodiment, the first electrode part 32a is provided between the n^+ type source region 3 and the first part 2a. According to such a configuration, compared to a case in which the n^+ type source region 3 is formed on both sides of the insulation portion 20, and a part of the source electrode 32 is embedded between the n^+ type source regions 3, a length of the first electrode part 32a in the X-direction and a length of the p^+ type contact region 4 in the X-direction can be formed to be greater.

[0086] For this reason, compared to a case in which the n^+ type source region is provided on both side of the insulation portion 20, the electric resistance between the p^- type base region 2 and the source electrode 32 can be further reduced.

[0087] In addition, in the embodiment, the first part 2a is formed between the first electrode part 32a and the insulation portion 20. By adopting such a configuration, when the trench for forming the first electrode part 32a is formed on the front surface of the base region 2, a possibility of etching the insulation portion 20 due to a deviation of a mask position, or the like can be reduced, and thus a yield of the semiconductor device can be improved.

[0088] Moreover, with respect to the semiconductor device 200 according to the embodiment, as a modified example of the first embodiment illustrated in FIG. 4, a structure in which the FP electrode 11 and the gate electrode 12 are arranged in the X-direction can be also applied.

[0089] In each of embodiments described above, a relative high and low level of the impurity concentration between each of the semiconductor regions can be recognized using, for example, a scanning capacitance microscope (SCM). Moreover, a concentration of carriers in each of the semiconductor regions can be the same as the impurity concentration active in each of the semiconductor regions. Accordingly, a relative high and low level of the concentration of the carriers between each of the semiconductor regions can be also recognized using the SCM.

[0090] In addition, the impurity concentration in each of the semiconductor region can be measured by, for example, a secondary ion mass spectrometry (SIMS).

[0091] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions. In regard to a specific configuration of each of components such as the n⁺ type drain region 5, the n⁻ type semiconductor region 1, the p⁻ type base region 2, the n⁺ type source region 3, p⁺ type contact region 4, the FP electrode 11, the gate electrode 12, the insulation portion 20, the drain electrode 31, and the source electrode 32, which are included in the embodiment, a person skilled in the art can appropriately select from a well-known technology. In addition, each of the embodiments described above can be performed by combining with each other.

1. A semiconductor device comprising:

- a first semiconductor region of a first conductivity type;
- a plurality of second semiconductor regions of a second conductivity type, each comprising a first part, on the first semiconductor region, wherein the second semiconductor regions are spaced apart in a first direction and extend in a second direction crossing the first direction;
- a third semiconductor region of the first conductivity type on each of the second semiconductor regions, the third semiconductor regions extending in the second direction parallel to the first parts;
- an insulation portion between two of the second semiconductor regions, the insulation portion having one side in contact with one of the first parts and the other side in contact with one of the third semiconductor regions;

- a first electrode separated from the first semiconductor region in the first direction by the insulation portion;
- a gate electrode spaced apart from the first electrode, and separated from the second semiconductor region in the first direction by the insulation portion; and
- a second electrode on the third semiconductor region, and electrically connected to the first electrode and the third semiconductor region.

2. The device according to claim 1,

wherein surfaces of the insulation portion in contact with one of the first parts and one of the third semiconductor regions are opposite surfaces of the insulation portion in the first direction.

3. The device according to claim 1,

wherein the second electrode includes a protruding portion that extends between one of the third semiconductor regions and one of the first parts.

4. The device according to claim 3, further comprising: a fourth semiconductor region of the second conductivity type between the second semiconductor region and the protruding portion of the second electrode,

wherein a concentration of carriers of the second conductivity type in the fourth semiconductor region is higher than a concentration of carriers of the second conductivity type in the second semiconductor region.

5. The device according to claim 1,

wherein a plurality of the third semiconductor region, the insulation portion, the first electrode, and the gate electrode is arranged in the first direction, and wherein each of the third semiconductor regions is provided on a different one of the second semiconductor regions and in contact with one of the insulation portions that surrounds one of the gate electrodes and one of the first electrodes.

6. The device according to claim 5,

wherein the first parts of the second semiconductor regions and the third semiconductor regions are alternately arranged in the first direction and not in contact with each other.

7. The device according to claim 6,

wherein the spacing between the multiple gate electrodes is 2.0 μm or less, and a concentration of carriers of the first conductivity type in the first semiconductor region is 1.0×10^{16} atm/cm³ or more.

8. The device according to claim 1,

wherein the spacing between the gate electrodes is 0.8 μm or more and a concentration of carriers of the first conductivity type in the first semiconductor region is 8.0×10^{16} atm/cm³ or less.

9. The device according to claim 1,

wherein a concentration of carriers of the second conductivity type in a portion of the first part of the second semiconductor region is equal to or higher than a concentration of carriers of the second conductivity type in other parts of the second semiconductor region.

10. A semiconductor device comprising:

- a first semiconductor region of a first conductivity type;
- a second semiconductor region of a second conductivity type on the first semiconductor region;
- first and second electrodes, each extending within the second semiconductor region in a first direction, the first and second electrodes being spaced from each another in a second direction crossing the first direction;

a first insulation layer separating the first electrode from the second semiconductor region and a second insulation layer separating the second electrode from the second semiconductor region; and

a third semiconductor region of the first conductivity type between the first and second insulation layers and in contact with the first insulation layer and not with the second insulation layer.

11. The device of claim **10**, further comprising a portion of the second semiconductor region between the first and second insulation layers and in contact with the second insulation layer and not with the first insulation layer, the portion of the second semiconductor region having a higher concentration of carriers of the second conductivity type than other portions of the second semiconductor region between the first and second insulation layers.

12. The device of claim **11**, further comprising a source electrode in contact with the second semiconductor region and the third semiconductor region.

13. The device according to claim **12**, wherein the source electrode includes a protruding portion that extends between third semiconductor region and the portion of the second semiconductor region.

14. The device according to claim **13**, further comprising: a fourth semiconductor region of the second conductivity type between the second semiconductor region and the protruding portion of the source electrode, wherein a concentration of carriers of the second conductivity type in the fourth semiconductor region is higher than a concentration of carriers of the second conductivity type in the second semiconductor region.

15. The device of claim **10**, further comprising: a first field plate electrode within the first insulation layer and separated from the first electrode in the first direction by the first insulation layer, the first field plate electrode being separated from the first semiconductor region in the second direction by the first insulation layer; and

a second field plate electrode within the second insulation layer and separated from the second electrode in the first direction by the second insulation layer, the second

field plate electrode being separated from the first semiconductor region in the second direction by the second insulation layer.

16. The device of claim **10**, wherein the first and second electrodes are gate electrodes and the spacing between the first and second electrodes is 0.8 μm or more.

17. The device of claim **10**, wherein the first and second electrodes are gate electrodes and the spacing between the first and second electrodes is 2.0 μm or less.

18. A method of manufacturing a semiconductor device, comprising:

providing a first semiconductor region of a first conductivity type;

forming first and second gate electrodes respectively within first and second insulation regions to be spaced apart in a first direction on either side of a second semiconductor region of a second conductivity type that is on the first semiconductor region; and

forming a third semiconductor region of the first conductivity type on the second semiconductor region between the first and second insulation regions, the third semiconductor region being in contact with the first insulation region and not with the second insulation region.

19. The method of claim **18**, further comprising:

ion-implanting carriers of the second conductivity type into a portion of the second semiconductor region, the portion having a concentration of carriers of the second conductivity type higher than other portions second semiconductor region between the first and second insulation regions and being in contact with the second insulation region and not with the first insulation region.

20. The method according to claim **19**, further comprising:

forming a source electrode to be in contact with the second and third semiconductor regions and the portion of the second semiconductor region.

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