



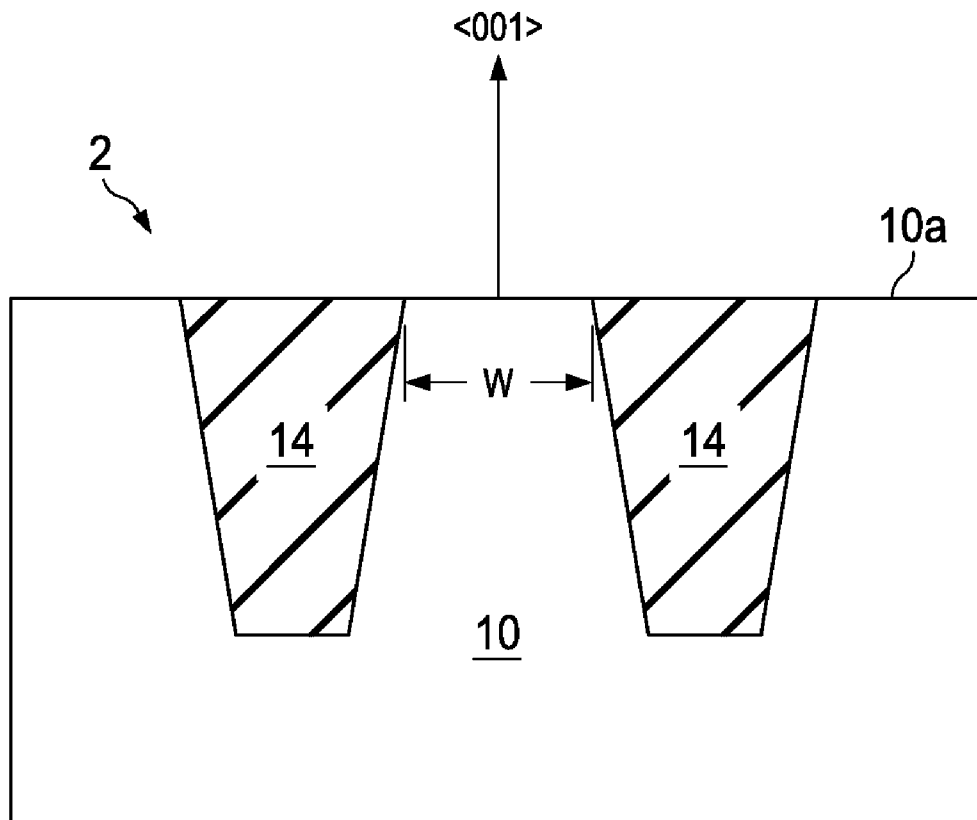
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Wann et al.(10) **Pub. No.: US 2014/0033981 A1**(43) **Pub. Date: Feb. 6, 2014**(54) **MOCVD FOR GROWING III-V COMPOUND
SEMICONDUCTORS ON SILICON
SUBSTRATES****Publication Classification**

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LTD.**, Hsin-Chu (TW)(21) Appl. No.: **14/046,360**(22) Filed: **Oct. 4, 2013****Related U.S. Application Data**(63) Continuation of application No. 12/814,088, filed on
Jun. 11, 2010, now Pat. No. 8,609,517.(57) **ABSTRACT**

A device includes providing a silicon substrate; annealing the silicon substrate at a first temperature higher than about 900° C.; and lowering a temperature of the silicon substrate from the first temperature to a second temperature. A temperature lowering rate during the step of lowering the temperature is greater than about 1° C./second. A III-V compound semiconductor region is epitaxially grown on a surface of the silicon substrate using metal organic chemical vapor deposition (MOCVD).



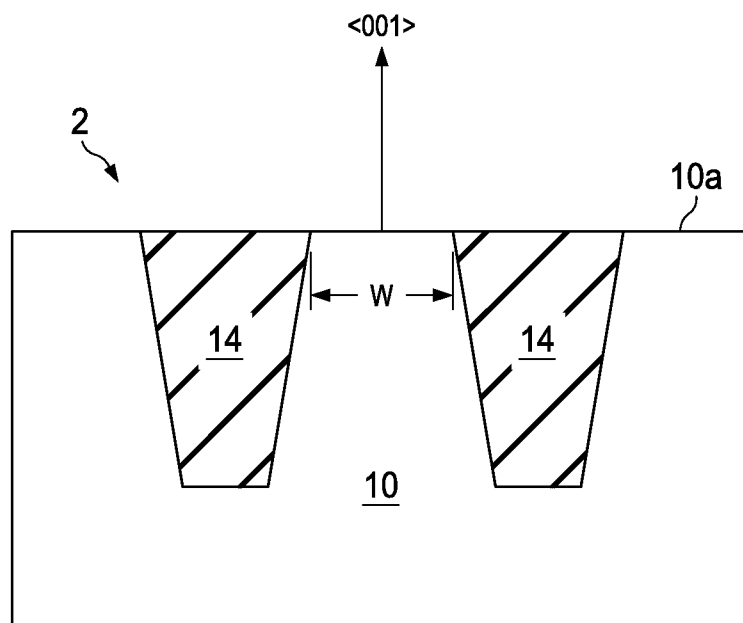


FIG. 1

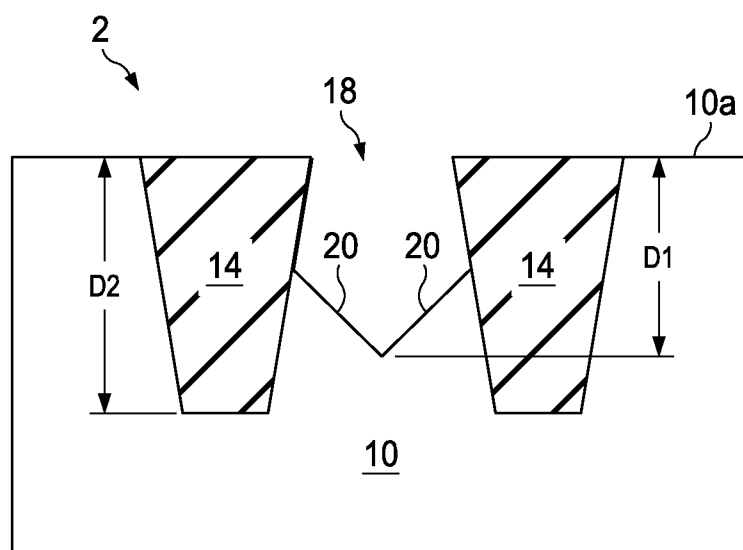


FIG. 2A

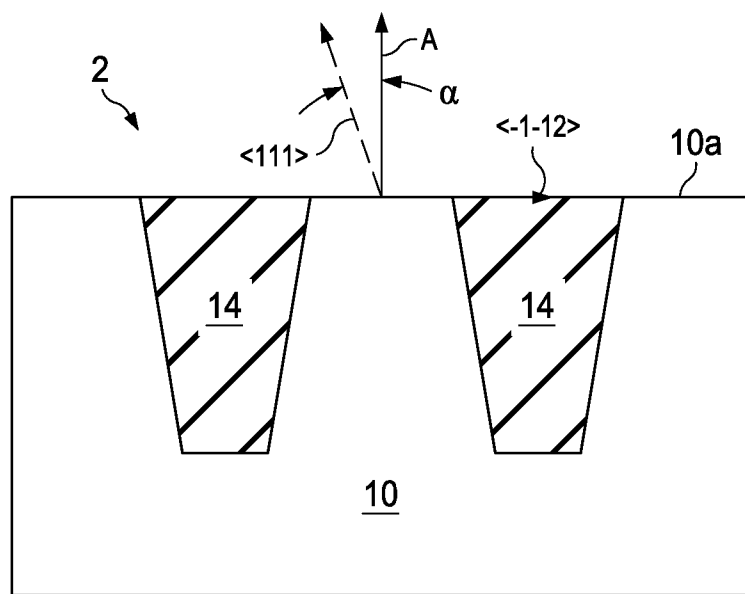
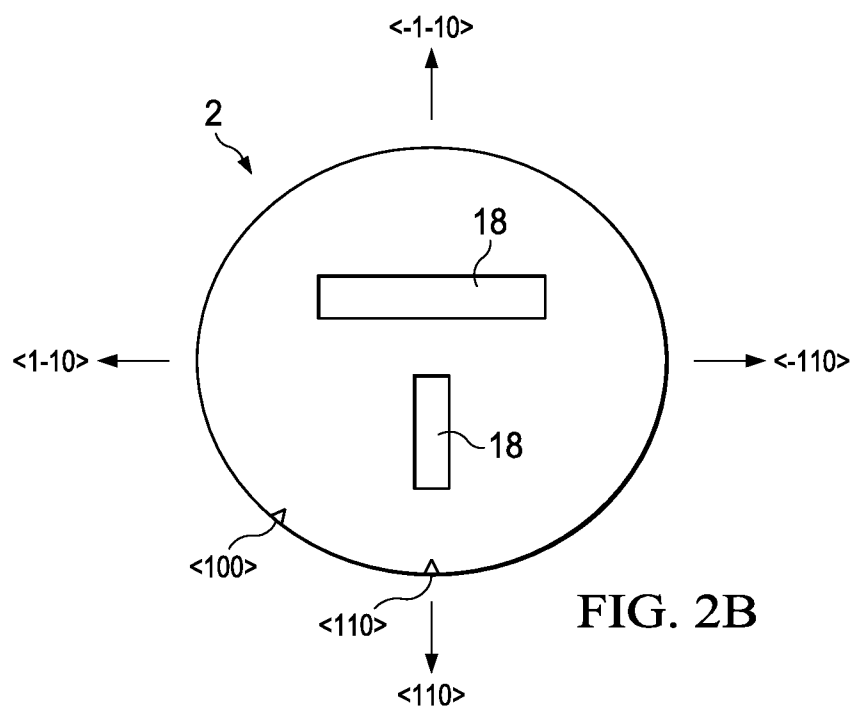


FIG. 3

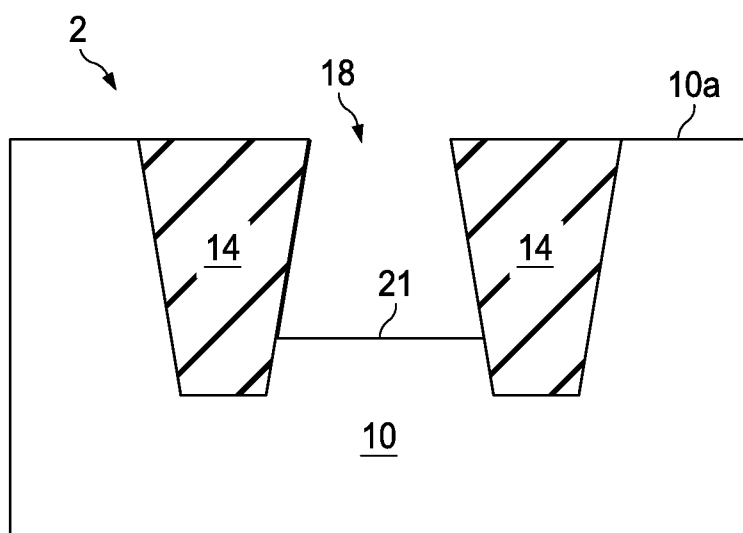


FIG. 4A

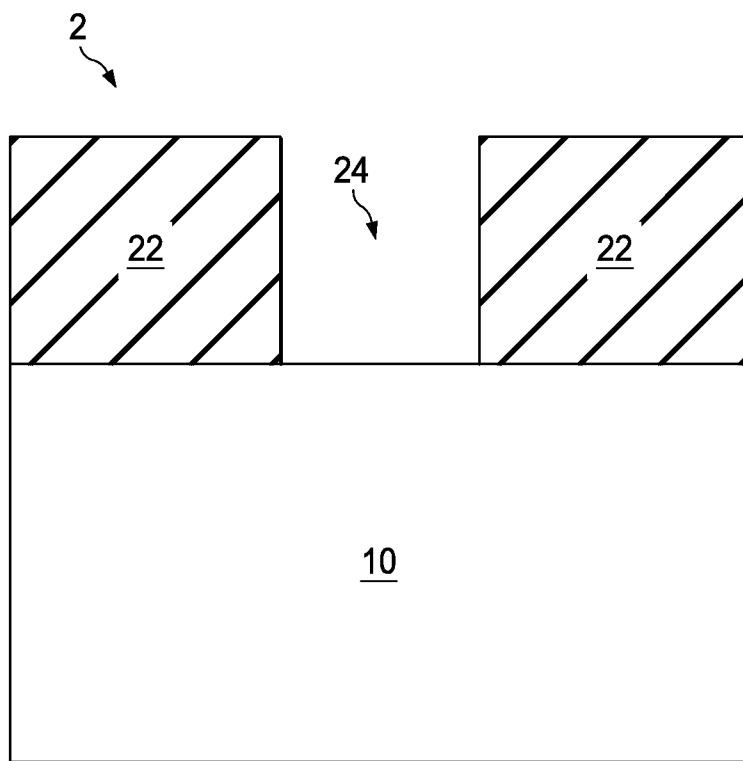
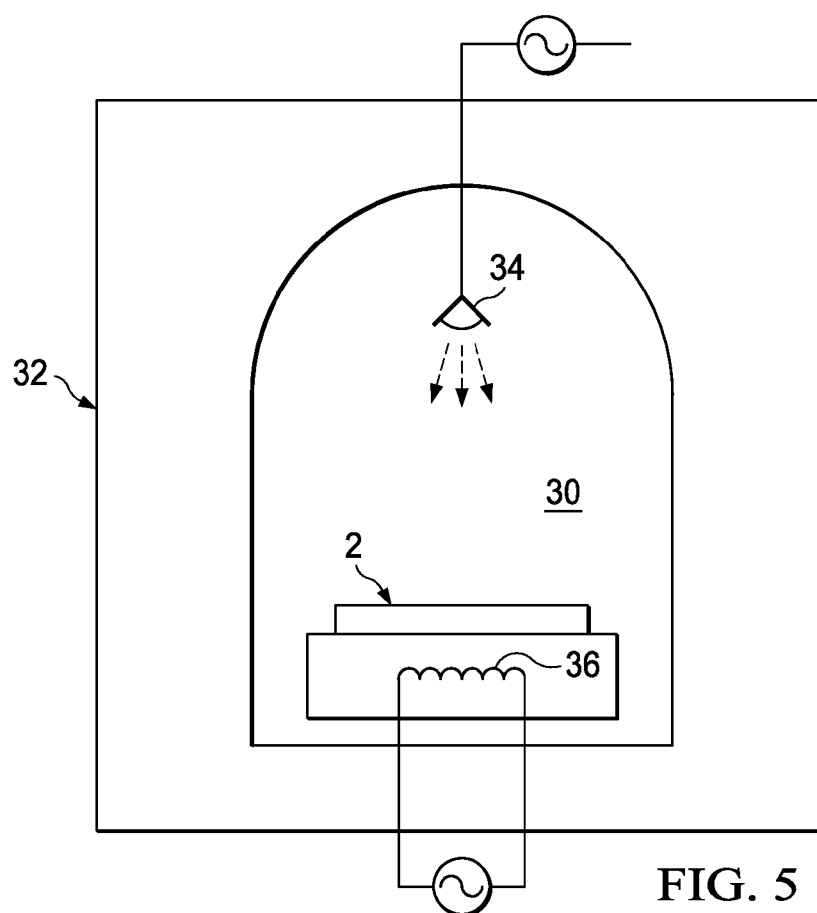
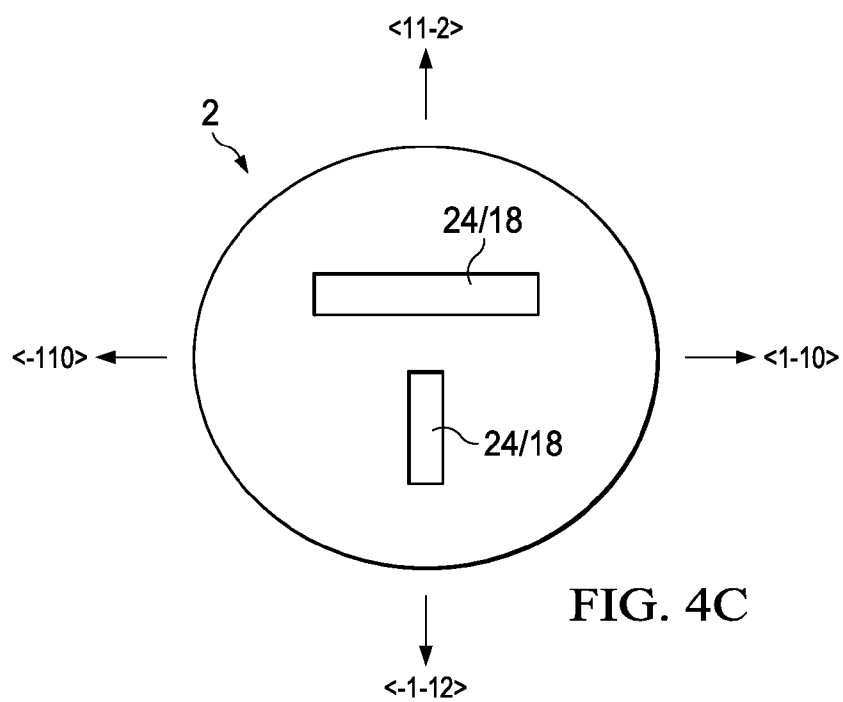


FIG. 4B



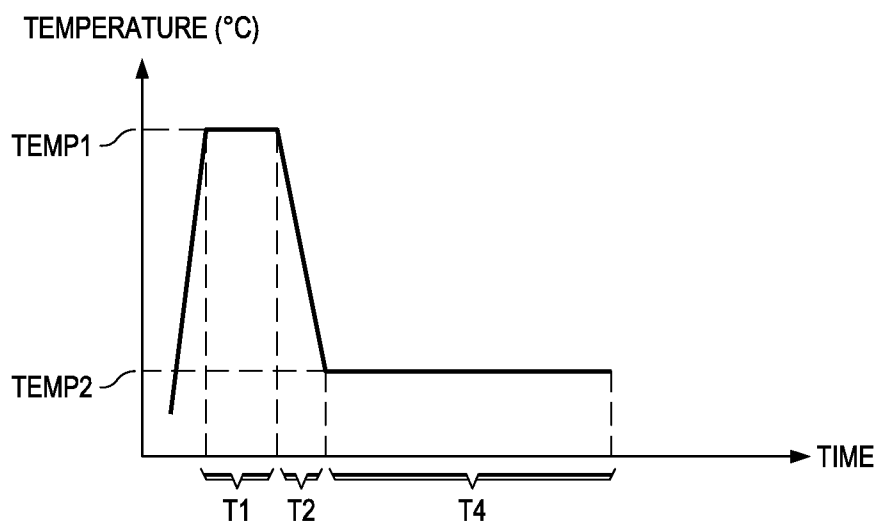


FIG. 6

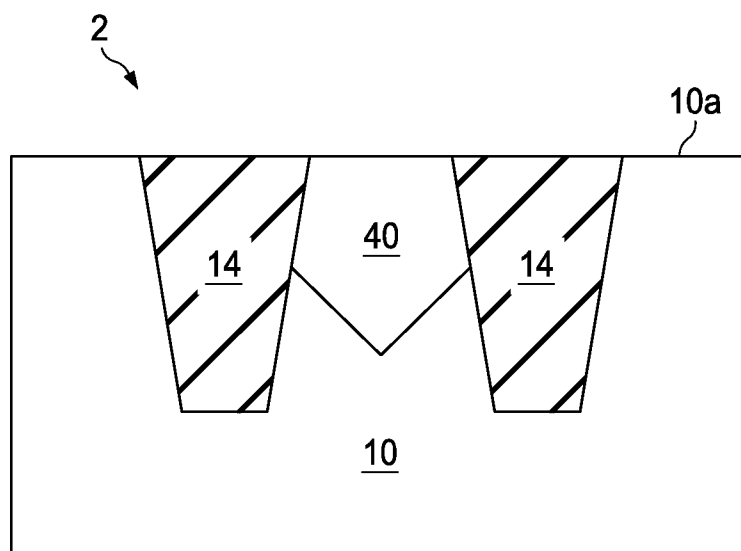


FIG. 7A

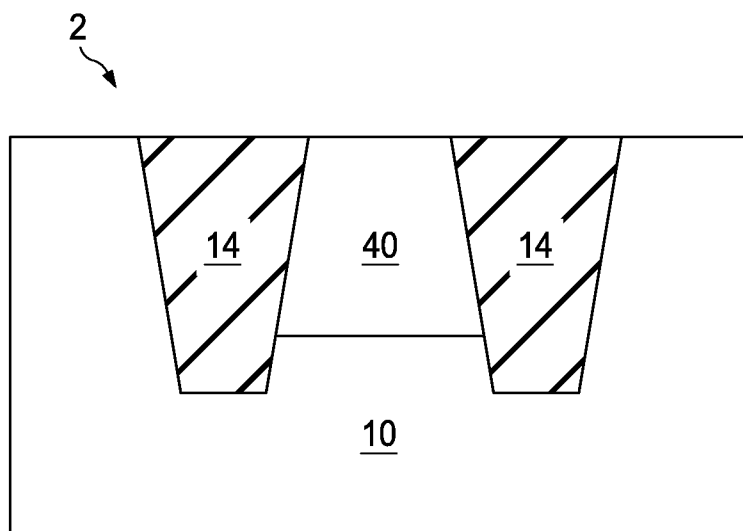


FIG. 7B

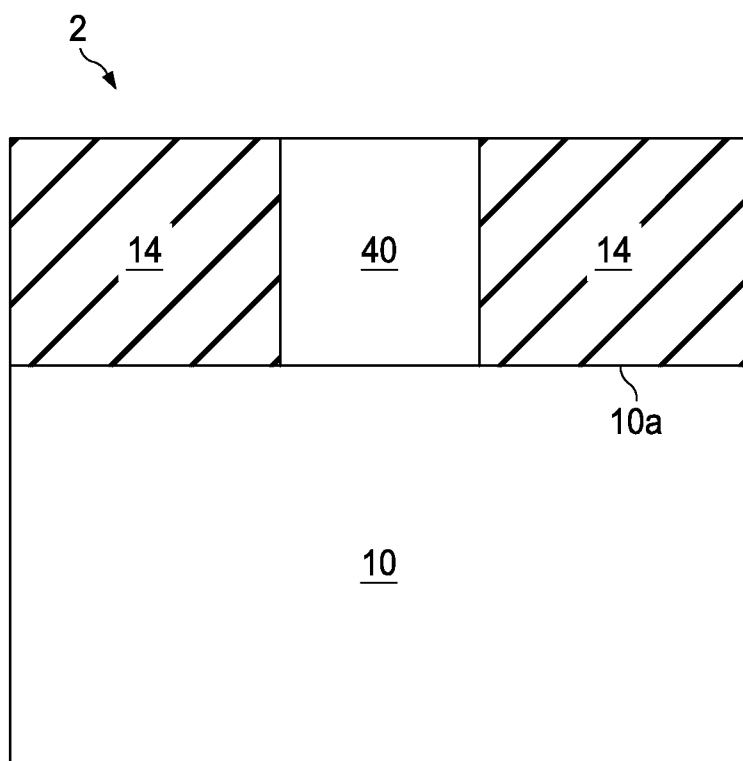


FIG. 7C

MOCVD FOR GROWING III-V COMPOUND SEMICONDUCTORS ON SILICON SUBSTRATES

[0001] This application is a continuation of patent application Ser. No. 12/814,088, entitled "MOCVD for Growing III-V Compound Semiconductors on Silicon Substrates," filed on Jun. 11, 2010 which is incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure relates generally to integrated circuit devices, and more particularly to the formation of III-V compound semiconductors on silicon substrates using metal organic chemical vapor deposition (MOCVD).

BACKGROUND

[0003] The speed of metal-oxide-semiconductor (MOS) transistors is closely related to the drive currents of the MOS transistors, which drive currents are further closely related to the mobility of charges. For example, NMOS transistors have high drive currents when the electron mobility in their channel regions is high, while PMOS transistors have high drive currents when the hole mobility in their channel regions is high.

[0004] Compound semiconductor materials of group III and group V elements (referred to as III-V compound semiconductors hereinafter) are good candidates for forming transistors due to their high electron mobility. Therefore, III-V based transistors have been explored. However, III-V compound semiconductor films need to be grown on other substrates because it is difficult to obtain bulk III-V crystals. The growth of III-V compound semiconductor films on dissimilar substrates faces difficulties because these substrates have lattice constants and thermal expansion coefficients different than that of the III-V compound semiconductors. Various methods have been used to form high quality III-V compound semiconductors. For example, III-V compound semiconductors were grown from trenches between shallow trench isolation regions to reduce the number of threading dislocations.

[0005] III-V compound semiconductors may be formed on silicon substrates with a <111> surface orientation, which silicon substrates are known as Si(111) substrates. It was found that immediately after being cleaved or etched, Si(111) substrates may have 1×1 or 2×1 reconstructions (with the respective surfaces denoted as Si(111):1×1 surfaces or Si(111):2×1 surfaces hereinafter). However, after being annealed at about 400° C., the Si(111) surface may be reconstructed to form a stable Si(111):7×7 surface (which is a Si(111) surface with a 7×7 reconstruction). The Si(111):7×7 surfaces are not suitable for growing high-quality III-V compound semiconductors. Previous research has revealed that through annealing at temperatures higher than 900° C., the Si(111):7×7 surfaces may be converted back to Si(111):1×1 surfaces. However, III-V compound semiconductors needs to be grown at temperatures lower than 900° C. When the temperatures of Si(111) substrates are lowered to the temperatures for growth, the Si(111):1×1 surfaces are again converted back to Si(111):7×7 surfaces, and the resulting III-V compound semiconductors may have many stacking faults.

SUMMARY OF THE INVENTION

[0006] In accordance with one aspect, a device includes providing a silicon substrate; annealing the silicon substrate

at a first temperature higher than about 900° C.; and lowering a temperature of the silicon substrate from the first temperature to a second temperature. A temperature lowering rate during the step of lowering the temperature is greater than about 1° C./second. A III-V compound semiconductor region is epitaxially grown on a surface of the silicon substrate using metal organic chemical vapor deposition (MOCVD).

[0007] Other embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] FIGS. 1 through 4C and FIGS. 7A through 7C are cross-sectional views and top views of intermediate stages in the epitaxial growth of a III-V compound semiconductor region on a silicon substrate in accordance with various embodiments;

[0010] FIG. 5 illustrates an apparatus for epitaxially growing III-V compound semiconductor region using metal organic chemical vapor deposition (MOCVD); and

[0011] FIG. 6 illustrates the temperature of a silicon substrate as a function of time.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0012] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

[0013] A novel method for forming III-V compound semiconductors comprising group III and group V elements is provided in accordance with an embodiment. The intermediate stages of manufacturing embodiments are illustrated. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0014] Referring to FIG. 1, substrate 10, which is a part of semiconductor wafer 2, is provided. In an embodiment, substrate 10 is a Si(001) substrate with major surface 10a having <001> surface orientation, and the respective surface is referred to as a Si(001) surface hereinafter. Insulation regions such as shallow trench isolation (STI) regions 14 are formed in substrate 10. The formation of STI regions 14 includes forming openings (now filled with STI regions 14) in substrate 10, and filling the openings with a dielectric material(s). Distance W between opposite sidewalls of STI regions 14 may be less than about 1,000 nm, for example, although different widths W may be used.

[0015] Next, as shown in FIG. 2A, the portion of substrate 10 between opposite sidewalls of STI regions 14 is etched to form trench 18. Recessing depth D1 may be less than thickness D2 of insulation regions 14. Furthermore, recessing depth D1 may be between about 100 nm and about 500 nm, for example. In an embodiment, the etching of substrate 10 is performed using a wet etch, with a KOH solution, for example, used as an etchant. Accordingly, slanted surfaces 20 are formed. Slant surfaces 20 may be substantially straight, and may be (111) surfaces, which are referred to as Si(111) surfaces hereinafter.

[0016] FIG. 2B illustrates a top view of wafer 2, wherein crystal directions $\langle 1-10 \rangle$, $\langle -1-10 \rangle$, $\langle -1-10 \rangle$, and $\langle 110 \rangle$ of silicon substrate 10 are marked. The $\langle 110 \rangle$ and $\langle 100 \rangle$ notches are also marked. In an embodiment, the longitudinal direction of trench 18 is parallel to $\langle 1-10 \rangle$ and $\langle -1-10 \rangle$ directions. Alternatively, the longitudinal direction of trench 18 is parallel to $\langle -1-10 \rangle$ and $\langle 110 \rangle$ directions.

[0017] FIGS. 3 through 4B illustrate alternative embodiments. Referring to FIG. 3, substrate 10 is a Si(111) substrate with major surface 10a being a Si(111) surface. Alternatively, as shown in FIG. 3, surface orientation A of major surface 10a may be close to $\langle 111 \rangle$ direction (surface orientation), with off angle α . Off angle α may be greater than about 6 degrees, greater than about 12 degrees, greater than about 15 degrees, and may even be greater than about 20 degrees. Further, off angle α may be between about 6 degrees and about 12 degrees. In an embodiment, off angle α deviates from $\langle 111 \rangle$ direction and tilts toward $\langle -1-12 \rangle$ direction, as schematically illustrated in FIG. 3. STI regions 14 is also formed in substrate 10.

[0018] Referring to FIG. 4A, trench 18 is formed by etching the portion of substrate 10 between opposite sidewalls of STI regions 14. In an embodiment, an etchant that attacks silicon in $\langle 111 \rangle$ direction more than other directions is used, so that substantially flat bottom 21 is formed. Accordingly, bottom surface 21 has essentially the same surface orientation as major surface 10a. In an exemplary embodiment, the etchant is an HCl solution.

[0019] In alternative embodiments, as shown in FIG. 4B, instead of forming STI regions 14 in substrate 10 and then recessing substrate 10, dielectric layer 22 is formed on surface 10a of substrate 10, for example, using a deposition method. A portion of surface 10a is exposed through trench 24 in dielectric layer 22. Dielectric layer 22 may be formed of silicon oxide, silicon nitride, or the like. Using this method, the exposed portion of surface 10a also has the original surface orientation.

[0020] FIG. 4C illustrates a top view of the structure shown in FIGS. 4A or 4B, wherein crystal directions of silicon substrate 10 are marked. In an embodiment, the longitudinal direction of trench 24/18 is parallel to $\langle -1-10 \rangle$ and $\langle 1-10 \rangle$ directions. Alternatively, the longitudinal direction of trench 24 is parallel to $\langle 11-2 \rangle$ and $\langle -1-12 \rangle$ directions.

[0021] It is observed that the Si(111) surfaces may have 1×1 reconstructions (with the respective surfaces referred to as Si(111): 1×1 surfaces hereinafter), for example, immediately after substrate 10 cleaved or etched. The Si(111): 1×1 surface may be undesirably converted to surfaces having a stable 7×7 reconstruction, which surfaces are referred to as Si(111): 7×7 surfaces hereinafter. Since Si(111): 7×7 surfaces are not suitable for growing III-V compound semiconductors, an annealing is performed on wafer 2 (as shown in FIGS. 2A, 4A, and 4B) to convert the Si(111): 7×7 surfaces back to Si(111): 1×1 surfaces. The annealing temperature may be between about 500°C . and about 900°C ., or even greater than about 900°C . In an exemplary embodiment, the annealing temperature is about 1000°C . During the annealing, process gases such as N_2 and AsH_3 may be introduced into the annealing chamber. The duration of the annealing may be between about 1 minute and about 30 minutes. After the annealing, the likely Si(111): 7×7 surfaces at the bottom of trench 18/24 are converted to Si(111): 1×1 surfaces.

[0022] Referring to FIG. 5, the annealing of wafer 2 may be performed in chamber 30 of production tool 32, which is

configured for performing metal organic chemical mechanical vapor depositions (MOCVDs). In conventional MOCVD chambers, the heating of wafers were achieved using coils, and when temperatures of the wafers need to be lowered, inert gases are introduced to cool the wafers. The temperature lowering rate was accordingly low. In MOCVD tool 32, however, the annealing of wafer 2 is achieved using radiation source 34, which may be used for rapid thermal annealing (RTA). In an exemplary embodiment, radiation source 34 is a flash lamp, which heats wafer 2 to the annealing temperature.

[0023] After the annealing, the temperature of wafer 2 is rapidly lowered to an epitaxial growth temperature used for epitaxially growing III-V compound semiconductor region 40, as shown in FIGS. 7A and 7B. In an embodiment, the epitaxial growth temperature is lower than about 400°C ., and may be about 350°C ., although it may be higher or lower. The steps of annealing wafer 2, the temperature lowering, and the epitaxially growth of III-V compound semiconductor region 40 may be in-situ performed, with no vacuum break occurring from the time the annealing is started to the time the epitaxial growth is ended. The lowering of the temperature may be achieved by either reducing the power of radiation source 34, or turning off the power of radiation source 34. The maintaining of the epitaxial growth temperature during the epitaxial growth may be achieved either through the use of coil 36 to heat wafer 2, or the use of radiation source 34 with the power provided to radiation source 34 lower than the power used for annealing.

[0024] FIG. 6 schematically illustrates the temperature of wafer 2 as a function of time. Initially, wafer 2 may be at a room temperature. To perform the annealing, radiation source 34 (FIG. 5) heats wafer 2, so that the temperature of wafer 2 is rapidly increased to temperature Temp1, which is the annealing temperature that is higher than about 900°C . After period of time T1, the annealing is finished, and Si(111): 7×7 surfaces of wafer 2 are converted to Si(111): 1×1 surfaces.

[0025] After the annealing, a quenched temperature lowering is performed, which time period is denoted as T2. During time period T2, the power of radiation source 34 (FIG. 5) is either reduced or turned off. In an embodiment, the temperature lowering rate during an entire time period T2 is higher than about $0.5^\circ\text{C}/\text{second}$, higher than about $1^\circ\text{C}/\text{second}$, or even higher than about $5^\circ\text{C}/\text{second}$ or $10^\circ\text{C}/\text{second}$. In an exemplary embodiment, the temperature lowering rate is between about $0.5^\circ\text{C}/\text{second}$ and about $10^\circ\text{C}/\text{second}$.

[0026] When the temperature of wafer 2 is lowered to temperature temp2, which is suitable for epitaxially growing III-V compound semiconductor regions, an epitaxial growth is performed to grow III-V compound semiconductor region 40 in trenches 18/24 (FIGS. 2A, 4A, and 4B). The exemplary resulting structures are shown in FIGS. 7A through 7C. With the rapid temperature lowering from temperature temp1 to temperature temp2 (FIG. 5), the Si(111): 1×1 surfaces formed at temperature temp1 do not change to Si(111): 7×7 surfaces, even if during the temperature lowering process, the temperature of wafer 2 may pass a temperature range in which the transition from Si(111): 1×1 to Si(111): 7×7 typically occurs. Accordingly, when the epitaxial growth of III-V compound semiconductor region 40 starts, the surface of substrate 10 is still a Si(111): 1×1 surface. The quality of the resulting III-V compound semiconductor region 40 is thus improved.

[0027] Referring again to FIGS. 7A through 7C, III-V compound semiconductor regions 40 may be formed of a III-V compound semiconductor material comprising, but is not

limited to, GaAs, InP, GaN, InGaAs, InAlAs, GaSb, AlSb, AlAs, AlP, GaP, combinations thereof, and multi-layers thereof. The top surfaces of III-V compound semiconductor regions **40** may be level with, higher than, or lower than, top surfaces **10a** of substrates **10**.

[0028] In the embodiments, by performing an annealing to a silicon substrate before a III-V compound semiconductor region is epitaxially grown thereon, the undesirable Si(111):7×7 surface is converted to desirable Si(111):1×1 surface that is better suited for growing III-V compound semiconductors. Further, by rapidly lowering the temperatures of wafers from the annealing temperature to the growth temperature of III-V compound semiconductors, the Si(111):1×1 surfaces resulted from the annealing may be preserved until the III-V compound semiconductors are grown.

[0029] Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. An apparatus for performing an epitaxial growth on a wafer, the apparatus comprising:
 - a production tool configured to perform a metal organic chemical vapor deposition (MOCVD) on the wafer, the production tool comprising:
 - a radiation source configured to heat the wafer to a temperature higher than about 900° C.
2. The apparatus of claim 1, wherein the production tool further comprises a chamber configured to maintain a vacuum environment, wherein the radiation source is located in the chamber.
3. The apparatus of claim 1, wherein the radiation source comprises a flash lamp.
4. The apparatus of claim 1 further comprising a coil configured to heat the wafer.
5. The apparatus of claim 4, wherein the radiation source is located over the wafer, and the coil is located under the wafer.

6. The apparatus of claim 1, wherein the radiation source is configured to perform rapid thermal annealing on the wafer.

7. The apparatus of claim 1, wherein the radiation source is configured to perform a Rapid Thermal Annealing (RTA) on the wafer.

8. The apparatus of claim 1 being configured to allow the wafer to cool at a temperature lowering rate higher than about 1° C.

9. The apparatus of claim 8 being configured to allow the wafer to cool at the temperature lowering rate higher than about 5° C.

10. The apparatus of claim 1 being configured to provide a first power to the radiation source, and a second power lower than the first power to the radiation source.

11. An apparatus for performing an epitaxial growth on a wafer, the apparatus comprising:

- a chamber configured to maintain a vacuum environment; and

- a flash lamp in the chamber and over the wafer, wherein the chamber and the flash lamp are comprised in a production tool configured to perform a metal organic chemical vapor deposition (MOCVD) on the wafer.

12. The apparatus of claim 11 further comprising a coil configured to heat the wafer in the chamber.

13. The apparatus of claim 12, wherein the coil is located under the wafer.

14. The apparatus of claim 11, wherein the flash lamp is configured to perform a Rapid Thermal Annealing (RTA) on the wafer.

15. The apparatus of claim 11 being configured to allow the wafer to cool at a temperature lowering rate higher than about 1° C.

16. The apparatus of claim 11 being configured to allow the wafer to cool at the temperature lowering rate higher than about 5° C.

17. The apparatus of claim 11 being configured to provide a first power to the flash lamp, and a second power lower than the first power to the flash lamp.

18. An apparatus for performing an epitaxial growth on a wafer, the apparatus comprising:

- a chamber;

- a flash lamp in the chamber and over the wafer, wherein the chamber and the flash lamp are comprised in a production tool configured to perform a metal organic chemical vapor deposition (MOCVD) on the wafer; and

- a coil configured to heat the wafer in the chamber.

19. The apparatus of claim 18, wherein the apparatus is configured to heat the wafer using the flash lamp during the MOCVD.

20. The apparatus of claim 18, wherein the apparatus is configured to heat the wafer using the coil during the MOCVD.

* * * * *