



- (51) **International Patent Classification:**
B41J 2/045 (2006.01) *B41J 2/14* (2006.01)
- (21) **International Application Number:**
PCT/US2013/067872
- (22) **International Filing Date:**
31 October 2013 (31.10.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant:** HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).
- (72) **Inventors:** YANG, Jianhua; 1501 Page Mill Road, Palo Alto, California 94304-1100 (US). GE, Ning; 1 Depot Road Plant 1150 Depot Rd, Singapore 109673 (SG). LI, Zhiyong; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US).
- (74) **Agents:** COLLINS, David et al.; Hewlett-Packard Company, Intellectual Property Administration, 3404 E. Harmony Road, Mail Stop 35, Fort Collins, Colorado 80528 (US).

(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to the identity of the inventor (Rule 4.17(i))

[Continued on next page]

- (54) **Title:** PRINTHEADS HAVING MEMORIES FORMED THEREON

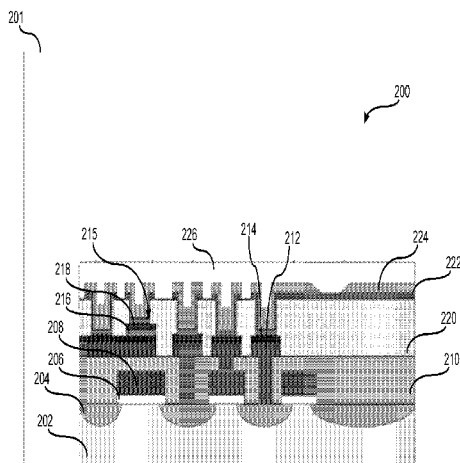


FIG. 2

(57) **Abstract:** Printheads having memories formed thereon are disclosed. An example apparatus includes a printhead body comprising a first metal layer. The example apparatus also include a memory formed on the printhead body. The memory includes the first metal layer as a first electrode, a second metal layer as a second electrode, and a switching oxide layer between the first and second metal layers.



Published:

— *with international search report (Art. 21(3))*

PRINTHEADS HAVING MEMORIES FORMED THEREON

BACKGROUND

[0001] Some printers have printheads that dispense ink on a substrate such as paper.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] FIG. 1A is a schematic illustration of an example printing apparatus implemented in accordance with the teachings of this disclosure.

[0003] FIG. 1B is a schematic illustration of an example printing apparatus implemented in accordance with the teachings of this disclosure.

[0004] FIG. 2 is an example integrated circuit that can be used to implement the example printing apparatus of FIG. 1A and/or FIG. 1B.

[0005] FIGS. 3 – 15 show example structures fabricated during a process of producing the example integrated circuit of FIG. 2.

[0006] FIG. 16 is an example flowchart representative of machine readable instructions that may be executed to produce the example integrated circuit of FIG. 2.

[0007] FIG. 17 is a printhead fabrication system including a processor platform to execute the instructions of FIG. 16 to produce the example integrated circuit of FIG. 2.

[0008] The figures are not to scale. Wherever possible, the same reference numbers will be used throughout the drawing(s) and accompanying written description to refer to the same or like parts. As used herein, stating that a layer is “on”, “above” or “below” another layer does not mean the two layers must be in “contact”; they may be in direct contact and intervening layers may or may not be present. The phrase “in contact with” is used to mean direct contact between two structures without an intervening structure or layer.

DETAILED DESCRIPTION

[0009] Examples disclosed herein relate to printheads (e.g., disposable integrated printheads (IPH), permanent printheads with off-axis ink supplies), printers and/or imaging devices (e.g., printers, copiers, etc.) that include memories (e.g., non-volatile memories, memristor memories (e.g., memristors having 1k – 5k memristor bits, memristors having greater than 5k memristor bits, etc.), etc.). Some example devices disclosed herein support implementing anti-counterfeiting (AFC) technologies and/or secure authentication information in printheads. Examples disclosed herein are useful to reduce production costs (e.g., reducing per-bit-cost) related to manufacturing printheads while improving printing performance and incorporating additional features (e.g., security features) into such printheads. Additionally or alternatively, example printheads disclosed herein are configured to store data associated with identification information, authentication information, cloud-based printing, market data, information, customer-appreciated value (CAV) functions, data, etc.

[0010] In some examples, a memory (e.g., a memristor, a resistive random-access memory) is integrally formed within or on a printhead using surfaces and/or structures (e.g., metal layers) of the printhead. Thus, a portion of the memristor itself is one or more layer(s) of an otherwise functional printhead. Examples disclosed herein may be produced using a NMOS process, a CMOS process, a BiCMOS, a Bipolar-CMOS-DMOS (BCDD) process or any other process of making printheads and/or semiconductors. Examples disclosed herein may be used to manufacture an integrated circuit (IC) chip (e.g., 2.5mm x 2.5mm size chips, 5x5mm size chips, etc.) or an IC die on a printhead using an anion-based bipolar memristor based on a metal oxide system. In such examples, metal oxide is deposited (e.g., sputtered, deposited using atomic layer deposition (ALD), physically deposited) on the printhead to form a memristor structure. Alternatively, a metal layer of the printhead is oxidized to form the memristor structure.

[0011] In some examples, a memristor is built on, formed on, fabricated on and/or integral to a printhead using a metal-oxide-metal structure (e.g., a metal-insulator-metal). Examples disclosed herein provide feasible,

cost-effective and highly manufacturable structures to form a printhead on a silicon area of suitable size (e.g., a relatively small area comparable to the space available on the printhead) to implement a bank of memory bits to store identification (ID) information and provide authentication. In some examples, the example memristor that is formed on and/or formed integral to the printhead is provided with an ID bits line or ID line to store identification information for authentication purposes. Examples disclosed herein use the ID line to store identification for authentication purposes. Examples disclosed herein use the ID line to receive and store security or authentication data. Such security or authentication data may be used to identify a corresponding printhead (or print cartridge) as an authentic product from a specific manufacture (e.g., an authentic HP print cartridge). In this manner, the ID line is useful for manufactures to distribute parts that are verifiable as authentic manufacturer parts. Such verifiable authenticity of parts aids in efforts to combat counterfeiting of after-market parts that are often of poorer quality and can sometimes damage machines or decrease performance of machines in which the counterfeit parts are installed. In some examples, the ID line may additionally or alternatively store encryption / decryption data (e.g., security keys) for use in secure printing that involves, just prior to printing, decrypting data sent to a printer in an encrypted format.

[0012] In the illustrated examples, a shift register or other addressing structure is connected to bit cells of a memristor array and to the ID line for memory bit addressing and/or other addressing method(s) (e.g., byte addressing, word addressing, etc.). In some examples, the ID line is coupled and/or connected to an external analog application-specific integrated circuit (ASIC) hosted in a printer having an electrical current source and an analog-to-digital converter (ADC) that measures resistance. In some examples in which the disclosed examples are implemented using a permanent printhead, there is on-chip DAC abilities and, thus, no dedicated ID line may be included. In some examples, the ASIC programs information (e.g., 512 bits, 1024 bits, etc.) into bits of the ID line by switching the memristor from an initial high-resistance state (HRS) to a low-resistance state (LRS) by applying a suitable

switching voltage. In some examples, the examples disclosed herein advantageously include memristor memories that, for example, are programmable one time. In some examples, the example memristor memories have relative low requirement for retention (e.g., >1.5 – 3 years). In some examples, the example memristor memories have two memory states (e.g., “1” and “0” with a resistance difference). In some examples, the example memristor memories have a relatively low resolution requirement for off-to-on programming ratio (e.g., > 2:1). In some examples, the example memristor memories have a bit size of less than 1-2k bits, are micron-size devices (e.g., 1-4um, 2.5um, 4um). In some examples, the example memristor memories have a relatively low performance requirement for switching speed (e.g., microseconds (ms)). In some examples, the example memristor memories have flexible current (e.g., <1.5 Amps), power and voltage (e.g., <15.5V) requirements and/or have a relatively flexible architecture (e.g., a one diode per memristor (1D1M) architecture, a one transistor per memristor (1T1M) architecture).

[0013] FIG. 1A shows an example block diagram of a printing and/or imaging apparatus 100 in which examples disclosed herein can be implemented. While FIG. 1A depicts the printing apparatus 100 as implemented with a permanent printhead, in other examples, the printing apparatus 100 and any of the examples disclosed herein can be equally implemented with a printing apparatus having an integrated printhead (e.g., a disposable cartridge).

[0014] As shown in FIG. 1A, in some examples, the printing apparatus 100 is coupled and/or otherwise in communication with a host system 102 such as a computer and/or microprocessor. In the illustrated example, the printing apparatus 100 includes a controller 104, an ink supply device 106 having a memory 107, a power supply 108 and an integrated printhead assembly 110. In some examples, the printhead assembly 110 is integrally coupled to the printing apparatus 100. In examples in which the printhead assembly 110 is, for example, a disposable printer cartridge, the printhead assembly 110 is removably coupled to the printing apparatus 100.

[0015] In the example of FIG. 1A, the ink supply device 106 is fluidly coupled to the printhead assembly 110 to enable ink to be selectively provided to the printhead assembly 110. In some examples, the printhead assembly 110 includes a processing driver head 112 and a memory (e.g., on-chip memory) 114. The example processing driver head 112 includes a processor 116 and a driver head 118. In the illustrated example, the memory 114 includes an ID bit line or ID line 120 to store authentication / security data. However, in examples in which the printing apparatus 100 is implemented with an integrated printhead and/or a permanent printhead using TJJ4 and having an on-chip DAC capabilities, an ID line 120 may not be present. In examples disclosed herein, the memory 114 is implemented using a memristor integrally formed in or on the printhead assembly 110.

[0016] In operation, the example power supply 108 provides power to the controller 104, the printhead assembly 110 and/or the processing driver head 112. In addition, the controller 104 receives data from the host system 102. For example, the data may be authentication / security data to be stored in the ID line 120 or the data may be print data. In some examples, the controller 104 processes the data into printer control information and/or image data that is provided to the ink supply device 106 and/or the printhead assembly 110 to efficiently control the printing apparatus 100. Additionally or alternatively, during an initial programming phase, the controller 104 stores received authentication / security data into the ID line 120 as part of a one-time programming (OTP) process. In such examples, the authentication / security data is useful for ACF features to, for example, confirm that an ink cartridge including the printhead assembly 110 is an authentic part. Additionally or alternatively, the authentication / security data may be used to implement secure printing based on data received at the printing system in an encrypted format.

[0017] The memory 107 and the memory 114 may be used to store any type of data. In some examples, the memory 107 stores ink supply specific data and/or ink identification data, ink characterization data, ink usage data, etc. In some examples, the memory 114 stores printhead specific data and/or

printhead identification data, warranty data, printhead characterization data, printhead usage data, authentication data, anti-counterfeiting data (ACF), etc. The memory 107 and/or the memory 114 can be written to at the time of manufacturing and/or during the operation of the printing apparatus 100.

[0018] FIG. 1B shows an example inkjet printing system 150 that includes an example inkjet printhead assembly 152 and an example ink supply assembly 154. In the illustrated example, the inkjet printing system 150 includes a mounting assembly 156, a media transport assembly 158, an electronic controller 160 and power supply 162 that provides power to the various electrical components of inkjet printing system 150.

[0019] In the illustrated example, the inkjet printhead assembly 152 includes a memory (e.g., on-chip memory) 154, one or more printhead die(s) 157 and one or more nozzle(s) 158. In the illustrated example, the memory 154 and an ID line 157 are communicatively coupled to the electronics controller 160.

[0020] In some examples, the printhead die (e.g., printhead) 157 ejects drops of ink through the nozzle 158 toward a print medium 160 so as to print onto print medium 160. In some examples, the printhead 157 is a fluid ejection device and the print media 160 is any suitable sheet material such as, for example, paper, card stock, transparencies, Mylar, fabric, etc. In some examples, the nozzles 158 are one or more columns and/or arrays that eject ink from the nozzles to produce characters, symbols, graphics, images, etc., on the print medium 160 as the inkjet printhead assembly 152 and the print medium 160 are moved relative to one another. The printhead assembly 150 may be used to eject ink, liquids, fluids, flowable materials (e.g., clear fluid), etc.

[0021] In the illustrated example, the ink supply assembly 154 includes a reservoir 162 for storing ink that is to be provided to the printhead assembly 152. In some examples, the ink supply assembly 154 is a one-way ink delivery system that provides ink to the inkjet printhead assembly 152 is consumed during printed. In other examples, the ink supply assembly 154 is a recirculating ink delivery system in that a portion of the ink provided to the printhead assembly 152 that is consumed during printing and another portion

of the ink provided to the printhead assembly 152 is returned to the reservoir 162 and/or the ink supply assembly 154.

[0022] In some examples, the inkjet printhead assembly 152 and the ink supply assembly 154 are housed together in an inkjet cartridge or pen. In other examples, the ink supply assembly 154 is separate from the inkjet printhead assembly 154 and provides ink to the inkjet printhead assembly 152 via a coupling and/or an interface connection (e.g., a supply tube). In the illustrated example, the reservoir 162 may be removed, replaced and/or refilled. In examples in which the inkjet printhead assembly 152 and the ink supply assembly 154 are housed together in an inkjet cartridge, the reservoir 162 may include a local reservoir located within the cartridge and/or a larger reservoir located outside of the cartridge. In some such examples, the larger reservoir, which may be removed, replaced and/or refilled, is fluidly coupled to and refills the ink supply of the smaller local reservoir.

[0023] In the illustrated example, the mounting assembly 156 positions the inkjet printhead assembly 152 relative to the media transport assembly 158 and the media transport assembly 158 positions the printhead medium 160 relative to the inkjet printhead assembly 152. Thus, in the illustrated example, a print zone 164 is defined adjacent the nozzles 158 between the inkjet printhead assembly 152 and the print medium 160.

[0024] In some examples, the inkjet printhead assembly 152 is a scanning type printhead assembly. In some such examples, the mounting assembly 156 includes a carriage that moves the inkjet printhead assembly 156 relative to the media 160 to enable scanning thereof. In other examples, the inkjet printhead assembly 152 is a non-scanning type printhead assembly. In some such examples, the mounting assembly 156 fixes the inkjet printhead assembly 152 relative to the media transport assembly 158 and the media transport assembly 158 positions and/or moves the print medium 160 relative to the inkjet printhead assembly 152.

[0025] In some examples, the electronic controller (e.g., printer controller) 160 includes a processor, firmware, etc. to communicate with and/or control the inkjet printhead assembly 152, the mounting assembly 156

and the media transport assembly 158. In the illustrated example, the electronic controller 160 receives data 166 from a host system and the data 166 is then sent to the inkjet printing system 150 along with electronic information, infrared information, optical information, information transfer path information, etc. In some examples, the data 166 is associated with a document and/or file to be printed and/or print job commands and/or command parameters.

[0026] FIG. 2 shows an example integrated circuit 200 that can be used to implement the printhead assembly 110 and/or the memory 114 of FIGS. 1A and 1B. The example illustrated in FIG. 2 can be implemented with NMOS based on a front end of line process (FEOL) or any other suitable process such as CMOS, BICMOS, BCD, etc. In the illustrated example, the integrated circuit 200 is incorporated into a printhead body (e.g., printhead silicon) 201 and includes a substrate layer (e.g., a first layer, P-type silicon substrate, N-type silicon substrate) 202 including doped regions 204 (e.g., N+ doping to decrease resistivity), a gate oxide layer (e.g., a second layer) 206 and a polysilicon layer (e.g., a third layer) 208. In the illustrated example, the gate oxide layer 206 is between the substrate layer 202 and the polysilicon layer 208. Additionally, in the illustrated example, the integrated circuit 200 includes an interlayer dielectric (ILD) layer (e.g., a fourth layer) 210 and metal layers (e.g., fifth and sixth layers) 212, 214. In the illustrated example, some portions of the ILD layer 210 are in contact with the substrate layer 202, some portions of the metal layer 212 are in contact with the substrate layer 202, other portions of the metal layer 212 are in contact with the ILD layer 210 and the metal layer 214 is in contact with the metal layer 212. In some examples, the ILD layer 210 includes borophosphosilicate glass (BPSG) and/or undoped silicate glass (USG) and may be used as a metal-oxide-semiconductor field-effect transistor (MOSFET) for logic and/or PowerEFT for the integrated circuit 200. In some examples, the metal layer 212 includes a metal such as an aluminum-copper alloy (AlCu or AlCuSi), and the metal layer 214 includes TiN, TaN, NbN, HfN, ZrN, RuO₂, IrO₂, Al, Ta, Ti, Cu, Co, Ni, Nb, Mo, W, Hf, Zr, Cr or any other suitable metal. In some such examples, the layers

including the substrate 202 through the metal layer 212 and/or the metal layer 214 are part of and/or are integral to the printhead assembly 110 and one or both of the metal layers 212, 214 forms a bottom electrode for a memristor 215. For example, the structure of the substrate layer 202 through the metal layer 214, and specifically including the bottom electrode layer 214, may be integral structures and/or layers of a printhead used for printing functionality. In some instances, examples disclosed herein may be used to advantageously form a memristor on the metal layer 212 and/or the metal layer 214 of the printhead.

[0027] In the illustrated example, the integrated circuit 200 includes a memristor switching oxide layer (e.g., a seventh layer) 216 and a metal layer (e.g., an eighth layer, a memristor top electrode layer) 218. The example memristor 215 is formed using the metal layer 214 that may be a bottom electrode of the memristor 215, the memristor switching oxide layer 216 (e.g., a memristor cross-bar structure) and the metal layer 218 that may be used as the top electrode of the memristor 215. In some examples, the memristor switching oxide layer 216 is formed by oxidizing one or more of the metal layers 212, 214 and/or by depositing and/or sputtering an oxide or nitride layer (e.g., HfO_x , TaO_x ($0 < x < 2.5$), ZrO_x ($0 < x < 2$), ZnO_x ($0 < x < 2$), NiO_x ($0 < x < 1.5$), FeO_x ($0 < x < 1.5$), CoO_x ($0 < x < 1.5$), YO_x ($0 < x < 1.5$), SiO_x ($0 < x < 2$), WO_x ($0 < x < 3$), NbO_x ($0 < x < 2.5$), TiO_x ($0 < x < 2$), AlO_x ($0 < x < 1.5$), MoO_x ($0 < x < 3$), GaO_x ($0 < x < 1.5$), AlN_x ($0 < x < 1.5$), GaN_x ($0 < x < 1.5$), AlGaIn_x ($0 < x < 1.5$), etc. where x is greater than 0 and less than (or up to) the stoichiometric amount thereon. Additionally, in this example, the integrated circuit 200 includes a dielectric layer (e.g., a ninth layer) 220, a metal layer (e.g., a tenth layer) 222, a thermal inkjet resistor layer (e.g., an eleventh layer and/or metal layer) 224 and/or a passivation layer (e.g., a twelfth layer) 226. In some examples, the thermal inkjet resistor layer 224 includes tantalum aluminum (TaAl), TaAlO_x , WSiN , TaSiN and/or an aluminum-copper alloy.

[0028] For ease of description, the nomenclature of first, second, third, etc. are used to facilitate in distinguishing between the layers 202, 204, 206, etc. of the integrated circuit 200. However, such first, second, third, etc.

naming convention is not intended to signify any priority, importance or inherent physical positioning of the layers relative to one another. That is, first, second, third, etc. terms may be arbitrarily applied to any layer to ease in identifying between different layers.

[0029] FIGS. 3 – 14 depict an example process of producing the example integrated circuit 200 of FIG. 2. In some examples, the process described below of incorporating the integration of memristor memories into the on-chip printhead occurs when fabricating the integrated circuit 200 of FIG. 2. While FIGS. 3 – 14 depict a particular number of layers being formed and particular layer(s) being formed in a particular order, the order in which any one or more of the layers are formed may be changed and/or the number of layers formed may be changed (e.g., increased, decreased, etc.).

[0030] As shown in the illustrated examples of FIGS. 3, 4, and 5, the process begins with the gate oxide layer 206 and the polysilicon layer 208 being blanket patterned above the substrate layer 202. In the illustrated example, to reduce cost, there is no field oxide (FOX) isolation, shallow trench isolation (STI) or deep trench isolation (DTI). In some examples, transition isolation is done through a looped transistor design. For example, the gate oxide layer 206 is formed on the substrate layer 202 in the example shown in FIG. 4 and the polysilicon layer 208 is formed on the gate oxide layer 206, as shown in FIG. 5. To remove portions of the gate oxide layer 206 and the polysilicon layer 208 as shown in the illustrated example of FIG. 5, a portion of the layers 206, 208 is patterned and/or etched away. In the illustrated example of FIG. 6, an in-situ doping and/or implanting process is used to provide the first layer 202 with the conductive doped regions 204 (e.g., a doping of N⁺ to create a very low resistivity in a range). In the illustrated example, the conductive doped regions 204 provide electrically conductive pathways for electrons to flow between, for example, separate structures of the gate oxide layer 206.

[0031] As shown in FIGS. 7 and 8, the example ILD layer 210 is formed or deposited on the substrate layer 202 and the patterned structures of the gate oxide layer 206 and the polysilicon layer 208. In the illustrated

example, the ILD layer 210 is contact patterned and/or etched away using, for example, a photo lithography process to form the patterned structures of the ILD layer 210 shown in the illustrated example of FIG. 8.

[0032] In the illustrated example of FIG. 9, the metal layers 212, 214 are deposited on the ILD layer 210 and the substrate layer 202. In some examples, the metal layer 214 is formed of TiN, TaN, NbN, HfN, ZrN, RuO₂, IrO₂, Al, Ta, Ti, Cu, Co, Ni, Nb, Mo, W, Hf, Zr, Cr, etc. and/or AlCuSi and is used as a bottom electrode for the memristor 215 (FIG. 2). In the illustrated example of FIG. 10, the memristor switching oxide layer 216 is deposited on and/or formed using the metal layer 214. In some examples, the memristor switching oxide layer 216 is TiO_x or TaO_x and has a thickness of between about, for example, a few nanometers to a dozen nanometers. In some examples in which the memristor switching oxide layer 216 is formed using the metal layer 214, the metal layer 214 is oxidized to form the memristor switching oxide layer 216.

[0033] In the illustrated example of FIG. 11, a memristor top electrode 218 is deposited on the memristor switching oxide layer 216. In some examples, the memristor top electrode 218 is formed using Ta and/or TaAl. In the illustrated example of FIG. 12, the memristor switching oxide layer 216 and/or the memristor top electrode layer 218 is patterned and/or etched using a photo lithography process. In the illustrated example of FIG. 13, the dielectric layer 220 is then deposited, patterned and/or etched on the ILD layer 210, the metal layer 212, the metal layer 214 and the memristor top electrode layer 218. In the illustrated example of FIG. 14, the metal layer 222 is formed on the dielectric layer 220, the metal layer 214 and the memristor top electrode layer 218. Also, in the illustrated example of FIG. 14, the thermal inkjet resistor layer 224 is formed on the metal layer 222. In the illustrated example, the thermal inkjet resistor layer is a dual layer including a high sheet resistive layer (e.g., tantalum aluminum (TaAl), TaAlO_x, WSiN, TaSiN) and a lower resistive layer (e.g., AlCu). In the illustrated example of FIGS. 14 and 15, the metal layer 222 and the thermal inkjet resistor layer 224 are patterned and/or etched to form bond pad openings. To protect against corrosion, the

passivation layer 226 of the illustrated example is formed on the dielectric layer 220, the metal layer 222 and the thermal inkjet resistor layer 224.

[0034] FIG. 16 illustrates a flowchart representative of example machine readable instructions that may be executed in connection with fabrication lines to produce the integrated circuit 200 of FIG. 2. In this example, the machine readable instructions comprise a production process program for execution by a processor such as the processor 1712 shown in the example processor platform 1702 discussed below in connection with FIG. 17. The production process program may be embodied in software stored on a tangible computer readable storage medium such as a CD-ROM, a floppy disk, a hard drive, a digital versatile disk (DVD), a Blu-ray disk, or a memory associated with the processor 1712, but the entire production process program and/or parts thereof could alternatively be executed by a device other than the processor 1712 and/or embodied in firmware or dedicated hardware. Further, although the example production process is described with reference to the flowchart illustrated in FIG. 16, many other methods of producing the example integrated circuit 200 may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined.

[0035] As mentioned above, the example processes of FIG. 16 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a tangible computer readable storage medium such as a hard disk drive, a flash memory, a read-only memory (ROM), a compact disk (CD), a digital versatile disk (DVD), a cache, a random-access memory (RAM) and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term tangible computer readable storage medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media. As used herein, "tangible computer readable storage medium" and "tangible machine readable storage medium" are used

interchangeably. Additionally or alternatively, the example processes of FIG. 16 may be implemented using coded instructions (e.g., computer and/or machine readable instructions) stored on a non-transitory computer and/or machine readable medium such as a hard disk drive, a flash memory, a read-only memory, a compact disk, a digital versatile disk, a cache, a random-access memory and/or any other storage device or storage disk in which information is stored for any duration (e.g., for extended time periods, permanently, for brief instances, for temporarily buffering, and/or for caching of the information). As used herein, the term non-transitory computer readable medium is expressly defined to include any type of computer readable storage device and/or storage disk and to exclude propagating signals and to exclude transmission media. As used herein, when the phrase "at least" is used as the transition term in a preamble of a claim, it is open-ended in the same manner as the term "comprising" is open ended.

[0036] The example process of FIG. 16 is described below in connection with the example structures described above in connection with FIG. 2 – 15. The example process of FIG. 16 begins by forming the gate oxide layer 206 on the substrate layer 202 (block 1602). The polysilicon layer 208 is then formed on the gate oxide layer 206 (block 1603). At block 1604, the gate oxide layer 206 and the polysilicon layer 208 are patterned and etched to form patterned structures of the gate oxide layer 206 and the polysilicon layer 208, as shown in FIG. 5 (block 1604). At block 1606, the substrate layer 202 undergoes an in-situ doping and/or implanting process to form the conductive and/or doped regions (e.g., N+ doping) 204 in the substrate layer 202, as shown in FIG. 6 (block 1606).

[0037] The first ILD layer 210 is then formed or deposited on the doped regions 204 and on the patterned structures formed by the polysilicon layer 208 and/or the gate oxide layer 206, as shown in FIG. 7 (block 1608). The ILD layer 210 is then patterned and/or etched, as shown in FIG. 8 (block 1610). At block 1612, the first metal layer 212 is deposited on the portions of the ILD layer 210 and portions of the doped regions 204 (block 1612). At block 1613, the second metal layer 214 is deposited on the first metal layer

212, as shown in FIG. 9 (block 1613). At block 1614, the first metal layer 212 and the second metal layer 214 are patterned and/or etched to form the etched structures of the first metal layer 212 and the second metal layer 214 as shown in FIG. 9 (block 1614). In some examples, the oxide layer (e.g., memristor switching oxide layer) 216 is formed on portions of the second metal layer 214 and the ILD layer 210, as shown in FIG. 10 (block 1615). For example, the oxide layer 216 may be formed by sputtering on or depositing on the second metal layer 214 and the ILD layer 210. Alternatively, the metal layer 214 and/or 216 may be oxidized.

[0038] At block 1616, the metal layer (e.g., a top memristor electrode) 218 is formed or deposited on the oxidized layer 216, as shown in FIG. 11 (block 1616). At block 1618, the oxide layer 216 and the third metal layer 218 are patterned and etched as shown in FIG. 12 (block 1618). The second ILD layer 220 is formed or deposited on the first ILD layer 210, the first metal layer 212, the second metal layer 214, the oxide layer 216 and the metal layer 218 (block 1620). The second ILD layer 220 is patterned and etched, as shown in FIG. 13 (block 1622).

[0039] At block 1624, the fourth metal layer 222 is deposited on the ILD layer 220, the metal layer 214 and the metal layer 218 (block 1624). At block 1624, the fifth metal layer 224 is deposited on the fourth metal layer (block 1625). At block 1626, the fourth and fifth metal layers 222, 224 are patterned and etched using a sloped metal etch or dry etch process to define the TIJ resistor, as shown in FIG. 14 (block 1626). To protect against corrosion, the passivation layer 226 is formed or deposited on the second ILD layer 220, the fourth metal layer 222 and the fifth metal layer 224, as shown in FIG. 15 (block 1628). The passivation layer 225 is then patterned and/or etched to form a bondpad opening (block 1630).

[0040] FIG. 17 is a printhead fabrication line 1700 showing example printheads 1701 being produced thereon. In the illustrated example, the example printheads 1701 include the integrated circuit 200 of FIG. 2. The printhead fabrication line 1700 includes a printhead fabrication system 1703 having a processor 1702 capable of executing the instructions of FIG. 16 to

produce the integrated circuit 200 of FIG. 2 and/or any of the example structures disclosed herein. The processor platform 1702 can be, for example, a server, a personal computer or any other type of computing device.

[0041] The processor platform 1702 of the illustrated example includes a processor 1712. The processor 1712 of the illustrated example is hardware. For example, the processor 1712 can be implemented by one or more integrated circuits, logic circuits, microprocessors or controllers from any desired family or manufacturer.

[0042] The processor 1712 of the illustrated example includes a local memory 1713 (e.g., a cache). The processor 1712 of the illustrated example is in communication with a main memory including a volatile memory 1714 and a non-volatile memory 1716 via a bus 1718. The volatile memory 1714 may be implemented by Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic Random Access Memory (RDRAM) and/or any other type of random access memory device. The non-volatile memory 1716 may be implemented by flash memory and/or any other desired type of memory device. Access to the main memory 1714, 1716 is controlled by a memory controller.

[0043] The processor platform 1702 of the illustrated example also includes an interface circuit 1720. The interface circuit 1720 may be implemented by any type of interface standard, such as an Ethernet interface, a universal serial bus (USB), and/or a PCI express interface.

[0044] In the illustrated example, one or more input devices 1722 are connected to the interface circuit 1720. The input device(s) 1722 permit(s) a user to enter data and commands into the processor 1712. The input device(s) can be implemented by, for example, a keyboard, a button, a mouse, a touchscreen, a track-pad and/or a trackball.

[0045] One or more output devices 1724 are also connected to the interface circuit 1720 of the illustrated example. The output devices 1724 can be implemented, for example, by display devices (e.g., a light emitting diode (LED), an organic light emitting diode (OLED), a touchscreen, a tactile output device, a printer and/or speakers). The interface circuit 1720 of the illustrated

example, thus, typically includes a graphics driver card, a graphics driver chip or a graphics driver processor.

[0046] The interface circuit 1720 of the illustrated example also includes a communication device such as a transmitter, a receiver, a transceiver, a modem and/or network interface card to facilitate exchange of data with external machines (e.g., computing devices of any kind) via a network 1726 (e.g., an Ethernet connection, a digital subscriber line (DSL), a telephone line, coaxial cable, a cellular telephone system, etc.).

[0047] The processor platform 1702 of the illustrated example also includes one or more mass storage devices 1728 for storing software and/or data. Examples of such mass storage devices 1728 include floppy disk drives, hard drive disks, compact disk drives, Blu-ray disk drives, RAID systems, and digital versatile disk (DVD) drives.

[0048] Coded instructions 1732 of FIG. 17 may include the example machine readable instructions represented by the flowchart of FIG. 16. In the illustrated example, the coded instructions 1732 may be stored in the mass storage device 1728, in the volatile memory 1714, in the non-volatile memory 1716, and/or on a removable tangible computer readable storage medium such as a CD or DVD.

[0049] From the foregoing, it will be appreciated that above disclosed methods, apparatus and articles of manufacture provide a print head and/or imaging device (e.g., printer, copier, etc.) with a large number of memory bits while using a significantly reduced foot-print and enabling significant cost saving. Additionally or alternatively, examples disclosed herein enable and/or facilitate programing and/or reading of secure data stored on a printhead to substantially prevent counterfeiting and/or assist with anti-counterfeiting technologies. Additionally or alternatively, examples disclosed herein increase the number of memory bits while using a smaller area on the printhead, thereby increasing the security of devices produced in accordance with the disclosed examples. In contrast to some known memories, such as erasable programmable read only memories (EPROM), example memristor memories are advantageously used in examples disclosed herein to form

memory on a printhead while using a relatively small amount of space on the print head. Example memristor memories are also used in examples disclosed herein to form memories on printheads while substantially reducing thinfilm damage on the printhead caused by fuse breakdown, reducing costs, etc. relative to known techniques for locating memory devices on printheads. For example, using the example memories disclosed herein as compared to some existing technologies, the number of bits that can be stored in ID lines (e.g., the ID line 120 of FIG. 1A) can be increased by approximately four times (e.g., from 256 bits to 1024 bits) and/or the amount of physical space used by the memories on a printhead may be reduced by approximately 88%.

[0050] Illustrated examples disclosed herein describe forming or manufacturing memristors integral to a printhead. In some examples, the memristors may be TiO_x -based devices where “x” is a non-stoichiometric compound or TaO_x -based device including TaSiO_x . In some examples, TiO_x -based devices advantageously provide high endurance with non-volatility, fast switching, low-energy operation, multiple-state operation, scalability and/or stackability characters. In some examples, TaO_x -based devices advantageously provide endurance and/or non-linearity. In some examples, example printheads disclosed herein include two metal layers being different metal layers and/or stacks where the first metal layer(s) includes AlCuSi and/or a bottom electrode for memristor memory and the second metal layer(s) includes a top electrode for the memristor memory and a thermal inkjet (e.g., a relatively high sheet resistive layer (e.g., TaAl , TaAlO_x , or WSiN) and a low sheet resistive layer (e.g., AlCu)).

[0051] In some examples, the forming and/or switching voltage for the memristors is less than 5 Volts (V). Often, the voltage available to integrated circuits such as the example integrated circuit 200 (FIG. 2) disclosed herein is up to approximately 15.5V. Thus, there is sufficient voltage to operate the memristors and no negative voltage is necessary for switching off. In addition, some example memristor structures on printheads manufactured using examples disclosed herein may be manufactured at even further significant cost savings based on some memristor implementations needing to

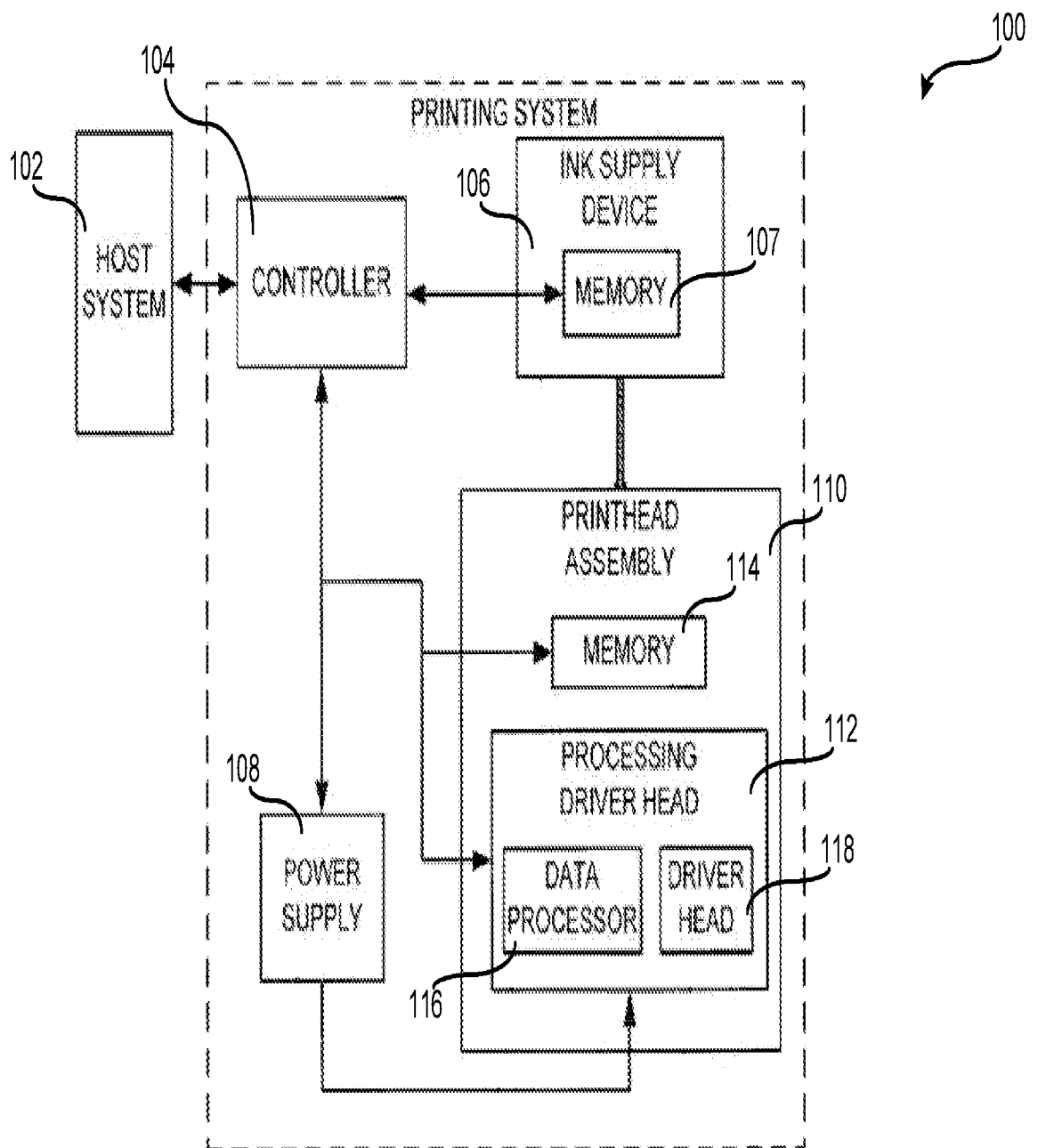
be able to withstand only a one-time-programming (OTP) process rather than multiple programming processes. That is, some memristors on printheads may only be programmed once (e.g., to store data in the ID line 120 of FIG. 1A) during initialization and/or in a manufacturing process.

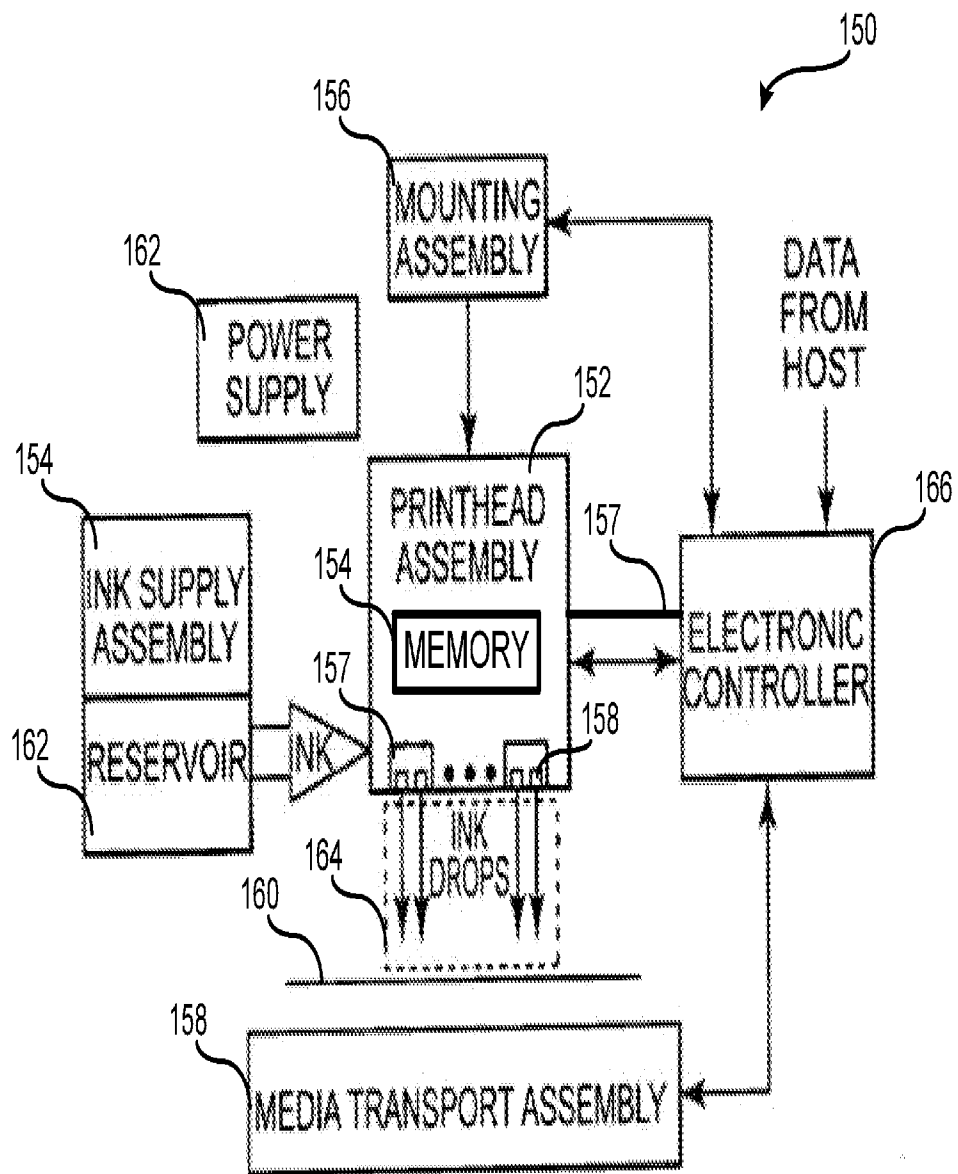
[0052] Although certain example methods, apparatus and articles of manufacture have been disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the claims of this patent.

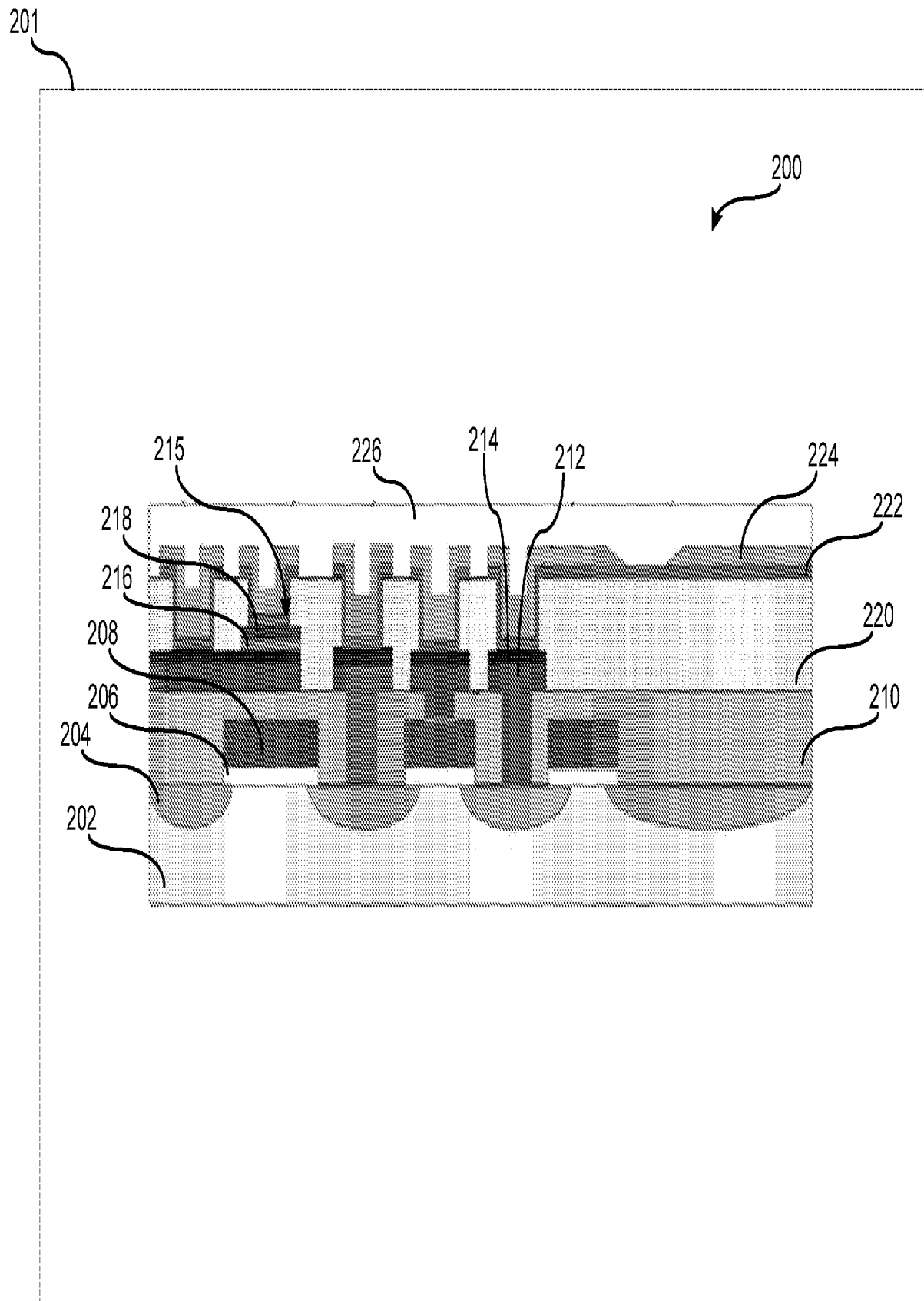
What Is Claimed Is:

1. An apparatus, comprising:
a printhead body comprising a first metal layer; and
a memory formed on the printhead body, the memory comprising the first metal layer as a first electrode, a second metal layer as a second electrode, and a switching oxide layer between the first and second metal layers.
2. The apparatus of claim 1, wherein the printhead body further comprises a doped substrate layer, a gate oxide layer, and a polysilicon layer, the gate oxide layer is positioned between the doped substrate layer and the polysilicon layer.
3. The apparatus of claim 2, wherein the printhead body further comprises a dielectric layer between the doped substrate layer and the first metal layer.
4. The apparatus of claim 3, wherein the printhead body further comprises a third metal layer, the dielectric layer being positioned between the doped substrate layer and the third metal layer.
5. The apparatus of claim 4, wherein the third metal layer comprises a thermal ink jet resistor layer.
6. The apparatus of claim 1, wherein the thermal ink jet resistor layer comprises one or more layers.

7. An apparatus, comprising:
 - an imaging device;
 - a printhead body for use with the imaging device, the printhead body comprising:
 - a first metal layer on the printhead body; and
 - a memory on the first metal layer, the memory comprising a switching oxide layer, the first metal layer, and a second metal layer, the first metal layer providing a first electrode, the second metal layer providing a second electrode.
8. The apparatus of claim 7, wherein the printhead body is removably coupled to the imaging device.
9. The apparatus of claim 7, wherein the imaging device comprises a printer or a copier.
10. The apparatus of claim 7, wherein the printhead body is integrally coupled to the imaging device.
11. The apparatus of claim 7, wherein the memory comprises a memristor.
12. A method, comprising:
 - fabricating a printhead body comprising a first metal layer;
 - integrally forming a memory with the printhead body by forming a switching oxide layer on the first metal layer and a second metal layer on the switching oxide layer, wherein the first metal layer comprises a first electrode of the memory and the second metal layer comprises a second electrode of the memory.
13. The method of claim 12, wherein forming the oxide layer comprises oxidizing a portion of the first metal layer.
14. The method of claim 12, wherein forming the oxide layer comprises depositing or sputtering the oxide layer on the first metal layer.
15. The method of claim 12, wherein integrally forming the memory comprises etching the oxide layer, the switching oxide layer, and the second metal layer.







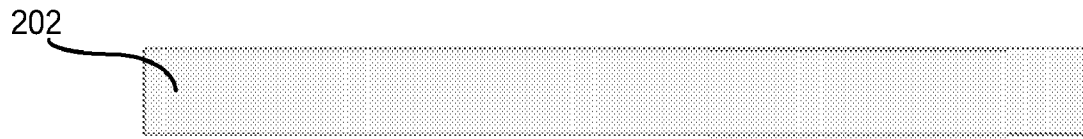


FIG. 3

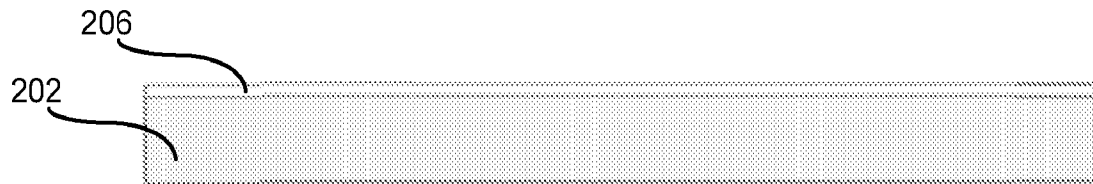


FIG. 4

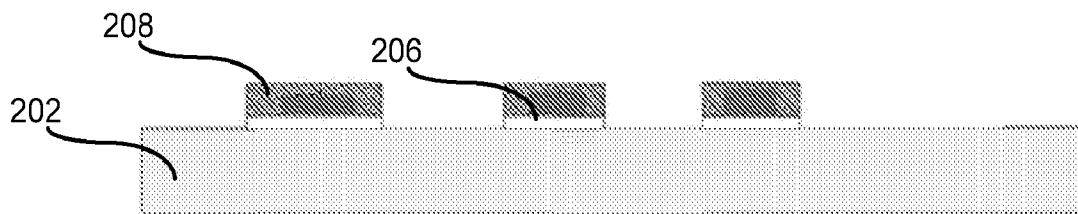


FIG. 5

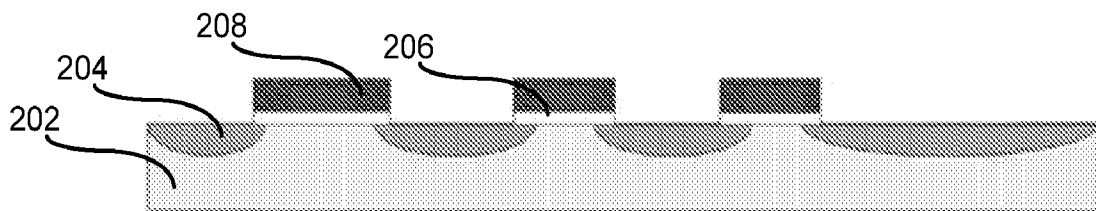


FIG. 6

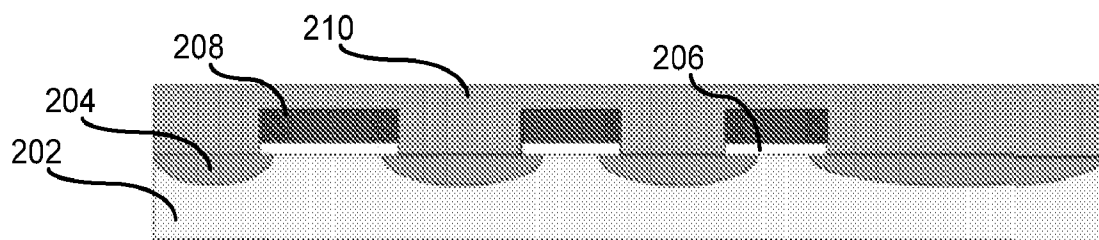


FIG. 7

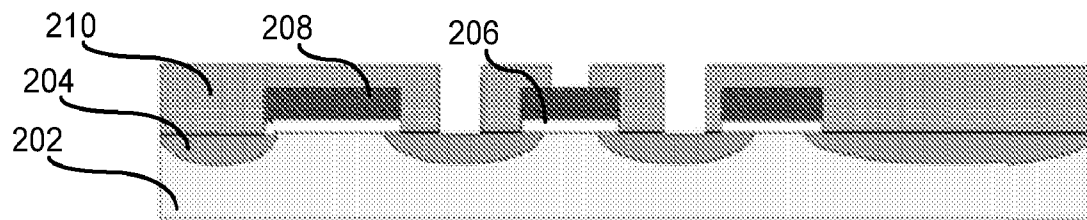


FIG. 8

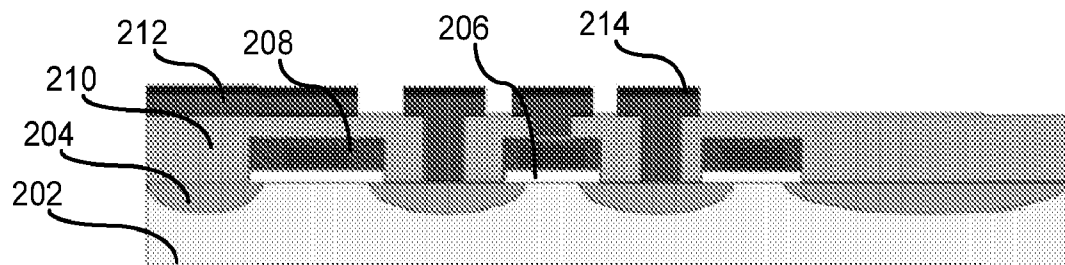


FIG. 9

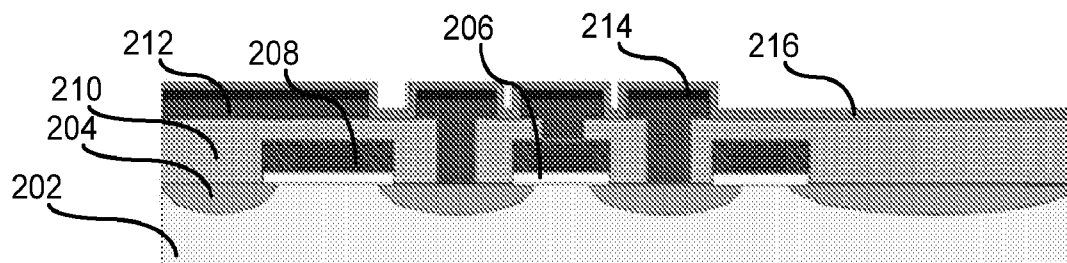


FIG. 10

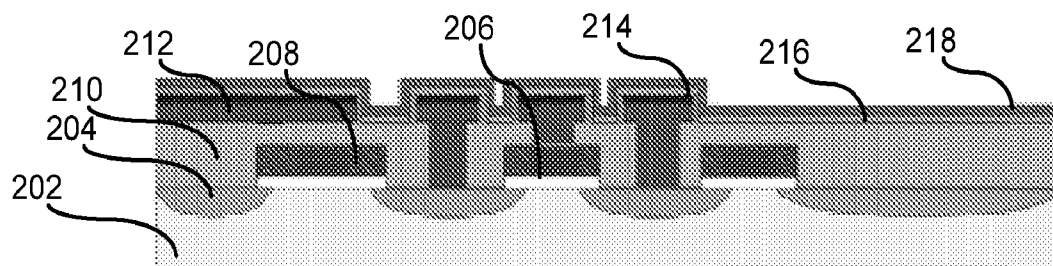


FIG. 11

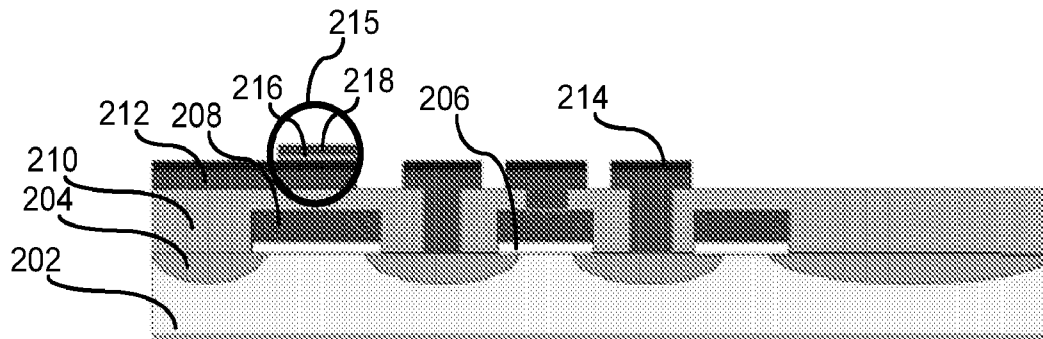


FIG. 12

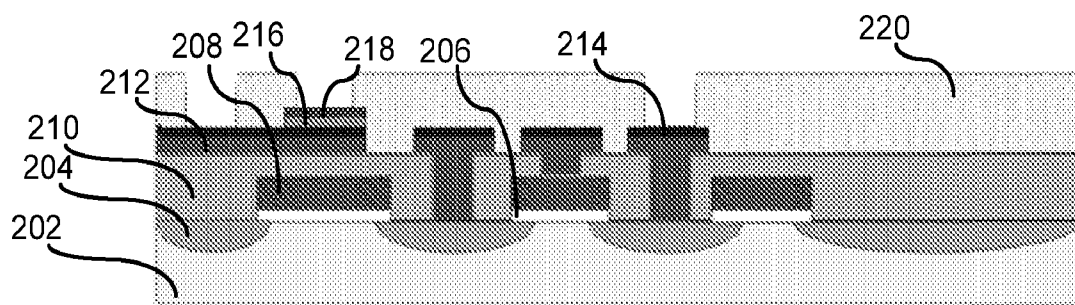


FIG. 13

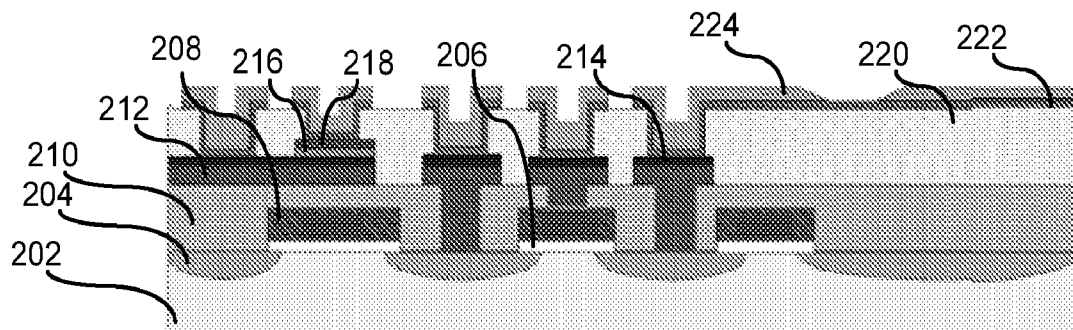


FIG. 14

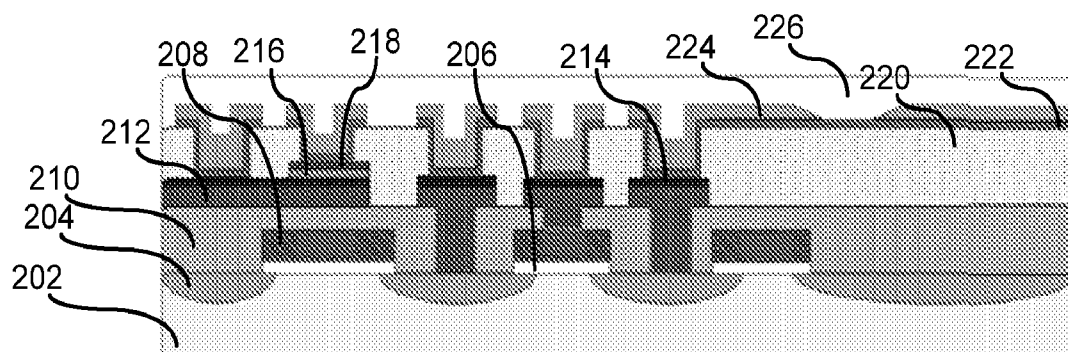


FIG. 15

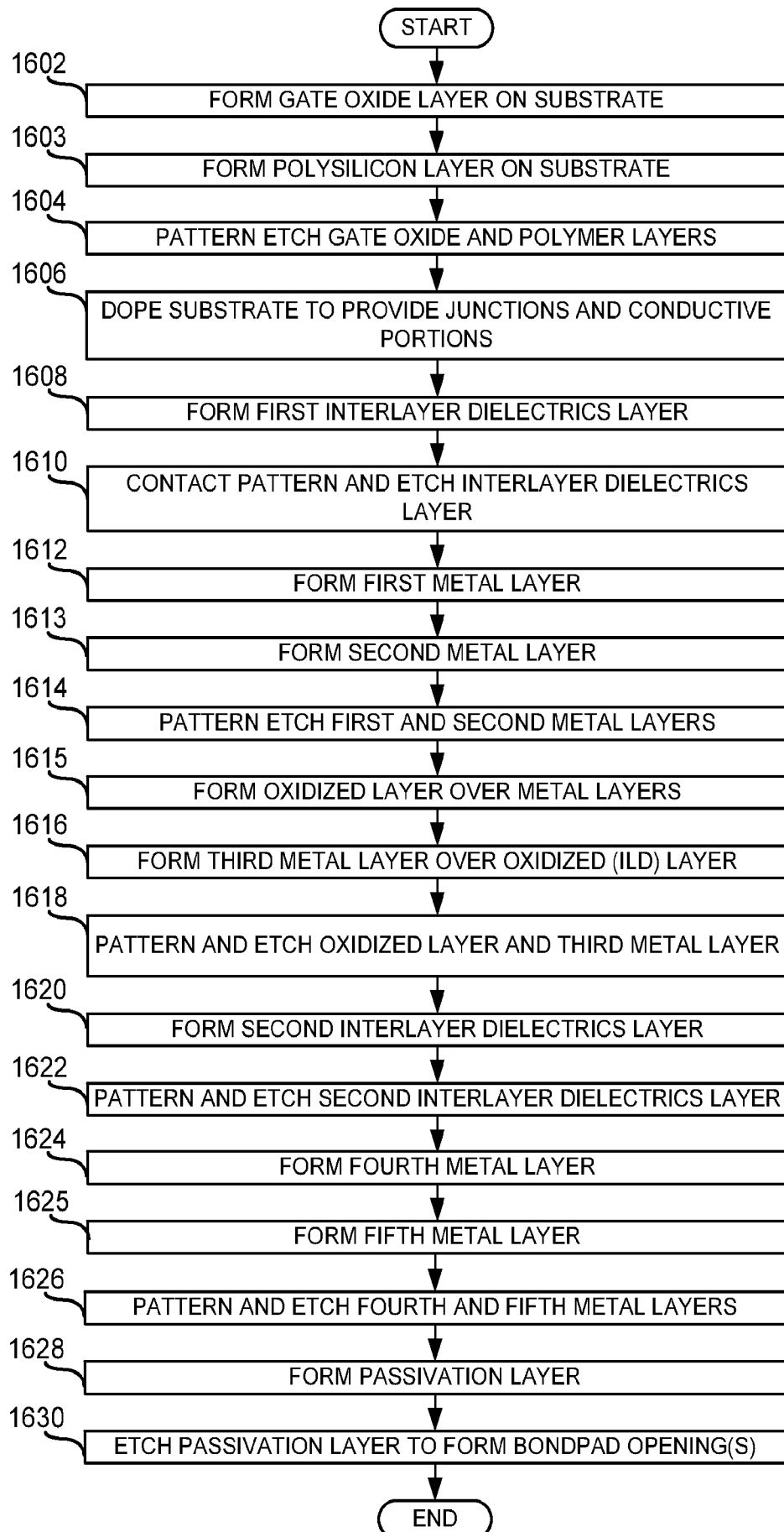
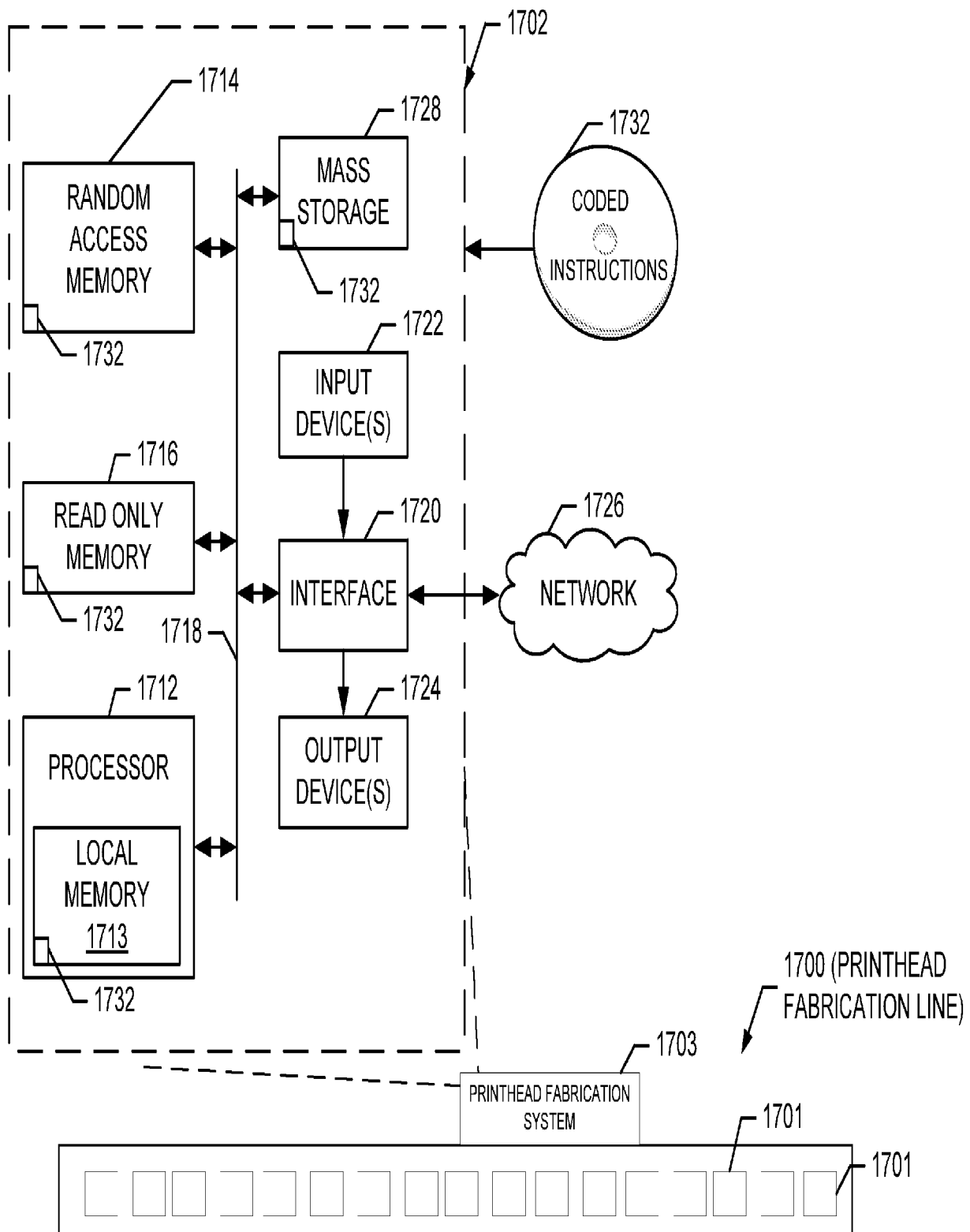


FIG. 16



A. CLASSIFICATION OF SUBJECT MATTER**B41J 2/045(2006.01)i, B41J 2/14(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

B41J 2/045; B41J 2/04; B41J 2/07; H01H 57/00; B41J 29/38; H01G 9/00; B41J 2/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: metal layer, electrode, oxide layer, memory, print, printhead, memristor, dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0106930 A1 (LEA et al.) 02 May 2013 See abstract, paragraphs [0020], [0022], [0023], [0032], [0035], and figures 2, 3A, 5A.	1, 7-15
Y		2
A		3-6
Y	US 2006-0238576 A1 (LEE et al.) 26 October 2006 See paragraphs [0034], [0035] and figure 2.	2
A	US 2006-0055745 A1 (YAGI, TAKASHI) 16 March 2006 See paragraphs [0047], [0050], [0053], [0054], [0057], [0058] and figures 2, 3.	1-15
A	US 2007-0242110 A1 (BRUCE et al.) 18 October 2007 See paragraph [0030] and figure 4.	1-15
A	US 2008-0048520 A1 (GULVIN et al.) 28 February 2008 See paragraphs [0047]-[0051] and figures 4A-5D.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 July 2014 (18.07.2014)

Date of mailing of the international search report

21 July 2014 (21.07.2014)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

KIM, Jin Ho

Telephone No. +82-42-481-8699



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/067872

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0106930 A1	02/05/2013	None	
US 2006-0238576 A1	26/10/2006	TW 250938 B US 7367657 B2	11/03/2006 06/05/2008
US 2006-0055745 A1	16/03/2006	JP 04802469 B2 JP 2006-086223 A US 7753497 B2	26/10/2011 30/03/2006 13/07/2010
US 2007-0242110 A1	18/10/2007	CN 101885268 A CN 101885268 B CN 1660564 A CN 1660564 B EP 1568498 A2 EP 1568498 A3 EP 1568498 B1 JP 04323442 B2 JP 2005-238843 A KR 10-1212053 B1 KR 10-2006-0041941 A SG 114671 A1 SG 131952 A1 US 2005-0185022 A1 US 7240997 B2 US 7798616 B2	17/11/2010 13/06/2012 31/08/2005 29/09/2010 31/08/2005 14/12/2005 21/12/2011 02/09/2009 08/09/2005 13/12/2012 12/05/2006 28/09/2005 28/05/2007 25/08/2005 10/07/2007 21/09/2010
US 2008-0048520 A1	28/02/2008	US 8450902 B2	28/05/2013