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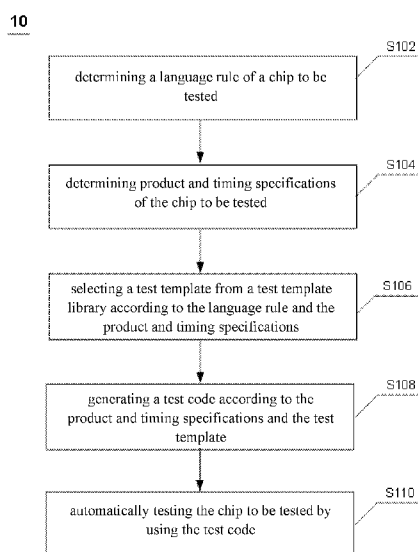


FIG. 1

(57) Abstract: A chip testing method, device, electronic apparatus, and computer readable medium are provided, relating to the field of chip testing. The method includes: determining a language rule of a chip to be tested; determining product and timing specifications of the chip to be tested; selecting a test template from a test template library according to the language rule and the product and timing specifications; generating a test code according to the product and timing specifications and the test template; and automatically testing the chip to be tested by using the test code. The chip testing method, device, electronic apparatus and computer readable medium can automatically generate a big-data test code for complex memories, and rapidly generate, in a standardized way, test codes for DDR4 memories of different specifications, thereby improving the efficiency of chip product verification analysis.



CHIP TESTING METHOD, DEVICE, ELECTRONIC APPARATUS AND COMPUTER READABLE MEDIUM

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority of the Chinese Patent Application No. 201811261790.3, filed on October 26, 2018 and entitled “CHIP TESTING METHOD, DEVICE, ELECTRONIC APPARATUS AND COMPUTER READABLE MEDIUM.” The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to the technical field of chip testing and, more specifically, to a chip testing method, apparatus, electronic apparatus, and computer readable medium.

BACKGROUND

[0003] With the rapid development in memory technologies and the rapid expansion of the memory market, memory chips with large capacity, fast read/write speed, and low price are dominating the market. To ensure long-term reliability of these memory chips, they need to undergo meticulous high speed tests before being released to the market.

[0004] In the related art regarding the testing of memory products, the majority of work need to be manually done by a tester. The tester first needs to confirm a corresponding model and speed for a memory product to be tested, and then a test scheme suitable for the memory product needs to be selected. After the test scheme is selected, the tester also needs to manually write the test codes. Codes need to be written for each test instruction in a test sequence, and then the memory product can be tested after the codes have been completed.

[0005] The chip testing that relies on manually-written codes requires substantial manpower and material resources and thus results in a low efficiency of memory testing. Moreover, with the development in memory technologies, more and more high-speed, high-

capacity memories come to the market, and chip testing for these memories requires increasingly complicate and voluminous test codes. For high-speed, high-capacity memories, chip testing with big-data test codes that need to be manually written has become a limiting factor in the development of memory testing industry.

[0006] Therefore, a new chip testing method, device, electronic apparatus, and computer readable medium that can address the aforementioned issues are desired.

[0007] The above information is only used to facilitate understanding the background of the present disclosure, and thus may include information that does not constitute prior art known to a person of ordinary skill in the art.

SUMMARY

[0008] In view of the limitations of existing technologies described above, the present disclosure provides a chip testing method, device, electronic apparatus, and computer readable medium, which can automatically generate a big-data test code for complex memory and improve chip testing efficiency.

[0009] Other features and advantages of the present disclosure will be apparent from the following detailed description or obtained in part from the practice of the disclosure.

[0010] One aspect of the present disclosure is directed to a chip testing method. The method may include: determining a language rule of a chip to be tested; determining product and timing specifications of the chip to be tested; selecting a test template from a test template library according to the language rule and the product and timing specifications; generating a test code according to the product and timing specifications and the test template; and automatically testing the chip to be tested by using the test code.

[0011] In some embodiments of the present disclosure, the method may further include: generating the test template library based on a plurality of test templates. The plurality of test templates may include: a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and a pre-charge power-down test template.

[0012] In some embodiments of the present disclosure, the chip may comprise a memory chip.

[0013] In some embodiments of the present disclosure, the memory chip may be a DDR4 chip.

[0014] In some embodiments of the present disclosure, determining the language rule of the chip to be tested may include: determining a language rule for the chip to be tested according to a specification document of the chip to be tested.

[0015] In some embodiments of the present disclosure, determining the product and timing specifications of the chip to be tested may comprise: determining a memory cell address, a memory row address, a memory column address, and a memory page size of the chip to be tested; and determining a model identification, a product identification, and parameters of the chip to be tested.

[0016] In some embodiments of the present disclosure, selecting a test template from a test template library according to the language rule and the product and timing specifications may comprise: determining a database of the chip to be tested according to the product and timing specifications; and selecting the test template from the test template library according to the language rule and the database.

[0017] In some embodiments of the present disclosure, selecting a test template from a test template library according to the language rule and the product and timing specifications may comprise: determining a database of the chip to be tested according to the product and timing specifications; and designating the test template from the test template library according to the language rule and the database.

[0018] In some embodiments of the present disclosure, generating a test code according to the product and timing specifications and the test template may comprise: inserting a timing sequence into the test template according to the product and timing specifications to generate the test code.

[0019] In some embodiments of the present disclosure, inserting a timing sequence into the test template to generate the test code according to the product and timing specifications may comprise: inserting the timing sequence into the test template according to the product and

timing specifications; and converting the inserted timing sequence by a high-speed test machine to generate the test code.

[0020] Another aspect of the present disclosure is directed to a chip testing device. The device may include: a parameter reading interface, a code generating module, and a high-speed test machine. The parameter reading interface may be configured to determine a language rule of a chip to be tested, and to determine product and timing specifications of the chip to be tested. The code generating module may be configured to select a test template from a test template library according to the language rule and the product and timing specifications, and to generate a test code according to the product and timing specifications and the test template. The high-speed test machine may be configured to automatically test the chip to be tested using the test code.

[0021] In some embodiments of the present disclosure, the device may further include: a test template library module. The test template library module may be configured to generate the test template library based on a plurality of test templates. The plurality of test templates may comprise: a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and pre-charge power-down test template.

[0022] In some embodiments of the present disclosure, the code generating module may comprise: a selection module, configured to select a test template from a test template library according to the language rule and a database.

[0023] Another aspect of the present disclosure is directed to a chip testing device. The device may include: an information module, a native random pattern creator, a format conversion module, and a test module. The information module may be configured to acquire related information of a chip to be tested. The native random pattern creator may be configured to generate random patterns for testing the chip to be tested according to a target test template, information in the information module and content of a database. The format conversion module may be configured to insert a timing sequence into the random patterns according to product and timing specifications, and to convert the inserted timing sequence by a high-speed test machine to generate a test code. The test module may be configured to generate an

automated test code.

[0024] In some embodiments of the present disclosure, the device may further include: a template library, configured to store a plurality of test templates; and a template model module, configured to store the target test template. The target test template may be one of the plurality of test templates.

[0025] Another aspect of the present disclosure is directed to an electronic apparatus. The apparatus may include one or more processors and a memory device. The memory device may be configured to store one or more programs. Upon being executed by the one or more processors, the one or more programs may cause the one or more processors to perform the chip test method in any of the aforementioned embodiments.

[0026] Another aspect of the present disclosure is directed to a computer readable medium storing a computer program executable by a processor. Upon being executed by the processor, the computer program may cause the processor to perform the chip test method of any of the aforementioned embodiments.

[0027] According to the chip testing method, device, electronic apparatus and computer readable medium of the present disclosure, a flexible architecture may be constructed specifically for the DDR4 memory test, and the DDR4 memory test code may be automatically generated according to the product specification. A big-data test code of for complex memories may be automatically generated, thereby improving the efficiency of chip product verification analysis.

[0028] It should be understood that the above general description and the following detailed description are merely exemplary, and it is not intended to limit the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The above and other objectives, features, and advantages of the present disclosure will become more apparent after reading the exemplary embodiments in view of the accompanying drawings. The drawings described below are only some of the embodiments of the present disclosure, and those skilled in the art can obtain other drawings based on these drawings without any creative work.

[0030] FIG. 1 shows a flow chart illustrating a chip testing method in accordance with one embodiment of this invention.

[0031] FIG. 2 shows is a schematic diagram of a chip testing method in accordance with one embodiment of this invention.

[0032] FIG. 3 shows a block diagram of a chip testing device in accordance with one embodiment of this invention.

[0033] FIG. 4 shows a block diagram of a chip testing device in accordance with another embodiment of this invention.

[0034] FIG. 5 shows a schematic diagram of a chip testing device in accordance with one embodiment of this invention.

[0035] FIG. 6 shows a block diagram of an electronic apparatus in accordance with one embodiment of this invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0036] Exemplary embodiments will now be described in detailed with reference to the accompanying drawings. However, the exemplary embodiments can be embodied in a variety of forms and should not be construed to be limited by the embodiments set forth herein. Instead, providing such embodiments may make the present disclosure comprehensive and complete, and completely convey the concept of the present disclosure to those skilled in the art. The same reference numerals in the drawings denote the same or similar parts, and the repeated description thereof will be omitted.

[0037] It shall be understood that, although the terms first, second, third, etc. may be used herein to describe various components, these components shall not be limited by these terms. These terms are used to distinguish one component from another. Thus, a first component discussed below could be termed a second component without departing from the teachings of the present disclosure. The term “and/or” as used herein includes any and all combinations of one or more of the associated listed items.

[0038] It shall be understood by those skilled in the art that the drawings are only a schematic diagram of the exemplary embodiments, and the modules or processes in the drawings are not

necessarily required to implement the disclosure, and therefore are not intended to limit the scope of the disclosure.

[0039] FIG. 1 shows a flow chart showing a chip testing method according to an exemplary embodiment. The chip testing method 10 may include at least steps S102 to S110.

[0040] As shown in FIG. 1, in step S102, a language rule of a chip to be tested may be determined. The chip to be tested may include: a memory, which may specifically be, for example, a DDR4 memory. The language rule of the chip to be tested can be determined according to a specification document of the chip to be tested.

[0041] In this application, “DDR” or “DDR SDRAM” may refer to a dual data rate synchronous dynamic random access memory. DDR4 memory is a new generation of memory specifications. Compared with DDR3, a previous generation of memory specifications, DDR4 has a 16-bit prefetch mechanism. At a same core frequency, the theoretical speed of DDR4 is twice that of DDR3. DDR4 has more reliable transmission specifications, and thus data reliability is further improved. Moreover, DDR4 has a decreased operating voltage of 1.2V, and thus is more energy efficient. DDR4 is also known as the second generation of memory, developed from DDR1, DDR2, DDR3 memory.

[0042] In one embodiment, the language rule of a DDR4 memory can be acquired by referring to the definition in JEDEC Standard No. 79-4B. JEDEC Standard No. 79-4B is the instruction manual for DDR4 SDRAM, which includes information about the features, functions, AC and DC characteristics, package and ball distribution of DDR4 SDRAM. The purpose of this standard is to define the JEDEC minimum standard for x4\x8\x16 DDR4 SDRAM from 2Gbit to 16Gbit.

[0043] In one embodiment, the language rule of a memory may also be acquired from other documents depending on the specifications of the memory. These documents may include, for example: DDR SDRAM STANDARD JESD79; DDR2 SDRAM STANDARD JESD79-2; DDR3 SDRAM STANDARD JESD79-3; and SmartTest 7.4.3 Documentation.

[0044] In one embodiment, the language rule of a chip may describe the operating logic of the chip. The operating logic may include, for example, when the chip is in an activated state, it can be converted to a memory library activated state by an automatic sequence instruction, and when the chip is in an idle state, it can be converted to an activated state by executing an

instruction. The operating logic may include other logics relating to the operation of the chip, which are not exhaustively enumerated herein.

[0045] In step S104, product and timing specifications of the chip to be tested may be determined.

[0046] In one embodiment, determining a product specification of the chip to be tested may include determining a memory cell address, a memory row address, a memory column address, and a memory page size of the chip to be tested.

[0047] In one embodiment, determining a timing specification of the chip to be tested may include determining a model identifier, a product identifier, and a parameter of the chip to be tested. The chip to be tested may include a DDR4 memory, and the product and timing specifications of the DDR4 memory may be defined in JEDEC Standard No. 79-4B.

[0048] The speed class of the DDR4 may include, for example, 3200/2933/2666/2400/2133/1866 and the like.

[0049] Table 1 shows a product specification of the chip according to one embodiment.

Structure		1Gb*4	512Mb*8	256Mb*16
Memory cell address	Number of groups	4	4	2
	Group address	BG0~BG1	BG0~BG1	BG0
	Memory cell address in the group	BA0~BA1	BA0~BA1	BA0~BA1
Memory row address		A0~A15	A0~A14	A0~A14
Memory column address		A0~A9	A0~A9	A0~A9
Memory page size		512B	1KB	2KB
Structure		2Gb*4	1Gb*8	512Mb*16
Memory cell address	Number of groups	4	4	2
	Group address	BG0~BG1	BG0~BG1	BG0
	Memory cell address in the group	BA0~BA1	BA0~BA1	BA0~BA1
Memory row address		A0~A16	A0~A15	A0~A15
Memory column address		A0~A9	A0~A9	A0~A9

Memory page size		512B	1KB	2KB
Structure		4Gb*4	2Gb*8	1Gb*16
Memory cell address	Number of groups	4	4	2
	Group address	BG0~BG1	BG0~BG1	BG0
	Memory cell address in the group	BA0~BA1	BA0~BA1	BA0~BA1
Memory row address		A0~A17	A0~A16	A0~A16
Memory column address		A0~A9	A0~A9	A0~A9
Memory page size		512B	1KB	2KB

[0050] Table 2 shows a timing specification of the chip according to one embodiment:

Model identifier		DDR4-2400P		DDR4-2400R	
Product identifier		15-15-15		16-16-16	
Product parameters	Symbol	min	max	min	max
Internal read command to the first data	tAA	12.50	18.00	13.32	18
Internal read command to read the first data of data inversion (DBI)	tAA_DBI	tAA(min) +3nCK	tAA(max) +3nCK	tAA(min) +3nCK	tAA(max) +3nCK
Open (ACT) to internal read or write delay time	tRCD	12.50		13.32	
Close (PRE) command cycle	tRP	12.50		13.32	
Open (ACT) to close (PRE) command period	tRAS	32	9*tREFI	32	9*tREFI
Open (ACT) to open (ACT) or close (PRE) command	tRC	44.50		45.32	

[0051] In step S106, a test template may be selected from a test template library according to the language rule and the product and timing specifications. For example, step S106 may

include: determining a database of the chip to be tested according to the product and timing specifications, and selecting the test template from the test template library according to the language rule and the database.

[0052] In one embodiment, the method may further include generating the test template library based on a plurality of test templates. The plurality of test templates may comprise: a X-direction/Y-direction fast write operation test template (X/Y fast Write pattern), a X direction/Y direction fast read operation test template (X/Y fast Read pattern), a X direction/Y direction fast read/write operation test template (X/Y fast Write/Read pattern), a self-refreshing test template (Self refresh), a refreshing test template (Refreshing), a ZQ calibration test template (ZQ calibration), a pre-charge power-down test template (Pre-charge Power down), and a mode register setting test template (Mode Register Set).

[0053] In one embodiment, selecting a test template from a test template library according to the language rule and the database may comprise: first selecting a plurality of test templates that meet the condition in the test template library according to the language rule. Then the plurality of test templates may be subjected to a secondary screening according to the content in the database corresponding to the chip to be tested, so that the templates that do not meet the requirements of the chip may be removed. Finally, a test template may be selected from the rest of the plurality of test templates.

[0054] In one embodiment, the number of selected test template may be one or more, which is not limited in this disclosure.

[0055] In one embodiment, the method may include: determining a database of the chip to be tested according to the product and timing specifications; and designating the test template from the test template library according to the language rule and the database. Specifically, the method may comprise: first selecting a plurality of test templates that meet the condition in the test template library according to the language rule. Then the plurality of test templates may be subjected to a secondary screening according to the content in the database corresponding to the chip to be tested, so that the templates that does not meet the requirements of the chip may be removed. Finally, according to the expert's opinions or based on the experience from history product analysis, a target test template may be designated from the rest of the plurality of test templates.

[0056] In step S108, a test code may be generated according to the product and timing specifications and the test template. In one example, step S108 may include: inserting a timing sequence into the test template according to the product and timing specifications to generate the test code.

[0057] In one embodiment, inserting a timing sequence into the test template according to the product and timing specifications to generate the test code may include: inserting the timing sequence into the test template according to the product and timing specifications; and converting the inserted timing sequence by a high-speed test machine to generate the test code.

[0058] In one embodiment, the high-speed test machine may be an HSM6800 high-speed test machine, and the HSM6800 high-speed test machine may have a programmable function to support the tests for advanced features of GDDR5 (Graphics Double Data Rate, version 5), which includes Address Bus Inversion (ABI), Data Bus Inversion (DBI), and Cyclic Redundancy Check (CRC). In addition, the test machine can test the memory of a common 8-bit data frame (frame) due to its flexible architecture, and can also be extended to test 10-bit data frame memory in the future. Thus the test machine can meet the requirements in performance, functionality and cost for the testing of all kinds of high-speed memories.

[0059] In step S110, the chip to be tested may be automatically tested using the test code. An automated test code may be generated by using the programmable function of the HSM6800 high-speed test machine and the language rules of DDR4 memory, which enables the test machine to automatically generate a big-data test code for memories. The generated test code may be used to simulate system environment test to expedite the unit test of the DDR4 memory.

[0060] In one embodiment, during the test, each write action may be recorded by the database while the read actions may be generated based on the current contents of the database.

[0061] FIG. 2 shows a schematic diagram of a chip testing method in accordance with one embodiment of this invention. FIG. 2 exemplarily shows a pattern of test codes for DDR4 memories of different specifications rapidly generated by the chip testing method of the present disclosure.

[0062] As shown in FIG. 2, the language rule and the product and timing specifications of the chip to be tested may be determined first. Then the test template may be selected from the

test template library according to the language rule and the product and timing specifications. Then the test code may be automatically generated according to the product and timing specifications and the test template, and the specific pattern of the test code may be a pulse code composed of 0 or 1.

[0063] According to the schematic diagram of the chip testing method as shown in FIG. 2, a user may inspect the relevant test parameters of the test template from the parameter setting area 202, and, if necessary, modify the test parameters. The user can inspect various test commands corresponding to the test template from the command selection area 204 to further understand the test. A specific test code is shown in the code region 206, and the specific test code consists of a pulse sequence composed of 0 or 1, wherein 1 may represent a high level, and 0 may represent a low level.

[0064] According to the chip testing method of the present disclosure, the test template may be selected from the test template library according to the language rule and the product and timing specifications. The test code may be generated according to the product and timing specifications and the test template. Therefore, a big-data test code of complex memory can be generated automatically, and the test codes for DDR4 memories of different specifications can be generated rapidly in a standardized way, thereby improving the efficiency of chip product verification analysis.

[0065] According to the chip testing method of the present disclosure, a flexible architecture may be constructed specifically for the DDR4 memory test, and the DDR4 memory test code may be automatically generated according to the content of the product specification. Compared to manually written codes, the automatically-generated codes may be created with much higher efficiency. Thus, the problem associated with manually writing a big-data test code for complex DDR4 memory in the related art can be solved.

[0066] According to the chip testing method of the present disclosure, the test codes for DDR4 memories of different specifications can be rapidly generated in a standardized way, thus human errors that are inevitable in manual coding can be avoided, and the quality of the test codes may be improved.

[0067] According to the chip testing method of the present disclosure, detailed coding procedural information can be provided, and each procedure in the test coding can be presented

to a human inspector. Therefore, in case an error is reported during a test, the human inspector can perform a positioning analysis according to the test code to quickly identify and remedy an issue, thereby improving the efficiency of the product analysis.

[0068] This invention further presents a chip testing device based on the aforementioned chip testing method. The device may be configured to implement the chip testing method according to the embodiments of the present disclosure. Any detail not disclosed herein can be obtained by referring to the embodiments for the method of the present disclosure.

[0069] FIG. 3 shows a block diagram of a chip testing device in accordance with one embodiment of this invention. The chip testing device 30 may include a parameter reading interface 302, a code generating module 304, and a high-speed test machine 306.

[0070] The parameter reading interface 302 may be configured to determine a language rule of the chip to be tested, and to determine product and timing specifications of the chip to be tested. The chip to be tested may include: a memory, which may be, for example, a DDR4 memory.

[0071] In one embodiment, the product and timing specifications of the DDR4 memory and the language specifications of the DDR4 memory may be acquired by referring to the definitions in JEDEC Standard No. 79-4B.

[0072] The code generating module 304 may be configured to select a test template from a test template library according to the language rule and the product and timing specifications, and to generate a test code according to the product and timing specifications and the test template.

[0073] In one embodiment, the code generating module 304 may determine a database of the chip to be tested according to the product and timing specifications, and select the test template from the test template library according to the language rule and the database.

[0074] In one embodiment, the code generating module 304 may insert a timing sequence into the test template according to the product and timing specifications; and convert the inserted timing sequence by a high-speed test machine to generate the test code.

[0075] The high-speed test machine 306 may be configured to automatically test the chip to be tested using the test code. An automated test code may be generated by the programmable function of the high-speed test machine 306 and the language rule of the DDR4 memory, which

enables the test machine to automatically generate a big-data test code for memory. The generated test code may be used to simulate system environment test to expedite the unit test of the DDR4 memory.

[0076] FIG. 4 shows a block diagram of a chip testing device in accordance with another embodiment of this invention. As shown in Fig. 4, the chip testing device 40 may further include a test template library module 402 in addition to the chip testing device 30 of Fig. 3.

[0077] The test template library module 402 may be configured to generate the test template library based on a plurality of test templates.

[0078] In one embodiment, the test template library may be generated based on a plurality of test templates. The plurality of test templates may include: a X-direction/Y-direction fast write operation test template, a X-direction/Y-direction fast read operation test template, a X-direction/Y-direction fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a pre-charge power-down test template, and a mode register setting test template.

[0079] According to the chip testing device of the present disclosure, the test template may be selected from the test template library according to the language rule and the product and timing specifications; and the test code may be generated according to the product and timing specifications and the test template. Therefore, a big-data test code of complex memory can be generated automatically, thereby improving the efficiency of chip product verification analysis.

[0080] FIG. 5 shows a schematic diagram of a chip testing device in accordance with one embodiment of this invention. As shown in Fig. 5, the chip testing device 50 may include: an information module 502, a template library 504, a native random pattern creator 506, a database 508, a native random pattern module 510, a format conversion module 512, and a test module 514.

[0081] The information module 502 may be configured to acquire related information of a chip to be tested, and the information module 502 may be configured to determine a language rule of the chip to be tested. The information module 502 may also be configured to determine the product and timing specifications of the chip to be tested.

[0082] The template library 504 may be configured to store a plurality of test templates. The plurality of test templates may include, for example, a X-direction/Y-direction fast write

operation test template, a X-direction/Y-direction fast read operation test template, a X-direction/Y-direction fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a pre-charge power-down test template, and a mode register setting test template.

[0083] The native random pattern creator 506 may be configured to generate random patterns for a test based on a test template from the template library 504, the information in the information module 502 and content in the database 508. Based on different combinations of a test template from the template library 504 and information of the chip to be tested (e.g., the language rule, the product and timing specification of the chip to be tested) in the information module 502, and the content in the database 508, the native random pattern creator 506 may generate a large number of random patterns for testing the chip to be tested.

[0084] In some embodiments, the content in the database 508 may include data that may be used to generate the random patterns for testing. Additionally, after a test on a chip is completed, the content in the database 508 may be used to compare with results returned from the test to determine an outcome of the test.

[0085] The native random pattern module 510 may be configured to store the generated random patterns.

[0086] The format conversion module 512 may be configured to insert a timing sequence into the generated random patterns using product and timing specifications, and to convert the inserted timing sequence by a high-speed test machine to generate a test code.

[0087] The test module 514 may be configured to generate an automated test code using the programmable function of a high-speed test machine and the language rules of DDR4 memory, which may enable the test machine to automatically generate a big-data test code for memories. The generated test code may be used to simulate system environment test to expedite the unit test of the DDR4 memory.

[0088] In some embodiments, the test module 514 may be a high-speed test machine, such as an HSM6800 high-speed test machine.

[0089] FIG. 6 shows a block diagram of an electronic apparatus in accordance with one embodiment of this invention.

[0090] An electronic apparatus 200 according to an embodiment of the present disclosure is described below with reference to FIG. 6. The electronic apparatus 200 shown in FIG. 6 is merely an example and should not limit the scope of function and use of apparatus according to the embodiments of the present disclosure.

[0091] As shown in Figure 6, the electronic apparatus 200 may be implemented as a general purpose computing device. The components of the electronic apparatus 200 may include, but are not limited to, at least one processing unit 210, at least one memory cell 220, a bus 230 connecting different system components (including the storage unit 220 and the processing unit 210), a display unit 240, and the like.

[0092] The memory cell may store a program code, and the program code can be executed by the processing unit 210, such that the processing unit 210 performs the method in any of the aforementioned embodiments. For example, the processing unit 210 can perform the method as shown in FIG. 1.

[0093] The memory cell 220 may include a readable medium in the form of a volatile memory cell, such as a random access memory cell (RAM) 2201 and/or a cache memory cell 2202, and may further include a read only cache memory (ROM) 2203.

[0094] The memory cell 220 may also include a program/utility 2204 having a set (at least one) of the program modules 2205 including but not limited to: an operating system, one or more applications, other program modules, and program data, each of or some combinations of these examples may include an implementation of a network environment.

[0095] Bus 230 may represent one or more of several types of bus structures, which may include a memory cell bus or a memory cell controller, a peripheral bus, a graphics acceleration port, a processing unit, or a local bus using any of the bus structures.

[0096] The electronic apparatus 200 can also communicate with one or more external devices 300 (e.g., a keyboard, pointing device, Bluetooth device, etc.), and can also communicate with one or more devices that enable the user to interact with the electronic apparatus 200, and/or with any device (e.g., a router, modem, etc.) that enables the electronic apparatus 200 to communicate with one or more other computing devices. The communication can take place via an input/output (I/O) interface 250. Moreover, electronic apparatus 200 can also communicate with one or more networks (e.g., a local area network (LAN), a wide area

network (WAN), and/or a public network, such as the Internet) via a network adapter 260. The network adapter 260 can communicate with other modules of electronic apparatus 200 via the bus 230. It should be understood that although not shown in the figures, other hardware and/or software modules may be utilized in conjunction with electronic apparatus 200, including but not limited to: microcode, device drivers, redundant processing units, external disk drive arrays, RAID systems, tape drives, and data backup storage systems, etc.

[0097] Based on the description of the above embodiments, those skilled in the art will readily understand that the exemplary embodiments described herein may be implemented by software, software or the combination thereof. Therefore, the technical solution according to an embodiment of the present disclosure may be embodied in the form of a software product, which may be stored in a non-volatile storage medium (which may be a CD-ROM, a USB flash drive, a mobile hard disk, etc.) or on a network. A plurality of commands are included to cause a computing device (which may be a personal computer, server, or network device, etc.) to perform the above method in accordance with an embodiment of the present disclosure, which may include: determining a language rule of a chip to be tested; determining product and timing specifications of the chip to be tested; selecting a test template from a test template library according to the language rule and the product and timing specifications; generating a test code according to the product and timing specifications and the test template; and automatically testing the chip to be tested by using the test code.

[0098] It will be understood by those skilled in the art that the above various modules may be distributed in the device according to the description of the embodiments, or may be correspondingly changed in one or more devices different from the embodiment. The modules of the above embodiments may be combined into one module, or may be further divided into a plurality of sub-modules.

[0099] Based on the description of the above embodiments, those skilled in the art can easily understand that the exemplary embodiments described herein may be implemented by software, or may be implemented by software in combination with necessary hardware. Therefore, the technical solution according to an embodiment of the present disclosure may be embodied in the form of a software product, which may be stored in a non-volatile storage medium (which may be a CD-ROM, a USB flash drive, a mobile hard disk, etc.) or on a network. A plurality

of commands are included to cause a computing device (which may be a personal computer, server, mobile terminal, or network device, etc.) to perform a method in accordance with an embodiment of the present disclosure.

[0100] The exemplary embodiments of the present disclosure have been particularly shown and described above. It should be understood that the invention is not limited to the details of the details of the embodiments of the disclosure.

CLAIMS

1. A chip testing method, comprising:
 - determining a language rule of a chip to be tested;
 - determining product and timing specifications of the chip to be tested;
 - selecting, according to the language rule and the product and timing specifications, a test template from a test template library;
 - generating, according to the product and timing specifications and the test template, a test code; and
 - automatically testing, using the test code, the chip to be tested.
2. The chip testing method of claim 1, further comprising:
 - generating, based on a plurality of test templates, the test template library,
 - wherein the plurality of test templates comprise:
 - a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and a pre-charge power-down test template.
3. The chip testing method of claim 1, wherein the chip comprises a memory chip.
4. The chip testing method of claim 3, wherein the memory chip is a DDR4 chip.
5. The chip testing method of claim 3, wherein determining a language rule of the chip to be tested comprises:
 - determining, according to a specification document of the chip to be tested, a language rule for the chip to be tested.
6. The chip testing method of claim 3, wherein determining product and timing specifications of the chip to be tested comprises:

determining a memory cell address, a memory row address, a memory column address, and a memory page size of the chip to be tested; and

determining a model identification, a product identification, and parameters of the chip to be tested.

7. The chip testing method of claim 1, wherein selecting, according to the language rule and the product and timing specifications, a test template from a test template library comprises:

determining, according to the product and timing specifications, a database of the chip to be tested; and

selecting, according to the language rule and the database, the test template from the test template library.

8. The chip testing method of claim 1, wherein selecting, according to the language rule and the product and timing specifications, a test template from a test template library comprises:

determining, according to the product and timing specifications, a database of the chip to be tested; and

designating, according to the language rule and the database, the test template from the test template library.

9. The chip testing method of claim 1, wherein generating, according to the product and timing specifications and the test template, a test code comprises:

inserting, according to the product and timing specifications, a timing sequence into the test template to generate the test code.

10. The chip testing method of claim 9, wherein inserting, according to the product and timing specifications, a timing sequence into the test template to generate the test code comprises:

inserting, according to the product and timing specifications, the timing sequence into the test template; and

converting, by a high-speed test machine, the inserted timing sequence to generate the test code.

11. A chip testing device, comprising:

a parameter reading interface, configured to determine a language rule of a chip to be tested, and to determine product and timing specifications of the chip to be tested;

a code generating module, configured to select, according to the language rule and the product and timing specifications, a test template from a test template library, and to generate, according to the product and timing specifications and the test template, a test code; and

a high-speed test machine, configured to automatically test, using the test code, the chip to be tested.

12. The chip testing device of claim 11, further comprising:

a test template library module, configured to generate, based on a plurality of test templates, the test template library,

wherein the plurality of test templates comprise:

a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and pre-charge power-down test template.

13. The chip testing device of claim 11, wherein the code generating module comprises:

a selection module, configured to select, according to the language rule and a database, a test template from a test template library.

14. A chip testing device, comprising:

an information module, configured to acquire related information of a chip to be tested;

a native random pattern creator configured to generate, according to a target test template, information in the information module, and content of a database, random patterns for testing the chip to be tested;

a format conversion module, configured to insert, according to product and timing specifications, a timing sequence into the random patterns, and to convert, by a high-speed test machine, the inserted timing sequence to generate a test code; and

a test module, configured to generate an automated test code.

15. The chip testing device of claim 14, further comprising:

a template library, configured to store a plurality of test templates, wherein the target test template is one of the plurality of test templates; and

a template model module, configured to store the target test template.

16. An electronic apparatus, comprising:

one or more processors; and

a memory device, configured to store one or more programs;

wherein, upon being executed by the one or more processors, the one or more programs cause the one or more processors to perform operations, comprising:

determining a language rule of a chip to be tested;

determining product and timing specifications of the chip to be tested;

selecting, according to the language rule and the product and timing specifications, a test template from a test template library;

generating, according to the product and timing specifications and the test template, a test code; and

automatically testing, using the test code, the chip to be tested.

17. The electronic apparatus of claim 16, wherein the operations further comprise:

generating, based on a plurality of test templates, the test template library,

and wherein the plurality of test templates comprise:

a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and a pre-charge power-down test template.

18. A computer readable medium, storing a computer program executable by a processor,

wherein, upon being executed by the processor, the computer program causes the

processor to perform operations, comprising:

- determining a language rule of a chip to be tested;
- determining product and timing specifications of the chip to be tested;
- selecting, according to the language rule and the product and timing specifications, a test template from a test template library;
- generating, according to the product and timing specifications and the test template, a test code; and
- automatically testing, using the test code, the chip to be tested.

19. The computer readable medium of claim 18, wherein the operations further comprises:

- generating, based on a plurality of test templates, the test template library,
- wherein the plurality of test templates comprise:
 - a fast read operation test template, a fast write operation test template, a fast read/write operation test template, a self-refreshing test template, a refreshing test template, a ZQ calibration test template, a mode register setting test template, and a pre-charge power-down test template.

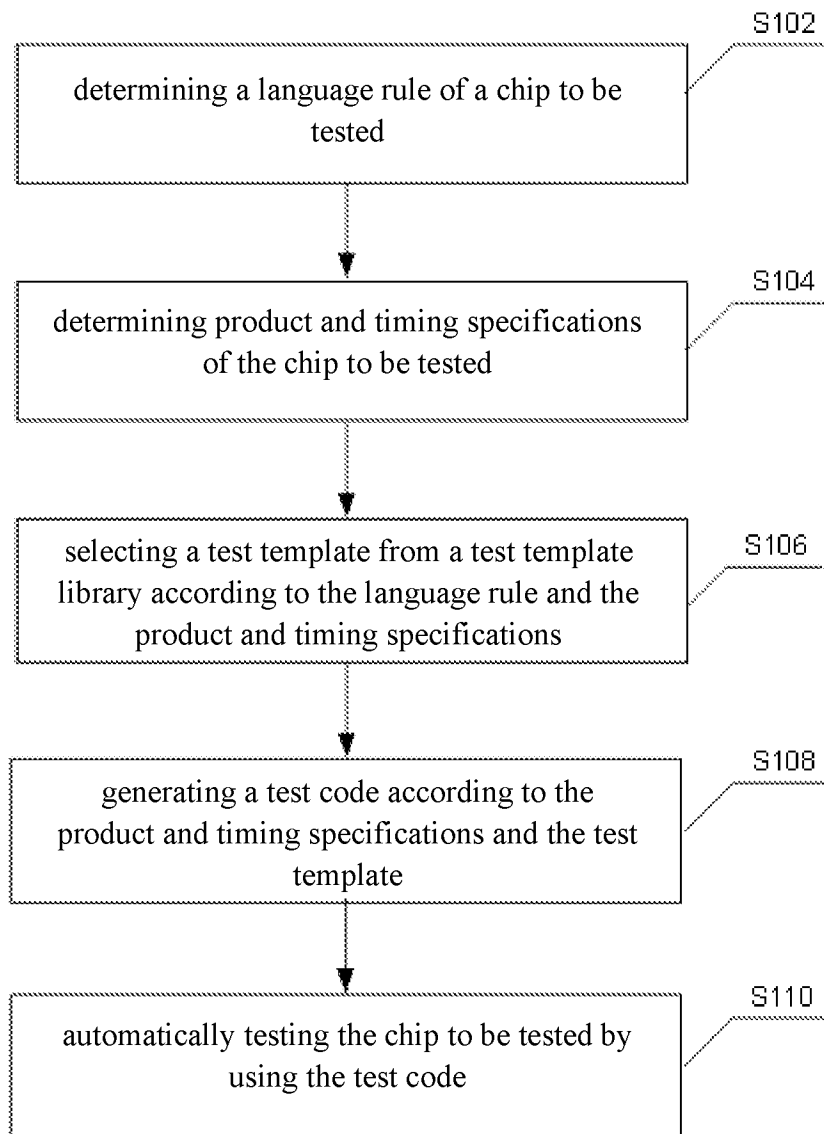
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FIG. 1

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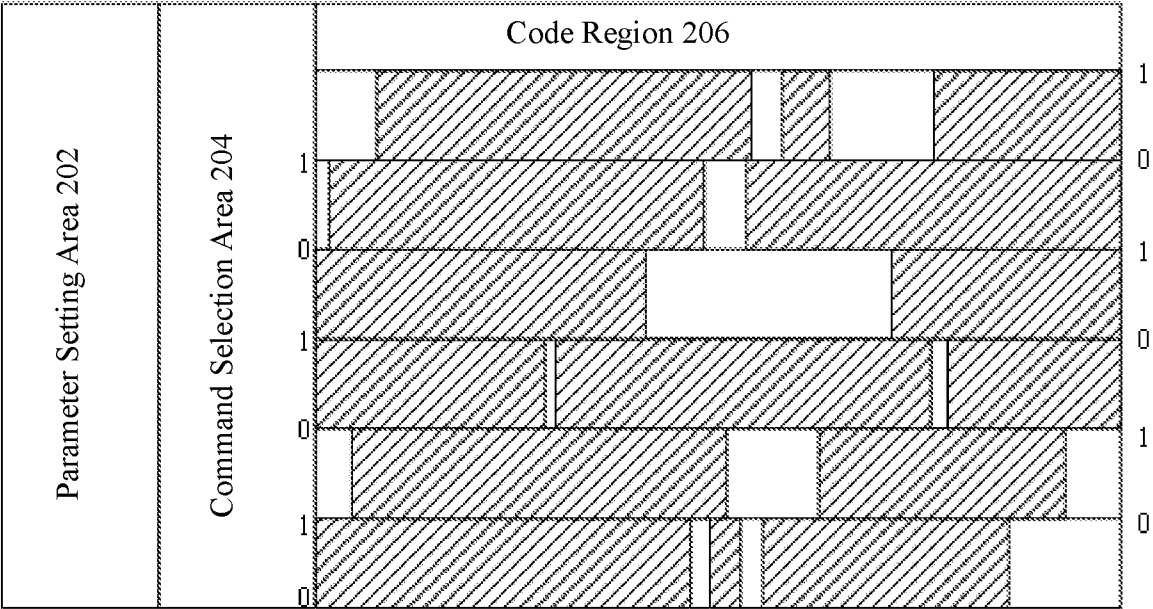


FIG. 2

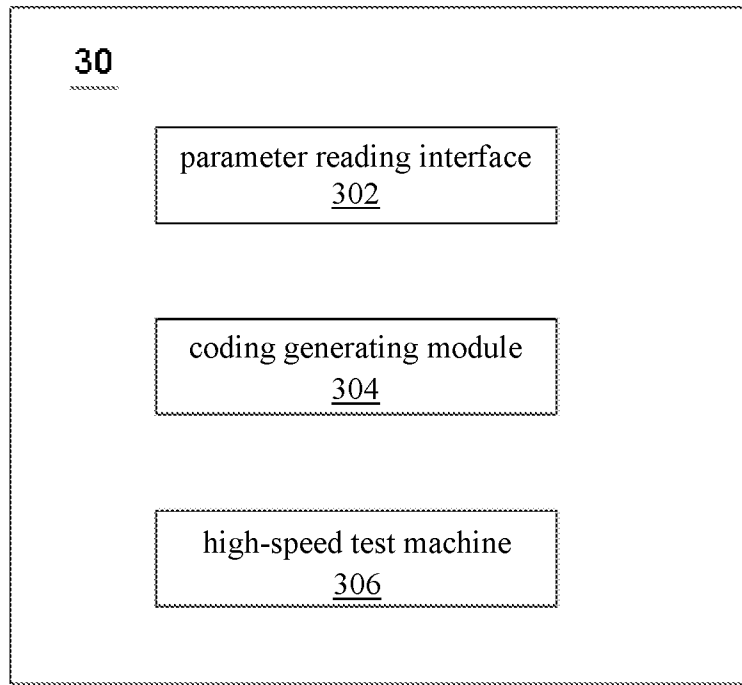


FIG. 3

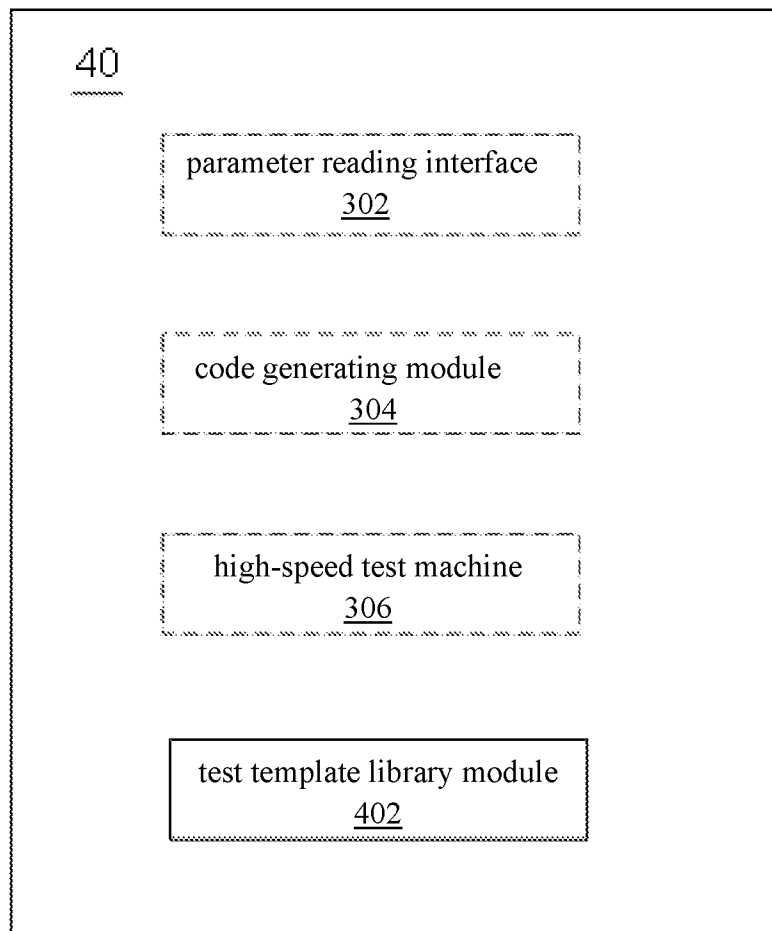


FIG. 4

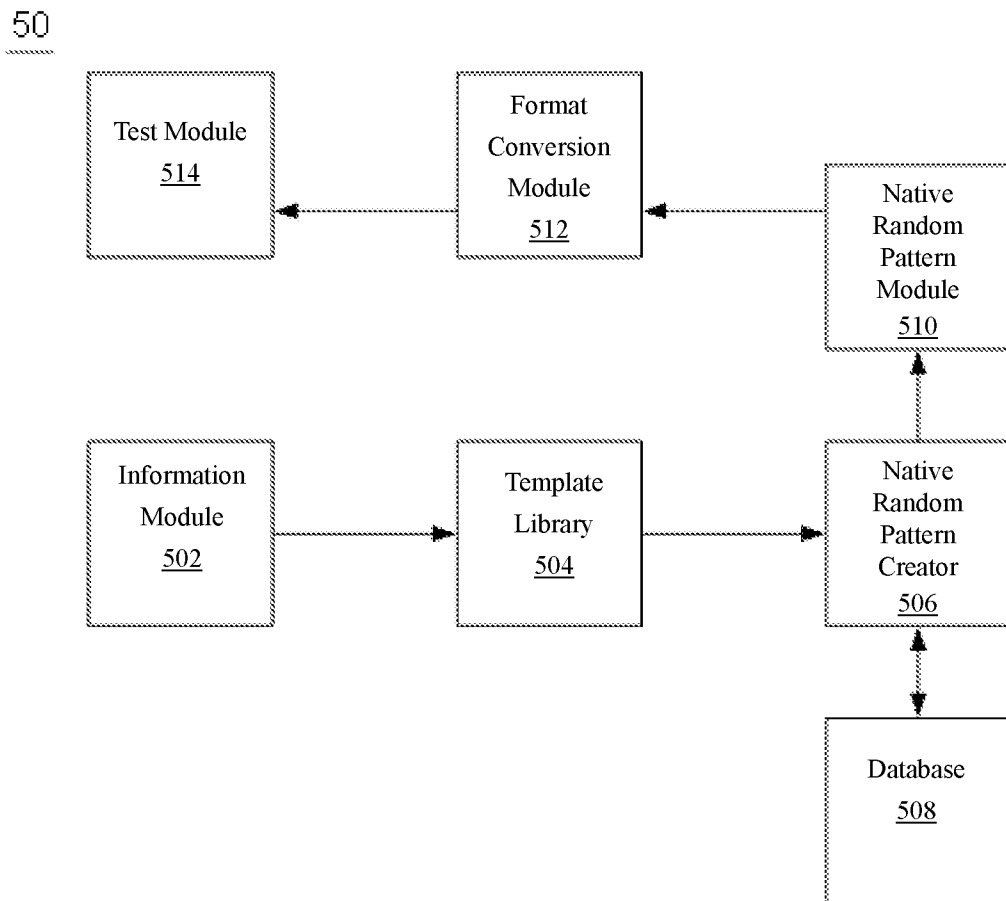


FIG. 5

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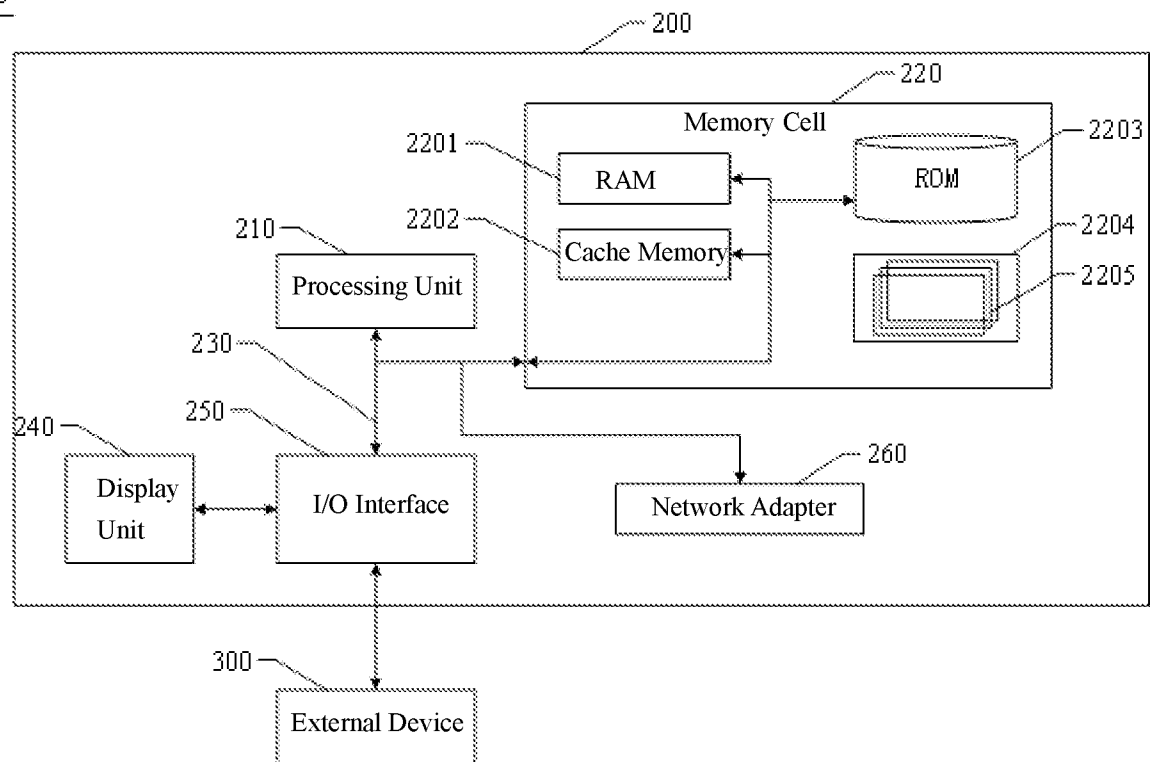


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/113246

A. CLASSIFICATION OF SUBJECT MATTER

G11C 29/56(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI;CNABS;CNKI;SIPOABS:template, chip, test, language, timing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 101118788 A (ZTE COMMUNICATION CO., LTD et al.) 06 February 2008 (2008-02-06) the whole document	1-19
A	CN 104298590 A (ADVANTEST CORP et al.) 21 January 2015 (2015-01-21) the whole document	1-19
A	CN 105158673 A (HISENSE ELECTRIC CO., LTD et al.) 16 December 2015 (2015-12-16) the whole document	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

09 January 2020

Date of mailing of the international search report

05 February 2020

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/113246

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				US	2015194223	A1	09 July 2015
				CN	104298590	B	10 May 2019
CN	105158673	A	16 December 2015	CN	105158673	B	06 April 2018