(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
09 September 2022 (09.09.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/187647 A1

(51) International Patent Classification:
H02M 3/16 (2006.01) *H02M 7/483* (2007.01)
H02M 3/02 (2006.01)

(21) International Application Number:
PCT/US2022/018940

(22) International Filing Date:
04 March 2022 (04.03.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/157,075 05 March 2021 (05.03.2021) US

(71) Applicant: **THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK** [US/US]; 412 Low Library, 535 West 116th Street, New York, NY 10027 (US).

(72) Inventors: **PREINDL, Matthias**; 500 West 120th Street, New York, NY 10027 (US). **JAHNES, Matthew**; 7 Sunrise Lane, Upper Saddle River, NJ 07458 (US).

(74) Agent: **RABINOVITCH, Ido**; Occhiuti & Rohlicek LLP, 50 Congress Street, Suite 1000, Boston, MA 02109 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: SYSTEMS AND METHODS FOR STACKED MULTI-LEVEL POWER CONVERTER IMPLEMENTATIONS WITH LINEAR SCALING

(57) Abstract: Disclosed are methods, systems, devices, and other implementations, including a voltage converter system that includes a plurality of energy storage elements, a plurality of switching devices, each of which is in electrical communication with at least one of the plurality of the storage elements, with the plurality of storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells. The system further includes a plurality of controllers to actuate one or more of the plurality of switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells. In some embodiments, the cells may include an arrangement of two capacitors and an inductor that define a buck-boost converter circuit. Alternatively, the cells may have a Dual Active Half Bridge (DAHB) converter configuration with a primary side separated from a secondary side by a transformer.

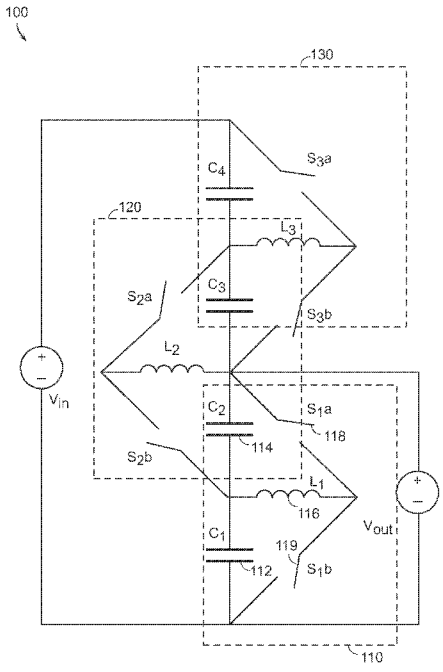

FIG. 1

WO 2022/187647 A1

SYSTEMS AND METHODS FOR STACKED MULTI-LEVEL POWER CONVERTER IMPLEMENTATIONS WITH LINEAR SCALING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of, and priority to, U.S. Provisional Application No. 63/157,075, entitled "A Fully Balanced Vertically Stacked Multilevel Power Converter Topology with Linear Scaling," and filed March 5, 2021, the content of which is incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0002] This invention was made with government support under Grant No. 1653574 awarded by the National Science Foundation (NSF). The government has certain rights in the invention.

BACKGROUND

[0003] Multi-level power converters serve to bridge the gap between high-voltage systems and lower voltage components. The potential applications of multilevel power conversion are wide, ranging from high-voltage DC transmission (HVDC), to medical devices, and to automotive technology. HVDC transmission systems achieve notable efficiency when controlled through multilevel topologies over traditional 2-level topologies. Electric vehicles, an inevitable future, also stand to benefit from the use of multilevel topologies.

[0004] Multilevel power converters have favorable advantages when compared to single-level power converters. For example, they can operate with higher voltages than individual converters and can also output higher quality waveform signals. Further, by distributing the full voltage across multiple discrete levels, a higher quality output waveform is achieved when switching between multiple discrete levels as opposed to a topology that has only one switched level.

[0005] Multi-level converters, however, often have complicated circuit topologies and can have unstable voltage balancing (which refers to the ability of the circuit to maintain a constant desired voltage between levels or across capacitors) across their circuit components. Full-bridge modular multilevel converters (MMC) have improved implementation over half-bridge MMC with respect to flexibility in capacitor voltages and balancing, but come at the cost of increased switching devices and control complexity. Likewise, the diode-clamped, capacitor clamped, and general D-shaped topologies also require extra attention to keep capacitor voltages balanced, more so as the number of levels increases.

[0006] Addressing these two common issues can greatly advance the integration of multilevel power converters into high power technologies, such as electric vehicle charging and electric grids.

SUMMARY

[0007] The present disclosure is directed to a simple and a highly efficient multi-level configurations of stackable voltage conversion. The stackable cells of the approaches described herein can be easily connected together with linear scaling and can also be individually controlled, lending the proposed topologies to a modular and readily expandable approach. The voltage conversion configurations of the present approaches provide a bidirectional and AC/DC or DC/DC capabilities that can be used for a variety of applications, ranging from electric vehicles to HVDC transmission. The ability to simultaneously sink or source current at any node along the center stack of energy storage elements (capacitors) can be beneficial for local power distribution systems. Also described herein are physical circuits implementations for the proposed topologies, procedures and techniques to control operation of the circuitry (e.g., through control of the duty cycles), and evaluation of the performance of the proposed topologies.

[0008] The proposed implementations and topologies have marked benefits over existing multilevel power converter topologies, with their simplicity at the forefront. Stackable cells can be easily connected together with linear scaling and can also be individually controlled, lending the proposed topologies to a modular and readily expandable approach.

[0009] The proposed topologies mitigate the various deficiencies of traditional multi-level converters through independently operable and stackable unit switching cells that can bidirectionally convert AC/DC or DC/DC while sustaining capacitor voltage balance. Neither the complexity of control nor circuit design of this topology increases with the number of levels. Component quantities scale linearly with number of levels.

[0010] The proposed topologies described herein also include an arrangement of discrete, identical, and individually controlled switching cells that are dual active half bridges with three degrees of freedom (3D-DAHB). In the DAHB voltage converter configuration, the individual cells can move power between any of the connected capacitors. The proposed DAHB topology operates by balancing the voltage of all connected capacitors.

[0011] Advantages of the topologies described herein is the reduced overhead (e.g., in terms of number of components) required to implement the proposed topologies relative to conventional topologies. Component quantities as a function of *n* levels (number of voltage levels) for a variety of multilevel converters and for the two example proposed Manhattan topologies described herein are provided in Table 1 below. Diode-clamped, capacitor-clamped, and the generalized D-shaped converters have exponentially increasing component counts as a function of number of levels. Modular Multilevel converters (MMC) have unbalanced voltages in steady state, making DC/DC implementations of these topologies challenging. The full-bridge MMC improves over the half-bridge MMC with respect to flexibility in capacitor voltages and balancing but comes at the cost of increased switching devices and control complexity. Likewise, the diode clamped, capacitor clamped, and generalized D-shaped topologies also require extra attention to keep capacitor voltages balanced, more so as the number of levels increases.

[0012] On the other hand, the two example topologies described herein (half-bridge Manhattan topology and the dual active half bridge Manhattan topology) require approximately half the number of switches and inductive components as conventional voltage converters. In addition, the DAHB Manhattan converter mitigates the problem of loop currents. The proposed implementations therefore offer a fully balanced power electronic topology that scales linearly to *n* levels with constant component size.

Topology	Semiconductors	Inductors/Transformers	Capacitors
Diode-Clamped	$n^2 - n$	1	$n - 1$
Capacitor-Clamped	$2(n - 1)$	1	$(n-1)+\frac{n^2-3n+2}{2}$
Generalized D-shaped	$n(n - 1)$	1	$\frac{n^2+n}{2}-n$
Half-Bridge MMC	$4(n - 1)$	2 or $4(n - 1)$	$2(n - 1)$
Full-Bridge MMC	$8(n - 1)$	2 or $4(n - 1)$	$2(n - 1)$
Half-Bridge Manhattan	$2(n - 1)$	$n - 1$	n
Dual-Active Half-Bridge Manhattan	n	$n/2$	n

Table 1: Number of Components in *n*-Level Converter Topologies

[0013] Thus, in some variations, a voltage converter system is provided that includes a plurality of energy storage elements, and a plurality of switching devices, each in electrical communication with at least one of the plurality of the energy storage elements, with the plurality of energy storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells. The system further includes a plurality of controllers to controllably actuate one or more of the plurality of switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

[0014] Embodiments of the system may include at least some of the features described in the present disclosure, including one or more of the following features.

[0015] Each of the multiple voltage converting cells may include an arrangement of two capacitors and an inductor that define a buck-boost converter circuit.

[0016] The multiple voltage converting cells may be arranged as one or more stacked cascades of converting cells, with each voltage converting cell in the one or more stacked cascades of conversion cells sharing at least one capacitor element with a neighboring voltage converting cell.

[0017] The plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells may be configured to achieve a voltage balance for the multiple voltage converting cells.

[0018] The plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of the each of the multiple voltage converting cells may be configured to determine and maintain at least one capacitor of the multiple voltage converting cells at a respective voltage level.

[0019] The plurality of controllers configured to controllably actuate the one or more of the plurality of switching devices may be configured to controllably actuate the one or more of the plurality of switching devices based at least in part on measured electrical properties of at least one of the multiple voltage converting cells.

[0020] The plurality of controllers may be configured to actuate the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements.

[0021] The plurality of controllers configured to controllably actuate the one or more of the plurality of switching devices may include at least one controller configured to determine an adjustable duty cycle behavior for at least one of the multiple voltage converting cells.

[0022] The at least one controller configured to determine the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may be configured to continually compute the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values.

[0023] The plurality of controllers configured to determine the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may be configured to derive duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions.

[0024] The one or more objective functions may include one or more of, for example, a) 1-norm objective function of all inductor currents in the voltage converter system to minimize overall current rating of the voltage converter system, b) a 2-norm squared objective function of all the inductor currents of the voltage converter system to minimize overall power loss in the voltage converter system, and/or c) an inf-norm objective function of all the inductor currents of the voltage converter system to minimize maximum currents levels in all the inductor currents.

[0025] At least one of the multiple voltage converting cells may include a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer, with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices.

[0026] The at least one DAHB converter configuration cell may include two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices.

[0027] The plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells may include at least one dedicated controller for the at least one DAHB converter configuration cell, the at least one dedicated controller configured to controllably actuate the two primary side switching devices and the two secondary side switching devices according to one or more pre-determined switching sequences defined for a particular time interval.

[0028] The one or more switching sequences for the at least one DAHB converter configuration cell may be defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events.

[0029] The multiple voltage converting cells each may include a respective cell with the DAHB converter configuration cell, with the multiple voltage converting cells being arranged as one or more stacked cascades of the cells with the DAHB converter configuration cell connected to a load.

[0030] The multi-level arrangement of the multiple voltage converting cells may include a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, with the plurality of controllers including a central controller in electrical communication with the multiple stacks of voltage converting cells to control electrical currents produced by the multiple stacks to power the load.

[0031] The load may include a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors, and the central controller may be configured to control duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque.

[0032] The plurality of controllers may include an individual cell controller for each of the multiple voltage converting cells, with the each of the multiple voltage converting cells including two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, and with the each individual cell controller for the each of the multiple voltage converting cells being configured to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level.

[0033] In some variations, a voltage conversion method is provided that includes obtaining electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being electrically coupled to at least one of the plurality of the energy storage elements. The plurality of energy storage elements and the plurality of switching devices are configured in a multi-level arrangement of multiple voltage converting cells. The method further includes controllably actuating by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

[0034] Embodiments of the method may include at least some of the features described in the present disclosure, including at least some of the features described above in relation to the voltage converter system, as well as one or more of the following features.

[0035] Controllably actuating the one or more of the plurality of switching devices may include independently controlling the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells to achieve a voltage balance for the multiple voltage converting cells.

[0036] Controllably actuating the one or more of the plurality of switching devices may include controllably actuating the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements.

[0037] controllably actuating the one or more of the plurality of switching devices may include determining an adjustable duty cycle behavior for at least one of the multiple voltage converting cells.

[0038] Determining the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may include continually computing the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values.

[0039] Determining the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may include deriving duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions.

[0040] At least one of the multiple voltage converting cells may include a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer, with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices. The at least one DAHB converter configuration cell may include two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices, and controllably actuating the one or more of the plurality of switching devices may include controllably actuating the two primary side switching devices and the two secondary side switching devices according to one or

more pre-determined switching sequences defined for a particular time interval. The one or more switching sequences for the at least one DAHB converter configuration cell may be defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events.

[0041] The multi-level arrangement of the multiple voltage converting cells may include a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, and controllably actuating the one or more of the plurality of the switching devices may include controlling, by a central controller from the plurality of controllers, electrical currents produced by the multiple stacks to power the load.

[0042] The load may include a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors, and controlling, by the central controller, the electrical currents produced by the multiple stacks may include controlling duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque.

[0043] Controllably actuating the one or more of the plurality of switching devices further may include controlling individually, by a dedicated cell controller for at least one of the multiple voltage converting cells, the at least one of the multiple voltage converting cells that includes two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level.

[0044] The multi-level arrangement of the multiple voltage converting cells may include a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, with each of the multiple voltage converting cell including a dedicated cell controller. Controllably actuating the one or more of the plurality of the switching devices may include controllably actuating, by the respective dedicated cell controller for the each of the multiple voltage converting cells, the one or more of the plurality of the switching devices to independently control voltage levels of the at least one energy storage element of the multiple voltage converting cells.

[0045] In some variations, a non-transitory computer readable media is provided that stores a set of instructions, executable on at least one programmable device, to obtain electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being in electrical communication with at least one of the plurality of the energy storage elements. The plurality of energy storage elements and the plurality of switching devices are configured in a multi-level arrangement of multiple voltage converting cells. The set of instructions is further configured to cause the programmable device to controllably actuate by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

[0046] Embodiments of the computer readable media may include at least some of the features described in the present disclosure, including at least some of the features described above in relation to the system and method.

[0047] Other features and advantages of the invention are apparent from the following description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0048] These and other aspects will now be described in detail with reference to the following drawings.

[0049] FIG. 1 is a circuit diagram of a three (3) cell stackable voltage conversion configuration (referred to as a Manhattan configuration).

[0050] FIG. 2 is a circuit diagram of a unit cell that can be used in multi-level voltage converter systems.

[0051] FIG. 3 is a circuit diagram of an example stacked voltage conversion system with five levels.

[0052] FIG. 4 is a circuit diagram of a generalized multi-level Manhattan topology with K cells, and N voltage levels.

[0053] FIG. 5 includes a portion of a stacked topology in which current paths are illustrated.

[0054] FIG. 6 is a circuit diagram with illustrated current paths for a seven-level converter with five voltage conversion cells.

[0055] FIG. 7 includes graphs showing capacitor voltages and inductor currents as functions of time for the 7-level converter of FIG. 6.

[0056] FIG. 8 includes a circuit diagram for a nine-level (seven cells), along with graphs showing the electrical behavior of the voltage conversion cells (e.g., capacitor voltages and inductor currents).

[0057] FIG. 9 is a circuit diagram for a seven-level converter with graphs showing the electrical behavior of the various components when the duty cycle of the center unit cell was swept from 0 to 1.

[0058] FIG. 10 is a schematic diagram of an example system for a stackable control structure to control operation of a three-phase motor.

[0059] FIG. 11 is a schematic diagram of a unit cell that includes a local controller.

[0060] FIG. 12 is a schematic diagram of a controlled motor system with a 3-phase inverter.

[0061] FIG. 13 includes graphs showing the motor torque and speed resulting from running a test profile on the motor configuration schematically depicted in FIG. 12.

[0062] FIG. 14 includes graphs showing the three voltage levels in multi-level converter stacks used for driving a 3-phase motor.

[0063] FIG. 15A is a schematic diagram of a Dual Active Half Bridge Converter (DAHB) unit / cell.

[0064] FIG. 15B includes a schematic diagram of another representation of a DAHB unit.

[0065] FIG. 16 is a table specifying possible switching configurations that lead to different behaviors of a DAHB unit.

[0066] FIG. 17 includes a graph showing the leakage inductor current during one period of the switching sequence corresponding to the 3rd row and 2nd column of the table of FIG. 16.

[0067] FIG. 18 includes a diagram showing the switching sequence regions forming a convex, nonoverlapping union spanning ±1/2 on each of the axes, and a diagram showing the sequence region corresponding to the position (3,2) of the table of FIG. 16.

[0068] FIG. 19 includes circuit diagrams for the DAHB Manhattan converter topologies for n (number of levels) =2, 4, 8, and 2^N.

[0069] FIG. 20 includes circuit diagrams of example stackable DAHB units / cells.

[0070] FIGS. 21A-B includes graphs for current waveforms for an $N = 4$ DAHB Manhattan topology in inverter operation driving a 3-phase motor, and graphs for the resultant toque, speed, and angle behavior for the 3-phase motor.

[0071] FIG. 22 is a flowchart of an example voltage conversion procedure based on the topologies and implementations described herein.

[0072] Like reference symbols in the various drawings indicate like elements.

DESCRIPTION

[0073] Disclosed are circuits, systems, methods, and other implementations (including hardware, software, and hybrid hardware/software implementations) directed to multi-level power converter topologies (referred to as "Manhattan" topologies, and implemented using different types of basic, stackable, circuit units, as will be described in greater detail below). The topologies described herein are fully balanced, can function bidirectionally for both DC/AC and DC/DC modes of operation, and can be expanded to an arbitrary N number of levels. Power converters of the Manhattan topologies are comprised of discrete switching cells across which the input voltage can be arbitrarily distributed. Each of these switching cells can be individually controlled and can operate as a standalone unit. The nature of this topology yields inherent capacitor voltage balancing. Each of the cells (which may have similar configurations) can operate individually as two-level power converters, maintaining internal voltage balancing without the need for additional components. Moreover, the voltage balancing within the

individual units is preserved when two or more individual cells are connected to form the multilevel power converter. Due to the simplified design, the component cells, when stacked, scale linearly with the number of circuit components, suggesting that there is no limit to the number of levels possible for the present multilevel power converter technology. As such, this technology has the potential to scale-up for large and simplified power-related industrial uses. Thus, in some embodiments, a proposed voltage converter system includes a plurality of energy storage elements (e.g., capacitors and/or inductors), a plurality of switching devices (e.g., different types of transistors, like MOSFET, FET, BJT) each in electrical communication with (i.e., electrically coupled to) at least one of the plurality of the energy storage elements, with the plurality of energy storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells. The converter system further includes a plurality of controllers to controllably actuate one or more of the plurality of switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells. For example, each converting cell may have its own dedicated individual controller to control the voltage output of the cell. Alternatively, some of the multiple cells may have their own dedicated individual controller (be it a closed-loop controller, a programmable controller, or otherwise), with other voltage converter cells being controlled by a joint controller(s) controlling the behavior of those voltage converter cells. In some embodiments, a central controller may be used to facilitate control of the multi-level voltage converter system in conjunction with at least one dedicated local controller (e.g., a controller to regulate the electrical behavior of one or more of the nodes / cells of the system).

[0074] An example of a generalized topology of the implementations described herein (the "Manhattan Converter" topology) is shown in the circuit diagram of FIG. 1. Specifically, FIG. 1 is a circuit diagram of a three (3) cell stackable voltage conversion configuration 100. In this example, the three-cell configuration defines a five-level voltage conversion system. The configuration 100 includes a first voltage conversion cell 110, a second voltage conversion cell 120, and a third voltage conversion cell 130. As can be seen, in the example configuration of FIG. 1, each voltage conversion cell comprises two capacitors (e.g., in the cell 110 those are capacitors 112 and 114, also marked as capacitors C_1 and C_2), an inductor element (inductor 116 in the cell 110, also marked as L_1) and two switching devices (e.g., 118 and 119 for cell 110, marked as switches s_1a and s_1b) that can be individually and independently

controlled by a plurality of controllers (e.g., a central processor-based controller controlling the behavior of some or all of the cells, in conjunction with at least one dedicated controller regulating the behavior of an individual or a group of the multiple cells; in FIG. 1 the controller is not specifically depicted) to thus control the duty cycle and periodicity of each of the stackable cells. As illustrated in FIG. 1, each cell shares at least one capacitor with an adjacent (neighboring cell). For example, the voltage conversion cell 110 and the voltage conversion cell 120 share the capacitor 114. In some embodiments, the various cells comprising a multi-cell voltage conversion topology can have different energy storage configurations, including some in which two or more cells share one or more components (storage elements, and/or switching devices). The plurality of controllers (coupled to the various voltage conversion cells in some cooperative configuration) can determine appropriate the behavior of the switching devices resulting for a voltage conversion system particular circuit configuration / topology.

[0075] Although the circuit topology in FIG. 1 is capable of bidirectionally converting DC/DC or DC/AC, for the sake of brevity the present discussion considers the converter in step-down buck-mode operation and the terms are labeled as such. Likewise, any node along the center capacitor stack can be utilized as the output, but the present discussion focuses on implementations where the output is at the center node and the derived equations (discussed below) to represent the voltages and/or currents at different cells or components reflect that. The center node is defined as having the same number of series capacitors above it as below it. It is important to note that, depending on the application, utilizing a non-centered node as the output may be used, and may be advantageous over using the center node.

[0076] The topologies described herein are expandable to an arbitrary N number of levels with component quantities scaling linearly, where N and K represent the number of levels and number of stackable unit cells, respectively, and where, generally, $N = K + 2$ In some embodiments, output is taken at the center node which is defined as having the same number of series capacitors above it as below it. . This is achieved through individually stackable and controllable unit cells (more particularly discussed below). The stacked cell nature of this topology eliminates the need for a bulk capacitance between the input and reference or between the output and reference. The series combination of the cell capacitances serves to support both the input and output nodes as well as the voltages within each cell. The individual capacitor voltages can be controlled as a function of the duty cycles of each unit cell, allowing for the

voltage across the entire stack to be balanced across the cells arbitrarily. This allows for the control and conversion of voltages higher than the voltage rating of any individual semiconductor or passive component. Since the output voltage is the sum of the capacitor voltages between the output node and reference, the ability to balance the capacitor voltages to any arbitrary ratio also allows for the output voltage to swing between full input voltage and reference.

[0077] The stackable unit cell that composes the multilevel topology (such as the topology depicted in FIG. 1, and the further example topologies of FIGS. 3-4) is illustrated in FIG. 2, showing a circuit diagram of a unit cell 200. Dashed lines denote connections to adjacent cells. Current flows through each unit cell in the same way it does in a typical inverting buck-boost converter. An equivalent circuit arrangement 250 is provided next to the circuit of the unit cell 200. The equivalent circuit 250 of FIG. 2 shows an inverting buck-boost converter with the nodes and components labeled as they align with the repeatable unit cell 200. In this manner, each unit cell can be considered an individual inverting buck-boost converter, and the stacking of unit cells a quasi-cascade.

[0078] The unit cell 200 (and similarly the equivalent circuit 250) includes capacitors 210 and 212, an inductor element 230, and two controllable switching devices (e.g., transistors) 220 and 222 that can be individually electrically actuated by control signaling provided through a controller (not shown in the figures) according to control procedure(s) discussed in greater detail below. By configuring each cell as an individual (possibly independent) inverter buck-boost converter, the individual cells can be stacked (to form a quasi-cascade of converters), resulting in a topology that can eliminate the need for bulk capacitance between the input and reference and/or output to reference as the series combination of the cell capacitance serves to support both the input and output nodes, as well as the voltages within each cell.

[0079] The individual capacitor voltages can be controlled as a function of the duty cycles of at least one of the unit cells, allowing for the voltage across an entire voltage conversion stack to be balanced across each cell to any arbitrary ratio. This allows the control and conversion of voltages higher than the voltage rating of any individual semiconductor or passive component. Because the output voltage is simply the sum of the capacitor voltages

between the output node and reference, the ability to balance the capacitor voltages to any arbitrary ratio also allows for the output voltage to swing between full input voltage and reference. The individual cells may, in some embodiments, be individually controlled to thus facilitate the modular nature of the multi-level voltage conversion implementation. Individual control can be supplemented through joint control (achieved through one or more controllers assigned to regulate a group of cells). Such joint control may also include central control (by a central controller) to provide global control signaling for some or all of the voltage conversion cells.

[0080] FIG. 3 is another example of a stacked voltage conversion system 300, which includes five levels (i.e., the system 300 includes five individual cells, each of which may be of a similar configuration as the unit cell 200 depicted in FIG. 2). FIG. 4 includes a generalized topology 400 with K cells, and N voltage levels (as noted, generally, $N = K + 2$).

[0081] The quasi-cascade nature of the proposed topology described herein induces circulating currents between adjacent cells. General current paths can be seen in FIG. 5, depicting a portion of a stacked topology 500 comprising three cells (constituted by 4 capacitors C_{i-1}, C_i, C_{i+1}, C_{i+2}). Following the path of the currents above and below an inductor 530 (marked L_i) forming a converter cell with capacitors 510 and 512 (marked C_i and C_{i+1}), and switches 520 and 522 (S_ia and S_ib), it can be seen that the center-most inductor 530 (L_i) must support the inductor currents of the cells above and below it. The exact ratio of currents between the inductors is a function of the duty cycles of each cell and the number of stacked cells, as will become apparent below.

[0082] Before discussing the current / voltage control procedures to control the voltages at different cell comprising a stackable voltage conversion system, the equations and relationships governing the voltages at different points of the stack topology will be described. The behavior of a stacked converter will be discussed in relation to a five (5) cell, 7 level converter, such as voltage conversion system 600 depicted in the circuit diagram of FIG. 6, but similar derivation of the governing relationship can be applied to topologies of any number of cells (and corresponding number of voltage levels). Using the notation shown in FIG. 6, the equations for average switching current, inductor current, and capacitor voltages are as follows:

$$V_{C_i} = V_{C_i+1}\left(\frac{D_i}{1-D_i}\right), \quad (1a)$$

$$I_{L_i} = I_{s_i a} + I_{s_i b}, \quad (1b)$$

$$I_{L_i} = I_{s_{i-1} a} + I_{s_{i+1} b}, \quad (1c)$$

$$I_{s_i a} = I_{L_i}(1-D_i), \quad (1d)$$

$$I_{s_i b} = I_{L_i} D_i, \quad (1e)$$

where Equations (1a) - (1e) align with the equations for a typical inverting buck boost converter and hold true for each individual unit cell within the multilevel converter. In the above equations, the notation D_i represents the duty cycle for the ith cell.

[0083] The output voltage, taken at the node labeled V_3 (fourth level), is the sum of all capacitors voltages between it and reference. Iteratively substituting in Equation (1a) for each cell below the output and algebraically rearranging in terms of V_{C6} produces the following sequence of equations:

$$V_{out} = V_{C1} + V_{C2} + V_{C3} \quad (2)$$

$$V_{C1} + V_{C2} + V_{C3} = \left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right) \quad (3)$$

$$V_{out} = V_{C6}\left(\begin{array}{l}\left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) + \\ \left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) + \left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)\end{array}\right) \quad (4)$$

[0084] Repeating this iterative process while moving from the bottom cell to the top cell produces results in:

$$V_{in} = V_{C6}\left(\begin{array}{l}\left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)+ \\ \left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)+ \\ \left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)+ \\ \left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)+\left(\frac{D_5}{1-D_5}\right)+1\end{array}\right) \quad (5)$$

[0085] Equations (4) and (5) thus provide expressions for V_{in} and V_{out} as a function of V_{C6}. Combining these two equations, simplifying, and using series sum and series product notation yields the following expression that gives V_{out}/Vin as a function of each cell's duty cycle:

$$\frac{V_{out}}{V_{in}} = \frac{\sum_{j=1}^{3}\left[\prod_{i=j}^{5}\left(\frac{D_j}{1-D_j}\right)\right]}{\sum_{j=1}^{5}\left[\prod_{i=j}^{5}\left(\frac{D_j}{1-D_j}\right)\right]+1} \quad (6)$$

[0086] A similar process can be used to find the voltage at any node along the center capacitor stack for a converter of N levels. Level $n = 0$ is considered as reference voltage and level $n = N$ as the input voltage. For clarity, these nodes are labeled V_0 and V_6 in FIG. 6, respectively. Level n is the voltage being calculated. This adapted derivation is as follows:

$$\frac{V_n}{V_{in}} = \begin{cases} \dfrac{\sum_{j=1}^{n-1}\left[\prod_{i=j}^{N-2}\left(\dfrac{D_j}{1-D_j}\right)\right]}{\sum_{j=1}^{N-2}\left[\prod_{i=j}^{N-2}\left(\dfrac{D_j}{1-D_j}\right)\right]+1} & 0<n<N \\ 1 & n=N \\ 0 & n=0 \end{cases} \quad (7)$$

[0087] It is important to note that Equation (7) provides the voltage of the node in question relative to reference, and not the individual capacitor voltages. Individual capacitor voltages can be found by calculating the voltages of the capacitor's two adjacent nodes and taking the difference.

[0088] Deriving the equations for currents begins at the middle node. The middle node is labeled V_3 in the example seven-level converter in FIG. 6. Equation (1c), above, serves to link two adjacent cells and is modified for taking the output at the middle node:

$$I_{L_3} = I_{s_4 b} + I_{s_2 a} + I_{out}, \quad (8)$$

where I_{L3} is the average current through the middle cell inductor. Iteratively substituting in Equations (1c), (1d), and (1e), alongside algebraic manipulation, produces:

$$I_{s_4 b} = I_{L_3}\frac{D_3(1-D_4)}{1-D_4(1-D_5)} \quad (9)$$

$$I_{s_2 a} = I_{L_3}\frac{D_2(1-D_3)}{1-D_1(1-D_2)} \quad (10)$$

which provides I_{s4b} and I_{s2a} as functions of exclusively D and I_{L3} . Substituting (9) and (10) into (8) and algebraically rearranging terms, results in:

$$I_{L_3} = I_{out}\left(1-\frac{D_3(1-D_4)}{1-D_4(1-D_5)}-\frac{D_2(1-D_3)}{1-D_1(1-D_2)}\right) \tag{11}$$

which provides the average current through the middle inductor as a function of output current I_{out} and duty cycles D. This same process can be taken to find the average current through the middle inductor for any odd-numbered level converter as a function of output current. This adaptation is as follows:

$$\frac{I_{out}}{I_j} = 1-\cfrac{D_m(1-D_{m+1})}{1-\cfrac{D_{m+1}(1-D_{m+2})}{1-\cfrac{D_{m+2}(1-D_{m+3})}{\cdots}}}-\cfrac{D_{m-1}(1-D_m)}{1-\cfrac{D_{m-2}(1-D_{m-1})}{1-\cfrac{D_{m-3}(1-D_{m-2})}{\cdots}}} \tag{12}$$

where m is used to denote the middle inductor (for the 7-level converter of FIG. 6, $m = 3$).

[0089] Lastly, the relationship between a known inductor current I_{Lj} and any two adjacent inductor currents $I_{Lj\text{-}1}$ and I_{Lj+1} can be calculated using the following equations:

$$\frac{I_{j+1}}{I_j} = 1-\cfrac{D_j}{1-\cfrac{D_{j+1}(1-D_{j+2})}{1-\cfrac{D_{j+2}(1-D_{j+3})}{\cdots}}} \tag{13}$$

$$\frac{I_{j-1}}{I_j} = \cfrac{1-D_j}{1-\cfrac{D_{j-2}(1-D_{j-1})}{1-\cfrac{D_{j-3}(1-D_{j-2})}{\cdots}}} \tag{14}$$

resulting in Equations (13), (14), and (7) allowing for all inductor current and node voltages of any odd-numbered level converter of this topology to be calculated. These equations have been validated through simulation, the results of which are discussed below.

[0090] Unlike other multilevel topologies, the allowable switching states of the topologies proposed herein (e.g., the Manhattan topology) do not depend on the entire converter as a whole, but rather just each unit cell. Each unit cell can be treated as an individual switching converter, meaning that the only switching state limitation is that both switches within the same

unit cell cannot be on simultaneously. Beyond that there are no other limitations, duty cycles between different cells do not need to be synchronized or even operating at the same frequency. The example 7-level topology illustrated in FIG. 6 was tested and validated using the parameters V_{in} = 800V , I_{out} = 10A, F_{sw} = 50kHz, C = 10μF, and L = 450μH. FIG. 7 includes graphs showing capacitor voltages and inductor currents as functions of time for the 7-level converter of FIG. 6, with the above stated values, and a constant duty cycle (D) of 0.5 for all cells.

[0091] Consider next, with reference to FIG. 8, a nine-level converter 800 (seven cells), with respect to which the electrical behavior of the voltage conversion cells (e.g., capacitor voltages and inductor currents) was computed according to the equations developed for the 7-level converter of FIG. 6 (and adapted for a N-level converter), and also tested (through simulation) to verify the correctness of the equations representing the behavior of the implementations / topologies proposed herein. Five distinct sets of arbitrary duty cycles were used validate the derived equations and can be seen in Table 2, below. The use of arbitrary duty cycles was necessary because simply sweeping all duty cycles with the same value would neglect the possibility of duty cycles being inadvertently switched in the derived equations.

D_{set}	D_1	D_2	D_3	D_4	D_5	D_6	D_7
D_{set1}	0.10	0.16	0.22	0.28	0.36	0.42	0.50
D_{set2}	0.20	0.26	0.32	0.38	0.46	0.52	0.60
D_{set3}	0.30	0.36	0.42	0.48	0.56	0.62	0.70
D_{set4}	0.40	0.46	0.52	0.58	0.66	0.72	0.80
D_{set5}	0.50	0.56	0.62	0.68	0.76	0.82	0.90

Table 2: Duty cycle values for a 9-level converter

[0092] As can be seen in FIG. 8, the calculated currents/voltages match the simulated currents/voltages. Slight disagreements between the simulated and computed behaviors can be attributed to simulation non-idealities.

[0093] As noted, the behavior of the voltage converter implementations described herein can be controlled through control of the duty cycles for the individual cells comprising the converters. Two example methods of duty cycle control are described herein, but it is to be

noted that other control methods / procedures may be used. The 7-level converter 600 depicted in FIG. 6 is used to illustrate the two proposed example control processes. For the purposes of the present discussion, all unit cells have the same capacitor and inductor values. The switches are ideal and the switching is synchronized. For both of the example control processes / methods, the output voltage is swung from reference to input voltage with a constant output current equal to I_{out}.

[0094] In a first example control method, the duty cycles for all but a single cell are set to a constant (static) value such as 0.5 (e.g., for the 7-level converter 600, the duty cycle for the center cell 610, comprising the components L_3, S_3a, S_3b, C_4, and C_5 is the cell that is controllably varied to control the current / voltage behavior of the converter, while the duty cycles for the other cells are maintained at 0.5, or some other fixed values). The output voltage, V_{out}, is thus controlled solely by the duty cycle D_3 of the center unit cell. The results of sweeping the duty cycle of the center unit cell from 0 to 1 while holding the other cells constant at $D = 0.5$ can be seen in FIG. 9. The first control method thus results in ideal splitting of cell voltages over the entire the duty cycle sweep. The capacitor voltages above the output node evenly split the voltage V_{in} - V_{out} while the capacitor voltages below the output node evenly split the output voltage V_{out}. Furthermore, the relationship between D_3 and V_{out}/Vin is linear. The average current through the center inductor L_3 is constant throughout the sweep at three (3) times the output current, which can be attributed to the circulating currents between adjacent cells.

[0095] A second example control method involves using the derived fundamental equations (as more fully presented in the appended materials) in conjunction with an optimization procedure (such as MATLAB's *fmincon* optimization function) to determine optimized duty cycles for one or more of the cells of a converter. In some embodiments, one constraint that can be imposed for the optimization procedure is to require that the middle node's voltage be controlled to a predetermined desired voltage which is swept from reference to V_{in} (this constraint is referred to as the equality constraint). Another constraint that may be imposed is the inequality constraint, which is configured to ensure that no single capacitor voltage is greater than some voltage level (e.g., no single capacitor voltage is greater than one-third of the input voltage). In this example, the value of one-third is chosen as being at the extremes of the output voltage swing for the three capacitors in series that hold the full input voltage, and one-third represents ideal voltage splitting. For the example optimization procedure of the second

example control method, three objective functions are considered (of course, there are many other possible objective functions that can be used):

1) A 1-norm of all inductor currents, which represents a minimization of overall current rating.

2) A 2-norm squared of all inductor currents, which represents a minimization of overall power loss.

3) An inf-norm of all inductor currents, which represents a minimization of the maximum current in the set of all inductor currents.

[0096] The results of the optimization with the 1-norm and 2-norm squared are identical, suggesting that the optimal duty cycles for minimizing the overall current rating and minimizing the I^2R power losses are the same. The results are similar for the inf-norm optimization. It is worth noting, however, that the 1-norm and 2-norm optimizations effectively turn cells off at the extremes of the output voltage swing while the inf-norm optimization keeps them on while allocating proportionally small voltage across them. The maximum current through any inductor throughout the output voltage sweep is less than 1.5x the output current for all optimization methods, a substantial reduction over the non-optimized control method.

[0097] While the above control methods are described with reference to controlling the central node (i.e., cell 3 in a seven-cell configuration that corresponding to a 9-level converter), in some embodiments, a non-central cell can be controlled (by controllably adjusting its duty cycle). In some embodiments, more than a single cell of a multi-cell converter can be controlled (e.g., dynamically adjusting the duty cycles of two or more cells in a multi-cell converter).

[0098] Additional details about techniques for switching and voltage / current control functionality (through duty cycle control) are also provided in US 2021/0126522 A1, entitled "Methods, Systems, and Devices for Soft Switching of Power Converters," the content of which is hereby incorporated by reference in its entirety.

[0099] Thus, in some embodiments, a voltage converter system is provided that includes a plurality of energy storage elements (e.g., capacitors and inductors), and a plurality of switching devices, each in electrical communication with at least one of the plurality of the

energy storage elements, with the plurality of energy storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells (such as the arrangements depicted in FIGS. 1 and 3-6). The voltage converter system further includes a plurality of controllers (which may include processor-based controllers and/or closed-loop controllers such as the different controller types shown in FIG. 10) to controllably actuate one or more of the plurality of switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells. In some examples, each of the multiple voltage converting cells may include an arrangement of two capacitors and an inductor that define a buck-boost converter circuit (such as the circuits 200 and 250 illustrated in FIG. 2). The multiple voltage converting cells may be arranged as one or more stacked cascades of converting cells (for example, FIG. 10, discussed more particularly below, shows three stacks, each with a plurality of voltage converting cells / units), with each voltage converting cell in the one or more stacked cascades of conversion cells sharing at least one capacitor element with a neighboring voltage converting cell (as illustrated in FIG. 1, the voltage conversion cells of FIG. 10 may or may not share capacitors with each other).

[00100] In some embodiments, the plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells may be configured to achieve a voltage balance for the multiple voltage converting cells. The plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of the each of the multiple voltage converting cells may be configured to determine and maintain at least one capacitor of the multiple voltage converting cells at a respective voltage level. The plurality of controllers configured to controllably actuate the one or more of the plurality of switching devices may be configured to controllably actuate the one or more of the plurality of switching devices based at least in part on measured electrical properties of at least one of the multiple voltage converting cells. In such embodiments, the plurality of controllers may be configured to actuate the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements (e.g., to change the duty cycle so as to increase or decrease the voltage of the cell being controlled, as needed).

[00101] The plurality controller configured to controllably actuate the one or more of the plurality of switching devices may include at least one controller configured to determine

an adjustable duty cycle behavior for at least one of the multiple voltage converting cells. The at least one controller may be configured to continually (continuously or intermittently, at regular or irregular intervals) compute the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values. The at least one controller configured to determine the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may be configured to derive duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions. In such situations, the one or more objective functions may include one or more of, for example, a) 1-norm objective function of all inductor currents in the voltage converter system to minimize overall current rating of the voltage converter system, b) a 2-norm squared objective function of all the inductor currents of the voltage converter system to minimize overall power loss in the voltage converter system, and/or c) an inf-norm objective function of all the inductor currents of the voltage converter system to minimize maximum currents levels in all the inductor currents.

[00102] With reference next to FIG. 10, a schematic diagram of a system 1000 for a stackable control structure to control operation of a three-phase motor is shown. The system 1000 includes a central controller 1010 (which may be implemented using a processor-based device) in electrical communication with three stackable multi-level converters 1020, 1022, and 1024 (each of which may be implemented similarly to the multi-converters described herein) that controllably provide a 3-phase currents to a motor 1030. The motor 1030 typically includes a stator (e.g., realized using magnets or having stator windings), and a rotor (e.g., realized using one or more permanent magnets). Upon controlled application of currents (provided by the stacked multi-level converters 1020, 1022, and 1024) through the stator windings, a magnetic field is generated inside the stator that interacts with the magnetic field of the permanent magnets and results in the generation of torque applied to the rotor, thus causing the rotor to rotate.

[00103] As illustrated in FIG. 10, the central controller performs continually or intermittently (at regular or irregular intervals) a control process 1012. The control process implemented by the central controller may include, in some embodiments, collecting digitized (ADC) samples of voltages and currents from the local modules (i.e., from one or more cells of

the stackable multi-level converters). Then, the motor speed and torque are controlled in the *dq* reference frame by, for example, a Park/Clarke transformation. The generated references are distributed to the local power modules for duty cycle controlled PWM. In some embodiments, duty cycle computation can be performed at the central controller 1010. However, in some embodiments, the duty cycle computation to control the duty cycles of individual cells comprising the multi-level converters (of which there are three, namely, 1020, 1022, and 1024, for the example electrical-motor-based implementation of FIG. 10) can be done at respective individual controllers controlling one or more of the converter cells. As can be seen in the example of FIG. 10, each cell of the multi-level converters may include its own dedicated and localized controller (e.g., a PWN controller) to control the respective duty cycles for the switching devices of the each cell. For example, the voltage converter cell 1040 of the multi-converter 1020, includes a "Ref & Duty & PWM" controller 1042 (also referred to as a "cell controller") to control the electrical behavior of the cell 1040 (including to control the voltage levels at the capacitors of the cell 1040 through controlled adjustment of the duty cycles for the switches M1 and M2 of the cell 1040, achieved through controlled actuation of the switches M1 and M2). The controlled interactions of the various currents provided by the three multi-level converters coupled to the motor (achieved through the central controller 1010 and the individual controllers of the voltage converter cells to vary the voltage of the various cells in a desired manner) produces the desired motor behavior by the motor 1030. In some embodiments, the system 1000 may be implemented without a central controller, but with the individual cells each comprising their own respective controllers (be it a processor-based controller, a closed-loop controller, or otherwise). In some embodiments, some other arrangement of multiple controllers to control the voltages of the multi-level conversion system may be used (e.g., an individual controllers for cells / nodes with adjustable duty cycles, with some or all of the other cells having fixed duty cycles controlled by a central / global controller).

[00104] In some embodiments, the proposed multi-level converters may be used as an inverter. The center stage output connection allows the output of a multi-level converter to swing from rail to rail while maintaining evenly distributed voltage stresses above and below the center. This voltage sharing allows the use of switches with lower voltage rating, as each must support only a fraction of the input voltage. MOSFET conduction loss grows faster than linearly with blocking voltage (and switching speed reduces), so overall efficiency can be improved by

sharing voltage between several low-voltage switches rather than using a single high-voltage switch.

[00105] Because each unit cell of the multi-level converter generally contains an inductor and a capacitor, if such cells were used open loop, these components would be prone to resonating, leading to instability of the converter. To mitigate this, in some embodiments, each cell may be equipped with a local feedback loop to damp the resonance and provide high-bandwidth control of each capacitor voltage. FIG. 11 is a schematic diagram of a unit cell 1100 (such as any of the cells included with the multi-level converters described herein) that includes a local controller 1110. The local controller 1110 may be implemented as a processor-based device, an application-specific integrated circuit, or according to other types of controller circuitries, configured to generate control signaling (according to measured electrical characteristics of the unit cell, and/or global control signaling provided from a central controller such as the controller 1010 of FIG. 10). In some embodiments, the cell-level controller is given a reference, which sets the desired ratio between the top and bottom voltage in the cell. Each cell may have a second-order response, and can be controlled well with an inner inductor current loop (I_L, shown as signal 1112) and outer voltage loop that includes, for examples, the signals V_{top} 1114, and V_{bot} 1116, corresponding to the respective voltages measured across the top and bottom capacitors of the cell 1100. The local feedback also decouples the cells from each other. This simplifies control of the whole stack, and allows scaling of the number of cells without significant changes to controller compensation or design. This allows design reuse between inverters of different voltage requirements and economies of scale for making the unit cells.

[00106] In an inverter application, the stack output must be controlled to follow a sinusoidal voltage or current reference (i.e., the output of the stack is continually varied in a controlled manner to cause the operation of the connected motor). This reference may be come from a top-level stack controller, such as the controller 1010 of FIG. 10, or a controller 1210 shown in FIG. 12, which is a schematic diagram of a controlled motor system 1200 with a 3-phase inverter. As illustrated in FIG. 12, the stack controller 1210 measures the output I_{abc} 1222 of the inverter 1220 (which may be configured similarly to the plurality of multi-level converters 1020, 1022, and 1024 comprising the stack of the system 1000), measures any other desired variables (such as angle θ_m and speed ω_m) for a motor 1230, and computes (and outputs) a

reference input 1212 for the stack. The stack controller also receives as input a tracked speed profile ω_{ref}. The reference signal 1212 may be configured to directly control only the center (output) cell. The other cells may be set, in some embodiments, set to maintain a 1:1 voltage ratio between their top and bottom capacitors. Modulating the center stage trades voltage between the middle two capacitors. These voltage changes then propagate up and down the stack as the other cells enforce the 1:1 ratio. This ensures that all the capacitors above the output share the same voltage, as do all those below the output. The conversion ratio of the stack therefore matches the conversion ratio of the center cell. The fast local feedback loops and capacitive energy storage on each cell ensure that voltage balancing is maintained through transients.

[00107] In one embodiment, three arrangements of a 3-cell topology and a top-level controller were used to construct a three-phase motor drive, with a configuration similar to that depicted in FIG. 12. The system tracked a speed profile ω_{ref} and responded to bidirectional torque disturbances illustrated in the graphs 1300 and 1310, respectively, of FIG. 13. FIG. 14 includes graphs showing the three voltage levels (in graph 1400) in the multi-level converter stack (with three converters, each corresponding to one of the three phases driving the motor), and its output current (in graph 1410). Thus, as indicated by the results of FIGS. 13 and 14, the topology successfully produces the required waveforms, and the motor tracked the desired speed profile while rejecting the torque disturbances.

[00108] Thus, in some embodiments, the multi-level arrangement of the multiple voltage converting cells may include a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load (such as a motor, like the one shown in FIGS. 10 and 12), with the plurality of controllers including a central controller (like the central controller 1010 of FIG. 10) electrically coupled to the multiple stacks of voltage converting cells to control electrical currents produced by the multiple stacks to power the load. The load may include a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors, and with the central controller being configured to control duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque. In some embodiments, the plurality of controllers may include at least one additional individual cell controller (such as the cell controller 1042 of FIG. 10; such a cell controller may be implemented as a closed-loop controller, as a processor-based

controller, or some other type of controller) for at least one of the multiple voltage converting cells, with the at least one of the multiple voltage converting cells comprising two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, and with the individual cell controller for the at least one of the multiple voltage converting cells being configured to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level. It is to be noted that in some embodiments, the controller of the voltage converter system may include individua cell controllers (or even just a single controller for one of the voltage converter cells) without using a central controller to implement joint control over the multi-level converter circuitry.

[00109] Another topology that may be used to implement multi-level converters is the Dual Active Half Bridges (DAHB) Manhattan topology. The proposed DAHB Manhattan topology uses a dual-active half bridge module, as opposed to the half-bridge (HB) modules of the generalized topology discussed in relation to FIGS. 1-14. The resulting DAHB topology requires half the number of switches and inductive components. In addition, the DAHB Manhattan converter mitigates the loop currents, and is thus a fully balanced power electronic topology that scales linearly to N levels with constant component size. It is to be noted that the proposed DAHB converter unit / cell may be used in place of the half-bridge Manhattan units used to realize the multi-level converter systems shown in FIGS. 1-14.

[00110] As will be discussed in greater detail below, regions of the Dual Active Half Bridge converter are defined by sequences of four switches that connect the circuit's capacitors through its transformer. The duty cycles of the primary and secondary sides (which are decoupled, or isolated from each other through the transformer), are controlled independently, and along with the phase shift between switching events across the primary and secondary sides, define the switching sequences. Twenty-four (24) unique switching sequences create corresponding operating regions that span the possible values of the three inputs. These regions are formed out of the six piecewise affine inequalities which emerge from the possible orderings of the switching events. Control of the switching sequences leads to arbitrary control over the energy in the four capacitors. This allows power to flow from one capacitor to another based on the switching region and key parameters such as voltage and initial transformer current. Knowledge of the switching states and the corresponding power flows in the converter can lead to more optimal designs for particular applications of the dual active half bridge.

[00111] Dual Active Half Bridge Converters (DAHBs) include four capacitors paired with four switches and a high frequency transformer to connect them. FIG. 15A is a schematic diagram of a DAHB unit 1500. This configuration results in the DAHB having efficient operation and wide applications as stand-alone devices and as subcircuits in more complex circuits such as in multilevel converters. In standalone applications, they can be used in low power circuits because, for a given power, fewer switches lead to higher current per switch when compared with a full bridge. However, this does not prevent use in higher power systems. DAHBs can be used as components for electric vehicle charging circuits, in battery charging applications, microgrids, and auxiliary power sources, making them a useful tool in the effort to electrify infrastructure as a means to mitigate the worst effects of climate change.

[00112] Power transfer between the primary and secondary sides in a DAHB is dependent on the current through the transformer leakage inductance. Control of this current is critical to managing DAHB's operation. Various control schemes based on state space modeling control the operation of a DAHB unit by controlling the duty cycles of the switches on each side of the transformer as well as the phase shift between the switches on the primary and secondary sides. The implementations proposed herein quantify the possible switching sequences of the DAHB in order to establish a model of the converter unlocking a total of three (3) degrees of freedom in which the DAHB can operate. With this new 3-dimensional DAHB (3D-DAHB) scheme, all possible orderings of switching events can be reached, allowing for selection by a controller to optimize 3D-DAHB operation. This in turns enables the movement of energy to any capacitor arbitrarily. The 3D-DAHB can be expressed as a decomposition of the DAHB circuit that includes two buck-boost converters, and a DAHB circuit, as illustrated in FIG. 15B. The switching sequences form piecewise affine inequalities in the space of the three input variables which defines a new class of control.

[00113] The 3D-DAHB configuration has many parameters that affect its operation, the most prominent of which are the voltages across the four capacitors, which are constrained by the total bus voltage. Because of the speed of the switching that occurs, typically between 100kHz and 1MHz, the simplifying assumption that these voltages are constant over the course of one period is made for the duration of the present analysis. The exact length of the period will also affect the amount of power transferred between the capacitors. Other relevant parameters are the leakage inductance of the transformer, and the initial leakage current at the beginning of each

period. The controlled variables are the relative duty cycles of the primary and secondary side switches, θ_1 and θ_2, and the phase shift between the primary and secondary switching events, ϕ. Each of these variables can be defined on a region spanning one period before they return to previously defined values. For the purposes of symmetry, all these have been defined on the region $\phi, \theta_1, \theta_2 \in [-1/2, +1/2]$.

[00114] There are twenty-four (24) possible switching configurations that lead to different behaviors of the 3D-DAHB. The sequences are shown in a table 1600 FIG. 16, illustrating the twenty-four switching sequences of possible operating modes (regimes) for the 3D-DAHB configuration when controlling the duty cycles and phase shifts. The switching events are as follows: $t_1 = T(1/2 - \theta_1)$, $t_2 = T\phi$, and $t_3 = T(1/2 - \theta_2 + \phi)$. Because the inputs are chosen as the more important or fundamental values θ_1, θ_2, and ϕ, the relevant time periods that define the switching states also include the midpoint of each period in addition to the beginning and end.

[00115] The operation of any DAHB is governed by the leakage inductor current in the high frequency transformer. Using the assumptions above, and the formula for inductor current in terms of the voltage across it, the current through the inductor can be summarized as follows:

$$i_{Lk}(t) = \begin{cases} i_{LK}(0) + \int_{t_a}^{t_b} \frac{V_{a1} + V_{a2}}{L_{LK}} dt & 0 < t \le t_a \\ i_{LK}(t_a) + \int_{t_a}^{t_b} \frac{V_{b1} + V_{b2}}{L_{LK}} dt & t_a < t \le t_b \\ i_{LK}(t_b) + \int_{t_b}^{t_c} \frac{V_{c1} + V_{c2}}{L_{LK}} dt & t_b < t \le t_c \\ i_{LK}(t_c) + \int_{t_c}^{T} \frac{V_{a1} + V_{a2}}{L_{LK}} dt & t_c < t \le T \end{cases} \quad (15)$$

where the time periods and voltages in each part of the piecewise function will change depending on the switching sequence regime. The time periods t_a, tb, and t_c will be one of t_1, t_2, or t_3, defined above, while the voltages will be V_1,$-V_2$, V_3, or $-V_4$. FIG. 17 includes a graph 1700 showing the leakage inductor current during one period of the switching sequence corresponding

to the 3rd row and 2nd column of the table 1610 of FIG. 16 (indicated as entry 1610) with the relevant time intervals marked. The results of the graph 1700 were obtained with values of ϕ = 0.25, $\theta_1 = -0.3$, and $\theta_2 = -0.2$, which were chosen to satisfy the constraints of this sequence.

[00116] Thus, the inductor current will be a piecewise linear function with four parts, whose slopes and intercepts differ among the different switching regimes. The slopes of each of the lines are dependent on the voltages on the two active capacitors in that region as well as the leakage inductance of the transformer while the intercepts are dependent on the previous value of the current. The length of each line segment depends on the particular choice switching variables ϕ, θ_1, and θ_2 that satisfy the constraints of the switching sequence region. The individual capacitor currents will be a subset of between one and three parts of the total inductor current. For example, in the switching sequence of position (3,2) of table 1600, the current in capacitor one will include the current between times (0, t_2) and between ($t2$, t_1) as shown in Equation 16 below. These currents do not necessarily have to be consecutive.

$$i_1(t) = \begin{cases} i_{Lk}(0) + \dfrac{t(V_1 + V_4)}{L_{Lk}} dt & 0 \le t \le t_2 \\ i_{Lk}(t_2) + \dfrac{(V_1 - V_3)(t - t_2)}{L_{Lk}} dt & t_2 \le t \le t_1 \end{cases} \tag{16}$$

where $i_{Lk}(t_2) = i_{Lk}(0) + \dfrac{t_2(V_1 + V_4)}{L_{Lk}}$ is the current at time t_2. The capacitor currents are fully defined by the voltages, switching region, and leakage inductance, leaving the current at beginning of the period as the only variable. The constraints defining a switching sequence can be derived by expanding the natural inequalities created by the sequences of FIG. 16. These, in turn, lead to a set of inequality constraints on θ_1, θ_2, and ϕ of the form:

$$Hx \le kx,$$

where $H \in \mathbb{R}^{6x3}, k \in \mathbb{R}^{6x1}, x = \begin{pmatrix} \phi \\ \theta_1 \\ \theta_2 \end{pmatrix}$. Each switch sequence is defined by the six greater and lesser inequalities for each switching event. For example, the switching sequence for the inductor current of FIG. 17 is:

$$H = T\begin{bmatrix} -1 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & -1 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & -1 \\ -1 & -1 & 1 \end{bmatrix}, k = \frac{T}{2}\begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} \quad (17)$$

[00117] The *H* and *k* matrices can be created for each of the 24 switching sequences. Each of the sequences now represents a piecewise affine region in the space formed by the θ1, θ2, and ϕ axes. These 24 regions are shown together in FIG. 18, providing a diagram 1800 showing all of the switching sequence regions forming a convex, nonoverlapping union spanning ±1/2 on each of the axes. Diagram 1810 of FIG. 18 shows the sequence region corresponding to the position (3,2) of the table 1600 of FIG. 16. The regions are thus unique and cover all possible values in their definitions.

[00118] The average power in capacitor *k* can be calculated by multiplying the voltage across the capacitor, which is constant over a single period, by the average current through that capacitor. The general case is given as

$$P_{k,avg} = (V_k)\left(\frac{1}{T}\int_0^T i_k(t)dt\right) \quad (18)$$

[00119] Using k = 1 and Equation 16 above, the resulting power for the first capacitor in switching sequence (3,2) is:

$$P_{1,avg} = \frac{V_1\left(2L_{Lk}i_{lk0}t_2 + (t_1 - t_2)(2L_{Lk}i_{lk0} + V_1t_1 + V_1t_2 - V_3t_1 + V_3t_2 + 2V_4t_2) + t_2^2(V_1 + V_4)\right)}{2L_{Lk}T} \quad (19)$$

[00120] Similar equations can be derived for each capacitor in each switching region. This outlines a total of 96 similar equations to fully define all possible capacitor powers in the 3D-DAHB.

[00121] Despite the high number of equations, several practical simplifications can be made in order to develop a controller. The first is to restrict operation of 3D-DAHB to one switching region at a time, which ensures only four equations are relevant at a time; transitions between regions can occur smoothly allowing for a controller to recognize and adapt to the appropriate region. In some embodiments, a state space piecewise affine model to control power flows may be developed.

[00122] Next, multi-level converter topologies based on the above-described controllable DAHB unit are described. The generalized topology for the DAHB Manhattan converter is shown in FIG. 19, where n represent the number of levels and number of stackable unit cells. Four different DAHB converters are depicted in FIG. 19, including a 2-level converter 1900, a 4-level ($n = 4$) converter 1910, an 8-level ($n = 8$) converter 1920, and a 2^N-level converter 1930. The circuit topology is capable of bidirectionally converting DC/DC or DC/AC and can be configured also in parallel. For the sake of brevity, the topologies depicted in FIG. 19 implement a multilevel phase leg, i.e., a step-down buck configuration that generates an output voltage $v_o(t)$ from a source voltage $v_s(t)$. The output voltage is time varying and can be a DC or AC signal that satisfies $v_o(t) \in [0, v_s(t)]$.

[00123] Example stackable unit cells 2000, 2010, and 2020 that comprise a DAHB multilevel topology are shown in FIG . 20 (the stackable cells / units of FIG. 20 may be similar to the units of FIGS. 15A and B). The DAHB configurations of the unit cells 2010 and 2020 include a T-transformer model and a π-transformer model, respectively. The 3D DAHB stackable unit cells of FIG. 20 can move power from and to any capacitor independently by acting on the three control variables: the phase shift between the primary and secondary side pulse-width modulation (PWM) signal θ, the duty cycle of the primary PWM signal $d_1(t)$, and

the duty cycle of the secondary side PWM signal $d_2(t)$. The PWM-related signals control and actuate the various switches included with each of the individual cell units. For example, actuating signals are produced by a controller (not shown), which may be a close-loop controller, based on electrical properties (e.g., current and voltages) measured / sensed in the circuitry of the individual cell 2000 and the desired electrical behavior of the individual cell, to controllably actuate one or more of the switches of the primary side 2002 switches, and controllably actuate secondary side 2004 switches. Current flows through each unit cell in the same way it does in a typical inverting buck-boost converter. Hence, this topology has three degrees of freedom and can set three capacitor voltages independently. The fourth capacitor voltage generally results from a boundary constraint such as the source voltage.

[00124] The stacked cell nature of this topology eliminates the need for a bulk capacitance between the input/output nodes to reference as the series combination of the cell capacitances serves to support both the input and output nodes as well as the voltages within each cell. Individual capacitor voltages can be controlled as a function of the duty cycles of each unit cell, allowing for the voltage across the entire stack to be balanced across each cell to any arbitrary ratio. This enables the control of voltages higher than the voltage rating of any individual semiconductor or passive component. As the output voltage is simply the sum of the capacitor voltages between the output node and reference, the ability to balance the capacitor voltages to any arbitrary ratio also allows for the output voltage to swing between full input voltage and reference.

[00125] For the n-level converters shown in FIG. 19, the voltage at any node along the center capacitor stack can be determined according to the equations

$$\frac{dv_{cj}(t)}{dt} = \begin{cases} i_{cj(t)} + i_s(t) & | \, j < n/2 \\ i_{cj(t)} + i_s(t) - i_o(t) & | \, j > n/2 \end{cases} \tag{20}$$

where v_{cj} are the capacitor voltages for a specific capacitor j, i_{cj} is the current moved by the 3D-DAHB to that specific capacitor, and $j = 1, \ldots, n$ identifies the capacitors.

[00126] It is generally assumed that either the source voltage or the output voltage is given, and the other voltage is the target voltage that is set by the converter. The former case identifies a multilevel buck converter case and the latter case identifies a multilevel boost. In

both cases, the output (and input) can be a DC signal or an AC signal with DC offset. Since it is common to operate on a stabilized DC bus, consider this use case that imposes the boundary condition:

$$v_s(t)=\sum_{j=1}^{n} v_{cj}(t)=V_s \tag{21}$$

[00127] Similarly, the output voltage is defined as:

$$v_o(t)=\sum_{j=n/2}^{n} v_{cj}(t) \tag{22}$$

[00128] Therefore, the Manhattan converter changes the output voltage by moving charge from the capacitors below the output node to the capacitors above that node and vice versa. Even in steady state conditions, the 3D-DAHB move current such that

$$\frac{dv_{cj}(t)}{dt}=0A \Leftrightarrow \begin{cases} i_{cj(t)}+i_s(t)=0A & | j<n/2 \\ i_{cj(t)}+i_s(t)-i_o(t)=0A & | j>n/2 \end{cases} \tag{23}$$

[00129] It is noted that in contrast to the HB Manhattan converter (discussed in relation to FIGS. 1-9), the DAHB Manhattan converter is a point-to-point conversion system as opposed to a semi-cascade. Therefore, the overall converter efficiency is the same as the efficiency of the DAHB modules.

[00130] The DAHB Manhattan converter was validated for a three-phase motor drive inverter. The $N = 4$ converter 1910 shown in FIG. 19 was put in parallel on the DC site. Then, the output of each phase was connected to a motor terminal. The converter uses the same capacitor and leakage inductor values of C = 10μF and L = 4.5μH. The switches were considered to be ideal and synchronized within one DAHB. V_s was set to 800V, I_{out} = 10A, and F_{sw} = 50kHz. The Manhattan three-phase inverter was connected to a PMSM motor with 10 poles, 0.4Ω stator resistance, 10.5mH and 12mH d-axis and q-axis inductance, respectively, and $0.35V_s$ permanent magnet rotor flux. The configuration used a higher-level motor control that communicates desired capacitor voltages and currents to the lower level controllers in the 3D-DAHB. The motor control included an inner PMSM vector control to control stator current and

torque as well as an outer speed controller. The Manhattan three-phase inverter drove a motor from standstill to 400rpm, maintained the speed, and then reverses the speed to -400rpm. During the 400rpm period, a positive and negative 4Nm load torque step was applied. FIGS. 21A-B includes graphs showing the results of the validation experiment for the DAHB Manhattan topology in the inverter operation driving the 3-phase motor. Specifically, FIG. 21A includes a graph illustrating current waveforms of the $N = 4$ DAHB Manhattan topology in inverter operation driving a 3-phase motor, and FIG. 21B includes graphs for the resultant toque, speed, and angle behavior for the 3-phase motor.

[00131] Thus, in some embodiments, at least one of the multiple voltage converting cells may include a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer (as shown, for example, in FIGS. 15A and 15B), with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices.

[00132] The at least one DAHB converter configuration cell may include two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices (as illustrated in FIG. 20, for example). In such embodiments, the plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells may be configured to controllably actuate the two primary side switching devices and the two secondary side switching devices according to one or more pre-determined switching sequences defined for a particular time interval. The one or more switching sequences for the at least one DAHB converter configuration cell is defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events.

[00133] In some examples, the multiple voltage converting cells may each include a respective cell with the DAHB converter configuration cell, and the multiple voltage converting cells may be arranged as one or more stacked cascades of the cells with the DAHB converter configuration cell connected to a load. For example, the individual voltage converter cells / units

depicted in FIGS. 1, 3-6, etc. (where the cells include non-decoupled buck-boost circuits) can be supplanted by the DAHB cell configuration discussed in relation to FIGS. 15-22 herein.

[00134] With reference next to FIG. 22, a flowchart of an example voltage conversion procedure 2200 that is based on the topologies and various implementations described herein is shown. The procedure 2200 includes obtaining 2210 electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being in electrical communication with at least one of the plurality of the energy storage elements, and with the plurality of energy storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells. For example, each of the multiple voltage converting cells may include an arrangement of two capacitors and an inductor that define a buck-boost converter circuit. The electrical properties data may be obtained by measuring currents and voltages at various points of the voltage converter system (using one or more current or voltage sensors deployed at such various points of the voltage converter system), and digitizing the measurements (through analog-to-digital converters, or ADC's).

[00135] The procedure 2200 further includes controllably actuating 2220 by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

[00136] In some examples, controllably actuating the one or more of the plurality of switching devices may include independently controlling the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells to achieve a voltage balance for the multiple voltage converting cells. Controllably actuating the one or more of the plurality of switching devices may include controllably actuating the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements. In some embodiments, controllably actuating the one or more of the plurality of switching devices may include determining an adjustable duty cycle behavior for at least one of the multiple voltage converting cells. In such embodiments, determining the

adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may include continually (e.g., continuously or intermittently, at regular or irregular time intervals) computing the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values. In some embodiments, determining the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells may include deriving duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions. In such embodiments, the one or more objective functions may include one or more of, for example, a) 1-norm objective function of all inductor currents in the voltage converter system to minimize overall current rating of the voltage converter system, b) a 2-norm squared objective function of all the inductor currents of the voltage converter system to minimize overall power loss in the voltage converter system, and/or c) an inf-norm objective function of all the inductor currents of the voltage converter system to minimize maximum currents levels in all the inductor currents.

[00137] As noted, in some embodiments, at least one of the multiple voltage converting cells may include a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer, with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices. For example, the at least one DAHB converter configuration cell includes two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices. In such examples, controllably actuating the one or more of the plurality of switching devices may include controllably actuating the two primary side switching devices and the two secondary side switching devices according to one or more pre-determined switching sequences defined for a particular time interval.

[00138] The one or more switching sequences for the at least one DAHB converter configuration cell may be defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events. The

multi-level arrangement of the multiple voltage converting cells comprises a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load. In such situations, controllably actuating the one or more of the plurality of the switching devices may include controlling, by a central controller (such as the central controller shown in FIG. 10), electrical currents produced by the multiple stacks to power the load. The load may include a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors. Controlling, by the central controller, the electrical currents produced by the multiple stacks may include, in such situations, controlling duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque. Controllably actuating the one or more of the plurality of switching devices may further include controlling individually, by a dedicated cell controller for at least one of the multiple voltage converting cells, the at least one of the multiple voltage converting cells (the dedicated cell controller may be a processor-based device, a close-loop controller, or some other type of control mechanism) that includes two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level.

[00139] In some embodiments, the multi-level arrangement of the multiple voltage converting cells may include a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, with each of the multiple voltage converting cell including a dedicated cell controller. Controllably actuating the one or more of the plurality of the switching devices may include controllably actuating, by the respective dedicated cell controller for the each of the multiple voltage converting cells, the one or more of the plurality of the switching devices to independently control voltage levels of the at least one energy storage element of the multiple voltage converting cells.

[00140] Performing the various techniques and operations described herein (including the control procedure 2200) may be facilitated by a controller device (e.g., a processor-based computing device). Such a controller device may include a processor-based device such as a computing device, and so forth, that typically includes a central processor unit or a processing core. The device may also include one or more dedicated learning machines

(e.g., neural networks) that may be part of the CPU or processing core. In addition to the CPU, the system includes main memory, cache memory and bus interface circuits. The controller device may include a mass storage element, such as a hard drive (solid state hard drive, or other types of hard drive), or flash drive associated with the computer system. The controller device may further include a keyboard, or keypad, or some other user input interface, and a monitor, e.g., an LCD (liquid crystal display) monitor, that may be placed where a user can access them.

[00141] The controller device is configured to facilitate, for example, the implementation of a multilevel voltage converter (e.g., by controlling the switching devices of the system). The storage device may thus include a computer program product that when executed on the controller device (which, as noted, may be a processor-based device) causes the processor-based device to perform operations to facilitate the implementation of procedures and operations described herein. The controller device may further include peripheral devices to enable input/output functionality. Such peripheral devices may include, for example, flash drive (e.g., a removable flash drive), or a network connection (e.g., implemented using a USB port and/or a wireless transceiver), for downloading related content to the connected system. Such peripheral devices may also be used for downloading software containing computer instructions to enable general operation of the respective system/device. Alternatively and/or additionally, in some embodiments, special purpose logic circuitry, e.g., an FPGA (field programmable gate array), an ASIC (application-specific integrated circuit), a DSP processor, a graphics processing unit (GPU), application processing unit (APU), etc., may be used in the implementations of the controller device. Other modules that may be included with the controller device may include a user interface to provide or receive input and output data. The controller device may include an operating system.

[00142] Computer programs (also known as programs, software, software applications or code) include machine instructions for a programmable processor, and may be implemented in a high-level procedural and/or object-oriented programming language, and/or in assembly/machine language. As used herein, the term "machine-readable medium" refers to any non-transitory computer program product, apparatus and/or device (e.g., magnetic discs, optical disks, memory, Programmable Logic Devices (PLDs)) used to provide machine instructions and/or data to a programmable processor, including a non-transitory machine-readable medium that receives machine instructions as a machine-readable signal.

[00143] In some embodiments, any suitable computer readable media can be used for storing instructions for performing the processes / operations / procedures described herein. For example, in some embodiments computer readable media can be transitory or non-transitory. For example, non-transitory computer readable media can include media such as magnetic media (such as hard disks, floppy disks, etc.), optical media (such as compact discs, digital video discs, Blu-ray discs, etc.), semiconductor media (such as flash memory, electrically programmable read only memory (EPROM), electrically erasable programmable read only Memory (EEPROM), etc.), any suitable media that is not fleeting or not devoid of any semblance of permanence during transmission, and/or any suitable tangible media. As another example, transitory computer readable media can include signals on networks, in wires, conductors, optical fibers, circuits, any suitable media that is fleeting and devoid of any semblance of permanence during transmission, and/or any suitable intangible media.

[00144] Although particular embodiments have been disclosed herein in detail, this has been done by way of example for purposes of illustration only, and is not intended to be limiting with respect to the scope of the appended claims, which follow. Features of the disclosed embodiments can be combined, rearranged, etc., within the scope of the invention to produce more embodiments. Some other aspects, advantages, and modifications are considered to be within the scope of the claims provided below. The claims presented are representative of at least some of the embodiments and features disclosed herein. Other unclaimed embodiments and features are also contemplated.

WHAT IS CLAIMED IS:

1. A voltage converter system comprising:

a plurality of energy storage elements;

a plurality of switching devices, each in electrical communication with at least one of the plurality of the energy storage elements, wherein the plurality of energy storage elements and the plurality of switching devices are configured in a multi-level arrangement of multiple voltage converting cells; and

a plurality of controllers to controllably actuate one or more of the plurality of switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

2. The voltage converter system of claim 1, wherein each of the multiple voltage converting cells comprises an arrangement of two capacitors and an inductor that define a buck-boost converter circuit.

3. The voltage converter system of claim 1, wherein the multiple voltage converting cells are arranged as one or more stacked cascades of converting cells, with each voltage converting cell in the one or more stacked cascades of conversion cells sharing at least one capacitor element with a neighboring voltage converting cell.

4. The voltage converter system of claim 1, wherein the plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells is configured to achieve a voltage balance for the multiple voltage converting cells.

5. The voltage converter system of claim 1, wherein the plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of the each of the multiple voltage converting cells is configured to determine and maintain at least one capacitor of the multiple voltage converting cells at a respective voltage level.

6. The voltage converter system of claim 1, wherein the plurality of controllers configured to controllably actuate the one or more of the plurality of switching devices is configured to controllably actuate the one or more of the plurality of switching devices based at least in part on measured electrical properties of at least one of the multiple voltage converting cells.

7. The voltage converter system of claim 6, wherein the plurality of controllers is configured to actuate the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements.

8. The voltage converter system of claim 1, wherein the plurality of controllers configured to controllably actuate the one or more of the plurality of switching devices includes at least one controller configured to determine an adjustable duty cycle behavior for at least one of the multiple voltage converting cells.

9. The voltage converter system of claim 8, wherein the at least one controller configured to determine the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells is configured to continually compute the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values.

10. The voltage converter system of claim 8, wherein the plurality of controllers configured to determine the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells is configured to derive duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions.

11. The voltage converter system of claim 10, wherein the one or more objective functions includes one or more of: a) 1-norm objective function of all inductor currents in the

voltage converter system to minimize overall current rating of the voltage converter system, b) a 2-norm squared objective function of all the inductor currents of the voltage converter system to minimize overall power loss in the voltage converter system, or c) an inf-norm objective function of all the inductor currents of the voltage converter system to minimize maximum currents levels in all the inductor currents.

12. The voltage converter system of claim 1, wherein at least one of the multiple voltage converting cells comprises a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer, with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices.

13. The voltage converter system of claim 12, wherein the at least one DAHB converter configuration cell includes two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices.

14. The voltage converter system of claim 13, wherein the plurality of controllers configured to independently control the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells includes at least one dedicated controller for the at least one DAHB converter configuration cell, the at least one dedicated controller configured to controllably actuate the two primary side switching devices and the two secondary side switching devices according to one or more pre-determined switching sequences defined for a particular time interval.

15. The voltage converter system of claim 14, wherein the one or more switching sequences for the at least one DAHB converter configuration cell is defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events.

16. The voltage converter system of claim 12, wherein the multiple voltage converting cells each includes a respective cell with the DAHB converter configuration cell, and wherein the multiple voltage converting cells are arranged as one or more stacked cascades of the cells with the DAHB converter configuration cell connected to a load.

17. The voltage converter system of claim 1, wherein the multi-level arrangement of the multiple voltage converting cells comprises a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, and wherein the plurality of controllers comprises a central controller in electrical communication with the multiple stacks of voltage converting cells to control electrical currents produced by the multiple stacks to power the load.

18. The voltage converter system of claim 17, wherein the load comprises a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors, and wherein the central controller is configured to control duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque.

19. The voltage converter of claim 17, wherein the plurality of controllers comprises an individual cell controller for each of the multiple voltage converting cells, with the each of the multiple voltage converting cells comprising two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, and wherein the each individual cell controller for the each of the multiple voltage converting cells is configured to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level.

20. A voltage conversion method comprising:

obtaining electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being electrically coupled to at least one

of the plurality of the energy storage elements, wherein the plurality of energy storage elements and the plurality of switching devices are configured in a multi-level arrangement of multiple voltage converting cells; and

controllably actuating by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

21. The method of claim 20, wherein each of the multiple voltage converting cells comprises an arrangement of two capacitors and an inductor that define a buck-boost converter circuit.

22. The method of claim 20, wherein controllably actuating the one or more of the plurality of switching devices comprises independently controlling the voltage levels of the at least one energy storage element of each of the multiple voltage converting cells to achieve a voltage balance for the multiple voltage converting cells.

23. The method of claim 20, wherein controllably actuating the one or more of the plurality of switching devices comprises controllably actuating the one or more of the plurality of switching devices according to a voltage level measured across at least one of the plurality energy storage elements.

24. The method of claim 20, wherein controllably actuating the one or more of the plurality of switching devices comprises:

determining an adjustable duty cycle behavior for at least one of the multiple voltage converting cells.

25. The method of claim 24, wherein determining the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells comprises continually computing the duty cycle behavior for the at least one of the multiple voltage converting cells that achieves a pre-determined output voltage for the voltage converter system, with other of the multiple voltage

converting cells, excluding the at least one of the multiple voltage converting cells, configured with respective substantially fixed duty cycle values.

26. The method of claim 24, wherein determining the adjustable duty cycle behavior for the at least one of the multiple voltage converting cells comprises deriving duty cycle characteristics for the multiple voltage converting cells to achieve a desired output voltage for the voltage converter system that optimizes one or more objective functions.

27. The method of claim 26, wherein the one or more objective functions includes one or more of: a) 1-norm objective function of all inductor currents in the voltage converter system to minimize overall current rating of the voltage converter system, b) a 2-norm squared objective function of all the inductor currents of the voltage converter system to minimize overall power loss in the voltage converter system, or c) an inf-norm objective function of all the inductor currents of the voltage converter system to minimize maximum currents levels in all the inductor currents.

28. The method of claim 20, wherein at least one of the multiple voltage converting cells comprises a Dual Active Half Bridge (DAHB) converter configuration cell that includes a primary side and a secondary side separated from the primary side by a transformer, with the primary side including one or more primary side energy storage elements and one or more primary side switches, and with the secondary side including one or more secondary side energy storage elements and one or more secondary side switching devices.

29. The method of claim 28, wherein the at least one DAHB converter configuration cell includes two primary side capacitors, two primary side controllable switching devices, two secondary side capacitors, and two secondary side switching devices, and wherein controllably actuating the one or more of the plurality of switching devices comprises controllably actuating the two primary side switching devices and the two secondary side switching devices according to one or more pre-determined switching sequences defined for a particular time interval.

30. The method of claim 29, wherein the one or more switching sequences for the at least one DAHB converter configuration cell is defined by duty cycles for the primary side and for the secondary side, and by a phase shift, ϕ, between a primary side and a secondary side switching events.

31. The method of claim 20, wherein the multi-level arrangement of the multiple voltage converting cells comprises a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, and wherein controllably actuating the one or more of the plurality of the switching devices comprises controlling, by a central controller from the plurality of controllers, electrical currents produced by the multiple stacks to power the load.

32. The method of claim 31, wherein the load comprises a multi-phase motor, with each of the multiple stacks of voltage converter cells providing a respective phased current for one of multi-phase inputs of the multi-phase motors, and wherein controlling, by the central controller, the electrical currents produced by the multiple stacks comprises controlling duty cycles of one or more switching devices in the multiple stacks to produce the multi-phase currents that result in one or more of a specified motor speed or a specified motor torque.

33. The method of claim 31, wherein controllably actuating the one or more of the plurality of switching devices further comprises controlling individually, by a dedicated cell controller for at least one of the multiple voltage converting cells, the at least one of the multiple voltage converting cells that includes two capacitors, two switching devices, and an inductor element arranged in a buck-boost converter configuration, to maintain a ratio between a first and second voltage levels of non-common terminals of the two capacitors at a specified level.

34. The method of claim 20, wherein the multi-level arrangement of the multiple voltage converting cells comprises a plurality of voltage converting cells arranged in multiple stacks of voltage converting cells connected to a load, with each of the multiple voltage converting cell including a dedicated cell controller, and wherein controllably actuating the one or more of the plurality of the switching devices comprises controllably actuating, by the respective dedicated cell controller for the each of the multiple voltage converting cells, the one or more of the

plurality of the switching devices to independently control voltage levels of the at least one energy storage element of the multiple voltage converting cells.

35. A non-transitory computer readable media storing a set of instructions, executable on at least one programmable device, to:

obtain electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being in electrical communication with at least one of the plurality of the energy storage elements, wherein the plurality of energy storage elements and the plurality of switching devices are configured in a multi-level arrangement of multiple voltage converting cells; and

controllably actuate by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.

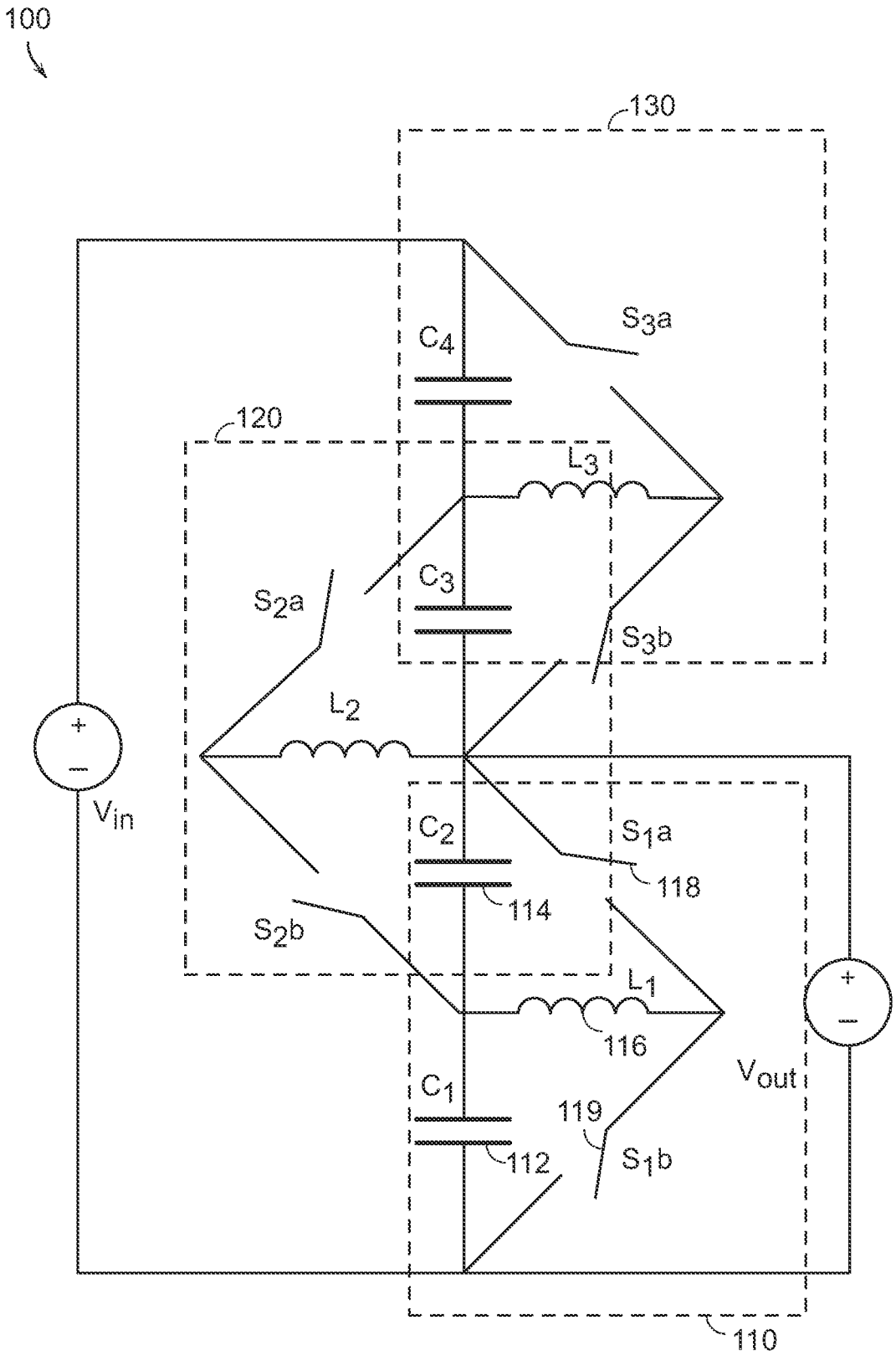
100
130
120
110
C_4
S_3a
L_3
C_3
S_2a
S_3b
L_2
V_{in}
C_2
S_1a
118
114
S_2b
L_1
116
V_{out}
C_1
119
112
S_1b

FIG. 1

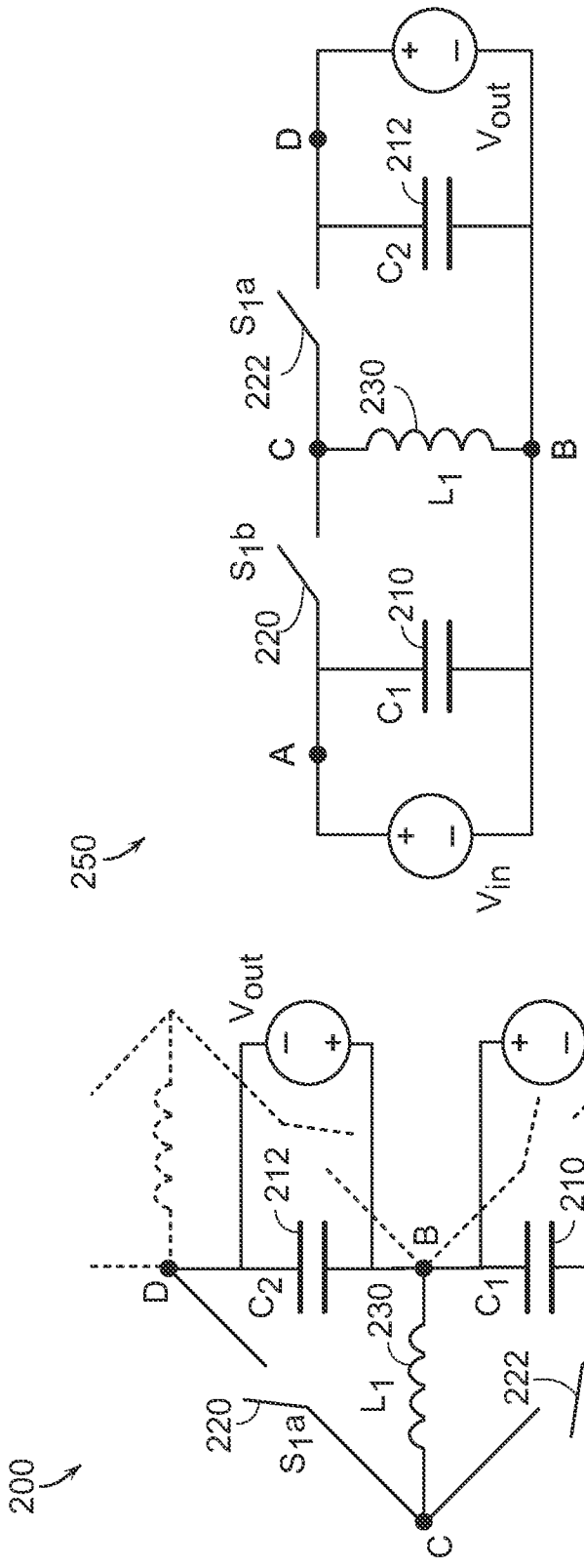

FIG. 2

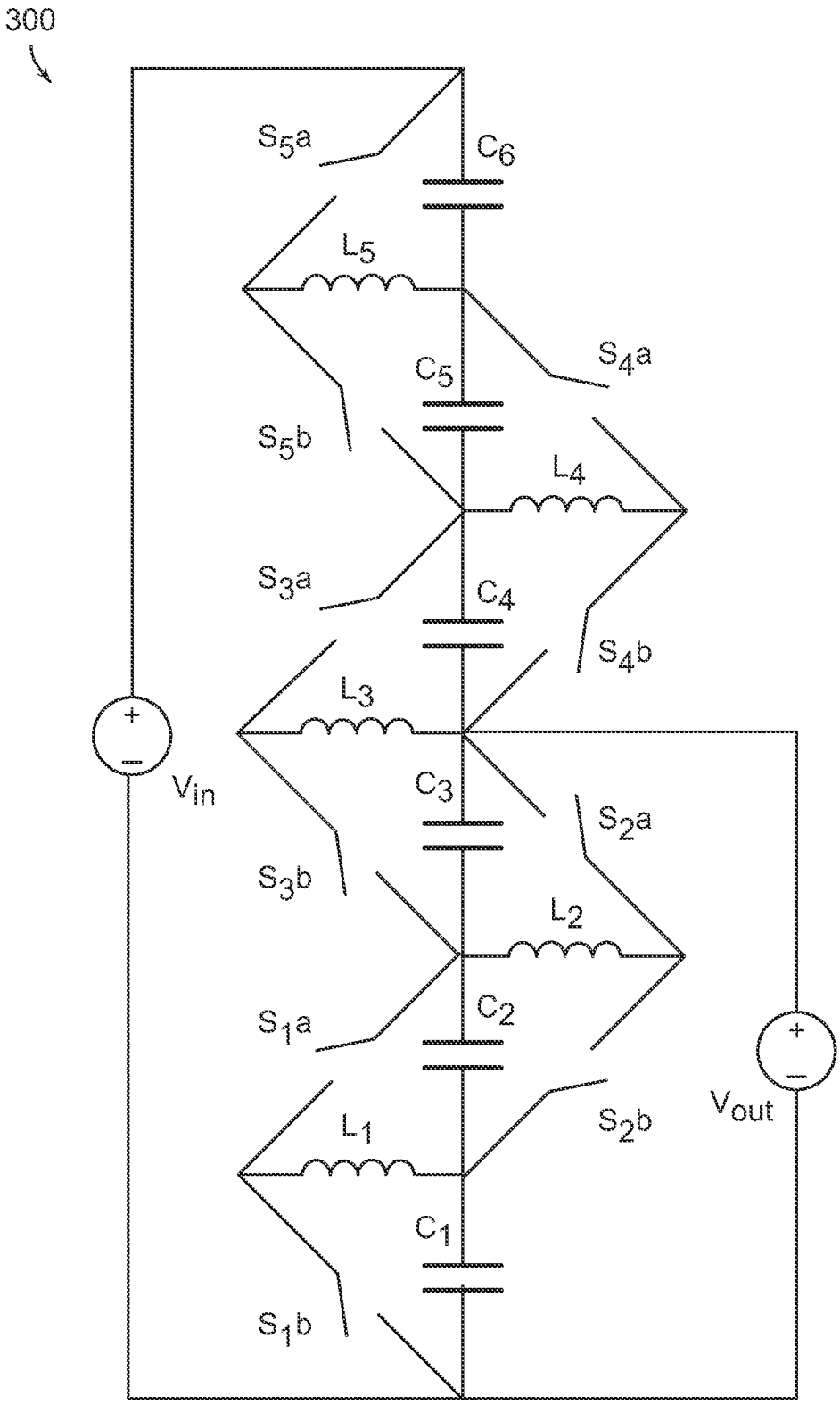
300
S_5a
C_6
L_5
S_4a
C_5
S_5b
L_4
S_3a
C_4
S_4b
L_3
V_{in}
C_3
S_2a
S_3b
L_2
S_1a
C_2
V_{out}
L_1
S_2b
C_1
S_1b

FIG. 3

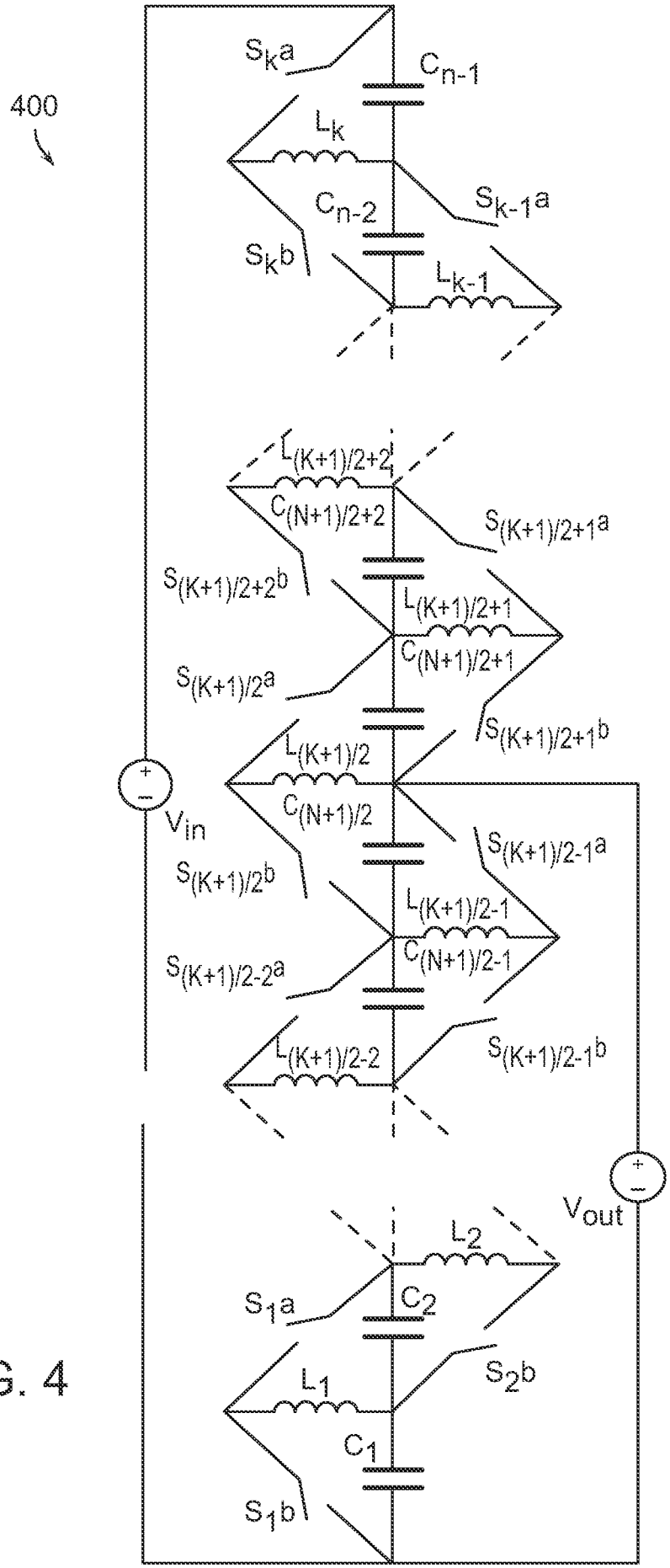
400
S_k^a
C_{n-1}
L_k
C_{n-2}
S_{k-1}^a
S_k^b
L_{k-1}
$L_{(K+1)/2+2}$
$C_{(N+1)/2+2}$
$S_{(K+1)/2+1}^a$
$S_{(K+1)/2+2}^b$
$L_{(K+1)/2+1}$
$C_{(N+1)/2+1}$
$S_{(K+1)/2}^a$
$S_{(K+1)/2+1}^b$
$L_{(K+1)/2}$
$C_{(N+1)/2}$
V_{in}
$S_{(K+1)/2-1}^a$
$S_{(K+1)/2}^b$
$L_{(K+1)/2-1}$
$C_{(N+1)/2-1}$
$S_{(K+1)/2-2}^a$
$L_{(K+1)/2-2}$
$S_{(K+1)/2-1}^b$
V_{out}
L_2
S_1^a
C_2
L_1
S_2^b
C_1
S_1^b

FIG. 4

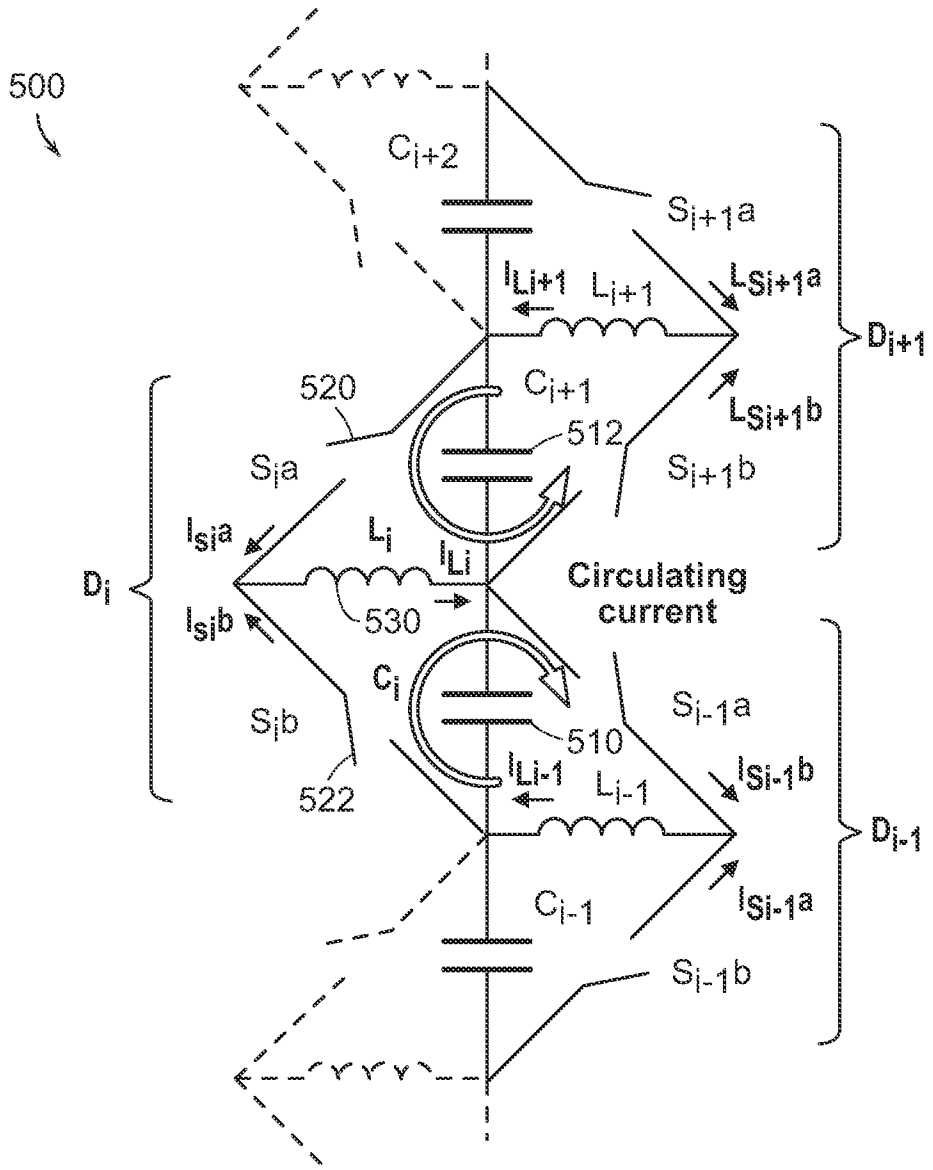
500
C_{i+2}
$S_{i+1}a$
I_{Li+1}
L_{i+1}
$L_{Si+1}a$
D_{i+1}
520
C_{i+1}
512
$L_{Si+1}b$
$S_{i+1}b$
$S_i a$
$I_{Si}a$
L_i
I_{Li}
D_i
Circulating current
$I_{Si}b$
530
C_i
$S_{i-1}a$
$S_i b$
510
I_{Li-1}
L_{i-1}
$I_{Si-1}b$
D_{i-1}
522
C_{i-1}
$I_{Si-1}a$
$S_{i-1}b$

FIG. 5

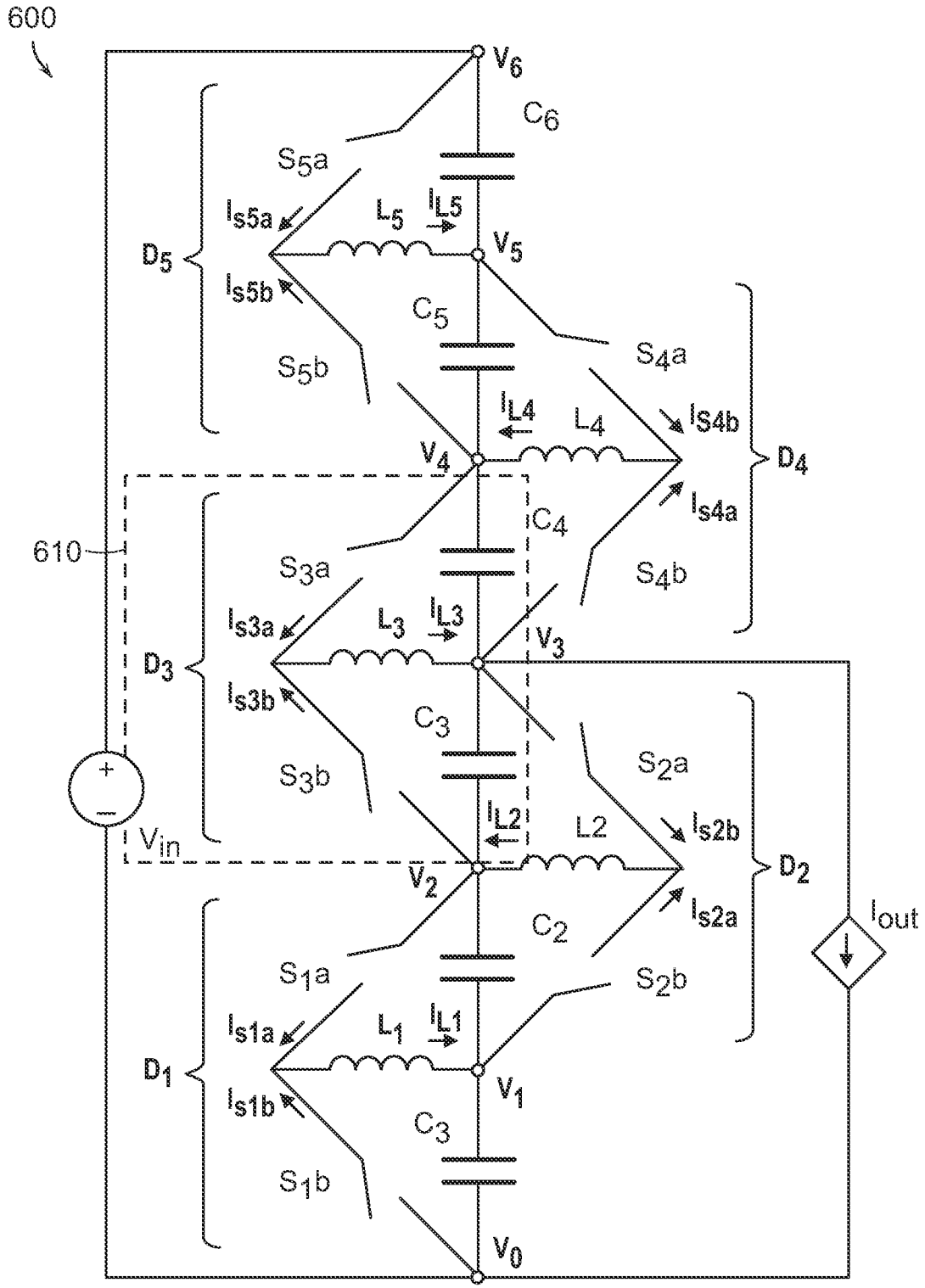
600
610
V_6
C_6
S_5a
I_{s5a}
L_5
I_{L5}
V_5
D_5
I_{s5b}
C_5
S_5b
S_4a
I_{L4}
L_4
I_{S4b}
V_4
D_4
I_{s4a}
C_4
S_3a
S_4b
I_{s3a}
L_3
I_{L3}
V_3
D_3
I_{s3b}
C_3
S_2a
S_3b
I_{L2}
$L2$
I_{s2b}
V_{in}
V_2
D_2
I_{s2a}
I_{out}
C_2
S_1a
S_2b
I_{s1a}
L_1
I_{L1}
D_1
V_1
I_{s1b}
C_3
S_1b
V_0

FIG. 6

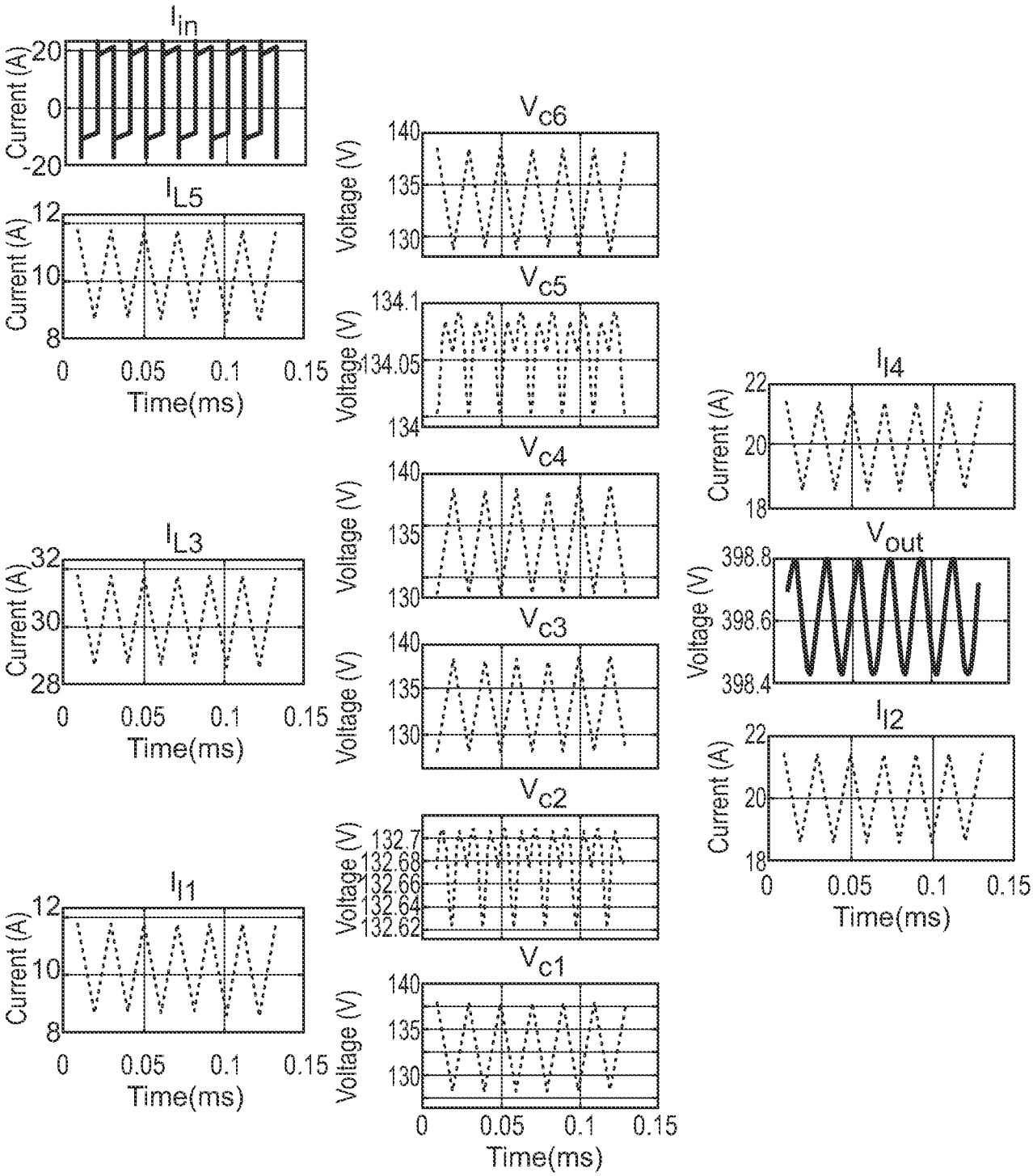
I_{in}
Current (A)
20
0
-20
I_{L5}
12
10
8
0
0.05
0.1
0.15
Time(ms)
I_{L3}
32
30
28
I_{l1}
V_{c6}
140
135
130
Voltage (V)
V_{c5}
134.1
134.05
134
V_{c4}
V_{c3}
V_{c2}
132.7
132.68
132.66
132.64
132.62
V_{c1}
I_{l4}
22
20
18
V_{out}
398.8
398.6
398.4
I_{l2}

FIG. 7

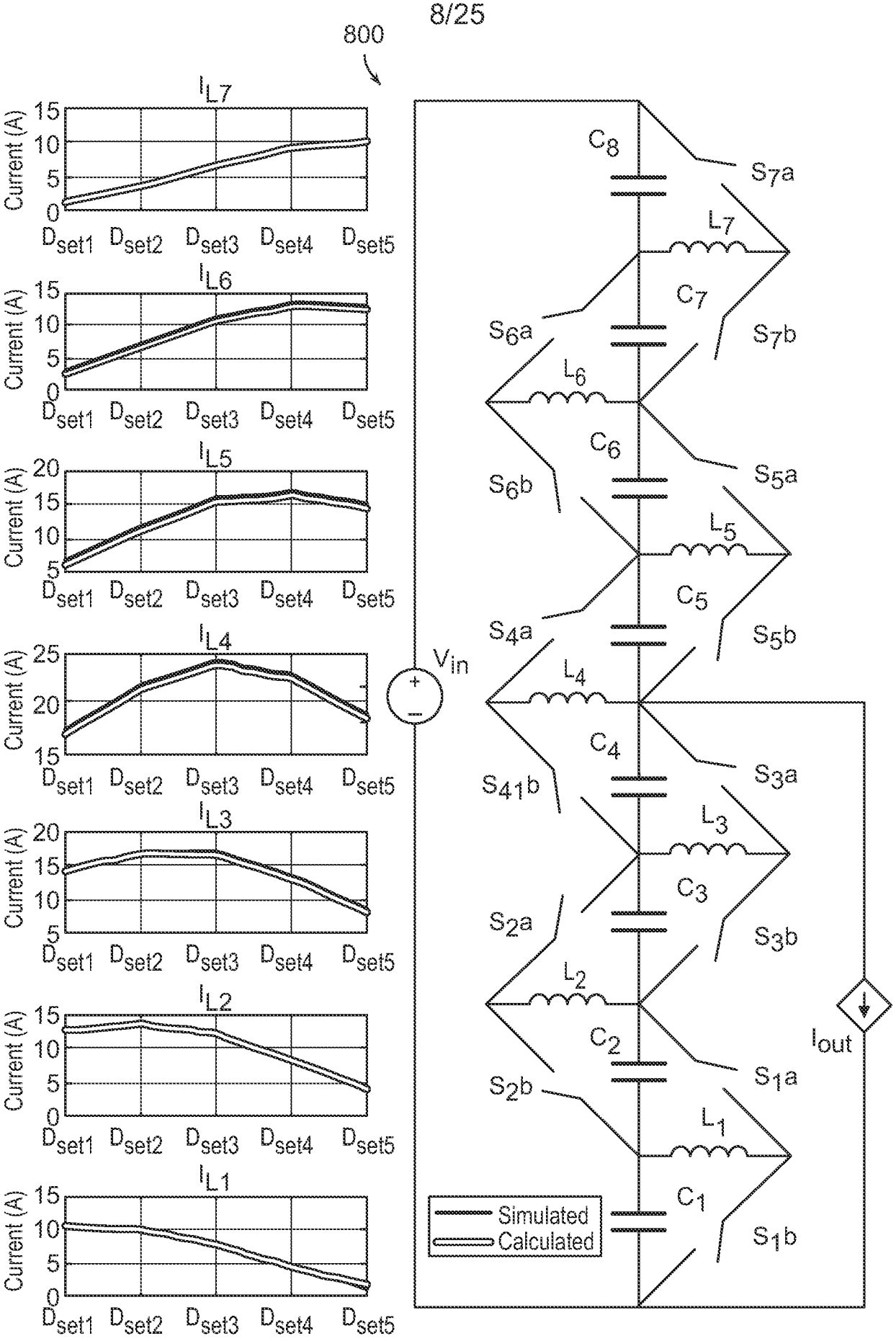
800
I_{L7}
I_{L6}
I_{L5}
I_{L4}
I_{L3}
I_{L2}
I_{L1}
Current (A)
D_{set1} D_{set2} D_{set3} D_{set4} D_{set5}
C_8
C_7
C_6
C_5
C_4
C_3
C_2
C_1
L_7
L_6
L_5
L_4
L_3
L_2
L_1
S_7a
S_7b
S_6a
S_6b
S_5a
S_5b
S_4a
$S_{41}b$
S_3a
S_3b
S_2a
S_2b
S_1a
S_1b
V_{in}
I_{out}
Simulated
Calculated

FIG. 8

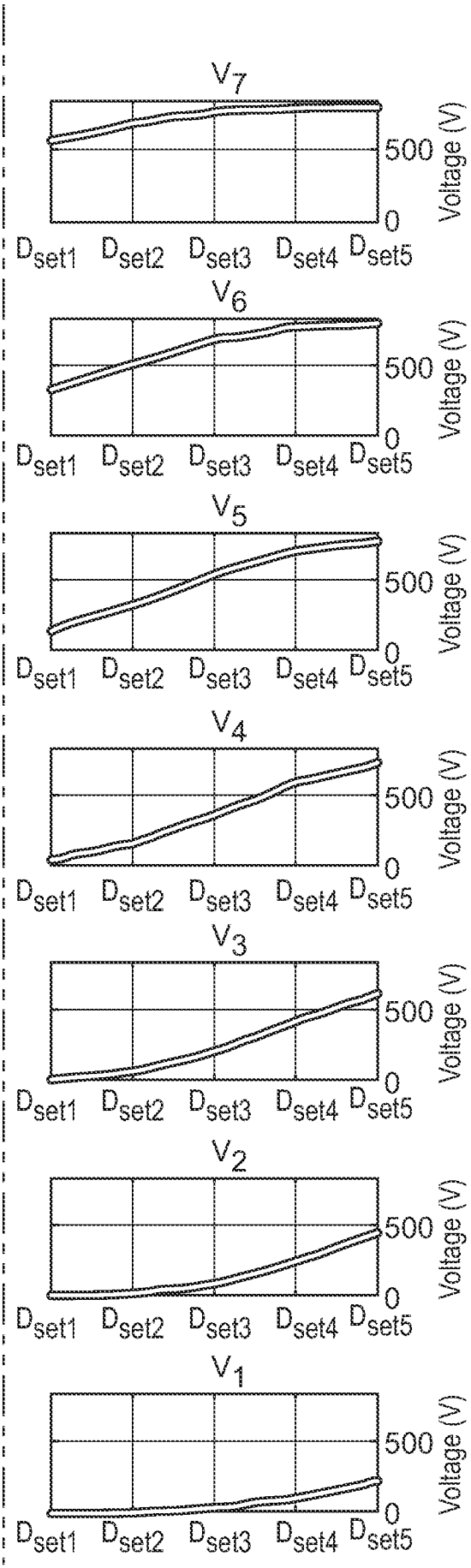
V7
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V6
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V5
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V4
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V3
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V2
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5
V1
500
0
Voltage (V)
Dset1 Dset2 Dset3 Dset4 Dset5

FIG. 8 (cont.)

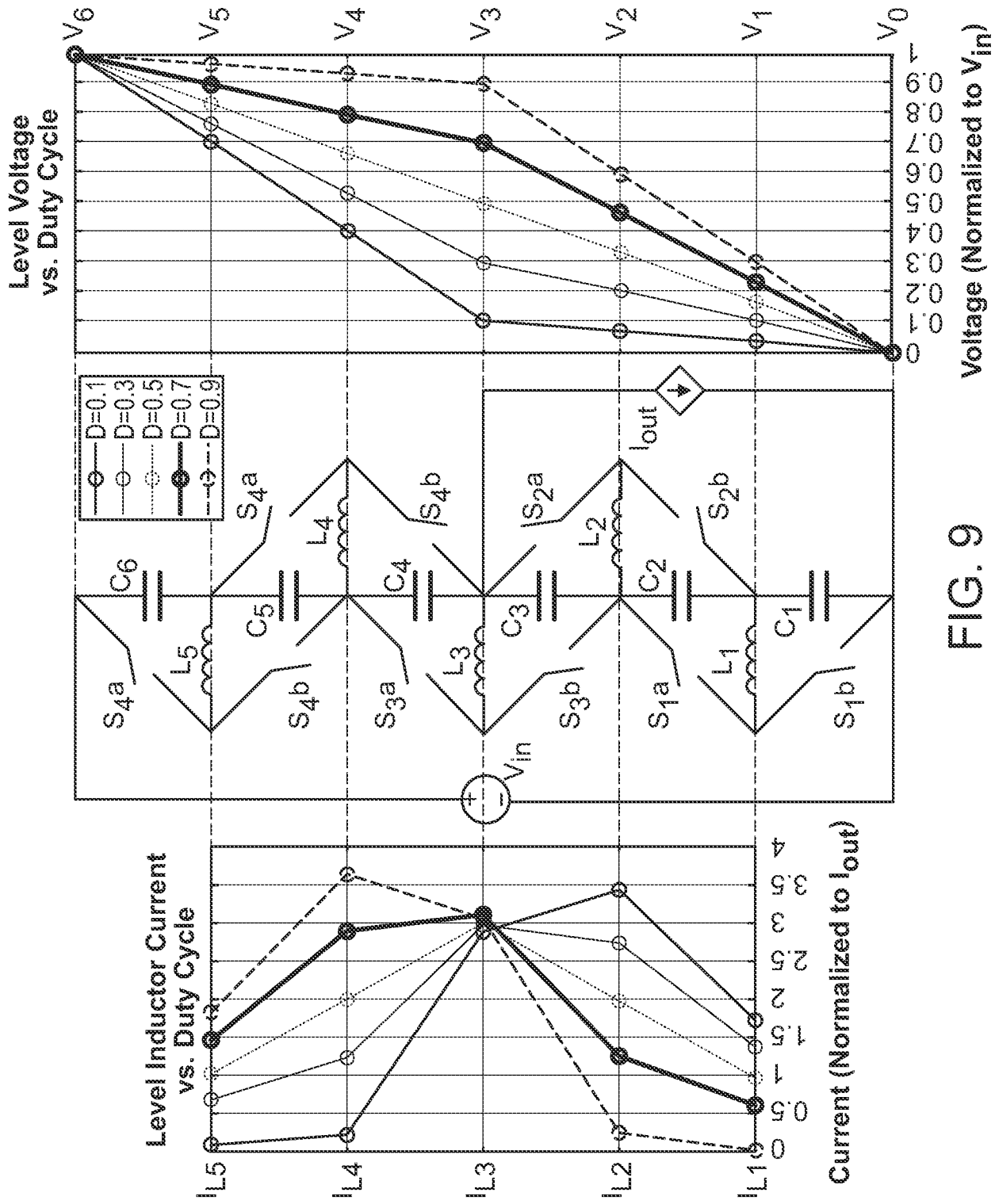
Level Voltage
vs. Duty Cycle
V6
V5
V4
V3
V2
V1
V0
Voltage (Normalized to Vin)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
D=0.1
D=0.3
D=0.5
D=0.7
D=0.9
S4a
S4b
S3a
S3b
S2a
S2b
S1a
S1b
L5
L4
L3
L2
L1
C6
C5
C4
C3
C2
C1
Vin
Iout
Level Inductor Current
vs. Duty Cycle
IL5
IL4
IL3
IL2
IL1
Current (Normalized to Iout)
0
0.5
1
1.5
2
2.5
3
3.5
4

FIG. 9

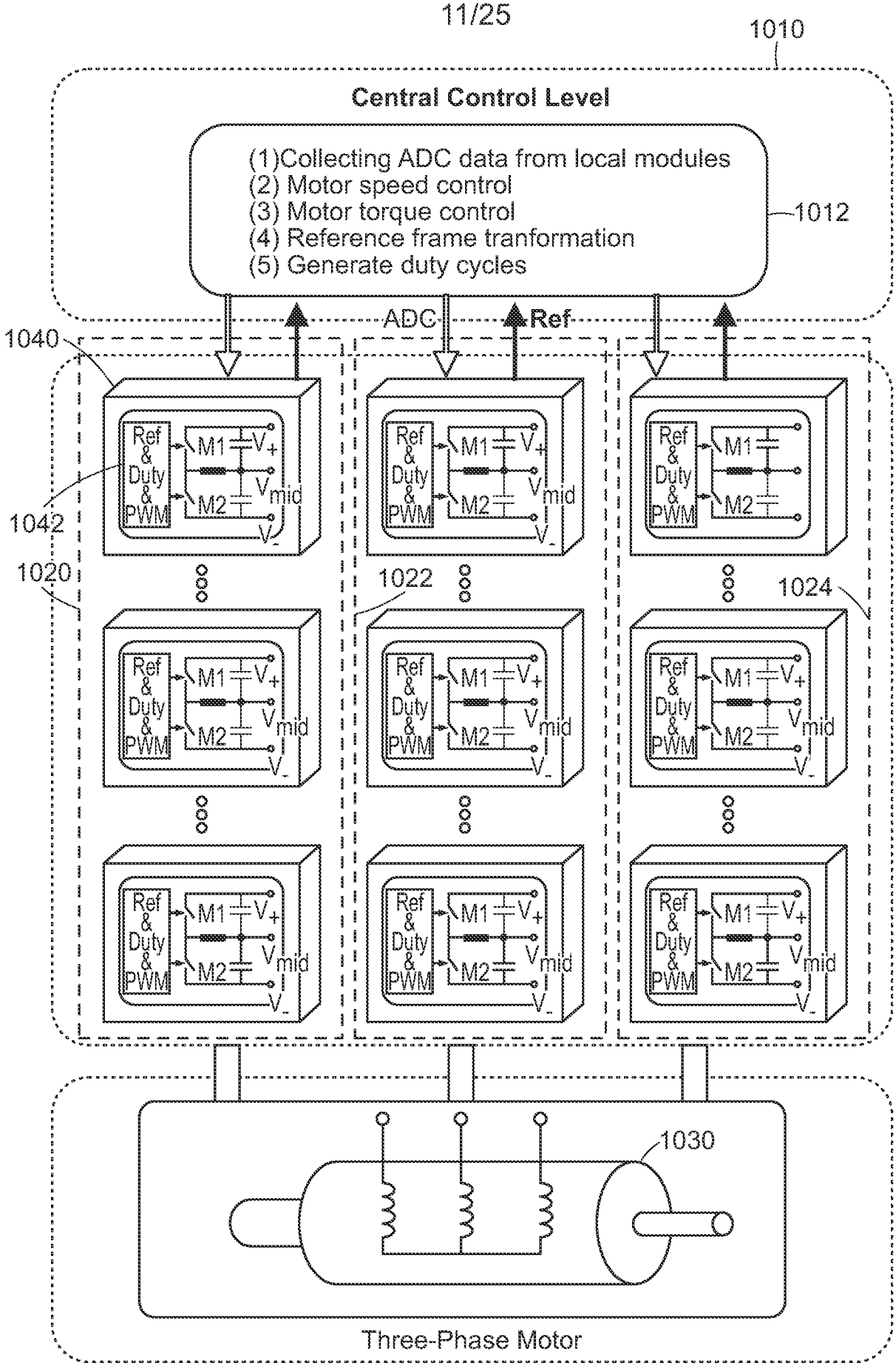
1010
Central Control Level
(1)Collecting ADC data from local modules
(2) Motor speed control
(3) Motor torque control
(4) Reference frame tranformation
(5) Generate duty cycles
1012
ADC
Ref
1040
1042
1020
1022
1024
Ref & Duty & PWM
M1
M2
V+
Vmid
V-
1030
Three-Phase Motor

FIG. 10

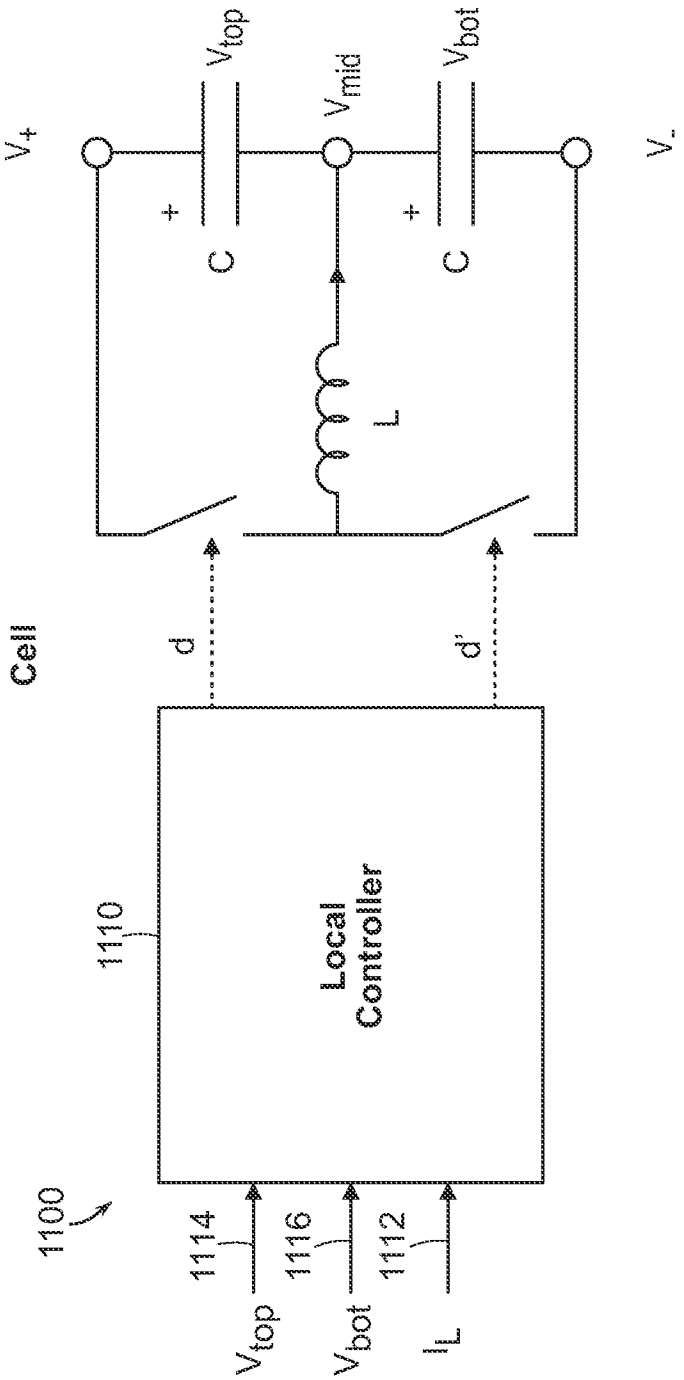
V+
V_top
V_mid
V_bot
V-
+
C
+
C
L
Cell
d
d'
1110
Local Controller
1100
1114
1116
1112
V_top
V_bot
I_L

FIG. 11

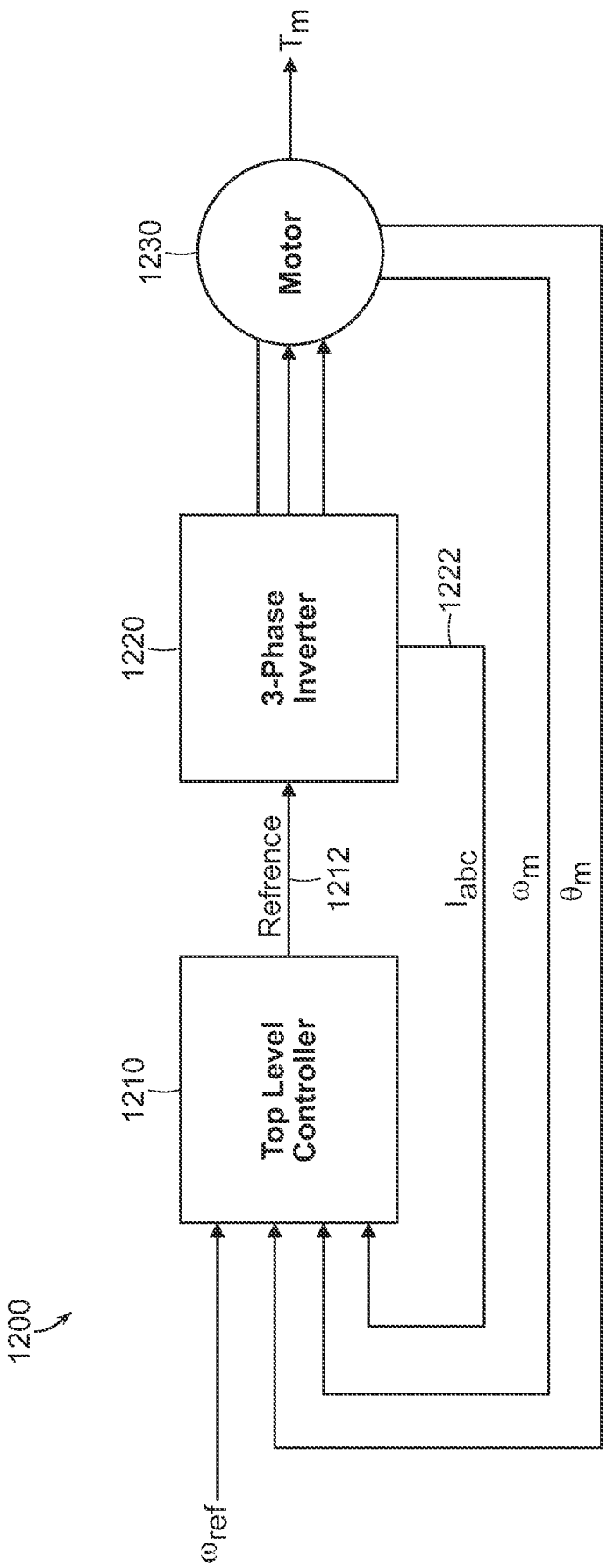
1200
1210
Top Level Controller
1212
Refrence
1220
3-Phase Inverter
1222
1230
Motor
T_m
ω_{ref}
I_{abc}
ω_m
θ_m

FIG. 12

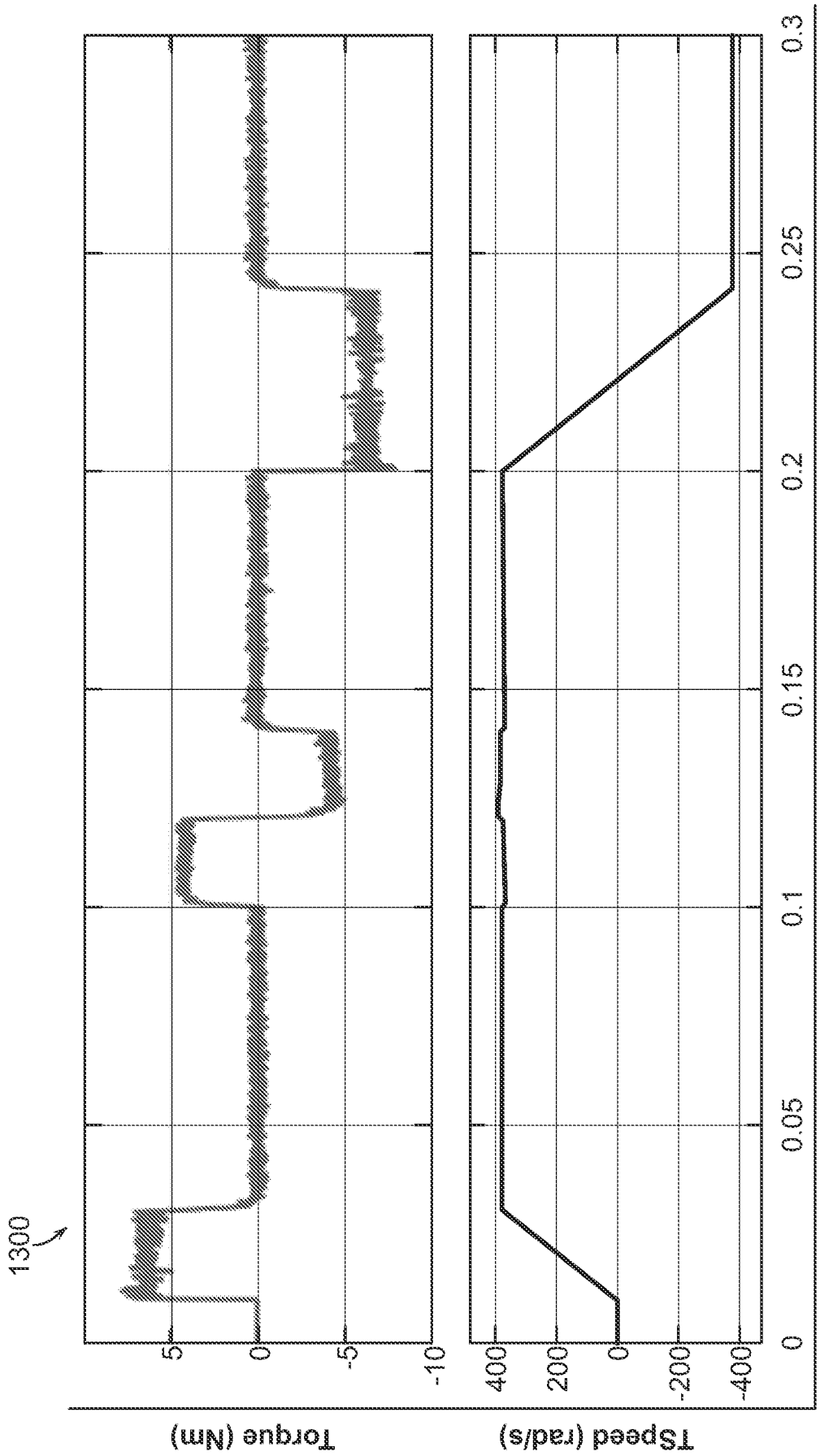
1300
1310
Torque (Nm)
TSpeed (rad/s)
Time (s)
5
0
-5
-10
400
200
0
-200
-400
0
0.05
0.1
0.15
0.2
0.25
0.3

FIG. 13

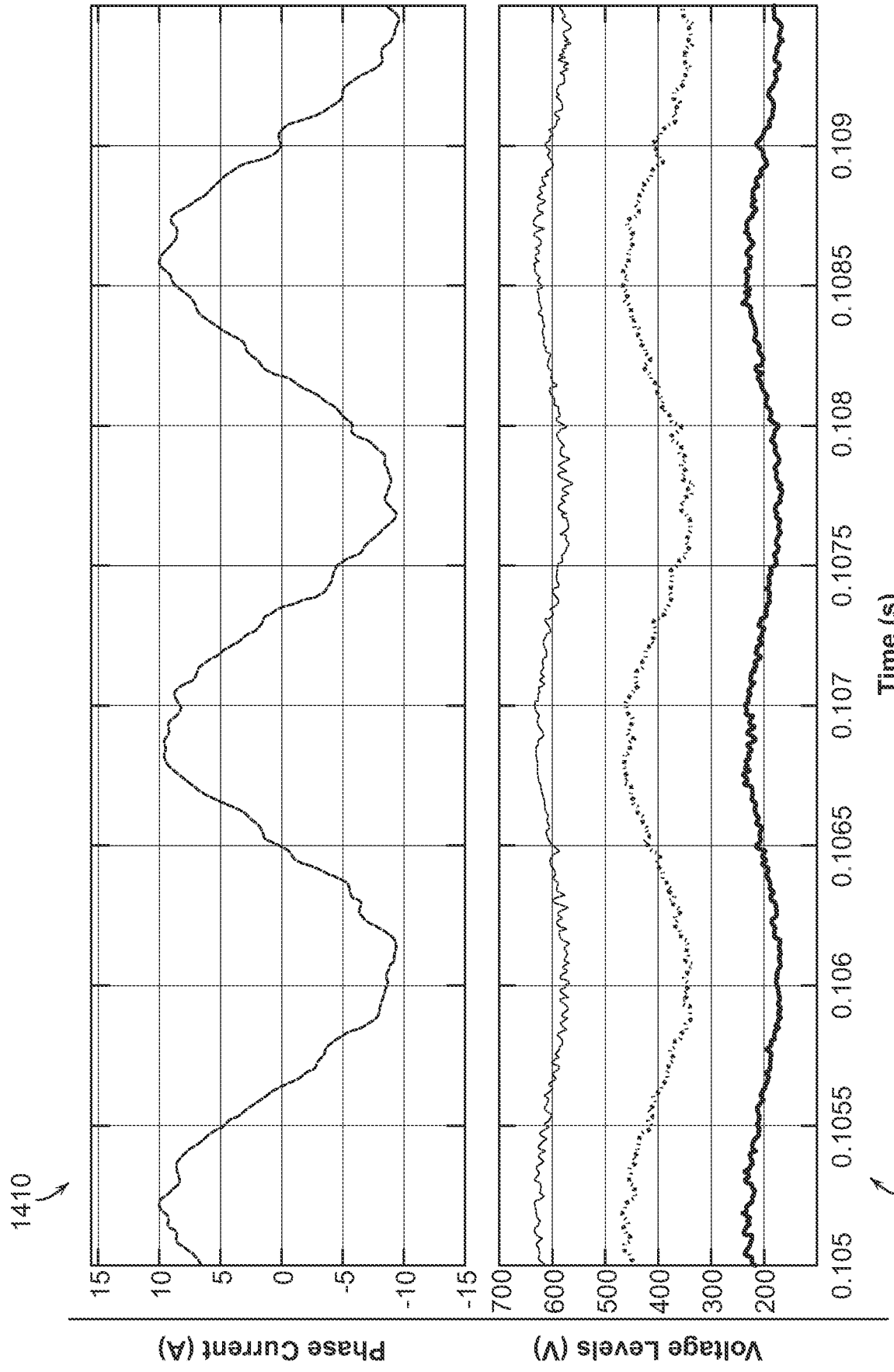
1410
1400
Phase Current (A)
Voltage Levels (V)
Time (s)
15
10
5
0
-5
-10
-15
700
600
500
400
300
200
0.105
0.1055
0.106
0.1065
0.107
0.1075
0.108
0.1085
0.109

FIG. 14

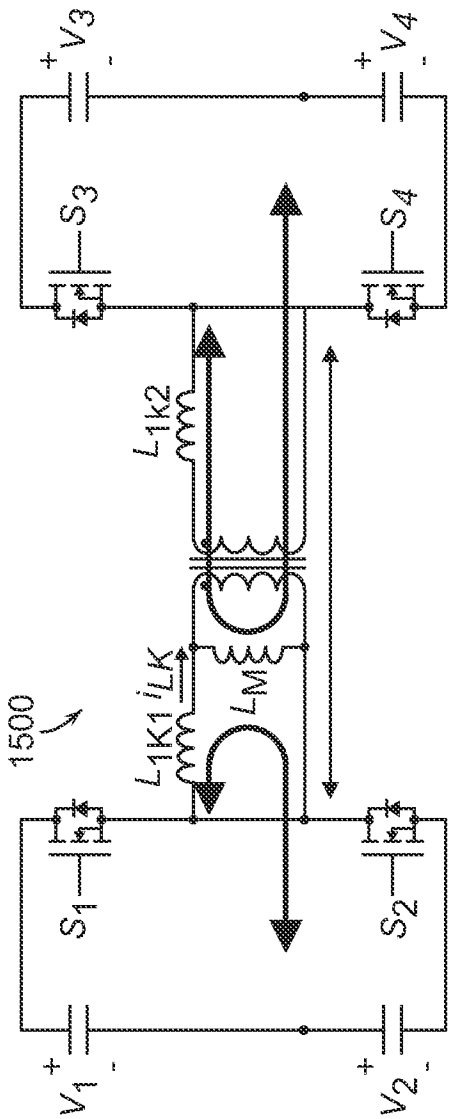

FIG. 15A

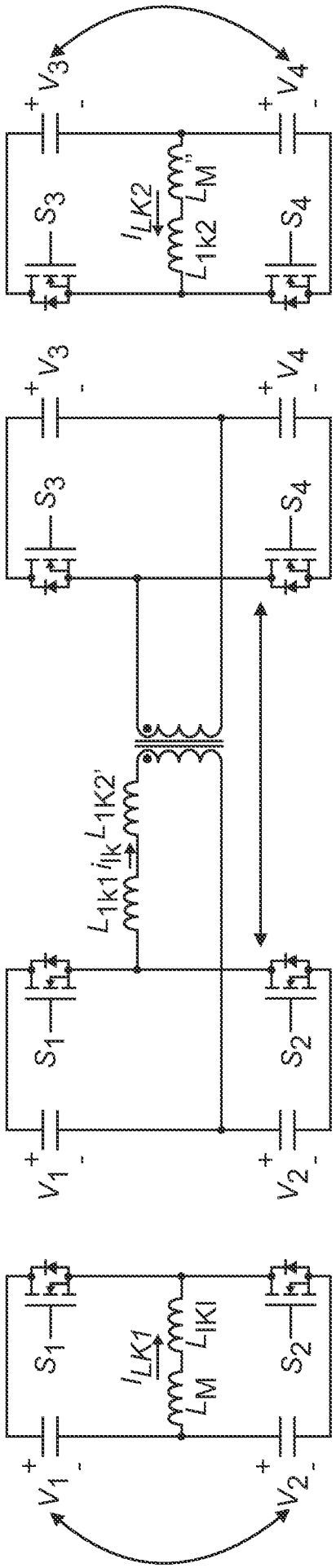

FIG. 15B

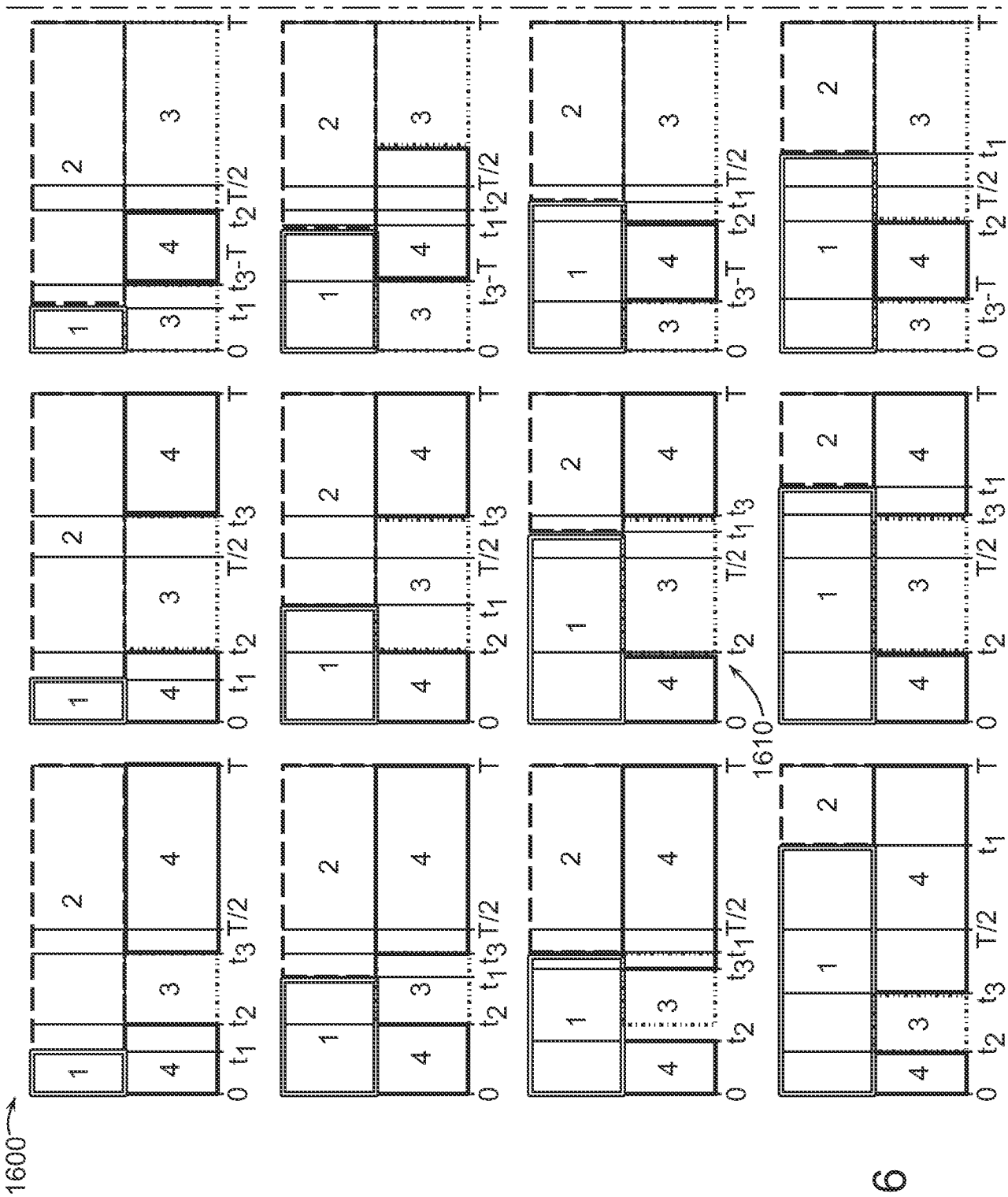

FIG. 16

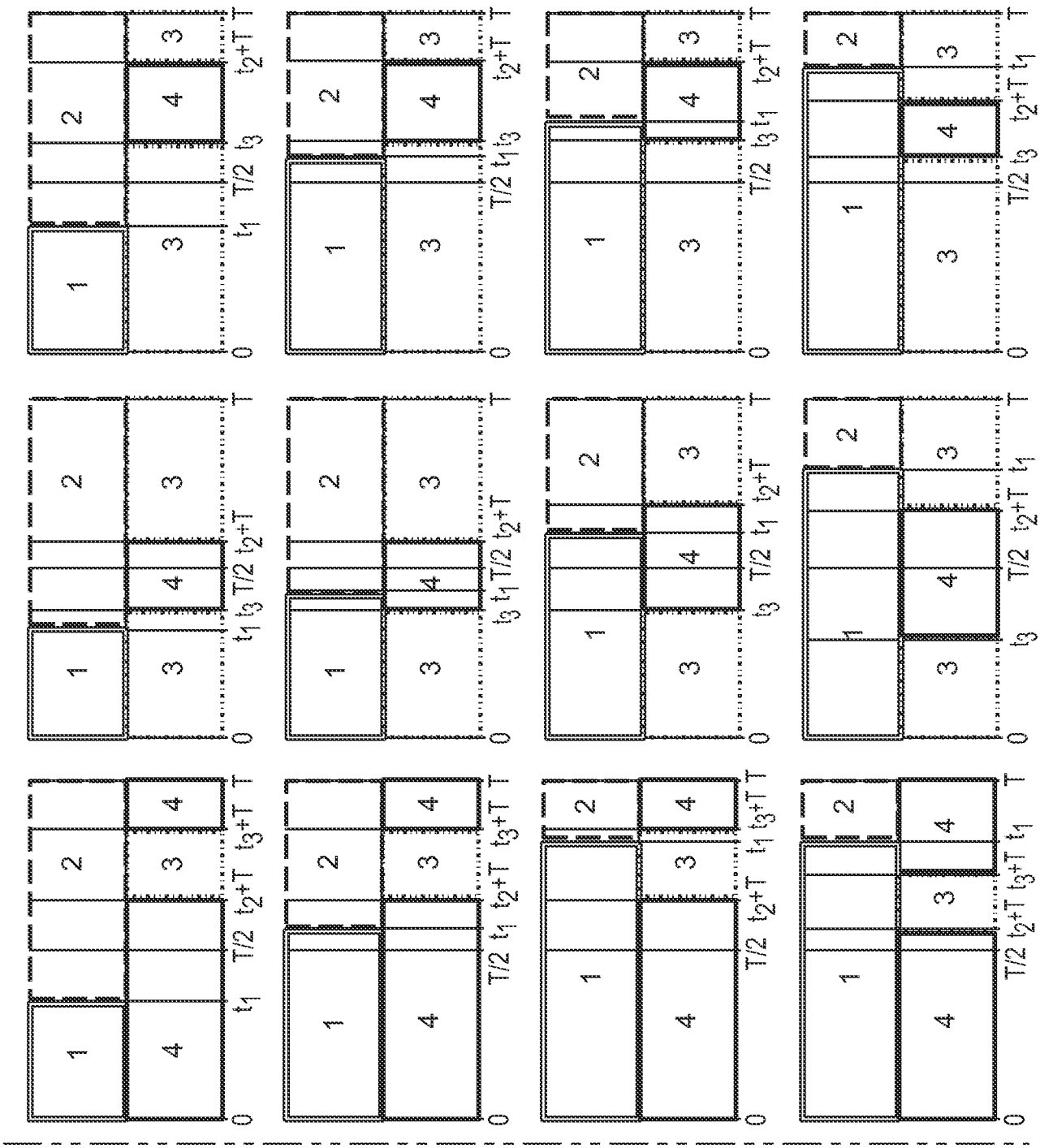

FIG. 16 (cont.)

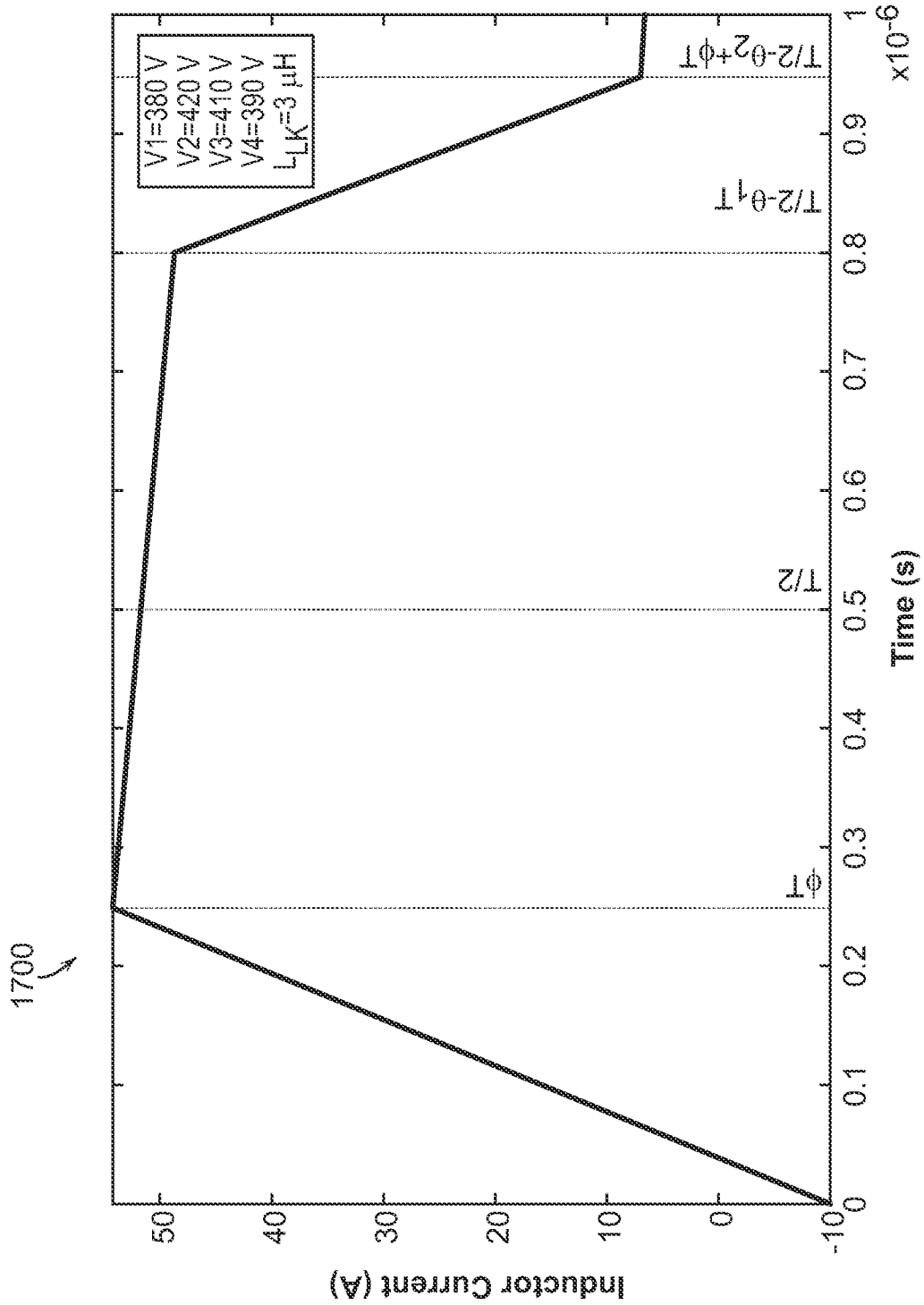
1700
V1=380 V
V2=420 V
V3=410 V
V4=390 V
L_{LK}=3 μH
ϕT
T/2
$T/2-\theta_1 T$
$T/2-\theta_2+\phi T$
Inductor Current (A)
Time (s)
$\times 10^{-6}$

FIG. 17

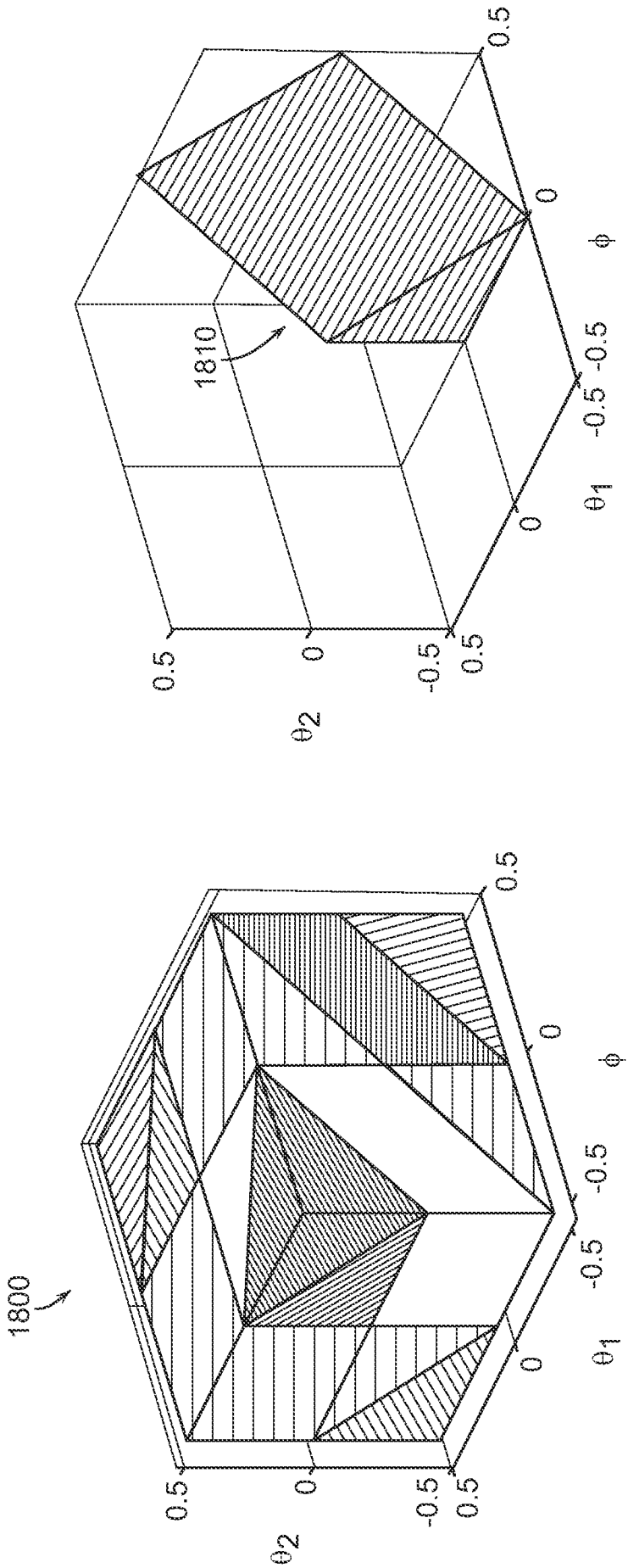

FIG. 18

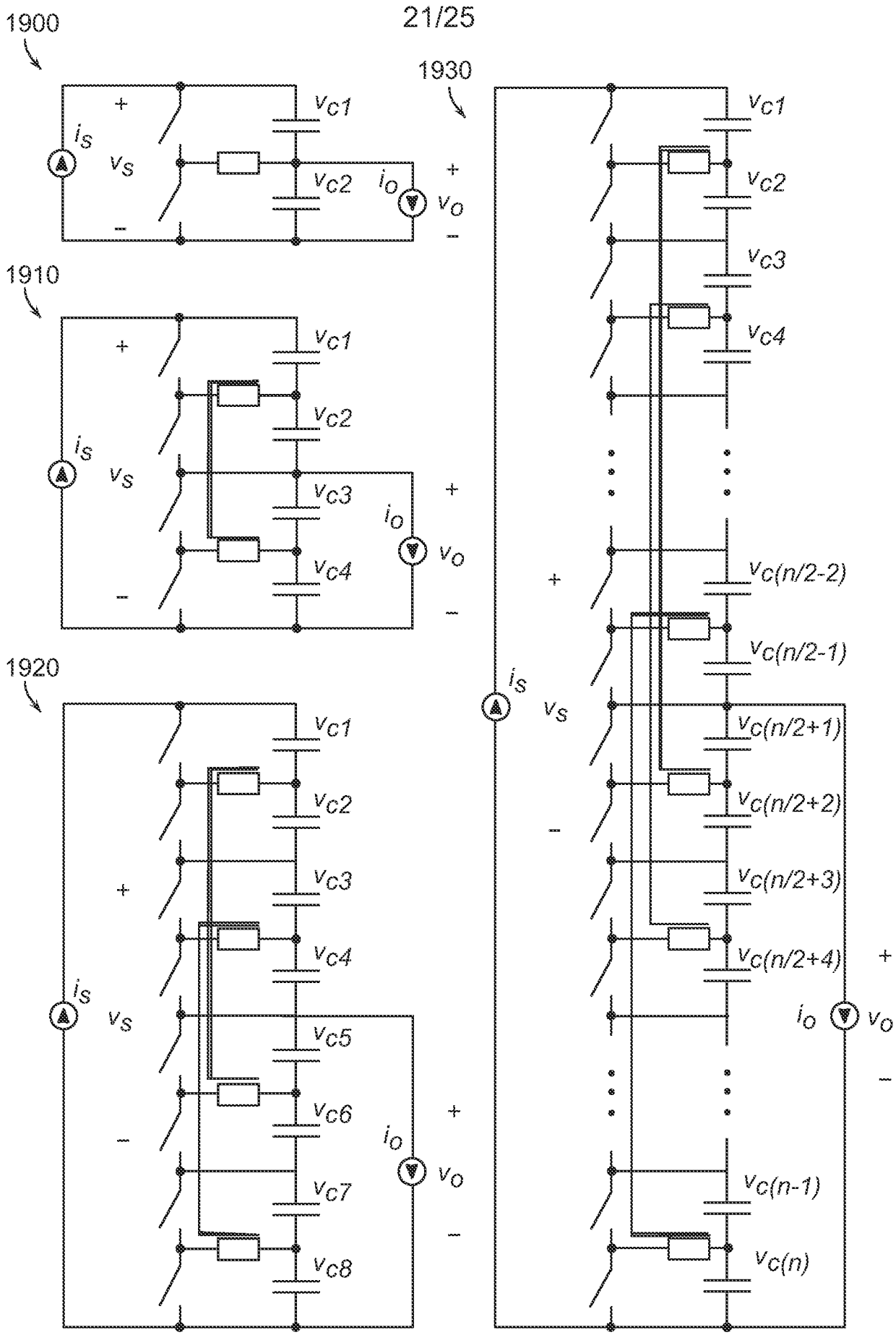
1900
1910
1920
1930
v_{c1}
v_{c2}
v_{c3}
v_{c4}
v_{c5}
v_{c6}
v_{c7}
v_{c8}
$v_{c(n/2-2)}$
$v_{c(n/2-1)}$
$v_{c(n/2+1)}$
$v_{c(n/2+2)}$
$v_{c(n/2+3)}$
$v_{c(n/2+4)}$
$v_{c(n-1)}$
$v_{c(n)}$
i_s
v_s
i_o
v_o
+
–

FIG. 19

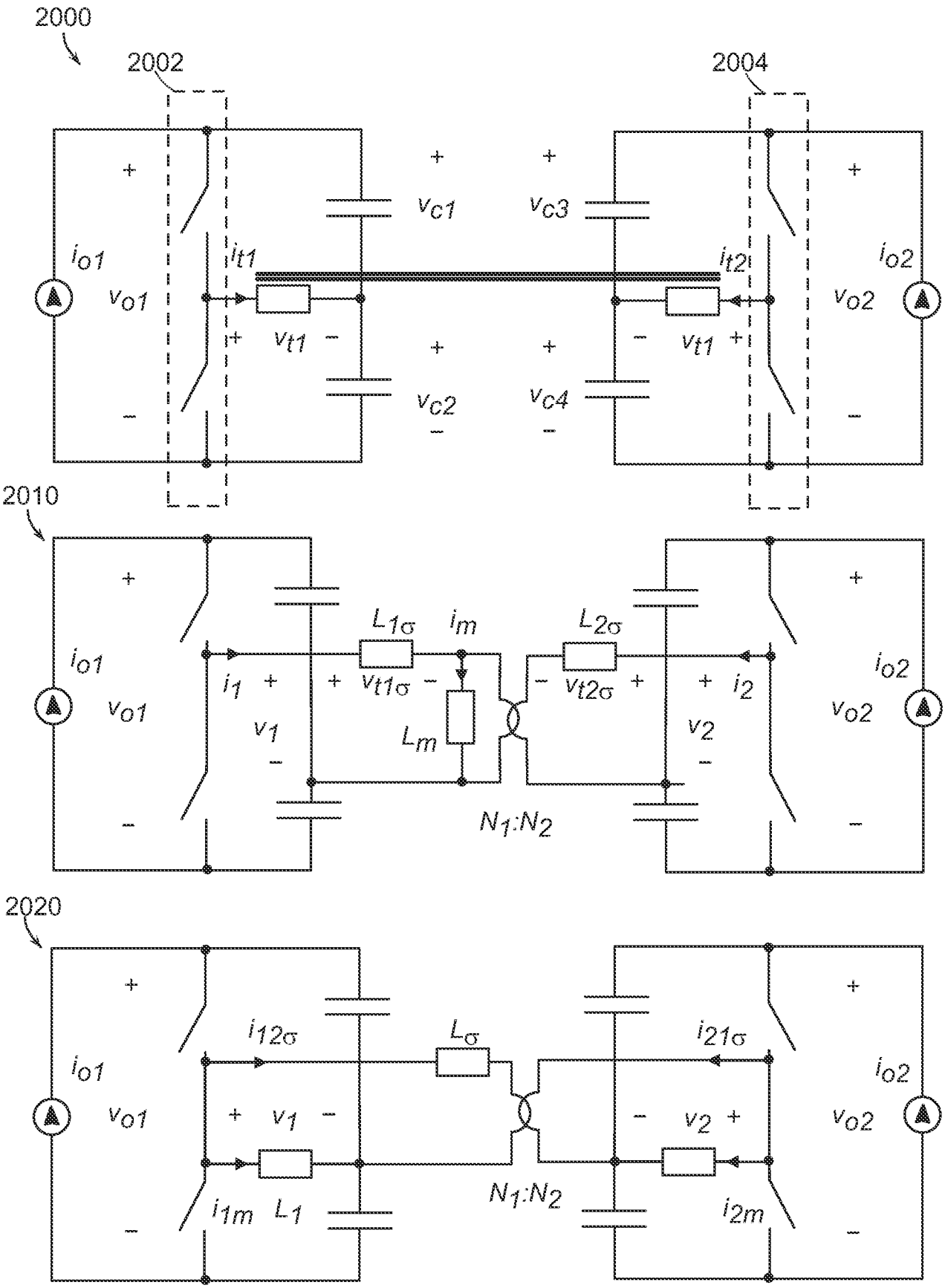
2000
2002
2004
v_{c1}
v_{c3}
i_{o1}
i_{t1}
i_{t2}
i_{o2}
v_{o1}
v_{t1}
v_{t1}
v_{o2}
v_{c2}
v_{c4}
2010
$L_{1\sigma}$
i_m
$L_{2\sigma}$
i_{o1}
i_{o2}
i_1
$v_{t1\sigma}$
$v_{t2\sigma}$
i_2
v_{o1}
v_{o2}
v_1
L_m
v_2
$N_1:N_2$
2020
$i_{12\sigma}$
L_σ
$i_{21\sigma}$
i_{o1}
i_{o2}
v_{o1}
v_1
v_2
v_{o2}
$N_1:N_2$
i_{1m}
L_1
i_{2m}

FIG. 20

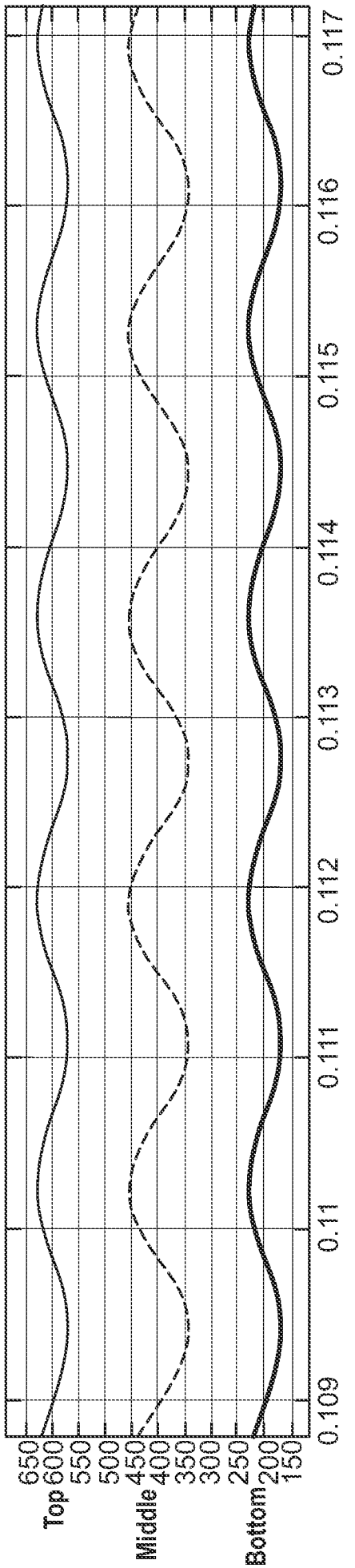
Top
Middle
Bottom
650
600
550
500
450
400
350
300
250
200
150
0.109
0.11
0.111
0.112
0.113
0.114
0.115
0.116
0.117

FIG. 21A

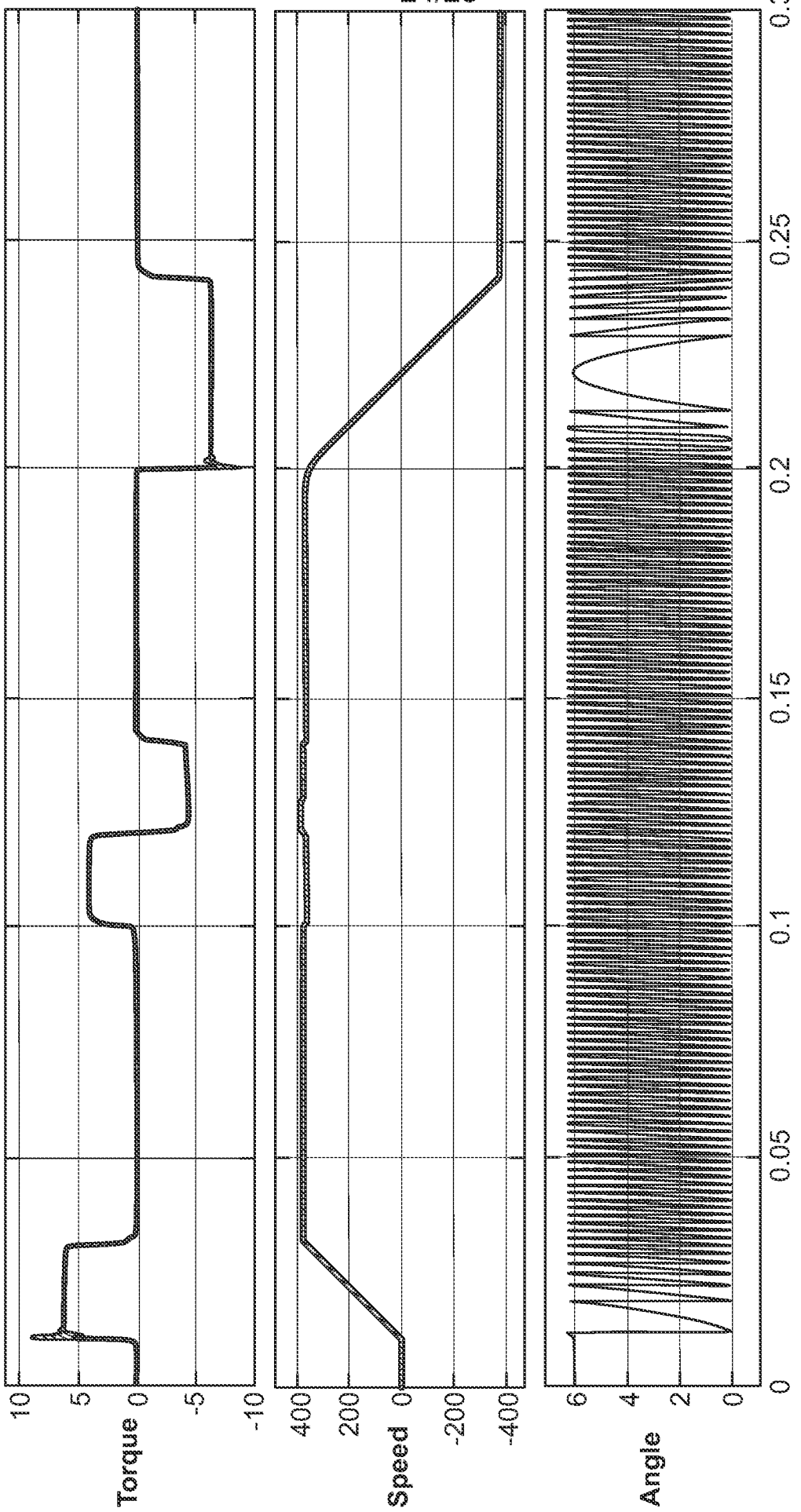
Torque
10
5
0
-5
-10
Speed
400
200
0
-200
-400
Angle
6
4
2
0
0
0.05
0.1
0.15
0.2
0.25
0.3

FIG. 21B

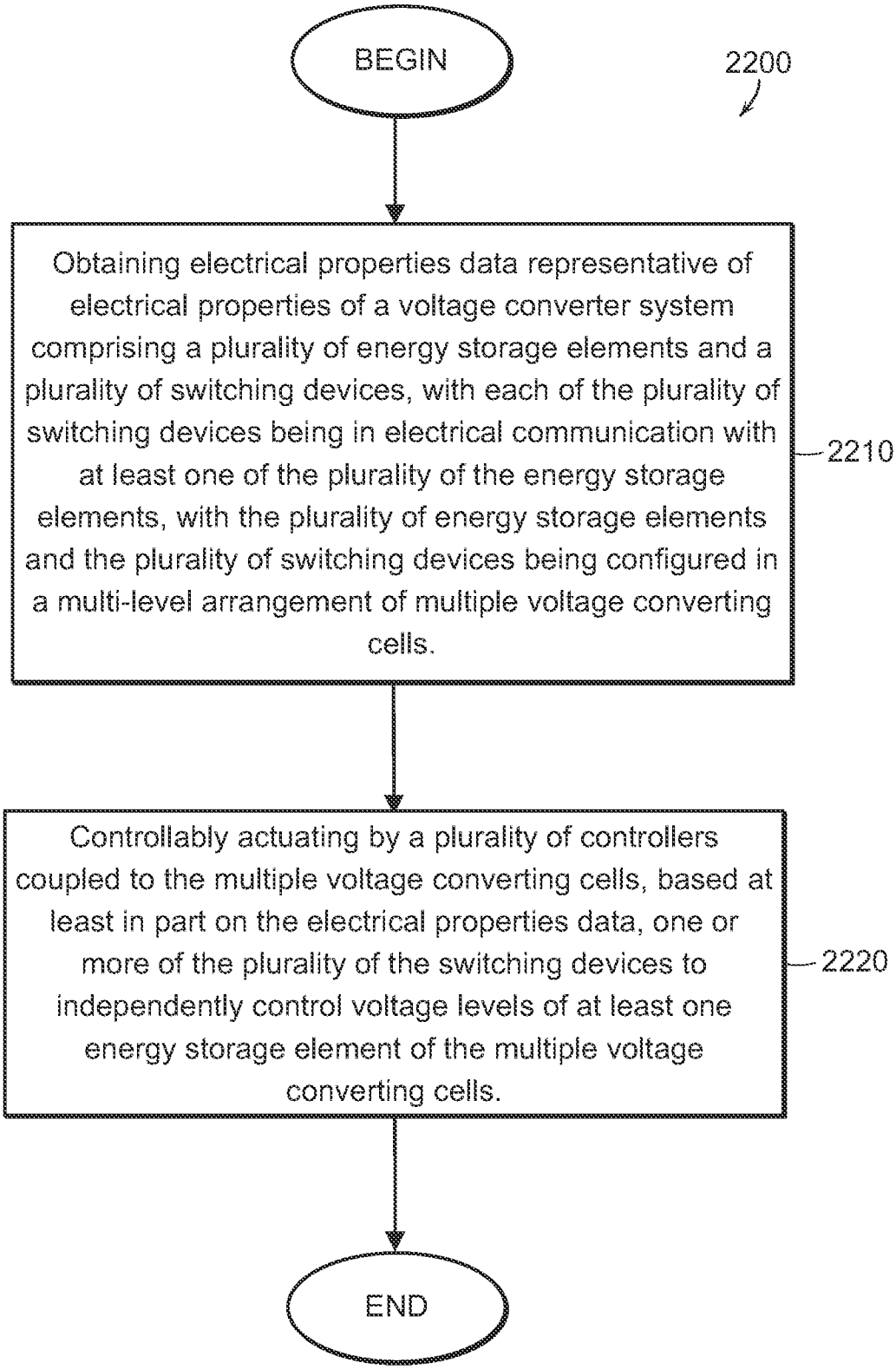
BEGIN
2200
Obtaining electrical properties data representative of electrical properties of a voltage converter system comprising a plurality of energy storage elements and a plurality of switching devices, with each of the plurality of switching devices being in electrical communication with at least one of the plurality of the energy storage elements, with the plurality of energy storage elements and the plurality of switching devices being configured in a multi-level arrangement of multiple voltage converting cells.
2210
Controllably actuating by a plurality of controllers coupled to the multiple voltage converting cells, based at least in part on the electrical properties data, one or more of the plurality of the switching devices to independently control voltage levels of at least one energy storage element of the multiple voltage converting cells.
2220
END

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US22/18940

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H02M 3/16; H02M 3/02; H02M 7/483 (2022.01)

CPC - H02M 3/1582; H02M 7/483; H02M 3/16; H02M 3/02; H02M 7/4837

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y --- A	US 2014/0184189 A1 (SALEM, L) 03 July 2014; figure 9A, paragraphs [0042], [0053], [0054], [0074], [0093], [0094]-[0101], [0114]	1-8, 12-13, 16-17, 20-24, 28, 31, 34-45 --- 9-11, 14-15, 18-19, 25-27, 29-30, 32-33
Y	US 2010/0039080 A1 (SCHOENBAUER, S ET AL.) 18 February 2010; figure 1, paragraph [0014]	2, 21
Y	US 6,040,990 A (COURAULT, J) 21 March 2000; column 2, lines 58-59, column 5, lines 21-49, claim 1	3
Y	US 2014/0293667 A1 (GENERAL ELECTRIC COMPANY) 02 October 2014; claim 13	4, 22
Y --- A	US 2009/0085546 A1 (PHADKE, J ET AL.) 02 April 2009; claim 11	8, 24 --- 9-11, 25-27
Y --- A	US 5,027,264 A (DEDONCKER, R ET AL.) 25 June 1991; figures 4, 17, column 2, line 67-column 3, line 17, column 4, line 59-column 5, line 19	12, 13, 16, 28 --- 14, 15, 29, 30
Y --- A	US 2005/0084745 A1 (COLELLO, G ET AL.) 21 April 2005; paragraphs [0048]-[0053], [0067]-[0069]	17, 31, 34 --- 18, 19, 32, 33

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2022 (31.05.2022)	JUN 0 8 2022
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US22/18940

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 3,940,680 A (TADOKORO, T ET AL.) 24 February 1976; the entire document	1-35