United States Patent [19]

Lazecki

[11] **3,713,135**

[45] **Jan. 23, 1973**

[54] DIGITAL SYMBOL GENERATOR

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[22] Filed: **May 24, 1971**

[21] Appl. No.: **146,343**

[52] **U.S. Cl.** .....**340/324 A**, 315/22

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** .....340/324 A, 324 AD; 315/22

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[57] **ABSTRACT**

A digital symbol generator uses simple arithmetic operations performed by digital logic components to determine the raster lines on a cathode ray tube where it is desired to display video. Two arithmetic operations are performed digitally for each disjunctive segment of a symbol to predict whether or not a raster line about to be swept, or a part thereof, for which the operations were performed, is used in displaying the symbol.

1 Claim, 4 Drawing Figures

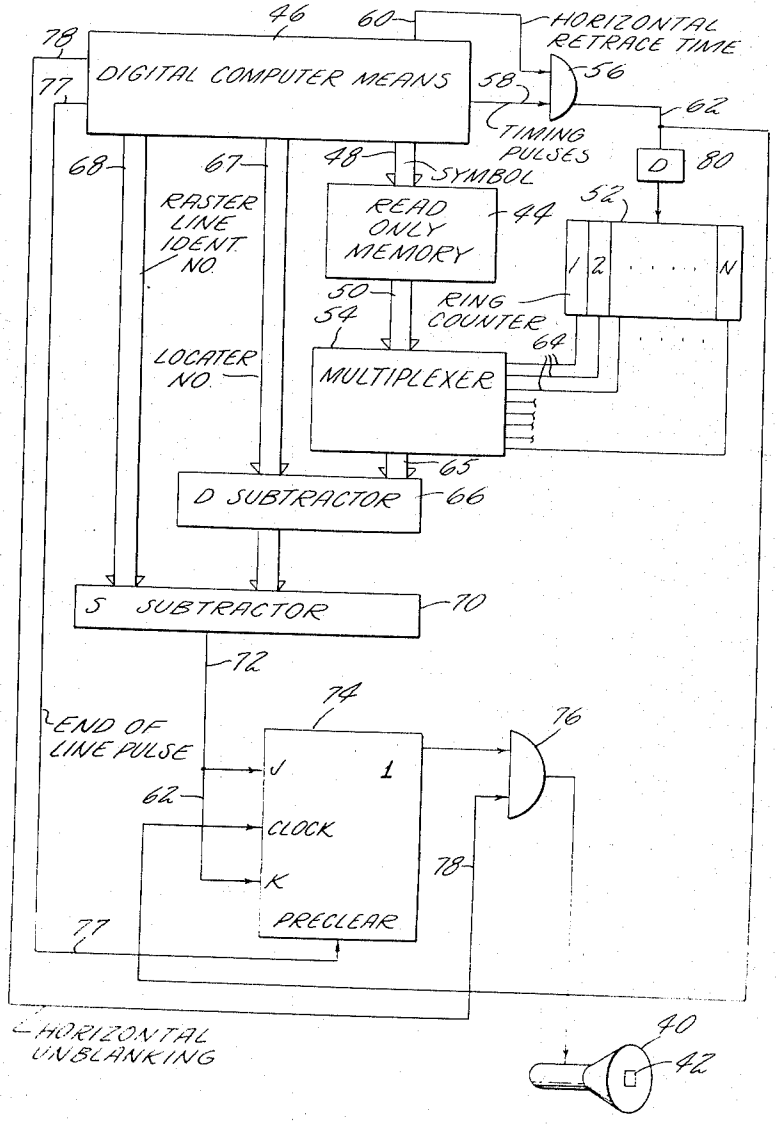
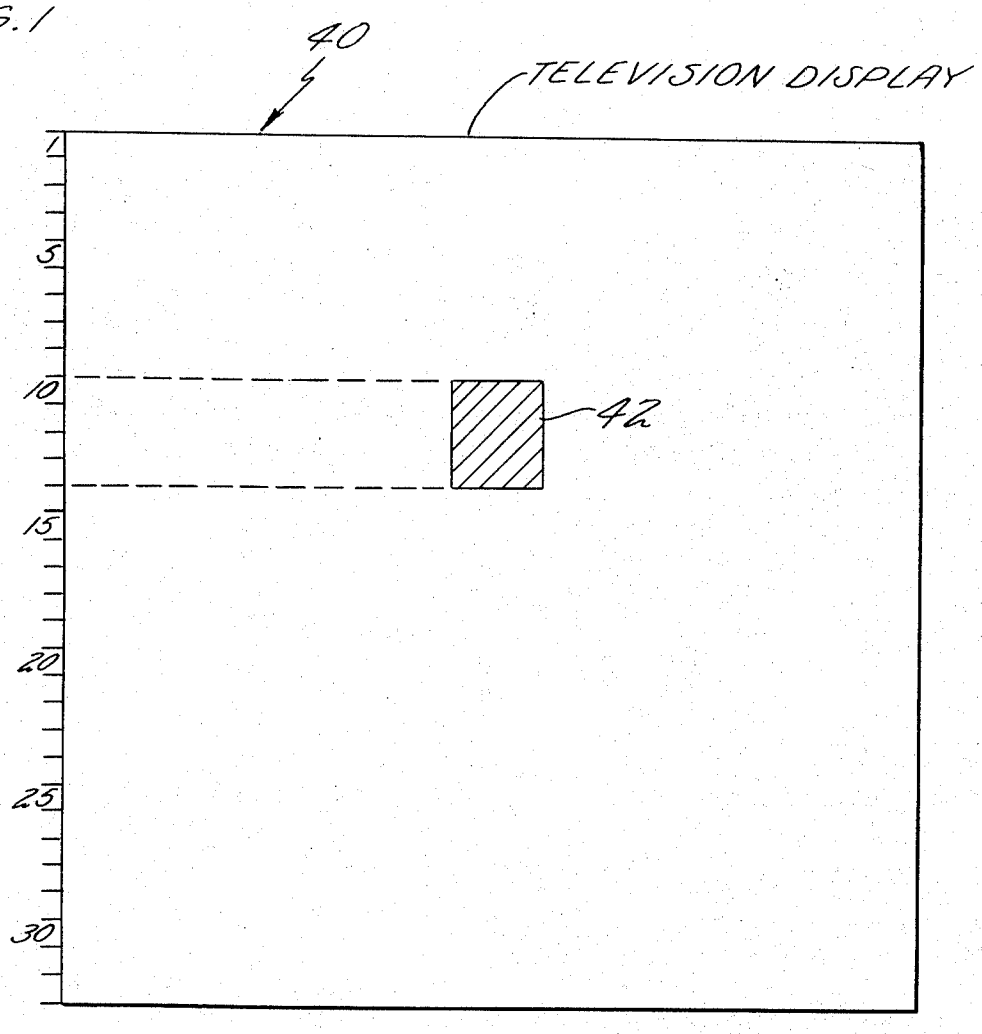


FIG. 1



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FIG. 2

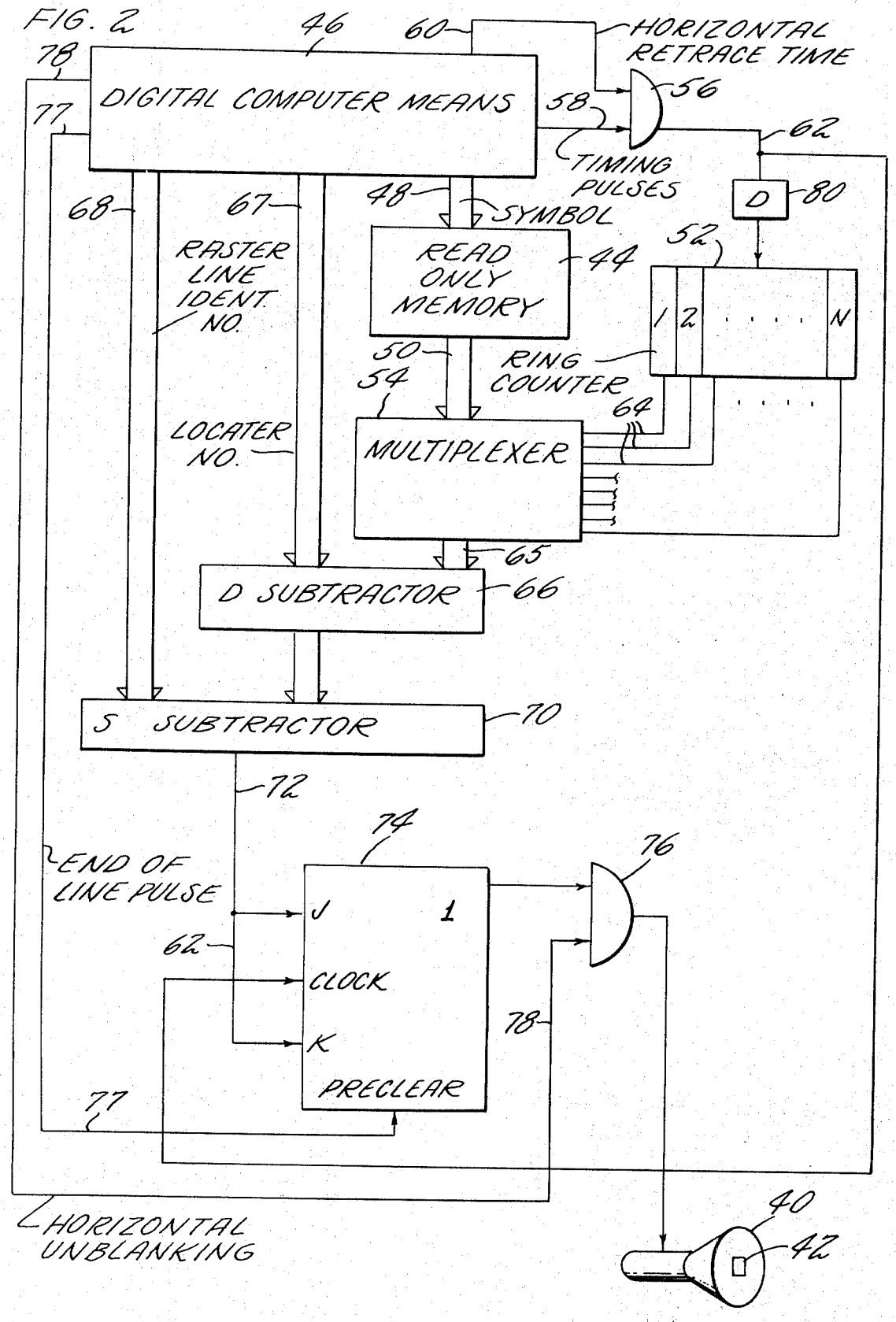

46
60
HORIZONTAL RETRACE TIME
78
DIGITAL COMPUTER MEANS
58
56
77
62
TIMING PULSES
D
80
68
67
48
SYMBOL
READ ONLY MEMORY
44
52
RASTER LINE IDENT. NO.
1
2
N
50
RING COUNTER
54
64
LOCATER NO.
MULTIPLEXER
65
D SUBTRACTOR
66
S SUBTRACTOR
70
72
74
76
END OF LINE PULSE
J
1
62
CLOCK
K
78
PRECLEAR
77
40
42
HORIZONTAL UNBLANKING

FIG. 3

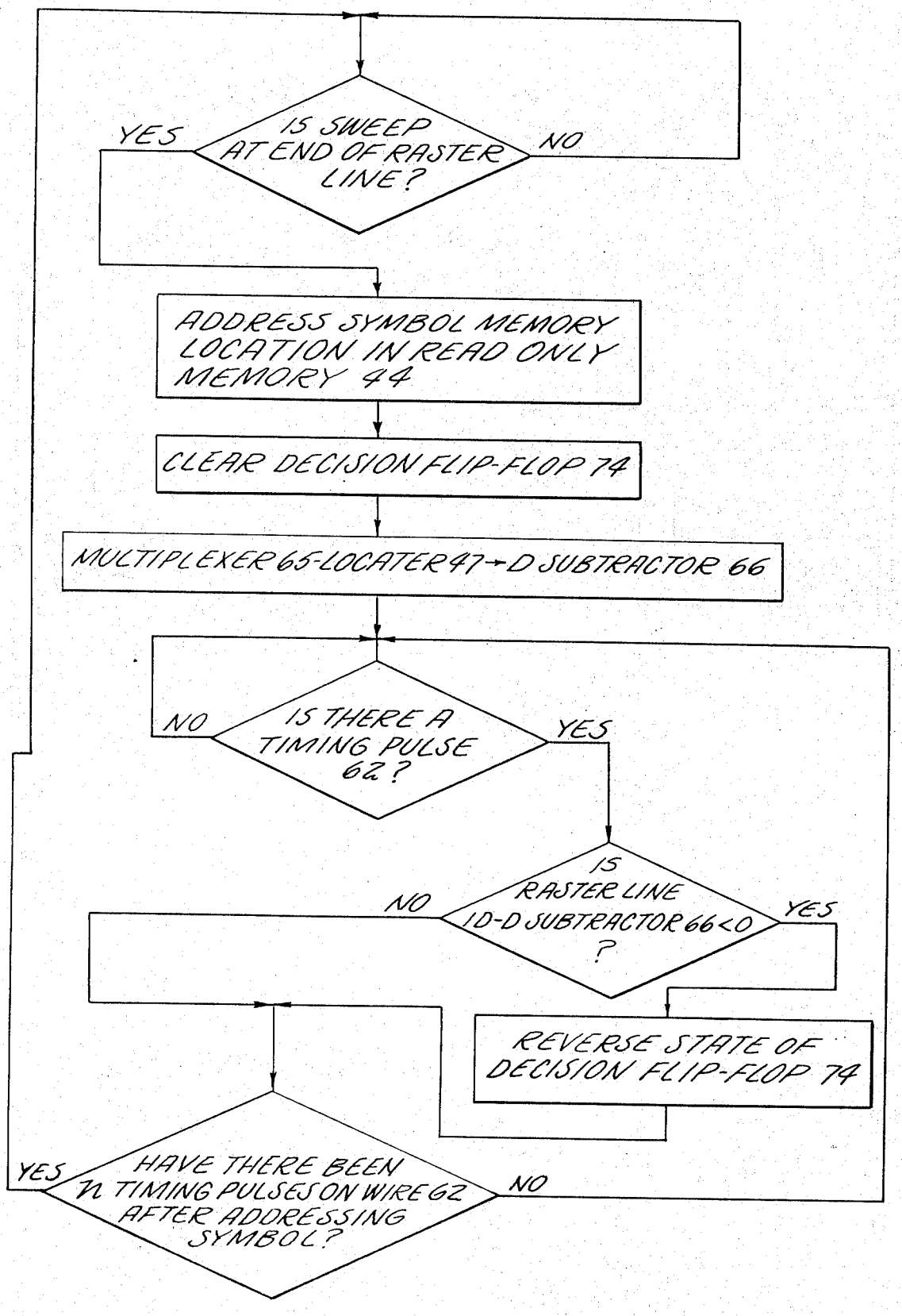
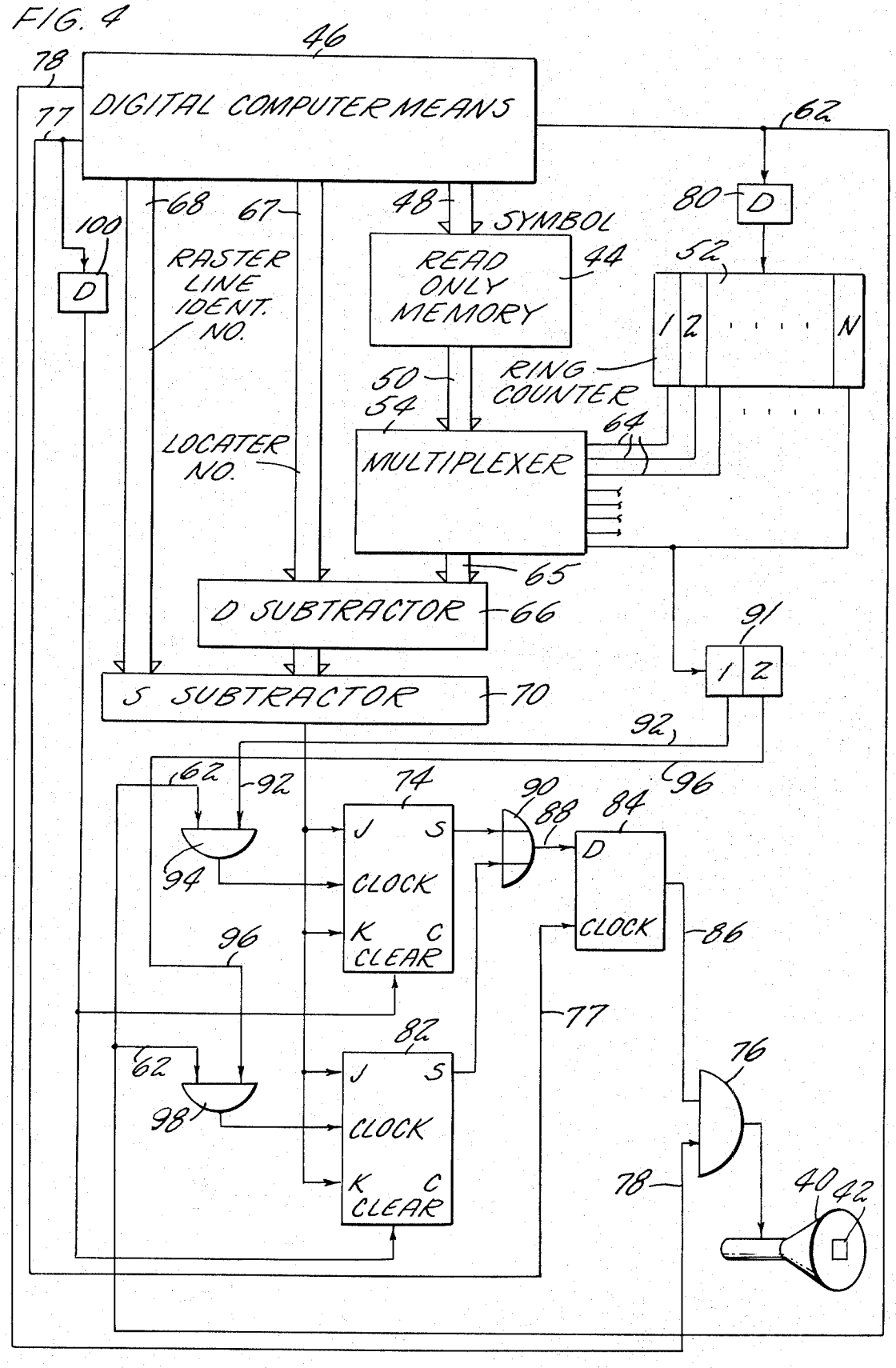

IS SWEEP AT END OF RASTER LINE?
YES
NO
ADDRESS SYMBOL MEMORY LOCATION IN READ ONLY MEMORY 44
CLEAR DECISION FLIP-FLOP 74
MULTIPLEXER 65-LOCATER 47→D SUBTRACTOR 66
IS THERE A TIMING PULSE 62?
NO
YES
IS RASTER LINE ID-D SUBTRACTOR 66<0 ?
NO
YES
REVERSE STATE OF DECISION FLIP-FLOP 74
HAVE THERE BEEN N TIMING PULSES ON WIRE 62 AFTER ADDRESSING SYMBOL?
YES
NO

FIG. 4


46
78
77
DIGITAL COMPUTER MEANS
62
80
D
68
67
48
SYMBOL
100
D
RASTER LINE IDENT. NO.
READ ONLY MEMORY
44
52
1
2
N
RING COUNTER
50
54
64
LOCATER NO.
MULTIPLEXER
65
D SUBTRACTOR
66
91
1
2
S SUBTRACTOR
70
92
62
92
74
90
88
84
J
S
94
CLOCK
D
K
C
CLEAR
CLOCK
86
96
77
82
62
76
J
S
98
CLOCK
78
40
42
K
C
CLEAR

DIGITAL SYMBOL GENERATOR

BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates to display of symbols on a cathode ray tube, and more particularly to symbol generation performed by digital logic circuitry used in cooperation with a digital computer.

2. Description of the Prior Art

The most common and inexpensive types of CRT display employs a raster sweep in which a beam is swept horizontally across the face of a CRT, and at the end of each horizontal sweep, during a brief retrace time, the beam is returned to the side of the CRT where the sweep started and another sweep is initiated. Each successive one of these raster sweep lines is slightly lower than the prior raster sweep line and after a CRT beam is swept across the lowest line, it is rapidly moved to a position to sweep the top line, and the sweep pattern is thereby iterated from top to bottom on the CRT. The entire array of horizontal raster lines swept across the face of the CRT comprises the raster.

The display of symbols on a raster-swept CRT display is accomplished by illuminating those portions of the raster which comprise the symbol, and by not illuminating other portions. In commercial black and white television, illumination is performed in varying degrees, thereby producing shades of grey. In CRT displays where characters or symbols are displayed, the usual practice is to fully illuminate portions of the raster where a part of a symbol appears and to keep the raster completely darkened in those portions of the raster where no part of a symbol appears. The raster is kept darkened by biasing the CRT below cutoff, and the term commonly applied to this condition is "blanking." Similarly, when a portion of the raster is to be illuminated, the CRT is biased well above cutoff and the term applied to this condition is "unblanking."

The persistence of the phosphor or other coating of the face of the CRT permits the unblanked portion of the raster to remain illuminated between successive sweeps of raster lines, and each sweep refreshes the illumination level where the CRT is unblanked. The raster sweep is sufficiently rapid and the raster sweep lines spaced closely enough so that the appearance of the CRT display to the eye is of a cohesive symbol, without time variation of CRT beam intensity on any portion of the face of the CRT. Therefore, as has often been pointed out in the literature, the appearance of symbols on a CRT display employing a raster is accomplished by a method analogous to repeatedly painting a picture with horizontal strokes of the brush.

Control over the time at which blanking and unblanking must occur with respect to the generation of the raster in order to generate a desired pattern requires identification of each individual horizontal trace, as well as the instantaneous position along the trace. In digitally controlled CRT displays known to the art, this information has been provided by two separate counters. A first counter relates to counting each horizontal trace of the raster, and is incremented after each horizontal trace, and reset after the bottom raster line is traced. The other counter identifies distinct resolvable positions along each of the horizontal traces. This is accomplished by incrementing the second counter on a periodic basis during the trace of each raster line, and resetting this counter at the termination of each line sweep. The counter must be adequate to uniquely identify as many positions along the sweep as is required to achieve the desired resolution: that is, if many elements must be resolvable horizontally, then a larger capacity counter, and a higher frequency of incrementing this counter, are required; for fewer resolvable elements, a smaller counter and a lower incrementing frequency may be used.

The span of the teachings of the prior art cover a wide variety of types of digital symbol generators. The incentive to create many types of digital symbol generators was, and still is, prompted by the multiplicity of purpose and usage of these devices. That is to say, a symbol generator which may have features of economy and utility in one application may have no utility in a great many other applications.

SUMMARY OF THE INVENTION

An object of the present invention is the provision of simplified digital symbol generators.

According to the invention, in a raster swept cathode ray tube display, where a sequence of horizontal raster lines are associated with a sequence of raster line identification numbers and upon which it is desired to display a segment of a symbol, a vertical location of said segment upon said display is completely described by a pair of dimension numbers, one dimension number being equal to the raster line identification number of the topmost line of said segment, and the other being equal to the raster line identification number of the line below said segment. For any raster line having an identification number forming a part of said segment, the subtraction of the greatest dimension number from the raster line identification number is a negative number and a subtraction of the least dimension number from the raster line identification number is either zero or a positive number. Performing a similar pair of subtractions for any other raster line produces differences which are either both negative, both positive or zero and positive. A single negative result in a pair of subtractions signals that the raster line having the identification number for which the subtractions were performed forms a part of the segment.

The present invention may be economically constructed using a read only memory and medium scale integrated semiconductor components, and is simpler and more reliable than other symbol generators known to the prior art.

Other objects, features and advantages of the present invention will become more apparent in the light of the following detailed description of a preferred embodiment thereof, as illustrated in the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a simplified pictorial view of the face of a cathode ray tube displaying a symbol comprised of a single segment;

FIG. 2 is a schematic block diagram of a preferred embodiment of the invention;

FIG. 3 is a logic flow diagram of the operation of the embodiment shown in FIG. 2; and

FIG. 4 is a schematic block diagram of a preferred embodiment of the invention for displaying two symbols.

DESCRIPTION OF THE PREFERRED EMBODIMENT

For illustrative purposes, and in order to enable the teaching of the principles of the invention without unduly complicating the details thereof, the exemplary embodiment disclosed herein includes a raster swept display comprised of **32** raster lines upon which a single symbol is displayed.

The invention hereinafter described relates to apparatus for predicting whether a horizontal raster line about to be swept is included in a symbol at its desired location on a CRT. Separate means are required for horizontally defining and locating the symbol.

Referring now to FIG. **1**, a CRT **40** is illustrated with raster line identification numbers at the vertical displacement where each raster line may appear. A symbol consisting of a single segment **42** is shown located upon the CRT **40**. As explained hereinafter, the vertical location of the segment **42** on the CRT **40** is completely described by the raster line identification numbers of the topmost raster line where the segment **42** is displayed (line 10) and the raster line immediately below the segment **42** (line 14). These numbers, critical to describing the segment **42** and its location, are hereinafter referred to as dimension numbers. The information needed for storage of a segment **42** displayed upon the CRT **40** at the position shown in FIG. **1** are the dimension numbers 10 and 14.

In order to predict whether a raster line about to be swept is included in the segment **42**, two arithmetic operations must be performed. The polarities of the signs resulting therefrom are interpreted to determine whether the CRT **40** will be unblanked during the raster line sweep. Specifically, each arithmetic operation is the subtraction of one of the dimension numbers from the raster line identification number of the next raster line to be swept, and one arithmetic operation for each dimension number must be performed for prediction purposes. The arithmetic operations required by this embodiment are indicated by the following equations:

$$F_T = R - D_T$$

$$F_L = R - D_L$$

where R = the raster line identification number of raster line to be swept

D_T = the top (or least) dimension numbers

For the segment **42** in the position illustrated in FIG. **1**: $D_T = 10$

D_L = the lower (or greatest) dimension number

For the segment **42** in the position illustrated in FIG. **1**: $D_L = 14$

and F_T and F_F = the results of respective arithmetic operations.

Relevant to the interpretation of the results of a pair of arithmetic operations, there are three distinct regions on the CRT **40** which are hereinafter examined; these are, the raster lines above the segment **42**, the raster lines below the segment **42** and the raster lines including the segment **42**. It is obvious that at the raster lines above the segment **42** the raster line identification numbers are all smaller than either of the dimension numbers. Therefore, in this region of the display, the results of a pair of arithmetic operations are a pair of negative numbers. At all of the raster lines below the segment **42**, neither of the dimension numbers are ever greater than a raster line identification number so that the result of each operation is a positive number or zero. Finally, for the raster lines having identification numbers where portions of the segment **42** are displayed, the arithmetic operations wherein the least dimension number is used always results in a number greater than or equal to zero (zero only occurs at the topmost raster line of the segment **42**) and the results therefore have a positive sign. However, when the greatest dimension number is used, the results of the operations are always negative numbers. Therefore, two arithmetic operations providing only a single negative sign determine that the raster line is included in the segment **42**.

Although the present invention is described with respect to the display of a symbol of only one segment **42**, it should be understood that when a symbol consists of n vertically disjunctive segments, **2n** arithmetic operations are required prior to the sweep of each raster line and when these operations produce an odd number of negative results, then and only then, does the raster line to be swept comprise a portion of the symbol. The reason for this is that for a raster line which is not included in any of the segments of the symbol, each pair of arithmetic operations for each segment will contribute either two positive numbers or two negative numbers; it is only when the raster line about to be swept is included in a segment that one pair of the *n* pairs of arithmetic operations produces a single negative sign thereby causing the total number of negative signs to be an odd number.

Referring now to FIG. **2**, a schematic block diagram of an exemplary embodiment of the invention is illustrated. The operation of the invention illustrated therein can best be understood by viewing FIG. **2** in conjunction with FIG. **3**, a logic flow diagram of the operation of the exemplary embodiment. The segment **42** is stored in the read only memory **44** in the form of reference dimension numbers. In this example, the reference dimension numbers are chosen so that they are the largest possible dimension numbers consistent with a position of the segment **42** on the CRT **40**. By so doing, dimension numbers representative of any other position on the CRT **40** are obtained by subtracting a locater number from the referenced dimension numbers. The locater number is never added to the reference dimension numbers since any of the resulting dimension numbers which would thereby be obtained would relate to locations off of the CRT **40**, for at least a portion of the segment **42**. The reference dimension numbers in the example are thirty-three and twenty-nine and are representative of the segment **42** on the CRT **40** wherein the bottom line of the segment **42** coincides with the bottom raster line (raster line identification number thirty-two) on the CRT **40**. A digital computer means **46** is similar to many of the assembly language programmed computers well known to the art and commonly used in cooperation with digital symbol generators and provides, on a plurality of signal lines **48**, signals representative of a memory location in the read only memory **44** where all of the reference dimension numbers of a symbol are located. The read only memory **44** provides, on a plurality of signal lines **50**, signals representative of these reference

dimension numbers. A ring counter **52** and a multiplexer **54** sequentially select and provide on a plurality of signal lines **55**, each of the reference dimension numbers so that the locater number can be subtracted from them. The ring counter **52** has as many different states as the maximum number of reference dimension numbers used to represent any single symbol stored in the read only memory **44**. That is to say, *n* (an even number) ring counter states are required when the maximum number of reference dimension numbers used to represent any symbol is equal to *n*. The state of the ring counter **52** is changed n times in response to *n* timing pulses generated during a horizontal retrace time interval by an AND gate **56** connected to a source of timing pulses provided by the digital computer means **46** on a signal line **58**. The pulse repetition rate of the timing pulses on the signal line **58** is such that exactly n pulses are generated during the retrace time interval. The other input of the AND gate **56** is connected to a horizontal retrace time signal provided by the digital computer means **46** on a signal line **60**. The gated output of the AND gate **56**, therefore, provides on a signal line **62**, n pulses during each horizontal retrace time interval, and each of a plurality of output signal lines **64** of the ring counter **52** are thereby sequentially brought to a logical one level once during each horizontal retrace interval. The signals on the signal lines **64** cause the multiplexer to sequentially provide, on a plurality of signal lines **65**, signals representative of each of the reference dimension numbers provided by the read only memory **44** on the plurality of signal lines **50**. It should be understood that for symbols containing less than *n* reference dimension numbers, the multiplexer **54** transmits, on the signal lines **65**, the number zero at a time when the ring counter state is not providing access to a reference dimension number of the addressed symbol. Since zero always represents a location off of the CRT **40** (whether or not a non-zero locater number is subtracted from it), and since the number of zeros thereby provided must be even (each segment contains two dimension numbers), they cannot contribute to an odd number of negative results of arithmetic operations. The subtraction of the locater number from the reference dimension number represented by signals on the plurality of signal lines **65** is performed by a D subtractor **66**. The locater number is represented by signals provided by the digital computer means **46** on a plurality of signal lines **67**.

The completion of an arithmetic operation is represented by subtracting the output of the D subtractor **66** (one of the dimension numbers representing the segment **42** in its currently desired location) from a raster line identification number of the raster line about to be swept. The raster line identification number of the raster line about to be swept is represented by signals provided by the digital computer means on a plurality of signal lines **68**.

An S subtractor **70** subtracts the output of the D subtractor **66** from the raster line identification number and generates a signal on a line **72** which is at a logical one level when the difference of the numbers represented by inputs to the S subtractor **70** is negative.

The line **72** is connected to the J and K inputs of a decision memory flip-flop **74** where the results of the arithmetic operations (two, in this example) are interpreted prior to the sweep of each raster line. A **1** output of the flip-flop **74** is connected to an input of a video gate **76**. The output of the video gate **76** provides an unblanking signal to the CRT **40**; hence the flip-flop **74** must assume the set state, to provide a signal at its **1** output, in order to unblank the CRT **40**. Prior to responding to the results of any of the arithmetic operations, the flip-flop **74** is precleared by an end of line pulse provided by the digital computer **46** on a line **77**. An arithmetic operation is interpreted by the flip-flop **74** upon receiving at its clock input a pulse generated at the output of the AND gate **56** on the line **62**. An arithmetic operation causing a negative sign (logical one at the J and K inputs of the flip-flop **74**) causes the flip-flop **74** to reverse its state, whereas a positive sign (logical zero) causes it to remain unchanged. For the two arithmetic operations in the example that must be completed after an end of line pulse and prior to a raster line sweep, there are three possible sets of results; these are, the two arithmetic operations resulting in successive positive signs, the two operations resulting in successive negative signs and the two operations resulting in successive unlike signs. Arithmetic operations resulting in successive positive signs permit the flip-flop **74** to remain in a cleared state after each operation since the J and K inputs are at logical zero at the time that the pulses on the line **62** occur. Operations resulting in successive negative signs cause the flip-flop **74** to reverse its state at the occurrence of each pulse on the line **62** since the negative sign is associated with a logical one level at the J and K inputs; the two reversals of state cause the flip-flop **74** to end up in its initially assumed cleared state. It is only when the two arithmetic operations produce unlike signs that the flip-flop **74** ends up in the set state. Therefore, at the completion of two arithmetic operations thus interpreted, the flip-flop **74** having assumed the set state is indicative that one of the two operations has produced a negative sign and the CRT **40** is to be unblanked during the following raste sweep. A horizontal unblanking signal provided by the computer means **46** on a line **78** to an input of the video gate **76** enables unblanking of the CRT **40** at discrete portions of a raster line sweep, thereby horizontally defining and locating the symbol upon the CRT **40**. Thus, signals on lines **48** selecting the symbol from the read only memory **44**, signals on line **47** associated with the locater number, and the horizontal unblanking signal on line **78** completely define the symbol and its position on the CRT **40**.

A delay element **80** is connected between the output of the AND gate **56** and the ring counter **52** so that the change in state of the ring counter **52** takes place a short time interval after the interpretation of the results of an arithmetic operation, thereby avoiding ambiguity at a time that change of the reference dimension number, represented by a change of the signals on the signal lines **65**, takes place.

It should be understood that in certain applications of the invention, the locater number may be added to the raster line identification number instead of subtracted from the reference dimension number. That alternative is an arithmetic equivalent to the arithmetic operation hereinbefore described. It should also be un-

derstood that the flip-flop **74** may be preset instead of precleared and the clear output instead of the set output connected to the input of the video gate **76**.

The invention may be adopted for use in displaying a plurality of symbols simultaneously upon the CRT **40**, as shown in FIG. **4**. In this embodiment, the timing pulses on signal line **62** are generated at a rate which produces $2n$ pulses during the time interval between two end of line pulses. During the first n timing pulses after the end of line pulse, signals representing the completion of all arithmetic operations for a first symbol are generated and during the second n timing pulses, signals representing the completion of all arithmetic operations for a second symbol are generated. The results of the interpretation of the arithmetic operations are transferred from decision memory flip-flops **74, 82** to a D flip-flop **84** when the end of line pulse occurs. The output of the D flip-flop **84** is brought to a logical one level if either or both of the symbols are comprised of the next raster line to be swept. It should be understood that the completion and the interpretation of arithmetic operations takes place during an entire raster sweep and retrace time in this embodiment.

The D flip-flop **84** is a shift register stage which transfers to an output signal line **86** the logical level that had been on a signal line **88** immediately prior to an end of line pulse being provided to its clock input on the line **76**. An OR gate **90** causes the signal line **88** to assume a logical one level when either or both of the flip-flops **74, 82** generate a logical one at their set outputs at the time that the end of line pulse occurs.

During a time interval that the first n timing pulses occur, a second ring counter **91** provides, on a signal line **92**, a logical one to an input of an AND gate **94** enabling timing pulses on the signal line **62** to be transmitted to the clock input of the flip-flop **74** and thereby permitting the flip-flop **74** to reverse its state in response to a logical one output from the S subtractor **70**. The occurrence of the nth timing pulse causes the second ring counter **91** to change its state so that a logical zero is provided to the signal line **92**, thereby inhibiting the timing pulses to the clock input of the flip-flop **74** so as to prevent it from reversing its state. A logical one is applied by a signal line **96** to one input of an AND gate **98** enabling the flip-flop **82** to reverse its state in response to a logical one output from the S subtractor **70**. Similarly, during the first n timing pulses, logical zero is provided by the second ring counter **91** to the AND gate **98**.

A delay element **100** is used to delay by a short interval of time the end of line pulse to the clear inputs of the flip-flops **74, 82** so that the output of the OR gate **92** does not change until the end of line pulse causes a transfer of the output of the OR gate **92** to the output of the D flip-flop **86**.

The signal line **78** transmits to an input of the video gate **76** a composite horizontal unblanking signal which locates and defines either one or two symbols upon the CRT **40**.

Although the invention has been shown and described with respect to the preferred embodiments thereof, it should be understood by those skilled in the art that the foregoing and other changes and omissions in the form and detail thereof may be made therein without departing from the spirit and the scope of the invention.

Having thus described a typical embodiment of my invention, that which I claim as new and desire to secure by Letters Patent of the United States is:

1. In a digital symbol generator including a cathode ray tube display apparatus and means for defining the vertical dimension of an area in which symbols may be generated, the improvement comprising:

first means for providing first signal representations identifying each one of a sequence of vertically spaced horizontal raster lines, and including means for generating a plurality of second signal representations identifying the limits of a range including one or more vertically spaced raster lines included in a symbol to be displayed upon said cathode ray tube in said vertical range;

sign signal generating means, connected to said first means, for generating a plurality of sign signal pairs, each pair corresponding to one of said first signal representations, one sign signal in each pair being representative of the sign of the difference between a number represented by said first signal representation and a number represented by a first one of said second signal representations, and the other sign signal in each pair representative of the sign of the difference between said first signal representation number and a number represented by another one of said second signal representations; and

means connected to said sign signal generating means for comparing each of said pairs of sign signals and generating a signal for enabling unblanking of said cathode ray tube in response to unlike signs in any of said pairs.

* * * * *