(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 March 2006 (30.03.2006)

PCT

(10) International Publication Number
WO 2006/033955 A2

(51) International Patent Classification:
H03K 19/017 (2006.01)

(21) International Application Number:
PCT/US2005/032907

(22) International Filing Date:
12 September 2005 (12.09.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/945,144 20 September 2004 (20.09.2004) US

(71) Applicant *(for all designated States except US)*: **ANALOG DEVICES, INC.** [US/US]; One Technology Way, Norwood, MA 02062-9106 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **TAM, Kimo, Y., F.** [US/US]; 11 Brooks Road, Lincoln, MA 01773 (US).

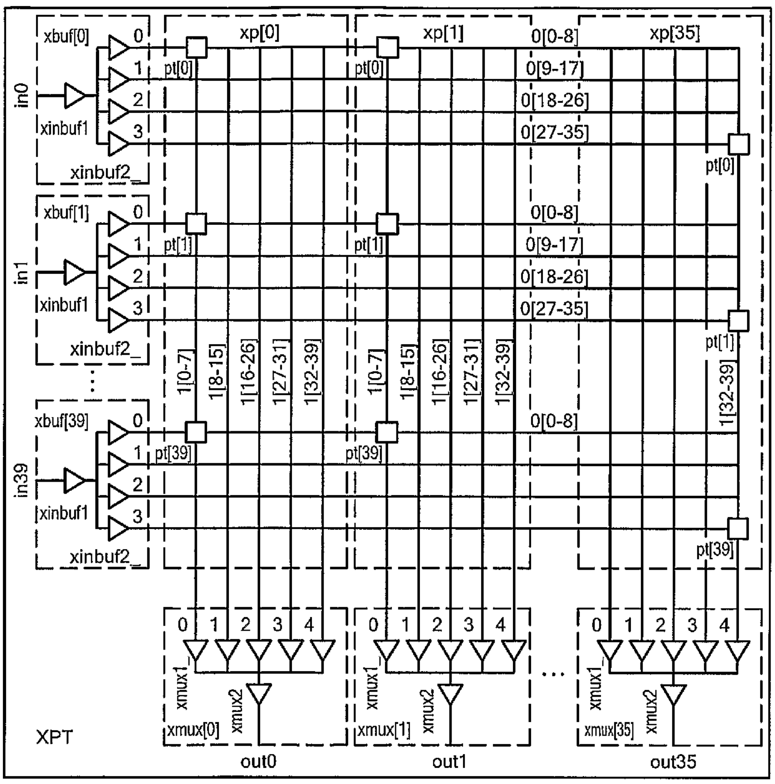
(74) Agents: **SUNSTEIN, Bruce, D.** et al.; Bromberg & Sunstein LLP, 125 Summer Street, Suite 1100, Boston, MA 02110-1618 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,

[Continued on next page]

(54) Title: HIGH-SPEED DIFFERENTIAL LOGIC MULTIPLEXER



(57) Abstract: A circuit for a high speed digital multiplexer has an active load circuit connected to an output of the digital multiplexer. The active load circuit loads the multiplexer output with a transimpedance stage with low input resistance to reduce the RC time constant at the multiplexer output. The active load circuit may be based on two active devices connected to the multiplexer output so as to form a differential cascode circuit.

WO 2006/033955 A2

RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

High-Speed Differential Logic Multiplexer

Field of the Invention

[0001] The invention generally relates to data switching circuits, and more specifically to an active load circuit for a high speed digital multiplexer.

Background Art

[0002] Complex digital data circuits use various architectures to distribute data signals between multiple locations. A digital crosspoint switch can selectably connect data signals between multiple inputs and multiple outputs. One way to implement a crosspoint switch is as an array of multiplexer stages. For example, a 32x32 crosspoint switch can be implemented as an array of thirty-two 32:1 multiplexers which share a 32-input bus.

[0003] Figure 1 shows the functional block architecture of a typical crosspoint switch. The left edge of the figure shows inputs 0-39 and the bottom edge shows outputs 0-35. Any input can be connected to any number of outputs. Each of the smaller dashed line boxes along the left side of Fig. 1 represents a two-stage input buffer. The larger dashed line boxes in the center of the figure are arrays of point cells to connect a selected input to a selected output. The smaller dashed line boxes along the bottom side of the figure are two-stage multiplexers to selectably connect multiple data paths to a given output port. As shown in Fig. 1, each of the second stage input buffers and first stage output multiplexers may serve only a subset of the output and input ports respectively. In addition, at high data speeds above 1 Gb/sec, the crosspoint may be further timesliced using parallel paths into alternating data slices at half the data rate each.

[0004] Figure 2 provides a slice of such a crosspoint switch showing a single path connecting one input port to one output port. The crosspoint switch can be conceptually divided into a high-speed data path (shown by thin lines in Fig. 2) and a lower-speed control plane that determines connectivity (shown by thick lines in Fig. 2). The control plane is run by a digital clocking signal and determines which pieces of the data path should be enabled for a given connectivity and when the enabling signals should change.

For the switch control plane, connectivity data to control the data path may be written into control latches or flip-flops.

[0005] In Fig. 2, the first stage buffer **21** provides a high impedance input (with reduced input capacitance) and converts signal levels, for example, from CMOS to current mode logic (CML). Driving four sets of input lines from each of the second stage input buffers **22** reduces the number of point cells **23** loading each input by a factor of four (only nine point cells **23** on each second stage buffer **22**). Groups of multiple point cells are provided to first stage multiplexers **24** to allow the associated data streams to be directed to selected output ports. The capacitance load on each point cell **23** (which may be simply resistively loaded CML buffers) is reduced by collecting five first stage multiplexers **24** for each second stage multiplexer **25** such that each first stage multiplexer collects eight inputs. The second stage multiplexer **25** also provides signal level conversion; for example, from CML to full swing CMOS.

[0006] A cross-point switch such as in Figs. 1 and 2 may be conveniently implemented using differential current mode logic because of its simplicity, relatively high-speed, low supply noise generation, and high supply noise immunity. But the loads for differential current mode logic circuits are simply resistors, and thus, current mode logic suffers from poor load drive capability and poor speed vs. fan-in (i.e., number of inputs in a gate) trade off. And as data speeds approach and surpass the 1 GHz threshold, circuit reactances create various problems which are not so significant at lower data speeds. In a 32-input multiplexer, the slow down in circuit speed due to delay and rise time would be on the order of 32 times slower than for a simple gate (such as an inverter). And increasing the scale of the input devices provides no speed improvement because the circuit is limited by self-loading.

Summary of the Invention

[0007] Embodiments of the present invention are directed to an active load circuit connected to an output of a high speed digital multiplexer, and to methods of operating such a circuit. The active load circuit loads the multiplexer output with an active transimpedance stage with low input resistance (near zero) to reduce the RC time constant at the multiplexer output. The high speed digital multiplexer may be, for example, a current mode logic circuit.

[0008] In further specific embodiments, the active load circuit may be based on two active devices connected to the multiplexer output so as to form a differential cascode circuit. Each active device may also have a biasing control resistor cross-coupled to a current supply path of the other active device. The biasing control resistor establishes a device biasing voltage that controls gain of the device. In such an embodiment, the value of each biasing control resistor may be equal to the inverse transconductance of its active device. A further embodiment may also include for each active device a swing setting resistor connecting an output node of the active device to the control biasing resistor of the other active device. The swing setting resistor establishes a voltage swing for its active device. The active devices may be medium threshold devices. In addition, to reduce the headroom penalty looking into the inputs of the active load, a replica circuit may bias the backgate terminals to a level near a drain supply voltage (for example, about one threshold voltage below the drain supply voltage).

[0009] Embodiments of the present invention also include a multiplexer containing any of the active load circuits above. Embodiments also include a crosspoint switch containing any of the active load circuits above.

Brief Description of the Drawings

[0010] Figure 1 shows the functional block architecture of a typical crosspoint switch.

[0011] Figure 2 provides a slice of a crosspoint switch according to Fig. 1 showing a single path connecting one input port to one output port.

[0012] Figure 3 shows the switching structure for a multiplexer according to one embodiment of the present invention.

[0013] Figure 4 shows an active load circuit for a high-speed multiplexer according to one embodiment of the present invention.

Detailed Description of Specific Embodiments

[0014] Various embodiments of the present invention are directed to techniques for using an active load circuit to reduce the RC time constant at the output terminals of a high speed digital multiplexer (common terminals which are also the active load circuit inputs) such as is used in a crosspoint switch. Such an approach allows for a current mode logic implementation of such high fan-in circuits with reduced delay and low-complexity overhead. The multiplexer can be implemented as an array of simple input stages and a low-input-impedance load. This facilitates implementation of high-speed crosspoint switches.

[0015] Figure 3 shows the switching structure for a multiplexer according to one embodiment of the present invention. One data path enters the figure on the upper left side as lines IPA and INA to the gates of differential switch pair MN11A and MN12A, and output via the drains of MN11A and MN12A. Another data path enters on lines IPB and INB to the gates of differential switch pair MN11B and MN12B, and output via the drains of MN11B and MN12B. Additional data paths are implemented similarly. The sources of each differential switch pair MN11A/12A and MN11B/12B etc. are coupled to respective switched tail current sources MN10A, MN10B, etc., which in turn are enabled by control switch MN1 controlled by the Control Logic block.

[0016] In the prior art, the load circuit for such a differential current mode switch circuit would be a simple passive resistor circuit. But as explained above, circuit reactances become significant at high data speeds (*e.g.,* 1 GHz and above) creating significant delays in signal rise and fall times which limit circuit response below what is required to support such high data speeds.

[0017] Figure 4 shows details of an active load circuit (seen in the upper right portion of Fig. 3) for a high-speed differential logic multiplexer according to one embodiment of the present invention. The drains of multiple differential outputs from point cells (e.g., MN11A/MN12A and MN11B/MN12B in Fig. 3) are connected on the lines IP and IN to the differential input terminals of an active transimpedance load stage, the sources of MN6 and MN7. The differential pair MN6 and MN7 together with an active multiplexer stage such as MN11A/MN12A form a differential cascode arrangement. The drains of MN6 and MN7 provide differential data output signals OP and ON.

[0018] Using a differential cascode stage as the multiplexer load, the RC time constant at the multiplexer output nodes can be reduced while maintaining a desired swing and current level. In such an arrangement, the differential small-signal impedance looking into the sources of the cross-coupled common gate devices (MN6 and MN7) can be made to approach zero by appropriately sizing the switches themselves and the gate biasing resistors (R5/R6, the top resistor in each voltage divider leg) such that the resistor values (R5/R6) are equal to the inverse transconductance ($1/g_m$) of the switch pair (MN6/MN7) under balance. Under these conditions increased current ΔI through one switch MN6 requires a $\Delta I / g_m$ increase in the gate-source voltage V_{gs} of MN6. However, MN7 current is also decreased by the same ΔI, which raises the gate voltage of MN6 by $R5 * \Delta I = 1/g_m * \Delta I$. Thus, the increased MN6 gate-source voltage V_{gs} is achieved without changing the actual circuit source voltage V_S, making $R_{in} = 0\Omega$. The bottom voltage divider resistors in each leg (R3/R4) are then sized to achieve the desired swing. For large signal operation, the transconductance g_m can not be assumed to be constant, so the matching of switch transconductance g_m to the gate biasing resistors R5/R6 will not be exact, but the resistance seen by the large wiring capacitance at the sources of the MN6/MN7 is still greatly reduced over purely resistive loads (~1kΩ vs. 2.5kΩ). The constant current sources CS1 and CS2 in Fig. 4 maintain each respective switch MN6 and MN7 in higher, more constant transconductance g_m, thereby improving the degree of cancellation.

[0019] In one specific embodiment, medium threshold devices are chosen to allow headroom for both the cross-coupled devices MN6/MN7 and the input devices (e.g., MN11B/MN12B). For MN6/MN7 to remain in saturation, the output swing should be less than the voltage threshold V_{th} of MN6/MN7. This would advise against using low voltage threshold LVT NMOS devices for the cross-coupled devices MN6/MN7. However, the larger voltage threshold V_{th} of medium threshold devices pushes the drain-source voltages V_{ds} of the input differential pair (e.g., MN11B/MN12B) below saturation $V_{ds,sat}$ by up to 150mV in the worst case corner. This issue could be addressed in various ways, such as reducing the threshold voltage by using a replica circuit to bias the backgate connections of MN6/MN7 to a level near the drain supply voltage V_{dd} (for example, about one threshold voltage below V_{dd}), thereby reducing the headroom penalty looking into the inputs of the active load. Alternatively, the input common mode level to the multiplexer stage could be reduced, being careful not to push the tail current source devices into triode operation. Using medium threshold devices may require scaling of the transistor widths due to the larger minimum width of these devices (e.g., 0.3μm vs. 0.18μm). This scaling may result in a significant capacitance penalty, but the wiring parasitics should still dominate the capacitance at this node.

[0020] Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention.

What is claimed is:

1. A circuit for a high speed digital multiplexer, the circuit comprising:
an active load circuit connected to an output of a high speed digital multiplexer and loading the multiplexer output with an active transimpedance stage having low input resistance to reduce the RC time constant at the multiplexer output.

2. A circuit according to claim 1, wherein the digital multiplexer is a current mode logic circuit.

3. A circuit according to claim 1, wherein the active load circuit further comprises:
two active devices connected to the multiplexer output so as to form a differential cascode circuit.

4. A circuit according to claim 3, further comprising:
for each active device, a biasing control resistor cross-coupled to a current supply path of the other active device, the biasing control resistor establishing a device biasing voltage that controls gain of the device.

5. A circuit according to claim 4, wherein the value of each biasing control resistor is equal to the inverse transconductance of its active device.

6. A circuit according to claim 4, further comprising:
for each active device, a swing setting resistor connecting an output node of the active device to the control biasing resistor of the other active device, the swing setting resistor establishing a voltage swing for its active device.

7. A circuit according to claim 4, further comprising:
for each active device, an associated current source for establishing the transconductance of the active device.

8. A circuit according to claim 3, wherein the active devices are medium threshold devices.

9. A circuit according to claim 8, where in the active devices are MOSFETs having gate, source, drain, and backgate terminals, and a replica circuit biases the backgate terminals to a level near a drain supply voltage.

10. A multiplexer containing an active load circuit according to any of claims 1-9.

11. A crosspoint switch containing an active load circuit according to any of claims 1-9.

12. A method for loading a high speed digital multiplexer, the method comprising:
connecting an active load circuit to an output of a high speed digital multiplexer so as to load the multiplexer with an active transimpedance stage having low input resistance to reduce the RC time constant at the multiplexer output.

13. A method according to claim 12, wherein the digital multiplexer is a current mode logic circuit.

14. A method according to claim 12, wherein the active load circuit includes two active devices connected to the multiplexer output so as to form a differential cascode circuit.

15. A method according to claim 14, further comprising:
for each active device, establishing a device biasing voltage that control gain of the device using a biasing control resistor cross-coupled to a current supply path of the other active device.

16. A method according to claim 15, wherein the value of each biasing control resistor is equal to the inverse transconductance of its active device.

17. A method according to claim 15, further comprising:
for each active device, providing a swing setting resistor connected an output node of the active device to the control biasing resistor of the other active device, the swing setting resistor establishing a voltage swing for its active device.

18. A method according to claim 15, further comprising:
for each active device, establishing the transconductance of the active device with an associated current source.

19. A method according to claim 14, wherein the active devices are medium threshold devices.

20. A method according to claim 19, wherein the active devices are MOSFETs having gate, source, drain, and backgate terminals, and a replica circuit biases the backgate terminals to a level near a drain supply voltage.

21. A multiplexer adapted to use a method for loading a high speed digital multiplexer according to any of claims 12-20.

22. A crosspoint switch adapted to use a method for loading a high speed digital multiplexer according to any of claims 12-20.

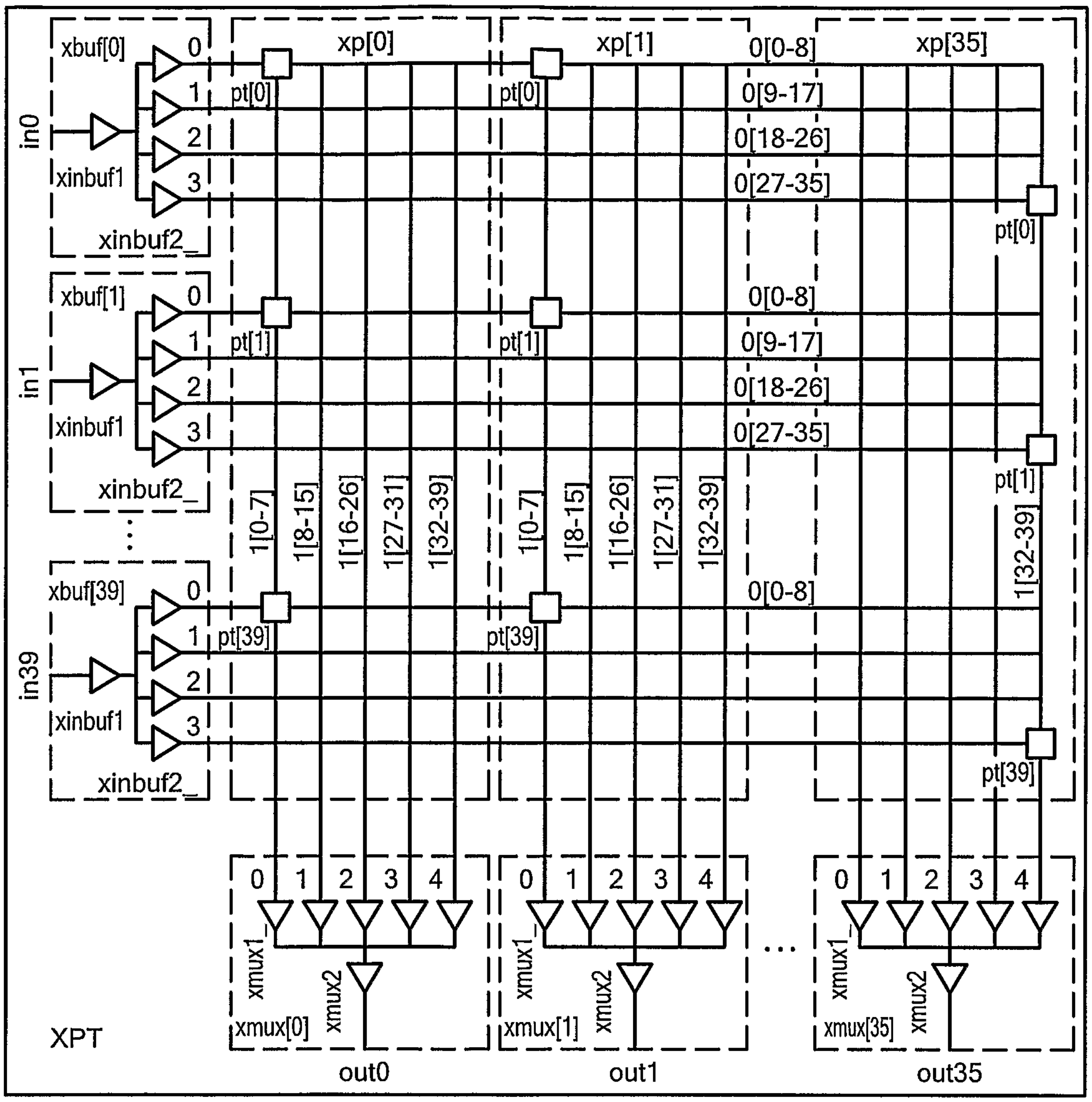


FIG. 1
(PRIOR ART)

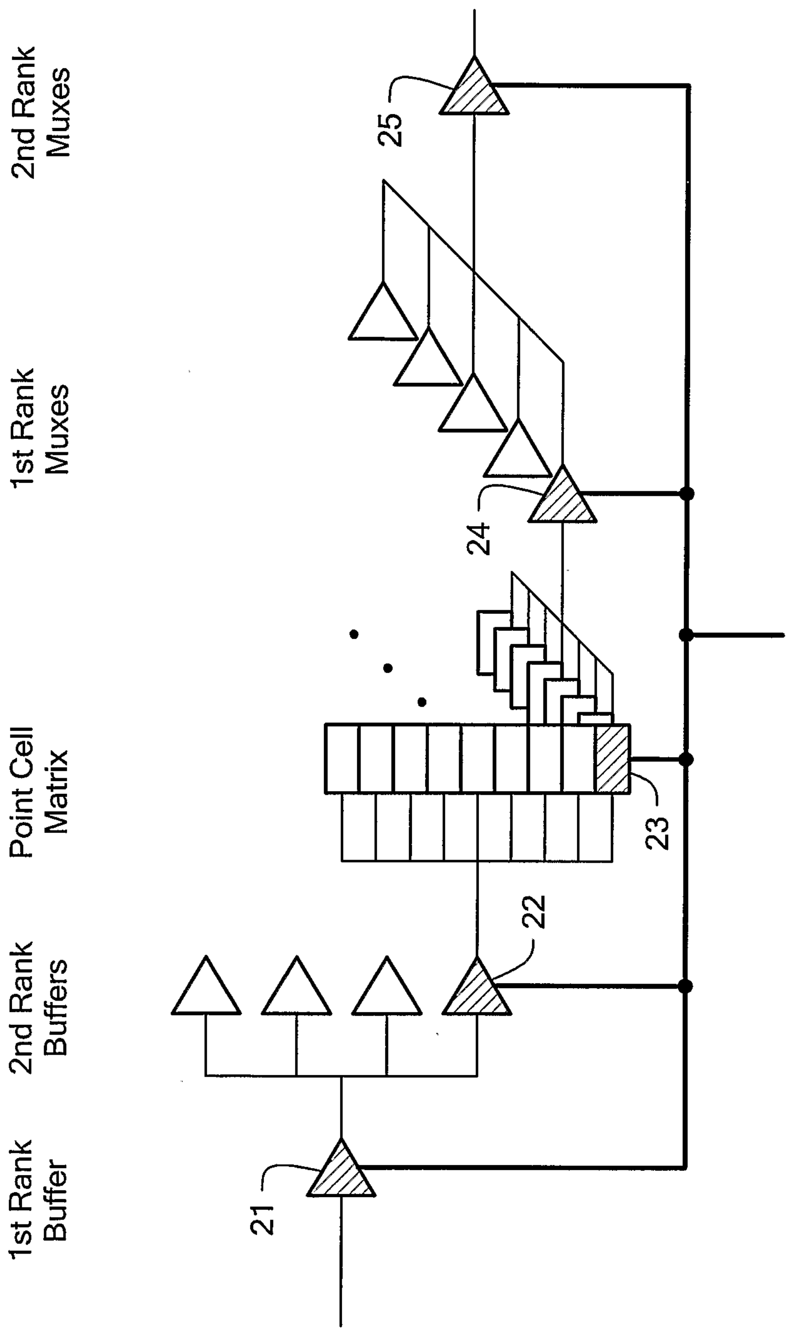


FIG. 2
(PRIOR ART)

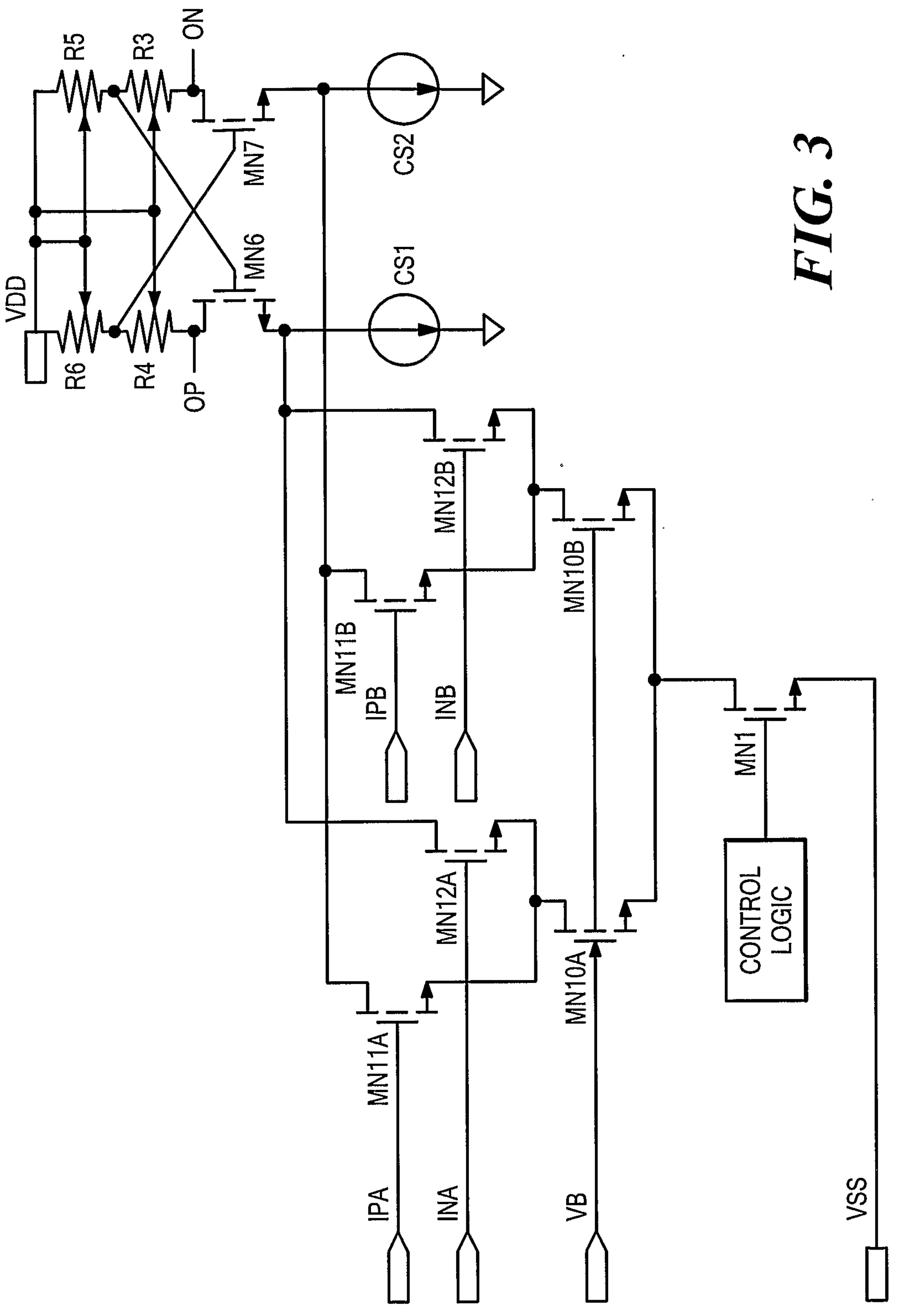

R5
R3
ON
VDD
MN7
MN6
CS2
CS1
R6
R4
OP
MN12B
MN10B
MN11B
IPB
INB
MN1
MN12A
CONTROL LOGIC
MN10A
MN11A
IPA
INA
VB
VSS

FIG. 3

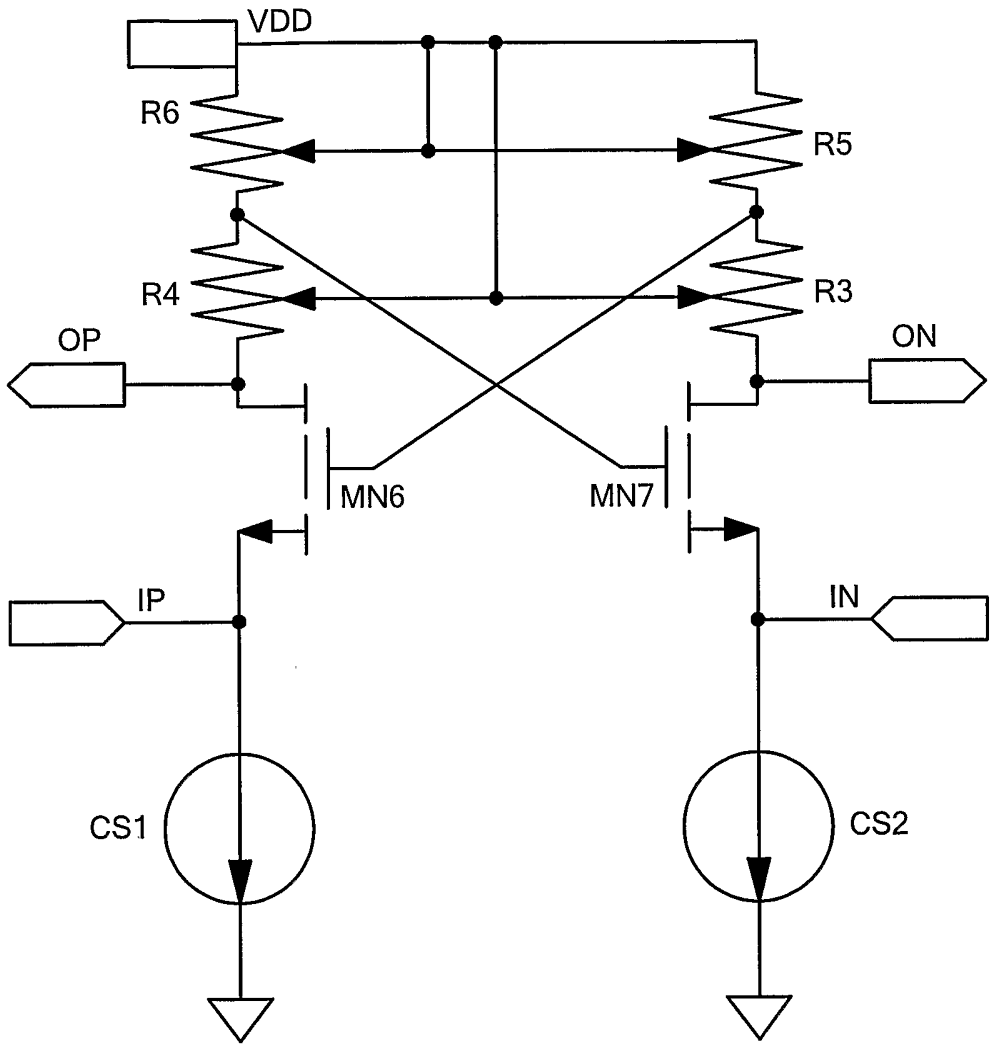


FIG. 4