



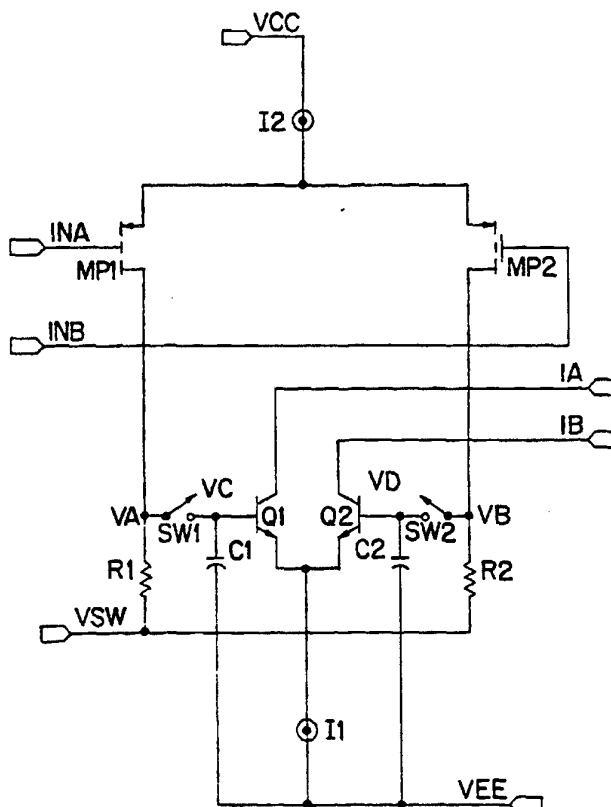
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(21) International Application Number: PCT/US94/09196 (22) International Filing Date: 12 August 1994 (12.08.94) (30) Priority Data: 08/106,047 12 August 1993 (12.08.93) US (71) Applicant: ANALOG DEVICES, INCORPORATED [US/US]; One Technology Way, Norwood, MA 02062 (US). (72) Inventor: MERCER, Douglas, A.; 13 Braewood Drive, Brad- ford, MA 01835 (US). (74) Agent: BOLLINGER, Howard, M.; Parmelee, Bollinger & Bramblett, 460 Summer Street, Stamford, CT 06901 (US).		(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: D/A CONVERTER WITH SYMMETRICAL DIFFERENTIAL SWITCHING CIRCUIT

(57) Abstract

A digital-to-analog converter including a plurality of binarily-weighted states each incorporating a differential switch-pair circuit which includes two matched bi-polar switch transistors (Q1, Q2) the bases of which are driven by a corresponding pair of complementary signal sources. Two additional switches (SW1, SW2) are included in this circuit, with each such switch being connected between a respective signal source and its corresponding transistor control electrode. These two switches are both opened before the clock-controlled activation of the complementary signal sources. A short time after such activation, sufficient to assure that the complementary signal voltages have stabilized at their new values, the two additional switches are reclosed simultaneously by a single control signal so as to effect synchronized switchover of the two switch transistors at that instant. Capacitors (L1, L2) included to maintain effectively constant the base voltages of the two switch transistors during the time that the two additional switches are open.



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D/A Converter With Symmetrical Differential Switching Circuit.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to digital-to-analog converters of the type employing differential switch circuits for switching the bit currents either to an output bus or to a circuit common line. More particularly, this invention relates to techniques for improving the performance of such differential switch circuits.

2. Description of the Prior Art

Digital-to-analog converters (DACs) generally have comprised a number of switches which are selectively operated by a multi-bit digital input signal to produce corresponding binarily-weighted bit currents to be summed as an analog output signal. Such converters ordinarily are formed as integrated circuits (ICs), with each switch comprising two bipolar transistors arranged as a differential

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switch-pair. As shown for example in U.S. patent 3,961,326 (R. B. Craven), the individual transistors of such a switch-pair typically are controlled by complementary signal sources which operate to turn one switch on while turning the other switch off. One of the two switches makes connection to a summing bus, and the other switch makes connection to a common line such as ground.

One problem with such prior art switching arrangements is that there is asymmetry in the switch turn-on and turn-off speeds. This can result in a momentary error in the DAC output until all of the switches have fully switched. This anomaly produces a glitch in the output which is code dependent and results in harmonic distortion or even non-harmonic spurs in the output spectrum.

A typical prior art switch circuit is shown in Figure 1. The form of the output current from terminals IA, IB of this switch circuit is a function of the symmetry of the switching signals, and distortion of the output current could result from asymmetrical switching signals. However, even if the applied input signals INA, INB were perfectly symmetrical, the P-type differential switches MP1 and MP2 would introduce asymmetry in the complementary switching voltages VA, VB which control the switch transistors Q1, Q2. Such asymmetry results in transient output current distortion in any individual switch circuit. It also results in misalignment between the turn-on/turn-off times of the multiple switch-circuits employed in a DAC; that is, the timing of the separate switches of the DAC will not be synchronized properly due to the lack of symmetry with code dependency of the output current.

SUMMARY OF THE INVENTION

In a preferred embodiment of the invention, to be described hereinbelow in detail, there is provided a differential switch-pair circuit which includes two matched bipolar switch transistors the control electrodes (bases) of which are driven by a corresponding pair of complementary signal sources. Two additional switches are included in this circuit, with each switch being connected between one signal source and its corresponding transistor control electrode. These two switches are both opened before the clock-controlled activation of the complementary signal sources. At the time of activation, the complementary signal source voltages change (from high to low and vice versa) if the input bit for that switch circuit requires a reversal in the on/off status of the two switch transistors. A short time after such activation, sufficient to assure that the complementary signal voltages have stabilized at their new values, the two additional switches are reclosed simultaneously by a single control signal so as to effect synchronized switchover of the two switch transistors at that instant.

The preferred embodiment also includes capacitors arranged to maintain effectively constant the control electrode (base) voltages of the two transistors during the time that the two additional switches are open. When the switches are thereafter reclosed, the new control electrode voltages are applied symmetrically to the respective transistor bases, and the on/off status of the transistors is reversed if required by the corresponding bit of the input signal. This simultaneous reclosure of the two additional switches results in a much more symmetrical switching of the two transistor output currents.

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Accordingly, it is an important aspect of the invention to improve the operation of differential switch-pair circuits. In another aspect, the invention provides significant improvements in the performance of digital-to-analog converters. Other objects, aspects and advantages of the invention will in part be pointed out in, and in part apparent from, the following description of a preferred embodiment considered together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a simplified circuit diagram of a prior art switch circuit for use in a DAC;

FIGURE 2 is a simplified circuit diagram like that of Figure 1, but modified in accordance with the present invention;

FIGURE 3 is a circuit diagram of a commercially practicable switch circuit in accordance with this invention;

FIGURE 4 is a timing diagram showing how certain voltages change with time during operation of the switch circuit of Figure 3;

FIGURE 5 is a circuit diagram of logic elements for use in controlling the timing of signals in a switch circuit as shown in Figure 3; and

FIGURE 6 is a circuit diagram showing in block format a digital-to-analog converter in accordance with this invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to Figure 2, there is shown a switch circuit comprising a pair of bipolar transistors Q1, Q2 having common emitter electrodes which are connected through a current source I1 to the negative supply line VEE. The collector electrodes are connected to respective terminals which lead respectively to an output current summing bus and a common line (typically circuit ground).

The base electrodes of transistors Q1, Q2 are connectible through respective switches SW1, SW2 to complementary signal sources which produce control voltages VA, VB. These signal sources include a current source I2 connected to the positive supply line VCC to produce currents for a differentially-operated pair of MOS transistors MP1 and MP2. The gates of these MOS transistors are driven by complementary input signals INA, INB, which together may represent one bit of a multi-bit input signal. The current from source I2 will flow either through MP1 or MP2, depending upon whether the input bit is high or low.

When the current from source I2 flows through MP1, it will produce a voltage across a resistor R1 and, when switch SW1 is closed, that voltage will turn transistor Q1 on. Alternatively, when the current from source I2 flows through MP2, it will produce a voltage across a resistor R2 and, when switch SW2 is closed, that voltage will turn transistor Q2 on. The bit current I1 thus will flow to either terminal IA or IB, depending upon the state of the digital input bit INA, INB.

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The input signals INA, INB are activated by clock signals (to be described) and, when the corresponding bit signal requires a change in the switch state, one input signal (INA or INB) will change from high to low, while the other input signal changes from low to high. The switches SW1 and SW2 are opened a short time before this clocked activation of the input signals so that, at the clock time, the new input voltages VA, VB will have no effect on the base voltages VC, VD of the transistors Q1, Q2.

Capacitors C1, C2 are provided at the bases of the transistors Q1, Q2 to assure that the base voltages do not change appreciably while the switches SW1, SW2 are open. A short time after the clocked activation of the input signals VA, VB, the switches SW1, SW2 will close, and the new voltages VA, VB (if reversal of the input signals has occurred) then will be applied to the transistor bases as new voltages VC, VD. Both voltages VC and VD will be applied simultaneously because the switches SW1 and SW2 are controlled by a single hold signal (as will be described). Thus the transistors Q1, Q2 will switch together, thereby preventing asymmetrical operation.

Referring now also to Figure 3, showing a practical implementation of the circuit of Figure 2, it will be seen that the bit current through transistors Q1 or Q2 is set by current source I1 which in this case comprises a bipolar transistor Q3 in series with a resistor R3 which is laser trimmed for precision setting of the bit current. The switches SW1 and SW2 are formed by respective MOS transistors MN1 and MN2, and two additional MOS transistors MN3, MN4 are provided as 1:1 buffer amplifiers between the switches SW1, SW2 and the corresponding control electrodes (bases) of the transistors Q1, Q2. The voltages VC and VD at the bases are the same as the voltages at the corresponding inboard switch terminals, as indicated on the diagram.

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The current source I2 is an MOS transistor MP5 having a fixed bias voltage ICR on its gate to set the current level properly. The operating current for the buffers MN3, MN4 is derived from the positive supply line VCC, and is controlled by current source transistors MN5, MN6 the gates of which are biased by a voltage IBS. The current from the current sources MN5, MN6 flows to the IC chip substrate SUBST.

The capacitors C1, C2 at the inboard terminals of the switches SW1, SW2 are formed by the gate leads for the buffer transistors MN3, MN4. That is, the conductive metallization of the integrated circuit which makes connection to the gates of those MOS transistors is dimensioned to produce correctly-sized equal capacitances C1 and C2 (approximately one-quarter of a pico-farad in one embodiment) with respect to the underlying substrate of the chip to assure that the base voltages VC, VD are maintained at their initial levels while the switches SW1, SW2 are open.

Referring now to Figure 4, the timing diagram presents an example where changes in the input voltages VA, VB are misaligned such as due to an asymmetry as described above. Specifically, in this example VA changes from high to low at a time before VB changes from low to high. As noted previously, such misalignment would produce a distorted DAC output signal in conventional prior art circuits. However, in the preferred embodiment described herein, this timing misalignment does not affect the operation of the switch transistors Q1, Q2 because as shown in Figure 4 the Hold signal went low to open switches SW1, SW2 before any change in either VA or VB. Thus these switches were, at the time of switchover of VA and VB, already open to prevent the changes in VA, VB from affecting the base voltages of the switch transistors.

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After the voltages VA, VB have stabilized at their new values, the Hold signal for switches SW1, SW2 is returned to its high state, and the switches then close simultaneously. Thus, the stabilized new values of VA, VB will be applied simultaneously to the bases of transistors Q1, Q2, and the currents through those transistors will accordingly change together to their new values, without any misalignment.

Figure 5 shows a circuit suitable for use in a DAC for developing the Hold signal referred to above. This circuit is for the most part basically a conventional logic

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circuit for receiving a master clock signal CLKIN, and producing clock signals CLKAA, CLKA, CLKBB and CLKB for the usual logic elements (not shown) associated with the registers used for temporarily storing the digital input signals prior to their application to the DAC current switches. The circuit also includes provision for disabling the clock signal activation upon a bias voltage being applied to the TRIM terminal for the purpose of conditioning the DAC circuitry for laser-trimming the resistor R3 to set the bit current with precision.

The circuit of Figure 5 also includes a cluster of MOS transistors generally indicated at 20 to develop the Hold signal as described above. These transistors 20 are driven by the master clock signal CLKIN, and are also controlled by a clock signal delayed by inverters G8, G9 and G10. This circuit switches the Hold signal low at the correct time and maintains this low state for a time period appropriate for achieving the results described above. That is, the switches SW1, SW2 are opened just before any switchover of the input signals VA, VB, and are closed just after the new voltages VA, VB have become stabilized.

Figure 6 shows in block outline a digital-to-analog converter formed by a plurality of binarily-weighted bit stages or cells 30-1, 30-2, ..., 30-N each comprising a differential switch circuit as described above. These differential switch circuits all are as shown in Figure 3, and each includes a pair of switches SW1, SW2 for isolating the initial change in voltages VA, VB to prevent such voltage change from affecting the bases of the transistors Q1, Q2.

After those voltages VA, VB have stabilized at their new values (if the voltages have been changed), the switches SW1, SW2 in all of the switch cells close simultaneously to apply the new voltages to the base

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electrodes of all of the switch transistors Q1, Q2 at the same instant. It should particularly be noted that the high Hold signal will be applied to all stages 30-1, 30-2, etc., of the DAC simultaneously, thereby assuring alignment of switchover times for all of those stages so as to avoid distortion in the output signal that would otherwise be caused by misalignment in switchover times between the individual DAC stages.

Although a preferred embodiment of the invention has been disclosed herein in detail, it is to be understood that this is for the purpose of illustrating the invention, and should not be construed as necessarily limiting the scope of the invention since it is apparent that many changes can be made by those skilled in the art while still practicing the invention claimed herein.

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What is Claimed is:

1. In a differential switch-pair circuit comprising two transistors each having two current-carrying electrodes and a control electrode; said switch-pair circuit including complementary signal sources connectible respectively to said transistor control electrodes and operable when activated to turn one transistor on and to turn the other transistor off;

that improvement in said switch-pair circuit which comprises:

first and second switches connected respectively between said complementary signal sources and the corresponding transistor control electrodes; and

means to open both of said switches prior to activation of said complementary signal sources and to close both of said switches together after such activation.

2. A switch-pair circuit as claimed in Claim 1 wherein said two transistors are bipolar devices.

3. A switch-pair circuit as claimed in Claim 2, wherein one common pair of current-carrying electrodes of said two transistors are effectively converted together; and

a current source connected to said common pair of electrodes to determine the magnitude of current flowing through the turned-on transistors.

4. A switch-pair circuit as claimed in Claim 3, wherein said other common pair of current-carrying electrodes are connected to respective current lines.

5. A switch-pair circuit as claimed in Claim 2, wherein said first and second switches are MOS transistors.

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6. A switch-pair circuit as claimed in Claim 1, including first and second capacitor means coupled to circuit points between said first and second switches and the corresponding control electrodes respectively, to tend to maintain the voltages at said control electrodes stable during the time that said two switches are open.

7. A switch-pair circuit as claimed in Claim 6, including first and second MOS buffers between said first and second switches and said corresponding control electrodes respectively.

8. A switch-pair circuit as claimed in Claim 7, wherein the connecting leads to said MOS buffers provide said first and second capacitance means.

9. A digital-to-analog converter comprising a plurality of switch circuits individually switchable into either of two states in accordance with an applied control signal representing one bit of a multi-bit input signal; each of said switch circuits serving when in one of said states to produce a current for an analog output signal; each of said switch circuits comprising a differential switch-pair circuit including:

- (1) two transistors each having two current-carrying electrodes and a control electrode;
- (2) one common pair of said current-carrying electrodes of said two transistors being effectively connected together and the other common pair of current-carrying electrodes being connected to respective current lines;
- (3) said switch-pair circuit further including complementary signal sources connectible respectively to said transistor control electrodes and operable when activated to turn one transistor on and to turn the other transistor off;

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(4) a set of first and second switches connected respectively between said complementary signal sources and the corresponding transistor control electrodes; and

(5) means to open both of said switches prior to activation of said complementary signal sources and to close both of said switches together after such activation.

10. A converter as in Claim 9, wherein both switches of all of said sets are controllable to open or closed condition by a hold signal;

means to produce a single hold signal for all of said sets of switches;

said single hold signal being effective to open both switches of all of said sets of first and second switches prior to activation of said complementary signal sources and to close all of said switches together after such activation.

11. A converter as in Claim 10, including a timing circuit for producing clock pulses for clocking the activation of said complementary signal sources.

12. A converter as claimed in Claim 11, wherein said timing means further includes means to control the timing of said hold signal so as to open and then close said switches respectively before and after the activation of said complementary signal sources.

13. A converter as in Claim 9, wherein said current lines for each switch pair are an output line and a common line respectively.

14. A converter as in Claim 9, wherein said switch-pair transistors are bipolar devices; and
said first and second switches are MOS devices.

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15. A converter as in Claim 9, including first and second MOS buffer devices between said first and second switches respectively and the corresponding transistor control electrodes.

16. A converter as in Claim 9, including capacitance means to tend to maintain a stable voltage on said transistor control electrodes while said switches are open.

17. A converter as in Claim 16, including first and second buffer devices between said first and second switches respectively and the corresponding control electrodes.

18. A converter as in Claim 17, wherein said capacitance means is provided by the leads connected to the inputs of said buffer devices.

19. A converter as in Claim 18, wherein said buffer devices comprise MOS transistors.

FIG. 1
PRIOR ART

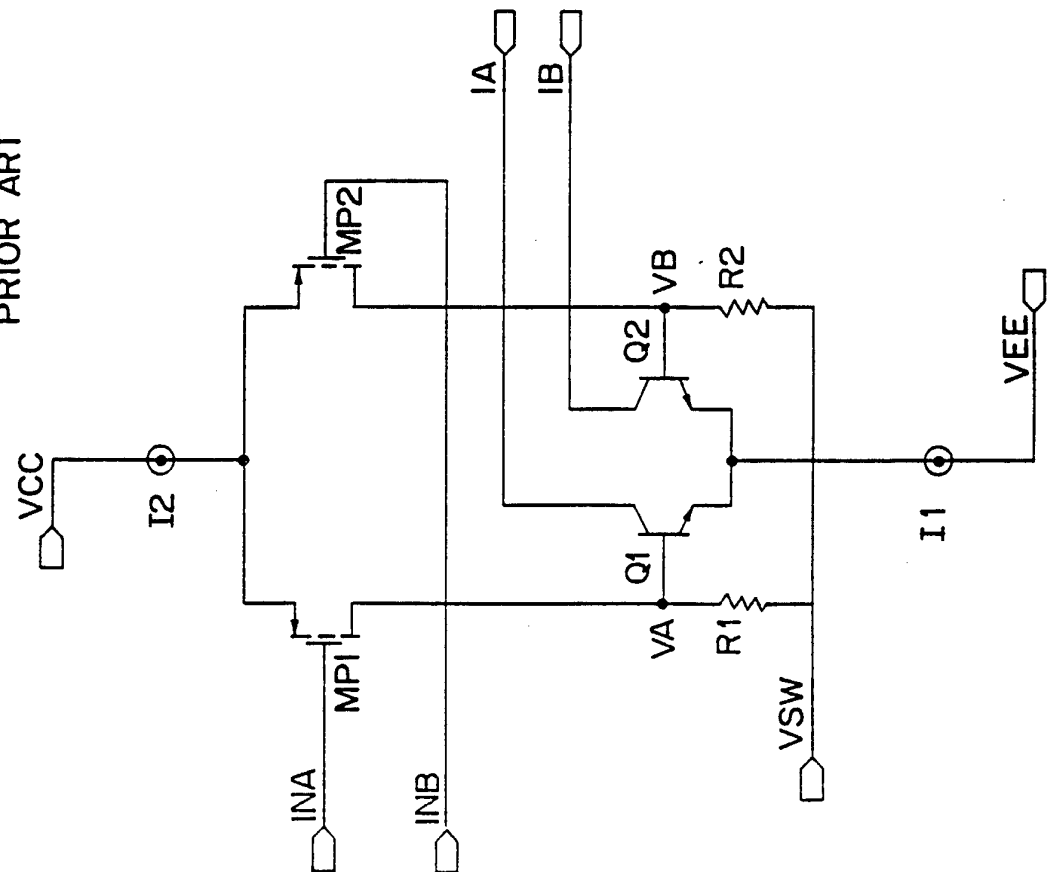
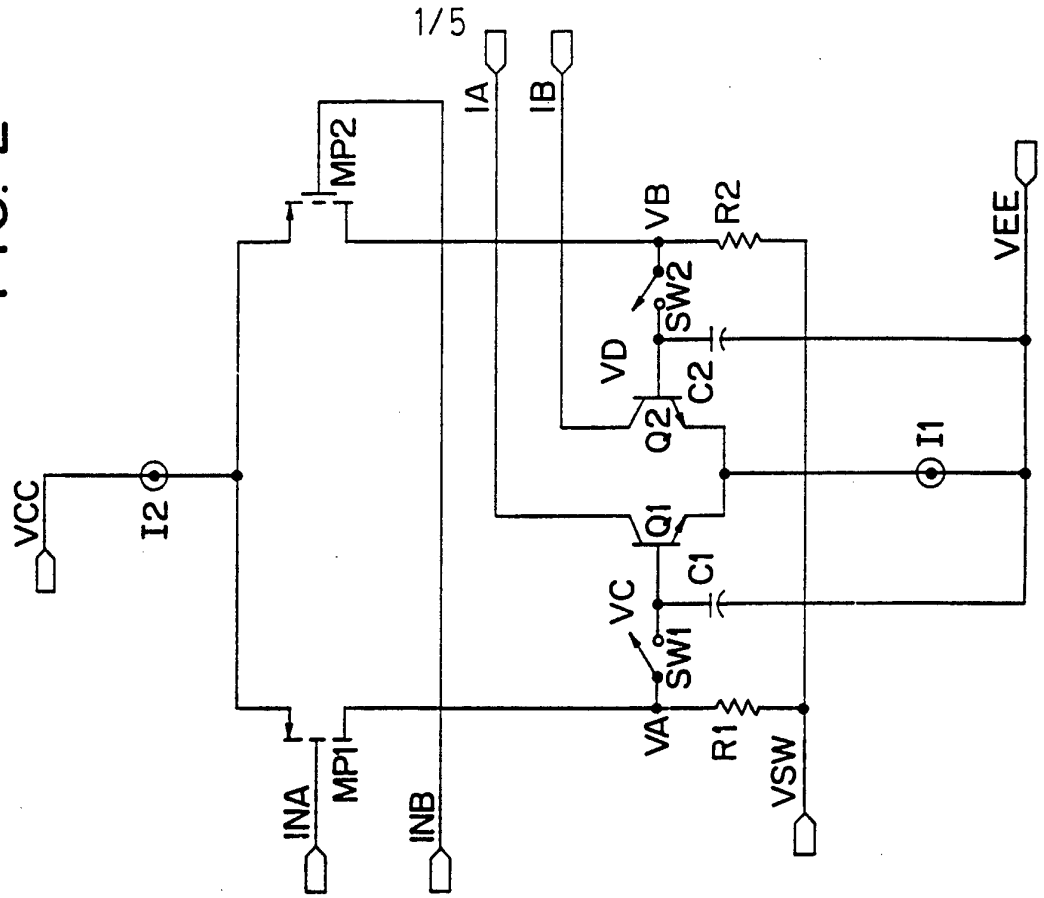


FIG. 2



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FIG. 4

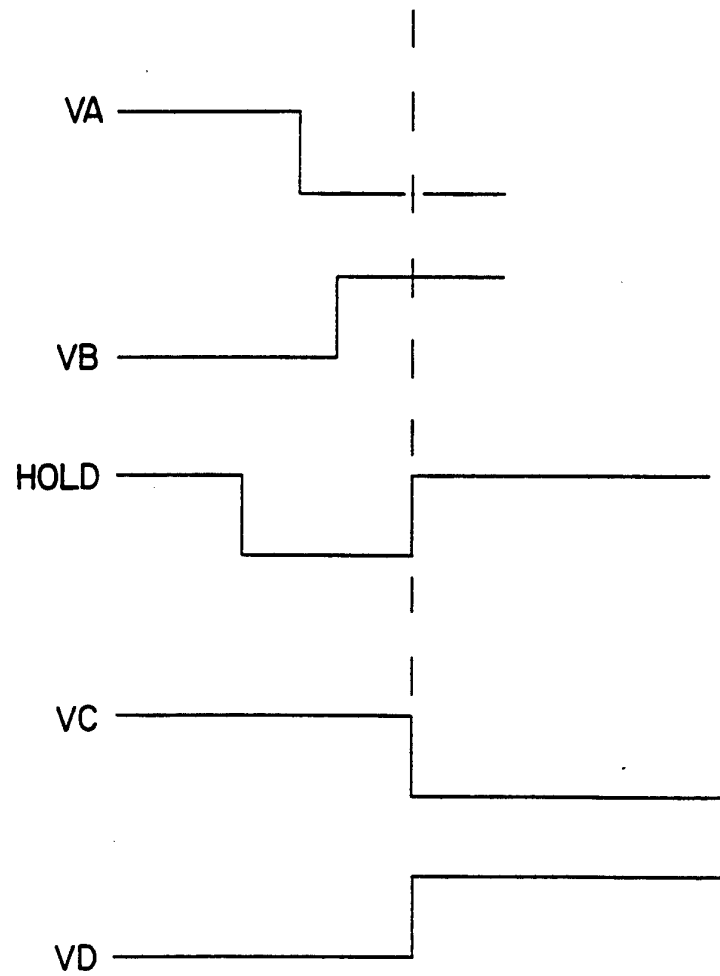


FIG. 5

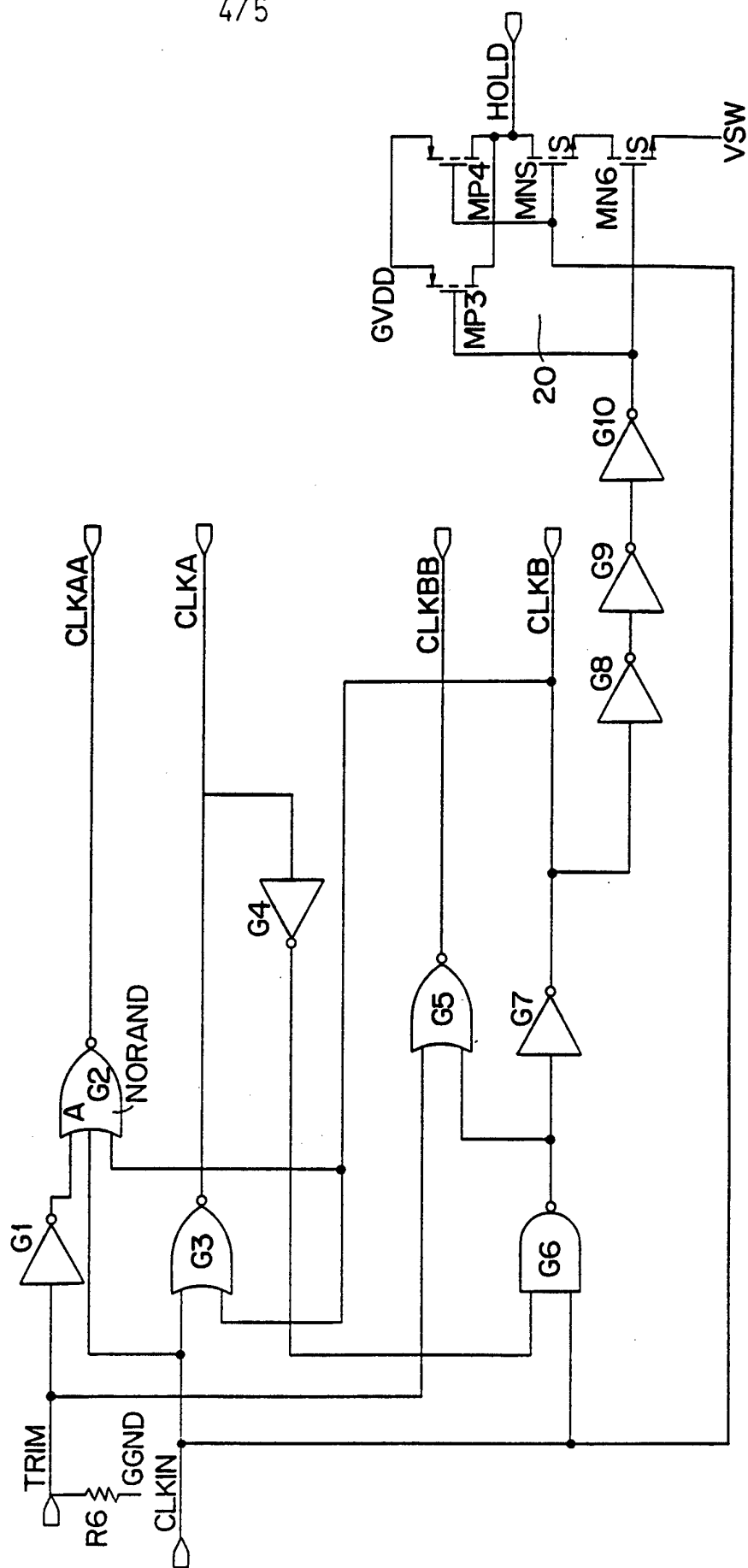
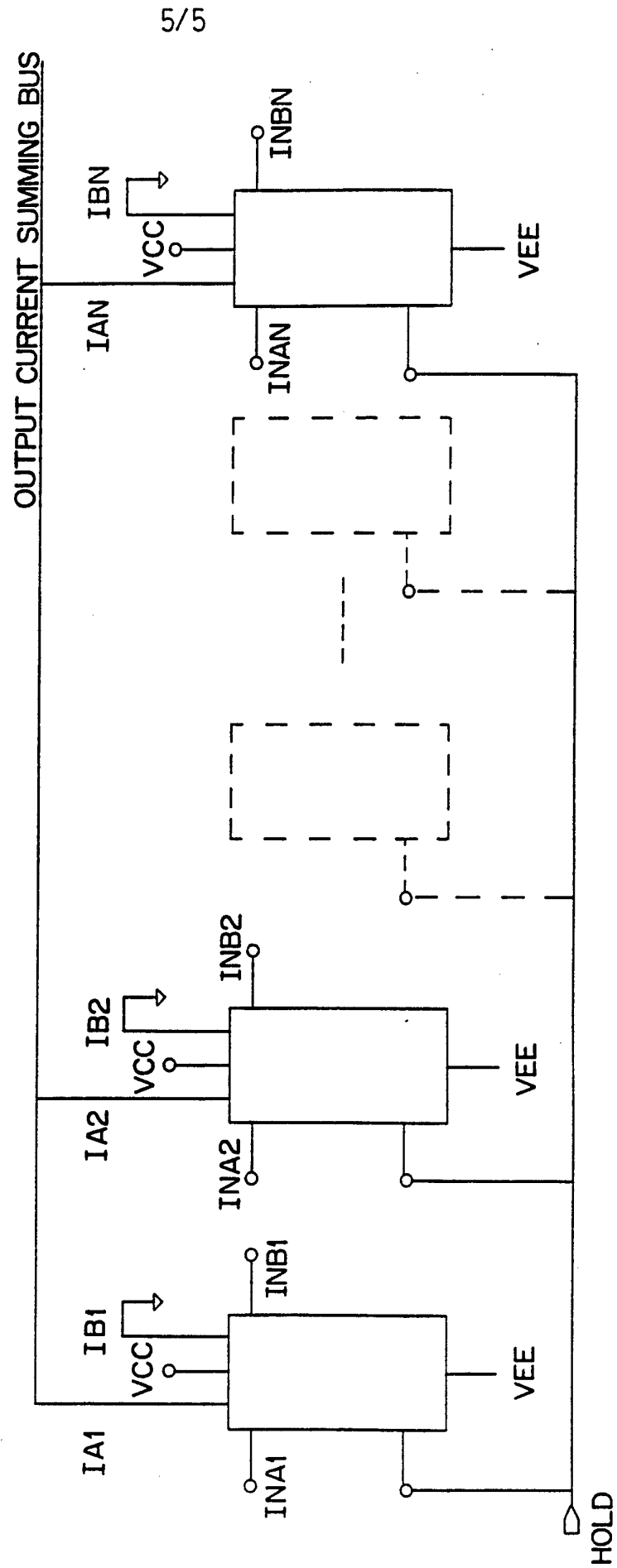


FIG. 6



INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER IPC(6) :H03M 1/80 US CL :341/153, 136; 307/570 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 341/153, 154, 136, 133, 144; 307/570, 571, 577, 248 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US, A, 5,148,164 (NAKAMURA ET AL.) 15 September 1992, see entire document.	1-19
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