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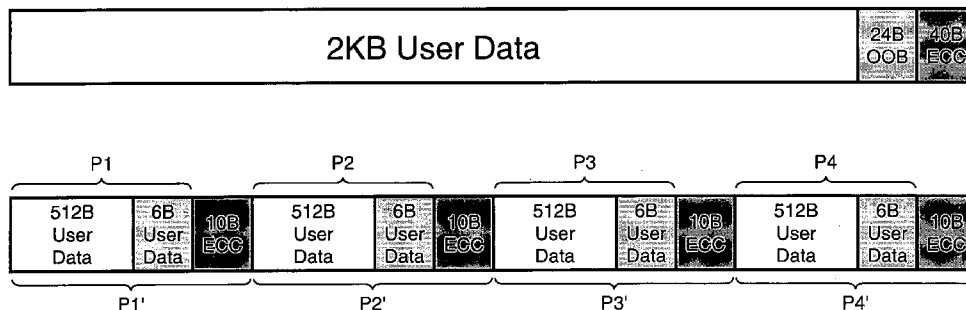
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(54) Title: METHOD AND DEVICE FOR RECONFIGURATION OF RELIABILITY DATA IN FLASH EEPROM STORAGE PAGES



(57) Abstract: A data processing system comprises a Flash memory (120) having a storage space partitioned in a plurality of storage pages (P). Each storage page comprises a memory reliability indicator indicative for the reliability of a storage region of the memory. Coupled to the Flash memory is a controller (150) for the Flash memory, that includes a facility for protecting data against errors occurring during storage in the Flash memory and for detecting and/or correcting errors in the data stored in the data, when retrieved from the Flash memory. A data processing unit (100) is coupled to the controller (150) that has access to a working page (P) comprising a first section of user data and a second section of management information, including a memory reliability indicator. The data processing system is characterized by a data re-arranging facility (105) for subdividing the data in the work page into a plurality of portions. Each portion comprises a part of the user data, and the last portion additionally comprises the management information including the memory reliability indicator. The controller (150) is arranged to subsequently generate redundant data for each of those portions and to write the content of the subsequent portions with its respective redundant data to the storage page (122).

WO 2008/068706 A1

METHOD AND DEVICE FOR TRANSFERRING DATA

FIELD OF THE INVENTION

The invention relates to a method for reading data from a Flash memory. The method further relates to a data processing device.

5 BACKGROUND OF THE INVENTION

Modern IC designs are more and more based on pre-existing functional units (IP-units) that are reused in a new combination. Such IP-units may comprise for example data processing units, storage units and interface units. Flash-memory, in particular NAND Flash memory is usually applied as a non-volatile storage medium.

10 Flash-memory is organized as large plurality (typically thousands) of storage blocks. Each storage block is subdivided in number (typically some tens, e.g. 32 or 64) of storage pages. The contents of the Flash-memory cannot be modified arbitrarily. Data can only be erased on a storage block basis and written on a storage page basis. Accordingly if new data is written to the Flash-memory, this is only possible if it is part of an entire storage
15 page that is written. Writing a storage page is only possible if that storage page was still erased. Otherwise, first the storage block to which the storage page belongs has to be erased.

An important difference between Flash-memory and other solid-state memories is that, when shipped, it is not guaranteed that all memory cells in a Flash-memory device operate correctly. It may be the case that some memory cells fail. During operation the
20 number of erroneous memory cells may even increase. Hence, redundant data is required to detect errors, and preferably to recover the data from failing memory cells. Redundant data will also be denoted here as ECC data.

To facilitate error correction the Flash-memory device reserves space for storage of ECC-data in addition to the data that was originally intended for storage (user
25 data). An ECC unit provides for the calculation of the ECC-data from the user data and for correcting the stored user data using the ECC-data. Various error correcting detecting methods are known, including for example Reed-Solomon and the Hamming method.

The earlier versions of Flash-memory typically have a storage page size of 528 bytes. The storage space includes room for storage of user data, for storage of ECC-data.

Outside the user data and the ECC-data, the storage pages of the Flash-memory also provide an additional space of a few bytes for storage of data known as Out Of Band data (OOB). Flash based file systems typically use this additional space to store metadata, like, for instance, information about the health of the page (defect or not). In addition the additional space is used by the manufacturer to store memory reliability data in order to mark a defective storage block. This location is the only one which is guaranteed to be correctly readable. The additional space may be more robust in the implementation of the Flash-memory. But this is not a requirement. It is however guaranteed by the manufacturer to be readable. Any device for which this is not the case will not be shipped.

The test procedure that each Flash-memory chip undergoes in the factory is quite elaborate to reliably detect faulty storage blocks. For example, during these tests the chips are stressed with higher and lower temperatures and higher and lower supply voltages. It is strongly advised to use the memory reliability data, as it may significantly reduce the chance of data loss.

In most older, small page Flash-memory chips the first 512 of the 528 bytes are reserved for user data, the next 6 bytes for OOB-data, and the last 10 bytes for ECC-data. One bad block marking scheme that is applied in those older Flash-memory chips, is that the 517th byte of the page (the sixth byte in the spare area), in the first and second page of each storage block indicates whether the storage block is unreliable. If this byte is unequal to 0xFF, the storage block should be considered unreliable. For 16-bit devices holds that the bad block marking is placed in the 256th and the 261th word (the first and the sixth word of the additional space) of the first and the second page of each block.

Commonly available Flash-memory IP is based on 512 + 16 byte pages. The interface accelerates reading and writing of Flash-memory by providing hardware ECC. The ECC hardware detects, and optionally attempts to correct errors.

However, most large Flash-memory devices are now only available in larger storage page sizes e.g. 2Kbytes, and even devices with 4 kB storage pages are under development. These modern Flash-memory devices are not compatible with the commonly available Flash-memory interface IP. Those larger page devices have another arrangement of OOB-data within the user data and ECC-data. For example in the 2Kbyte page the first 2048 is intended for user data, the next 24 bytes for OOB-data and the last 40 bytes for ECC-data.

The common way of overcoming this incompatibility is to treat the large page as a collection of small ones, each with it's own ECC.

This would necessitate transferring the OOB-data to a different location in the large page, which is not guaranteed to be correctly readable. Additionally software compatibility is lost.

5 SUMMARY OF THE INVENTION

It is a purpose of the invention to provide a method of storing the data provided by the IP-block in the Flash memory that prevents that the OOB-data is lost.

It is a further purpose of the invention to provide a data processing system that during operation provides for storage of the data while preventing that OOB data is lost.

10 According to the present invention these purposes are achieved by the method for reading data as claimed in claim 1, a method for storing data as claimed in claim 3 and the data processing system as claimed in claim 4.

The method according to claim 1 allows using an application suitable for use with a Flash memory having a relatively large page size, while reusing an error
15 correction/detection facility suitable for a Flash memory having a relatively small page size.

The method according to claim 3 allows using an application suitable for use with a Flash memory having a relatively large page size, while reusing an error protection facility suitable for a Flash memory having a relatively small page size.

20 Likewise the data processing system as claimed in claim 4 and claim 5 allows using an application suitable for use with a Flash memory having a relatively large page size, while reusing an error protection facility suitable for a Flash memory having a relatively small page size.

At startup the application usually scans the entire Flash memory, and for each storage block of the Flash memory it verifies the memory reliability indicator. During this
25 process a bad block table is constructed in a memory, e.g. a volatile memory, e.g. a DRAM. The bad block table may for example comprise a list of pointers to the bad blocks, or simply a list indicating for each block whether it is reliable or not.

If during operation the controller detects an amount of errors exceeding a predetermined level for a block, then the memory reliability indicator for said block is
30 updated. A new value for the indicator indicating that the block is unreliable is stored in the Flash memory. In the method and system according to the invention the reliability indicator has the same relative position in the work page as in the storage page. Accordingly the reliability indicator is reliably stored, as the manufacturer either uses a more robust

technology for storage of the original indicator, or extensive testing has guaranteed that this storage space is reliable.

The data arrangement obtained in this way is surprising. The skilled person aiming to reuse an error protection/detection/correction facility intended for a Flash memory with relatively small storage pages in data processing system with relatively large storage pages would divide the user data of the working page in equal portions. This would have the consequence that the reliability indicator is stored in the storage page at a relative position deviating from that of the position which is guaranteed to be reliable.

10 BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the inventions are described in more detail with reference to the drawing. Therein:

Fig. 1 schematically shows a prior art electronic device.

Fig. 2 shows a first storage convention for a first type of Flash-memory device.

Fig. 3 shows a second storage convention for a second type of Flash-memory device.

Fig. 4 shows a conventional way of storing data in a second type of Flash-memory device.

Fig. 5 shows a way of storing data in a second type of Flash-memory device with a method according to the invention.

Fig. 6 schematically shows a device according to the invention.

Fig. 7 shows a first method according to the invention.

Fig. 8 shows a second method according to the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Fig. 1 schematically shows a prior art electronic device, comprising a data-processing unit 10 for providing and/or consuming data and a Flash-memory 20. The data processing unit is coupled via a data bus 30 and control lines 40 to an interface 50 that controls the Flash memory 20. The interface 50 on its turn is coupled via a data bus 31 and control lines 41 to the Flash memory.

The data-processing unit 10 is for example a processor, e.g. a digital signal processor, but may alternatively be a memory, e.g. an SRAM.

The interface 50 and the Flash-memory 20 are designed to exchange data via the data bus 31. The data is stored in storage pages of the Flash-memory according to the format as shown in Fig. 2. The storage pages have a size of N data-units. In this case N = 528, wherein the data units are bytes. In the storage page a first section with 512 bytes is reserved for user data, a second section of in total 6 bytes includes management data including memory reliability data (denoted as OOB) and a third section is reserved for 10 bytes of redundant data. The redundant data may include any data that allows for detection and/or correction of errors in the user data. The redundant data is denoted as ECC in the Figures. The memory reliability data may include an indication indicative for the reliability of the location where the storage page is stored in the Flash-memory, or for a set of locations (e.g. a block) comprising the storage page. The indication is usually provided by the manufacturer of the memory and based on a rigorous testing procedure. However, an indication originally indicating that a storage location is reliable may be assigned a value indicative for unreliability if the data processing unit 10 or an application being processed thereon detected unrecoverable errors occurring when attempting to read the page.

Flash-memory having a page size of 528 bytes has been generally used for a long time. However, gradually Flash-memory types with larger sized storage pages (macro-pages) have been developed. Fig. 3 shows by way of example the layout of a storage-page of such a more modern Flash-memory. In that example the storage-page has a total size of 2112 bytes and comprises a first section of 2048 byte for user data, a second section of 24 bytes for management data, including the reliability data, and a third section of 40 bytes for redundant data.

It is desirable to be able to use an existing interface with newer types of Flash-memory in order to prevent that each unit has to be developed from scratch.

Fig. 4 shows the common way in which this is achieved. Therein simply a sequence of data packets (here 4 packets) that are each formatted in the format as shown in Fig. 2 for Flash memory using the smaller page size are stored in the macro-page. This has the disadvantage that the memory reliability data is stored in a location that is less reliable than the location selected by the manufacturer.

Fig. 6 shows an embodiment of a data processing system according to the invention. The data processing system comprises a Flash memory 120 having a storage space partitioned in a plurality of storage pages. Each storage page comprises a memory reliability indicator indicative for the reliability of a storage region of the memory.

An interface 150, also denoted as controller, for the Flash memory is coupled thereto that includes a facility for protecting data against errors occurring during storage in the Flash memory 120 and for detecting and/or correcting errors in the data, when retrieved from the Flash memory 120.

5 A data processing unit 100 is coupled to the controller 150. The data processing unit has access to a work page P. The data processing system further includes a data re-arranging facility 105 for subdividing the data in the work page P into a plurality of portions P1, P2, P3, P4. Each portion comprises a part of the user data, and the last portion additionally comprises the management information including the memory reliability
10 indicator. The controller 150 has a buffer 151 for storage of a portion. The controller 150 extends the portions P1, P2, P3, P4 with respective redundant data and writes these extended portions P1', P2', P3' and P4' to a buffer 121 of the Flash memory. If this buffer is full the Flash memory writes the content to one of its storage pages 122.

In the embodiment shown the work page P comprises 2048 bytes of user data and 24 bytes of management data. When writing to the Flash memory, the data is rearranged
15 by rearrangement facility 105 in 4 portions wherein the first three portions P1, P2, P3 each comprise 518 bytes of user data. The last of the four portions P4 comprises 494 bytes of user data and the 24 bytes of management information.

Each time a portion is stored into the buffer 151 of the controller 150, the
20 controller 150 calculates a number of 10 redundant bytes. The data finally stored in the pages 122 of the Flash memory is formatted as shown in Fig. 5. Accordingly the reliability indicator has the same relative position in the storage space as in the work page.

An application driven by processing unit 100 will usually generate a bad block table during start-up of the data processing system. In the data processing system of the
25 present invention the controller 150 for the Flash memory 120 operates with pages having a relatively small size as compared to the size of the storage pages of the Flash memory. This has the advantage that the controller 150 only needs to transfer the part of the content of the storage page 122 that comprises the management data to obtain the reliability indicator. This saves time at start-up.

30 When reading, the controller 150 is arranged to retrieve the content of subsequent extended portions P1', P2', P3' and P4' of a storage page, and applying error detection and/or error correction to each portion. The data re-arranging facility 105 combines the corrected data of the extended portions into a work page P for use by the data processing

unit 100. Therein, the corrected user data is contiguously arranged, and the reliability indicator has the same relative position as in the storage page P'.

Fig. 7 shows a first embodiment of a method according to the invention for reading data from a Flash memory.

5 In step S1 a counter **n** is initialized at 1
 In step S2 portion **n** is read from the buffer 121 of the Flash memory.
 In step S3 error detection/correction is applied to the portion **n** and the checked /corrected data is temporarily stored, for example in the work page.
 In step S4 the counter is incremented by one.
10 In step S5 it is verified whether the value of the counter is greater than a value 2^M .

 If this is the case control flow continues with step S6.

 Otherwise control flow returns to step S2.

 In step S6 the data is re-arranged to the format shown in Fig. 3.

15 The steps S1 to S6 may be repeated after step S6 is completed.

 Since the ECC-data is no longer required after error correction has taken place no additional buffer space is required for the re-arrangement than the space already used as work-page. Preferably rearrangement already takes place on the fly, when in step S3 the corrected data is stored.

20 In that step the user data for portion **n** may immediately be written after the user data for portion **n-1**. When writing the last portion, again writing starts at the first free location after the space written by the but one last portion. After writing the first 464 bytes of the last portion a space of 30 bytes is reserved. Subsequently the 24 bytes of management data is written to the work page, and then the last 30 bytes of user data in the last portion are
25 written in the reserved space.

 Fig. 8 shows a method for storing data from a work page into a storage page of a Flash memory.

 In step S11 a counter **n** is initialized at 1.

 In step S12 a portion **n** of the user data is selected from the work-page.

30 In step S13 redundant data is created from the user data for error protection purposes.

 In step S14 the user data and the redundant data is written to the storage page.

 In step S15 the counter **n** is incremented by 1.

In step S16 it is verified whether the value of the counter is less than a value 2^M .

If this is the case control flow returns to step S12.

Otherwise control flow continues with step S17.

5 In step S17a data packet is created from portion 2^M of the work-page, comprising a first amount of user data, here 464 bytes, the management data, here 24 bytes, and a second amount of user data, here 30 bytes.

In step S18 redundant data is created from the user data and management data for error protection purposes.

10 In step S19 the data packet including the redundant data is written to the storage page.

Now the data is re-arranged to the format shown in Fig. 5, so that the reliability indicator has the same relative position as in the work page.

15 An embodiment of the invention is described above that comprises a Flash memory with storage pages of size 2048 B (excl. 24 bytes of management data and 40 bytes of redundant data and a controller that provides for error correction of pages of size 512 B (excl. 6 bytes of management data and 10 bytes of redundant data).

20 The invention is however equally applicable to other data processing systems where the controller operates on pages having a size smaller than that of the Flash memory controlled by it.

When using page formats as shown in the table below, any controller of type k, may be used with any Flash memory of type $> k$. Therein the column "user data" shows the number of user data bytes, the column "man data" shows the number of management data bytes, and the column "red. data" shows the number of redundant data bytes.

25

	User	Man.	red.
Type	data	data	data
1	512	6	10
2	1024	12	20
3	2048	24	40
4	4096	48	80

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Parts of the system may implemented in hardware, software or a combination thereof. For example, the controller 150 may be implemented by a

generally programmable microcontroller which is suitably programmed. Alternatively however, the controller may be partly or completely be implemented by dedicated hardware. It may for example comprise dedicated hardware to rearrange the data on the fly. The various components may be provided as a single integrated circuit. Alternatively the components
5 may be available as a chip set. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in a claim. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed general purpose processor. The
10 invention resides in each new feature or combination of features.

CLAIMS:

1. Method for reading data from a Flash memory having data stored in a plurality of storage pages, each storage page comprising user data, redundant data and management data including a reliability indicator indicative for the reliability of a storage region of the memory, the method including the steps of:

- 5 - reading the storage page in subsequent portions, each portion comprising a part of the user data and a part of the redundant data, and a last of the portions comprising in addition the management data with the reliability indicator,
- applying error detection/correction to each portion,
- combining the corrected data of the portions into a work page wherein the
- 10 corrected user data is contiguously arranged, and the reliability indicator has the same relative position as in the storage page.

2. Method for reading data according to claim 1, wherein the redundant data is stored as a contiguous block of data in the work page.

15

3. Method for storing data from a work page into a storage page of a Flash memory, the data from the work page at least comprising a section of user data and management data including a memory reliability indicator, the method comprises the steps of:

- 20 - subdividing the work page into a plurality of portions, each portion comprising a part of the user data, and the last portion additionally comprising the memory reliability indicator,
- applying error protection to each portion in order to create redundant data,
- storing the portions together as subsequent sections into a storage page
- 25 wherein the reliability indicator has the same relative position as in the work page.

4. A data processing system comprising:

- a Flash memory (120) having a storage space partitioned in a plurality of storage pages (P'), each storage page comprising management data including a memory

reliability indicator indicative for the reliability of a storage region of the memory,

- a controller (150) for the Flash memory, coupled to the Flash memory including a facility for protecting data against errors occurring during storage in the Flash memory and for detecting and/or correcting errors in the data stored in the data, when

5 retrieved from the Flash memory,

- a data processing unit (100) coupled to the controller (150) that has access to a working page (P) comprising a first section of user data and a second section of management information, including a memory reliability indicator,

10 characterized by a data re-arranging facility (105) for subdividing the data in the work page into a plurality of portions, each portion comprising a part of the user data, and the last portion additionally comprising the management information including the memory reliability indicator, and in that the controller (150) is arranged to subsequently generate redundant data for each of those portions and to write the content of the subsequent portions with its respective redundant data to the storage page (122).

15

5. A data processing system according to claim 4 wherein the controller (150) is further arranged to retrieve subsequent portions of the data obtained from the storage page (122) and to apply error detection and-or correction to each portion, wherein the data re-arranging facility is further arranged for combining corrected data of the portions into a work
20 page (P) for use by the data processing unit, wherein the corrected user data is contiguously arranged, and wherein the reliability indicator has the same relative position as in the storage page (122).

1/4

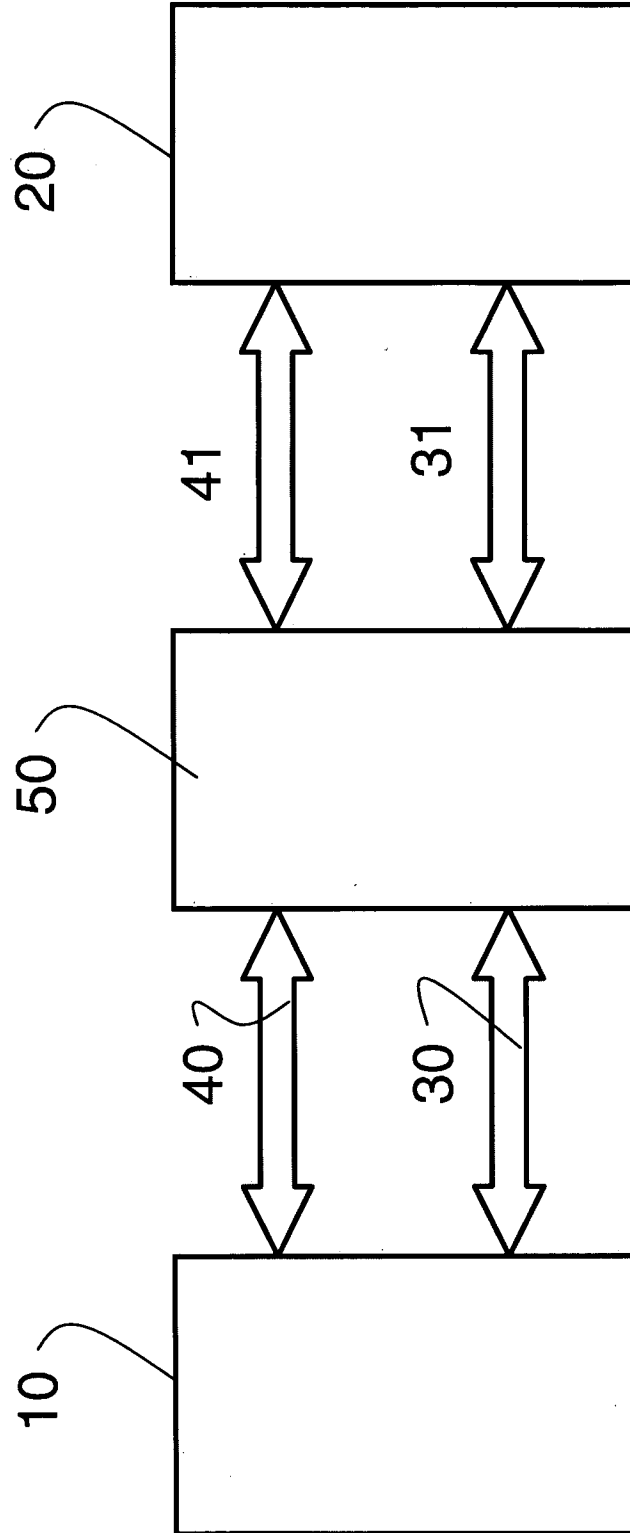


FIG. 1

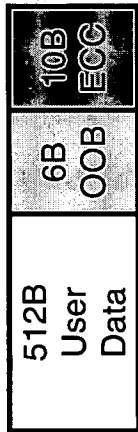


FIG. 2

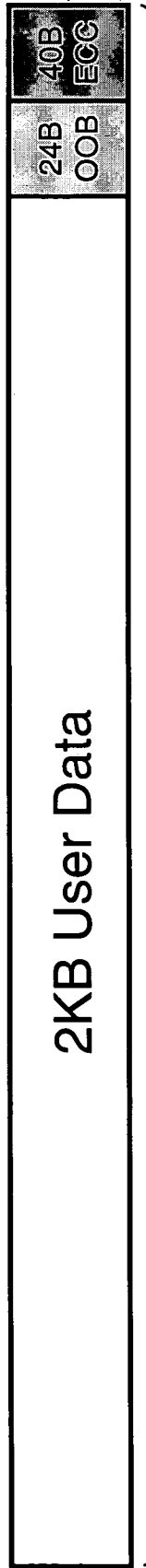


FIG. 3

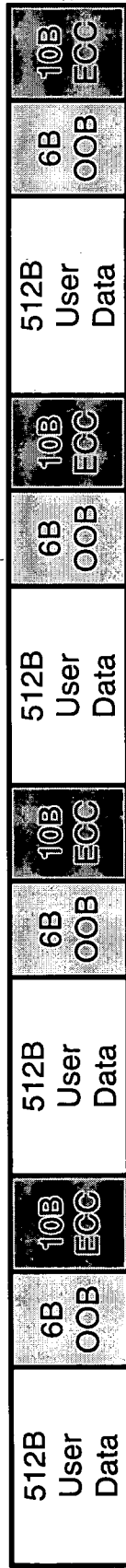


FIG. 4

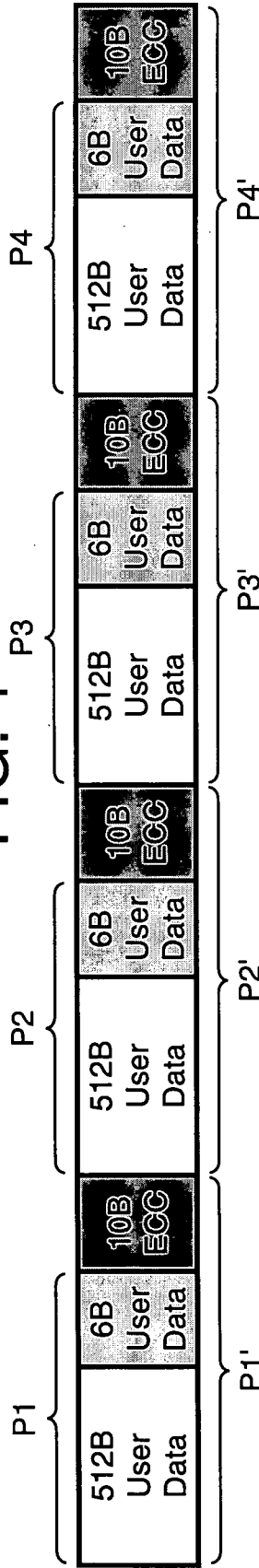


FIG. 5

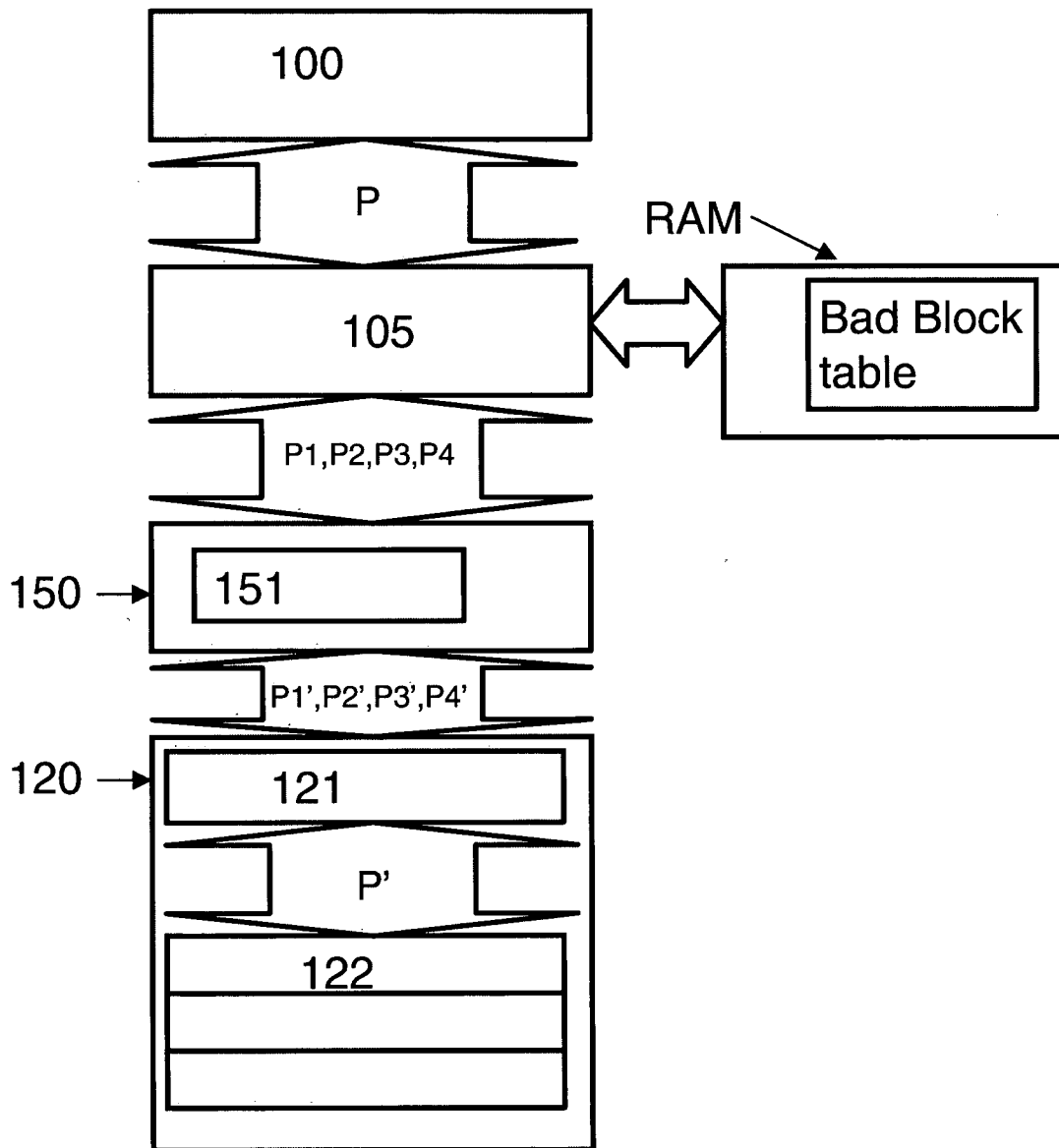


FIG. 6

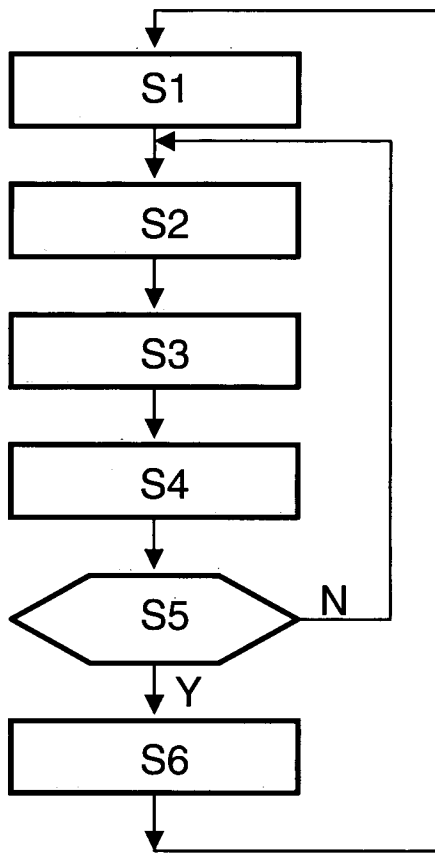


FIG. 7

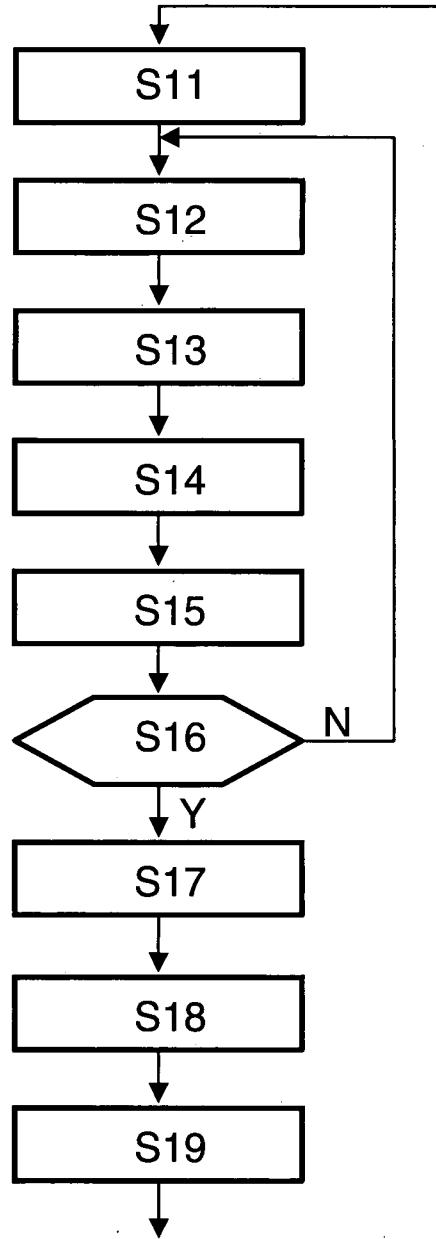


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2007/054896

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C29/00 G06F11/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 041 001 A (ESTAKHRI PETRO [US]) 21 March 2000 (2000-03-21) column 5, line 23 - line 45 column 7, line 51 - column 9, line 64; figure 4 -----	1, 3, 4
A	US 2006/114726 A1 (KOZAKAI KENJI [JP] ET AL) 1 June 2006 (2006-06-01) abstract; figures 4-11 -----	1, 3, 4
A	EP 1 577 774 A (NIPPON ELECTRIC CO [JP]) 21 September 2005 (2005-09-21) abstract; figure 7 -----	1, 3, 4

Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search

17 March 2008

Date of mailing of the international search report

26/03/2008

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Wolff, Norbert

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/IB2007/054896

Patent document cited in search report	Publication date	Patent family member(s)	Publication date									
US 6041001	A	21-03-2000	NONE									
US 2006114726	A1	01-06-2006	NONE									
EP 1577774	A	21-09-2005	<table style="width: 100%; border: none;"> <tr> <td style="width: 15%;">CN</td> <td style="width: 30%;">1658163 A</td> <td style="width: 55%;">24-08-2005</td> </tr> <tr> <td>JP</td> <td>2005234883 A</td> <td>02-09-2005</td> </tr> <tr> <td>US</td> <td>2005185476 A1</td> <td>25-08-2005</td> </tr> </table>	CN	1658163 A	24-08-2005	JP	2005234883 A	02-09-2005	US	2005185476 A1	25-08-2005
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