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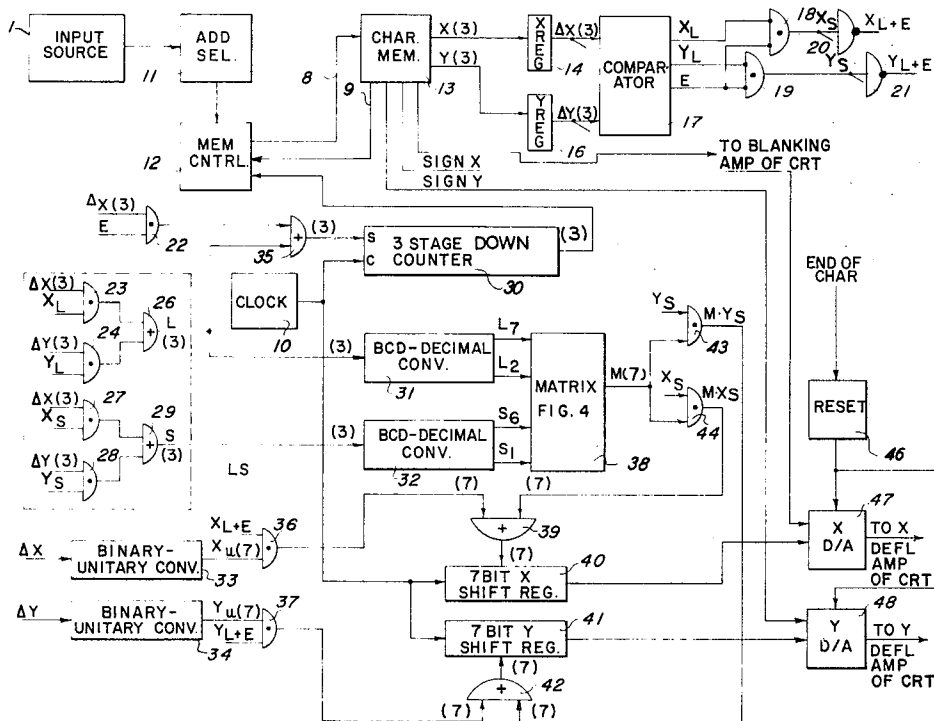
3,533,096	10/1970	Bouchard.....	340/324 A
3,329,948	7/1967	Halsted	340/324 A

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Apparatus for generating characters or symbols on the

screen of a cathode ray tube by deflecting the electron beam along a predetermined path in accordance with signals derived from a character memory. When the deflection increments along the X and Y axes are equal, signals are generated in binary to unitary converters for input to X and Y shift registers which in turn generate bit streams to be applied to digital to analog converters. The bit streams are integrated in the digital to analog converters and strokes generated. The strokes are then applied to the deflection amplifiers of the cathode ray tube. When the deflection increments along the X and Y axes are unequal, the smaller increment is determined by a comparator circuit. The smaller and larger increments are then routed to binary to decimal converters and thereafter to a matrix circuit where signals are generated for application to the shift register having the smaller increments. In this mode of operation the larger increment is loaded into the shift register via a binary to unitary converter as in the case where the increments are equal.

6 Claims, 5 Drawing Figures



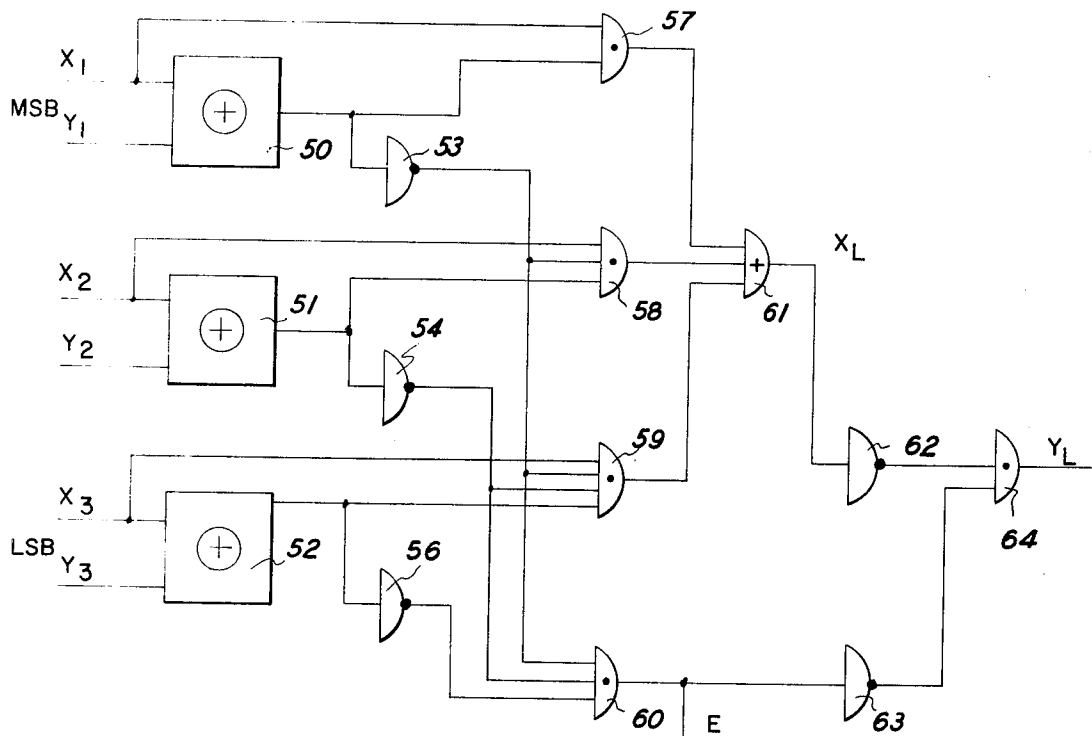
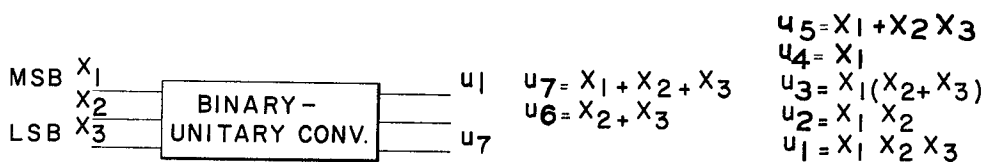
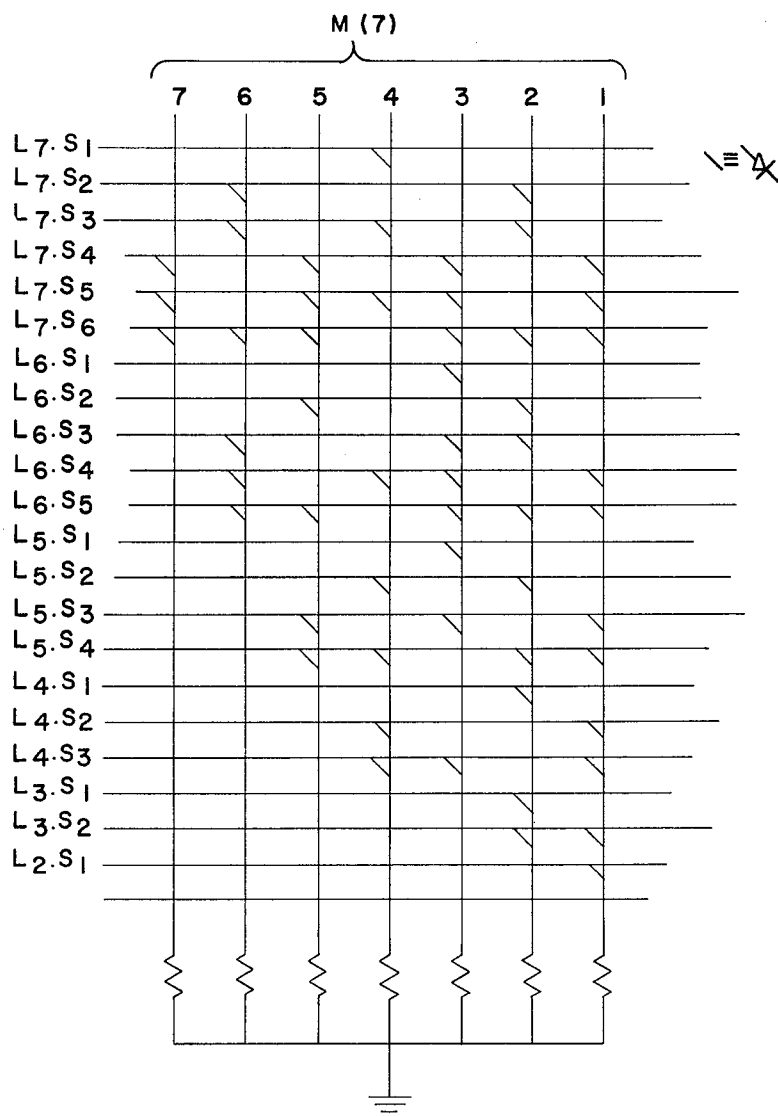


FIG. 2



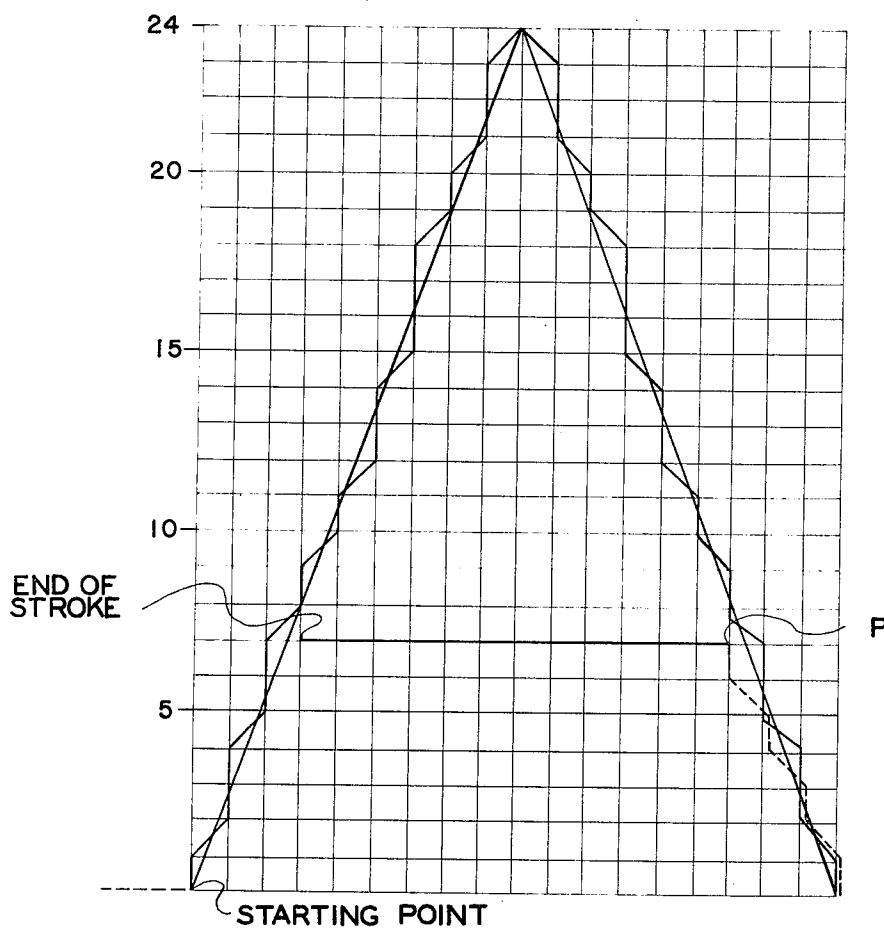
LOGIC EQUATIONS FOR
 BINARY- UNITARY CONVERTER

FIG. 3



—AN IMPLEMENTATION FOR MATRIX 38—

FIG. 4



Δx	Δy	S_x	S_y	B
3	0	1	1	0
2	6	1	1	1
3	7	1	1	1
2	7	1	1	1
2	4	1	1	1
2	4	1	0	1
2	7	1	0	1
3	7	1	0	1
2	6	1	0	1
3	7	0	1	0
7	0	0	0	1
5	0	0	0	1
EOC	0	0	0	0

14 x 9 = 117 BITS

EXAMPLE OF CHARACTER CODING

FIG. 5

ELECTRONIC DISPLAY DEVICE

This invention relates to character generating apparatus and, more particularly, to an electronic character generator in which the electron beam of a cathode ray tube is deflected in a predetermined path in order to form characters or symbols on the tube screen.

BACKGROUND OF THE INVENTION

With the advent of the computer and other rapid data transmission devices, there has come a need for systems which can effectively and speedily display the intelligence from these sources. Improvements in electro-mechanical printers have substantially increased their speed. Nevertheless, because of problems of mechanical inertia, printers soon reach a practical upper limit speed. To fill the need for fast responding display devices a number of solely electronic devices have been proposed. Among these are character generators with matrix, bit stream or stroke character encoding employing a cathode ray tube.

Character generation by means of a cathode ray tube has the objective of displaying line traces on the face of the tube or screen. The line traces may represent vectors, alphanumeric characters or symbols. To provide such a display, the electron beam of the cathode ray tube is deflected from point to point along a predetermined path. To deflect the electron beam along the predetermined path, it is necessary at each point of direction change in the path to apply the proper deflection signals to the horizontal (X-axis) and vertical (Y-axis) deflection circuits of the cathode ray tube to move the electron beam to the next point of deflection change. In digitally operated display systems these deflection signals are stored in the character memory and applied to the input circuits of the cathode ray tube at timed intervals. Digitally operated display systems of the past required a great deal of programming and calculations of values of deflection signals in order to drive the electron beam across the tube screen. In addition, depending on the number and type of symbols to be generated, digital storage and logic circuits were generally quite numerous. Also the deflection control circuits of these prior art display systems had the disadvantages of requiring precision components as well as being difficult to control.

In these prior art systems numerous current sources such as transistors and balancing resistors were utilized in order to generate line segments of characters or symbols. Since a group of transistors no matter how carefully manufactured inherently have different operating characteristics, compensating circuitry is required to offset their differing characteristics. The effects of drift and the difficulty of maintaining equal character stroke intensity are also disadvantages frequently encountered in these systems. These deficiencies of prior art systems served not only to increase the complexity but also the expense of the display apparatus.

Accordingly, it is an object of this invention to provide an improved and inexpensive character generating apparatus.

It is another object of this invention to provide a character generating apparatus requiring less current sources for generating character strokes.

It is still another object of this invention to provide a character generating apparatus wherein all the character strokes are confined to a grid simplifying the coding of stroke signals.

It is further object of this invention to provide a character generating apparatus wherein the electron beam of the cathode ray tube is automatically deflected to trace a symbol or character by a data bit stream input to circuits which control tube deflection.

SUMMARY OF THE INVENTION

In accordance with principles illustrative of this invention, a cathode ray tube is advantageously provided for character generation. Stroke generators activate the deflection circuits of the cathode ray tube by delivering fixed voltage pulses to current sources which in turn charge or discharge capacitors. The strokes are coded as binary bit streams for the X and Y axes. A binary 1 bit causes a fixed amount of charge to be deposited or removed from the capacitor associated with appropriate coordinates of X and Y. A binary 0 bit causes no change in the quantity of charge on the respective capacitor. As is well known in the art, the amount of charge on a capacitor determines the velocity of the cathode ray tube electron beam in the coordinate associated with that capacitor.

A received character code is converted into an address which is used to access a memory storing character stroke information bits. These information bits are processed in accordance with the inventive principles to derive X and Y incremental bit streams. The bit streams are utilized to generate strokes forming the different characters.

After processing, the incremental X and Y bit streams are loaded into respective shift registers. The bits from the shift registers are then clocked out for input into integrating digital to analog converters. The system is designed so that all bits of the larger of the X and Y increments, or all the bits of both increments if the increments are equal in magnitude, are packed toward the output end of the shift register. Logic circuits are provided to determine if the increments in X and Y are equal or if one is larger than the other. Binary to unitary converters assemble the bit streams where the number of 1's are numerically equal to the stroke length and all the 1's appear in lower order position. The shift registers are loaded from the binary to unitary converters only if their stroke lengths magnitudes are equal or larger. However, if there is an inequality in stroke lengths the shift register for the smaller increment is loaded from a matrix by way of binary to decimal decoders which indicate the magnitude of the larger and smaller increments. In addition, the invention provides means for minimizing digitization error and means for maintaining the intensity of each stroke substantially constant.

DESCRIPTION OF THE DRAWING

The foregoing will be more readily understood upon a reading of the following description in conjunction with the drawing in which:

FIG. 1 is a block schematic diagram of a preferred embodiment of the present invention;

FIG. 2 is a schematic diagram showing the comparator circuit for determining the magnitude of the X or Y increment;

FIG. 3 shows the logic equations of the binary to unitary converter;

FIG. 4 shows the matrix circuit which generates a bit configuration for the smaller increment; and

FIG. 5 shows a sample character and the code for its generation.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1 there is depicted a block schematic diagram of an illustrative embodiment incorporating the principles of this invention. All of the circuitry to implement this embodiment as well as timing is well known to one of ordinary skill in the art and no detailed description thereof will be given. Six binary bits of information from an input source 1, such as a computer, data keyboard, magnetic tape, etc., are fed into address selector 11. The six binary bits are character selection bits and may be in ASCII, EBCDIC or other standardized code. In address selector 11 the six bit binary code is translated into a nine bit binary code designating the starting address for each character in character memory 13. This translation may be done by any of various well known prior art techniques. Memory control 12 controls the transmission of the translated address to character memory 13. It is to be noted that any codes specified herein are intended to be illustrative and not limiting, since it will occur to those skilled in the art that other codes could be used depending upon the number of characters or symbols desired and the amount of storage available. Information for controlling the generation of a character is stored as a block of contiguous words, each word corresponding to a stroke. The aforementioned translated address defines the first word of the block.

Memory control 12 receives the nine binary bit address code from address selector 11 and controls the accessing of character memory 13. Memory control 12 addresses character memory 13 via line 8 and monitors the outputs from character memory 13 via line 9. At the output of character memory 13 there is a nine binary bit word comprising three bits for X, 3 bits for Y, and one bit each for sign X, sign Y, and blanking. The number in parentheses in FIG. 1 after the X and Y at the output of character memory 13 denotes that there are three conductive lines connecting the X and Y increments to their respective registers. Similarly the numbers in parentheses appearing elsewhere in FIG. 1 denote the number of lines into and out of the indicated block. Moreover, in order to simplify the schematic the actual number of gates are shown representatively by only one gate in most instances. It is therefore understood that where there are a number of lines into a gate there are a number of gates for each line.

The X and Y bits from memory 13 are fed to buffer registers 14 and 16 respectively and the sign X and sign Y bits are fed to the X and Y digital to analog converters 47 and 48 respectively. The blanking bit from character memory 13 is fed directly to the cathode ray tube blanking amplifier (not shown). From buffer register 14, ΔX bits are fed to comparator 17, binary to unitary converter 33 and AND gates 22, 23 and 27. ΔY bits are fed from buffer register 16 to comparator 17, binary to unitary converter 34 and AND gates 24 and 28. Comparator 17 determines whether ΔX or ΔY is larger (X_L and Y_L respectively) or if they are of equal magnitude. When the magnitudes of ΔX and ΔY are equal, the outputs $X_L + E$ and $Y_L + E$ of inverters 20 and 21 are logically true. The outputs of the binary to unitary converters 33 and 34 are then loaded into the X and Y shift registers. The function of the binary to unitary convert-

ers is to form bit streams for insertion into registers 40 and 41 where the number of 1's are numerically equal to the stroke length and all the 1's appear in the lower order positions. For example, $X = 5 = 101$ provides the output 0011111. FIG. 3 shows the logic equations of the outputs resulting from the ΔX increment input to the binary to unitary converter. The logic circuitry to implement these equations is simple combinational logic well known to any skilled logic designer. X_1 is the most significant bit (MSB) and X_3 is the least significant bit (LSB) of the ΔX increment. Through these logic equations the bit stream is formed in the desired manner. Similar equations are provided for the ΔY increment input. The system is designed so that all the bits of the larger increment or all the bits of both increments when they are equal in magnitude are packed toward the output end of the shift register, u_7 being the bit position closest to the output end of the shift register. In FIG. 1, $X_u(7)$ is the output of binary to unitary converter 33 in accordance with the equations of FIG. 3. The bits of the smaller increment are positioned so that the generated stroke will have minimum digitization error. For instance, the stroke $\Delta X = 5$, $\Delta Y = 3$ will appear in shift registers 40 and 41 respectively as:

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0011111
0010101

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Packing the bits toward the output end of the shift registers minimizes the time it takes to generate a stroke and thereby increases exposure for a fixed character generation rate.

Assuming that ΔX and ΔY have equal magnitudes, output shift registers 40 and 41 are loaded from binary to unitary converters 33 and 34 respectively. The output from binary to unitary converter 33 is seven bits designated as X_μ and is fed to AND gates 36 along with a signal $X_L + E$ from inverter 20. The outputs from AND gates 36 are then applied to OR gates 39 which provide seven lines to shift register 40. The output from binary to unitary converter 34 is designated Y_μ and is fed to AND gates 37 together with a signal $Y_L + E$ from inverter 21. The outputs from gates 37 are then applied to OR gates 42 which provide seven lines to shift register 41. Shift registers 40 and 41 are each then pulsed by clock 10 until all "ones" have been shifted out of the registers.

The three stage down counter 30 is initially loaded by way of OR gates 35 with the length of the larger, or equal, increment. After each clock pulse, counter 30 counts down one count until all three stages of the counter are set to logical zero. The output from counter 30 is applied to memory control 12 where it serves to generate an end of stroke signal which conditions memory control circuits therein to route signals to character memory 13 to begin the next stroke.

The bit stream clocked out of X shift register 40 is fed to digital to analog converter 47 where it is integrated and converted to strokes which are in turn sent to the X deflection amplifier of the cathode ray tube (not shown). Simultaneously, a Y bit stream is clocked out of Y shift register 42 and sent to digital to analog converter 48 where it is integrated and converted to strokes which are in turn sent to the Y deflection amplifier of the cathode ray tube (not shown).

An end of character pulse is fed from memory control 12 to reset circuit 46 when all the strokes of the character have been written. Reset circuit 46 in turn feeds end of character pulses to X and Y digital to ana-

log converters 47 and 48 to reset the converters in preparation for the start of new character. The sign X and sign Y inputs to the digital to analog converters are applied at appropriate times to change the vertical and horizontal direction of the electron beam movement.

When either ΔX or ΔY is the smaller increment, as determined by comparator 17, the path taken by signals representing the smaller increment is through binary to decimal converters 31 and 32 and matrix 38. Assuming for purposes of illustration that ΔX is the smaller increment, then at the output of comparator 17 there is a signal only on conductor Y_L (Y is larger). From the output of AND gate 18 a signal X_S (X is smaller) is fed to inverter 20. Signal Y_L is fed to one input conductor of AND gates 24. At the other input conductor of AND gates 24 is a signal ΔY fed from buffer register 16. Since these two signals are in coincidence, outputs from AND gates 24 are fed to OR gates 26. There are two sets of inputs to OR gates 26; one from AND gates 23 and the other from AND gates 24. As X is smaller, in the case at hand, logical zero signals appear at the input conductors designated X_L of AND gates 23. The signals from OR gates 26 contain the larger increment and are applied to counter 30 and to binary to decimal converter 31. At the same time that Y_L signals are applied to the input conductors of AND gates 24, signals X_S are applied to the inputs of AND gates 27. At the other input conductors of AND gates 27, a ΔX signal is applied. These two sets of signals being in coincidence provide output signals from AND gates 27 to OR gates 29. Signals will appear at the outputs of OR gates 29 if there are inputs to it from either AND gates 27 or from AND gates 28. Since X is smaller, there is no Y_S signal applied to the conductors of AND gates 28 and therefore logical zero outputs therefrom. OR gates 29 then pass the signals from AND gates 27 to binary to decimal converter 32. The situation at this time is signals representing the larger increment appearing at the inputs to binary to decimal converter 31 and signals representing the smaller increment appearing at the inputs to binary to decimal converter 32. The outputs from the binary to decimal converters 31 and 32 indicate the magnitude of the larger and smaller increments, respectively. Each binary to decimal converter provides at its output a signal on only one of its six output lines. For example, if the magnitude of the larger increment is five, there is a signal on line L_5 . If the magnitude of the smaller increment is three, there is a signal on line S_3 . These lines are inputs to matrix 38, where they are logically combined to form all 27 possible combinations of unequal increment values.

Matrix 38, shown in FIG. 4 and described in more detail hereinafter, provides at its output a seven binary bit configuration which is loaded into the output shift register for the coordinate with the smaller increment. In this case the smaller increment is ΔX . Therefore at the output of diode matrix 38 a seven bit word designated M is fed to one input of AND gates 44. The other input to AND gates 44 is X_S which is derived from AND gate 18. These two inputs to AND gates 44 being in coincidence provide an output signal designation MX_S from AND gates 44 which is fed to X shift register 40 by way of OR gates 39. Since ΔY is the larger increment, this signal takes the path through binary to unitary converter 34. From binary to unitary converter 34 a signal Y_μ is fed to one input conductor of AND gates 37. On

the other input conductor of AND gates 37 a signal Y_L is applied. The output from AND gates 37 is loaded into Y shift register 41 by way of OR gates 42 at the same time that the signal MX_S is loaded into X shift register 40. The bit streams from shift registers 40 and 41 are applied to digital to analog converters 47 and 48, respectively, as discussed above.

When ΔX is the larger increment, the signals are fed to AND gate 18, inverter 20, AND gates 23, OR gates 26, binary to decimal converter 31 and matrix 38. Simultaneously a Y_S signal is fed from AND gate 19 to AND gates 28, OR gates 29, binary to decimal converter 32 to matrix 38. From AND gates 43 a signal MY_S is sent to OR gates 42 and Y shift register 41. Thus, only when the ΔX or ΔY increment is smaller is use made of the seven bit word output from matrix 38.

Referring to FIG. 2 a detailed schematic of comparator 17 is shown. When the signal X_L on the output conductor of OR gate 61 is a binary 0 bit and the signal Y_L on the output conductor of AND gate 64 is a binary 1 bit, then the ΔY increment is larger than ΔX increment. When the binary bits are reversed from the above, ΔX is the larger increment. When both gates 61 and 64 have the same binary bit on their output conductors, the increment in ΔX is equal to ΔY . The equality of ΔX and ΔY appears at the output of AND gate 60.

Gates 50, 51 and 52 of FIG. 2 are EXCLUSIVE OR circuits which have a truth table shown in Table I as follows:

TABLE I

X	Y	
0	0	0
0	1	1
1	0	1
1	1	0

It is seen from Table I that when $X = Y$ the output of the EXCLUSIVE OR gate is 0. In the case where ΔY is greater than ΔX (e.g., $X_1 = 0$, $X_2 = 0$, $X_3 = 0$ and $Y_1 = 1$, $Y_2 = 1$, $Y_3 = 1$) comparator circuit 17 operates as follows:

One input conductor of AND gate 57 will have a 0 and the other input conductor will have a 1 since according to the truth table a $X = 0$, $Y = 1$ input to the EXCLUSIVE OR gate 50 will furnish a 1 output. Since AND gate 57 has input signals which are not in coincidence there is a "0" output. An output 1 bit from EXCLUSIVE OR gate 50 is also applied to inverter 53. At the output of inverter 53 there is a 0 which is applied to AND gates 58, 59 and 60. At the output of EXCLUSIVE OR gate 51 there is a 1 which is applied to inverter 54 and to one of the three input conductors of AND gate 58. AND gate 58 has a 0 from line X_2 and a 0 from inverter 53 on its other two input conductors. Since there is no signal coincidence at the input conductors of AND gates 58, it provides a 0 output signal. At EXCLUSIVE OR gate 52 there is also a 1 output which is applied to AND gate 59 and inverter 56. AND gate 59 has three other input conductors. On the first conductor there is a 0 from line X_3 . On the second and third conductors there are 0 from inverters 58 and 54. At the three input conductors of AND gate 60 there are 0's in coincidence which provide a 0 at the output of AND gate 60. Also at this time there are three 0's on the input conductor of OR gate 61 which derived from AND gates 57, 58 and 59. The output of OR gate 61 is a 0 which is applied to inverter 62, giving a 1 output.

From AND gate 60 a 0 is applied to inverter 63, giving a 1 output. These latter two 1's are applied to the input conductors of AND gate 64. Therefore, at the output of AND gate 64 there is a 1 which signifies that the increment ΔY is greater than the increment ΔX . Where the increment in ΔX is greater than ΔY then $X_L = 1$ and $Y_L = 0$.

FIG. 4 depicts a schematic of an illustrative embodiment of matrix 38 utilizing diodes. There are seven outputs columns numbered 1-7 from right to left. The 27 input rows furnish all possible combinations in which ΔX and ΔY may appear as the smaller or larger increment. Thus, where ΔX is smaller and of a length 6 and ΔY is larger and of a length 7, then line L_7, S_6 is enabled and 1's appear at output terminals 1, 2, 3, 5, 6 and 7 and a 0 appears at terminal 4 of matrix 38. At the cross-points of the selected terminals are diodes which are connected in series with current limiting resistors to ground.

FIG. 5 shows an example of character coding for the letter A. It is seen from FIG. 5 that it takes 117 bits to form the letter A. As can be seen from FIG. 5, the resultant character is generated in continuous line segments of substantially equal stroke lengths on the grid. This permits characters having substantially constant intensity. Moreover, the characters are formed at high speed and have good character definition independent of character size and location.

It will be apparent to those skilled in the art that the present invention may be used generally in display systems and is not limited to the embodiment described. Numerous other variations, modifications and adaptations of the present invention will be apparent to those skilled in the art, and such as come within the spirit and scope of the appended claims are considered to be embraced by the present invention.

What is claimed is:

1. Character generating apparatus for controlling the deflection control circuits of a cathode ray tube to move an electron beam across the screen of said cathode ray tube to display a character thereon, said character being formed of a plurality of straight line segments, said apparatus comprising

means for receiving a character code and transforming said character code into an address code,
memory means responsive to said address code for sequentially providing words each containing a horizontal and vertical deflection increment and beam control signals for a line segment of said character,
logic means for converting said horizontal and verti-

cal deflection increment signals in each of said words into respective binary bit streams each having as many 1's as the length of the respective coordinate component of the line segment, said logic means comprising binary to unitary converting means for converting a binary representation of a number into a binary word having an amount of 1's equal to said number, said binary to unitary converter including means for packing said 1's at one end of said binary word, and

means for converting said bit streams into stroke signals for application to said deflection circuits.

2. The apparatus of claim 1 wherein said logic means further includes comparison means for determining the larger and smaller of the horizontal and vertical deflection increments and means responsive to said comparison means for enabling said binary to unitary converter means to convert the larger, or both if equal, of said horizontal and vertical deflection increment signals into said binary word.

3. The apparatus of claim 2 wherein said logic means further includes distributing means responsive to said comparison means for converting the smaller of unequal horizontal and vertical deflection increment signals into another binary word having the 1's distributed in accordance with the relative values of the larger and smaller increment signals.

4. The apparatus of claim 3 wherein said distributing means includes a matrix circuit having input rows corresponding to the possible combinations of larger and smaller increments and output columns corresponding to positions in said another binary word, each of said rows being connected to the columns corresponding to the distribution of 1's in said another binary word for that combination of larger and smaller increments.

5. The apparatus of claim 4 wherein said logic means further includes means for converting said binary word and said another binary word into said respective binary bit streams.

6. The apparatus of claim 2 wherein said logic means further includes count down means, means for setting said count down means to the larger value of said increments, means for decrementing said count down means in synchronism with the application of stroke signals to said deflection circuits, means responsive to the decrementing of said count down means to a predetermined number for generating an end-of-stroke signal, and means responsive to said end-of-stroke signal for controlling said memory means to provide the next sequential line segment word.

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