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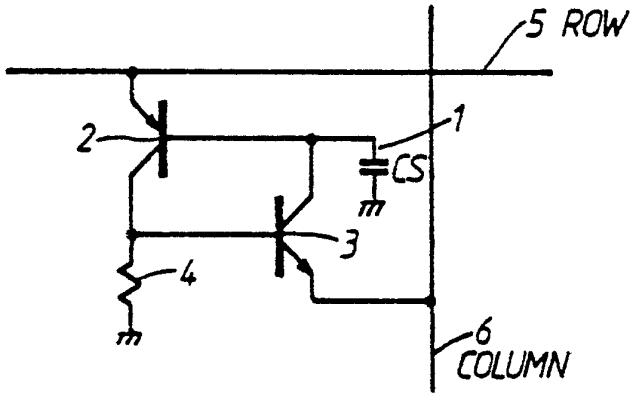
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(54) Title: LIGHT TO ELECTRICAL ENERGY TRANSDUCER CELL



(57) Abstract

A light to electrical energy transducer cell including a capacitor which, when charged and exposed to light, loses an amount of charge dependent on the quantity of light received by the capacitor, switch means so arranged to be controlled by the charge storage means and by the voltage level of a first of its control ports that it assumes a state indicative of the relative voltage levels of its control port and the charge storage means, and input and output means for charging the charge storage means by way of the switch means and for measuring the voltage level of the charge storage means by the application of a varying voltage to the switch control port to cause a change of state of the switch means.

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Light to electrical energy transducer cell

The present invention relates to a light to electrical energy transducer cell particularly suitable for fabricating an array for converting a light image into an electrical image.

Semiconductor charge-coupled devices, arranged as an array of elements in each of which an electrical charge package is stored in a well structure, have been used as imaging devices. In the application of charge coupled device elements as an imaging device, light from each part of an object to be reproduced as an electrical image is directed to one or more of the charge wells to cause a reduction in the size of the electrical charge packages according to the amount of light energy received from the particular part of the object. In the operation of the known electrical imaging devices, the packet of charge remaining in each well at the end of the exposure period is removed from the well and each packet is subjected to various signal processing steps in order to provide an electrical signal which forms part of the complete electrical image of the object. The complete electrical image of the object is obtained by treating it as an array of picture elements and employing an imaging array in which each imaging element is arranged to provide the electrical image of a

corresponding picture element.

At least one difficulty with the known imaging elements is the requirement for the transfer of the small amount of charge from the storage well to an output port of the imaging element and the subsequent processing of the transferred charge to provide a usable signal.

It is an object of the present invention to provide a light to electrical energy transducer cell which represents an improvement over the known prior art imaging element.

It will be understood that a range of electromagnetic radiations capable of generating electrical charge carriers in materials are included within the scope of the term light as used herein.

In accordance with the present invention, a light to electrical energy transducer cell includes charge storage means which, when exposed in a charged state to light, loses an amount of charge dependent on the quantity of light received by the charge storage means, switch means connected to the charge storage means arranged to facilitate charging of the charge storage means, the switch means being arranged also to be so controlled by the charge storage means and by the voltage level of a first control port as to assume a state indicative of the voltage levels of its control port and the charge storage means, and input and output

means not connected to the charge storage means and preferably connected only to the switch means for charging the charge storage means and for measuring the voltage level of the charge storage means by varying the voltage level of the control port of the switch means to cause a change of state of the switch means.

Preferably, the charge storage means is conected between a second control port of the switch means and a reference point within the cell.

Advantageously, a third control port of the switch means is connected to the reference point within the cell by way of a resistive means.

In one arrangement of the cell, an input means is connected to the first control port of the switch means and an output means is connected to a fourth control port of the switch means.

In one arrangement of the cell, the switch means is a PNPN device connected between the input and the output means, and the charge storage means is connected between the inner N- layer and an internal ground potential point of the cell.

A light to electrical energy converter includes a transducer cell and means connected to the input and output means for charging the charge storage means, and means for measuring the voltage level of the charge storage means.

Preferably, the means for measuring the voltage

level of the charge storage means inlcudes means arranged to detect a change of state of the switch means and to provide an output signal indicative of the time of the change of state of the switch means relative to the time at which the change would take place when the charge storage means is at its initial voltage.

Preferably, the means for measuring the voltage level of the charge storage means is arranged to provide a digital output.

Preferably, the means for measuring the voltage level of the charge storage means includes a ramp generator arranged to vary the voltage level of a control port of the switch means which is arranged to switch as the ramp generator voltage approaches the charge storage means voltage, and a digital down-counter arranged to count during a period between the start of the ramp and the change of state of the switch means.

A light to electrical energy transducer block includes a plurality of light to electrical signal transducer cells arranged in a matrix of rows and columns with respective row conductors arranged as the input means and respective column conductors arranged as the output means, and means shared by the signal transducer block for charging the charge storage means of the cells and for measuring the voltage levels of the cells.

One form of transducer block includes multiple

transducer cells forming the elements of the matrices, and associated multiple row and column conductors.

Preferably, a transducer block includes input and output buffer amplifiers and input and output transfer gates connected to the row and column conductors.

Preferably, in a transducer block the means for measuring the voltage levels of the cells includes means arranged to detect a change of state of each the switch means, one row at a time, and to provide an output signal indicative of the time of the change of state of each of the switch means, one row at a time, relative to the time at which the change would take place when the charge storage means of the cell is at its initial voltage, and means for storing the results from each of the cells one row at a time.

Preferably, in a transducer block alternate rows of the block are connected to respective first and second sets of means for storing the results from the cells.

Preferably, in a transducer block, the means for measuring the voltage levels of the cells is arranged to provide a digital output.

Preferably, in a transducer block, the means for measuring the voltage levels of the cells includes a ramp generator arranged to vary the voltage level of a

control port of each of the switch means, one row at a time, which switch means are each arranged to switch as the ramp generator voltage approaches the voltage of its associated charge storage means, a digital down-counter arranged to count during the ramp, and means for storing the count reached for each cell, a row at a time, at the time of the change of state of its switch means.

Advantageously, an array of the transducer cells occupies an entire semiconductor wafer.

The invention provides a method of converting energy from an electromagnetic source into an electrical signal including the steps of charging a charge storage means which, when exposed in a charged state to the electromagnetic energy, loses an amount of charge dependent on the quantity of the electromagnetic energy received by the charge storage means, exposing the charge storage means to the electromagnetic energy, measuring the voltage level of the charge storage means by comparing it with a ramp voltage, and generating, as an output signal, the difference between the voltage levels of the charge storage means before and after exposure to the electromagnetic energy.

Preferably, in the performance of the method, the output signal is generated as a count downwards from a value corresponding to the voltage level of the charge storage means before exposure to the electromagnetic energy, the count being halted when the ramp voltage

reaches the voltage of the charge storage means after exposure to the electromagnetic energy.

One form of light to electrical energy transducer cell, in accordance with the present invention, and an electrical imaging device employing an array of the light-to-electrical energy transducer cells, now be described, by way of example only, with reference to the accompanying drawings, in which:-

Fig. 1 is a circuit diagram representation of a light to electrical energy transducer cell in accordance with the present invention,

Fig. 2 is a diagrammatic representation of the transducer cell of Fig. 1 with the drive circuits required to provide an output signal in digital form,

Fig. 3 is a diagrammatic representation of an ideal drive waveform, and an ideal output waveform, for the light to electrical energy transducer cell of Fig. 1,

Fig. 4 is a diagrammatic representation of the actual drive and output waveforms of the light to electrical energy tranducer cell of Fig. 1 for a high level of incident light,

Fig. 5 is a diagrammatic representation of the actual drive and output waveforms of the light to electrical energy transducer cell of Fig. 1 for a low level of incident light,

Fig. 6 is a diagrammatic representation of the conversion characteristic of the light to electrical energy transducer cell of Fig. 1 for three different drive waveforms,

Fig. 7 is a diagrammatic representation of the drive waveform used in obtaining the results illustrated by Fig. 6,

Fig. 8 is a diagrammatic representation of an image forming device employing an array of light to electrical energy tranducer cells in accordance with the present invention,

Fig. 9 is a diagrammatic representation of a block arrangement for the light to electrical energy transducer cells suitable for forming part of an array of cells, illustrating the provision of redundancy in the block,

Fig. 10 is a more detailed representation of part of the block of Fig. 9,

Figs. 11a, 11b, and 11c illustrate a first monolithic integrated circuit form of the transducer cell of Fig. 1, and,

Fig. 12a, 12b, and 12c illustrate a second monolithic integrated circuit form of the transducer cell of Fig. 1.

Referring to Fig. 1, a light to electrical energy transducer cell includes a semiconductor capacitor 1 having one plate connected to zero or earth potential

for the system, and the other plate of the semiconductor capacitor 1 connected to the collector electrode of an NPN bipolar transistor 3 and to the base electrode of a PNP bipolar transistor 2. The emitter electrode of the PNP transistor 2 is connected to a row address conductor 5 and the collector electrode of the transistor 2 is connected, by way of a resistor 4, to zero or earth potential for the system. The base electode of the NPN transistor 3 is connected to the collector electrode of the PNP transistor 2 and the emitter electrode of the NPN transistor 3 is connected to a column address conductor 6.

Referring to Fig. 1, the PNP transistor 2 and the NPN transistor 3 form a PNPN structure and the positioning of the semiconductor capacitor 1 and the resistor 4 are such that the semiconductor capacitor 1 is connected between a first gate electrode of the PNPN structure and earth potential for the system, and the resistor 4 is connected between a second gate electrode of the PNPN structure and earth potential for the system.

The light-to electrical energy transducer cell of Fig. 1 is operated by first charging the semiconductor capacitor 1 to some convenient voltage level then exposing the semiconductor capacitor 1 to a light source for a given period long enough to cause partial discharge of the semiconductor capacitor 1. The charge

lost by the capacitor, represented by the reduction of its inter-plate voltage, then represents the intensity of the light source to which the semiconductor capacitor 1 was exposed. The intensities of other light sources relative to that first used may then be determined by repeating the operation for the other light sources for the same period, provided of course that the range of light intensities being investigated is such that the highest intensity source just discharges the capacitor 1 in the given exposure period.

In the arrangement represented by Fig. 1, the semiconductor capacitor 1 may be charged to a convenient positive datum voltage by allowing the column address conductor 6 to "float", or by applying a positive voltage to the emitter electrode of the NPN transistor 3 by way of the column address conductor 6, to prevent conduction of the transistor 3 while charging the semiconductor capacitor 1 from the row address conductor 5 by way of the emitter-base diode circuit of the PNP transistor 2 to the datum voltage level. The datum voltage supply is then removed, followed by the removal of the positive voltage blocking conduction of the NPN transistor 3, if appropriate, leaving the semiconductor capacitor 1 with a charge which holds the base electrode of the PNP transistor 2 positive with respect to its emitter electrode. Exposure of the semiconductor capacitor 1 to light will reduce its stored charge

leading to a reduction in its inter-plate voltage. The reduced voltage level may be measured by applying, to the row address conductor 5, a ramp voltage rising from zero volts to the datum voltage to which the semiconductor capacitor 1 was charged initially. When the ramp voltage becomes ~~nearly~~ about equal to the voltage of the semiconductor capacitor 1, the PNP transistor 2 will begin to conduct and will act regeneratively with the NPN transistor 3 to cause both transistors to become fully conductive and to connect the row address conductor 5 to the column address conductor 6, causing the voltage level of the column address conductor 6 to rise abruptly from zero volts to about the level of the ramp voltage being applied to the row address conductor 5. The voltage appearing abruptly on the column address conductor 6 is equal to the residual voltage on the semiconductor capacitor 1 following its exposure to light, and this voltage may be converted to a voltage representing the intensity of the irradiating light by generating a signal representing the difference between the capacitor residual voltage and its initial voltage.

A convenient arrangement for generating a signal representing the difference between the capacitor residual voltage and its initial voltage is represented by Fig. 2 in which a clock oscillator 10 controls the operation of a ramp generator 7 through an interface circuit 9. The interface circuit 9 also controls a

circuit block 8 which is arranged to act as a down counter and to count down for the period between the start of the ramp cycle and the appearance of the ramp voltage at the column address conductor 6. The circuit block 8 acts as an n-bit counter and is arranged to count from its initial value of 2^n to zero in the interval occupied by the ramp waveform. The output count of the circuit block 8 is then a digital representation of the difference between the capacitor residual voltage and its initial voltage. The ramp generator 7 may be an analogue device providing a smooth waveform or it may be a staircase generator having 2^n levels to correspond to the 2^n states available from the circuit block 8.

The upper waveform of Fig. 3 represents the ramp waveform available from the analogue form of the ramp generator 7 and the lower waveform of Fig. 3 represents the waveform which appears at the column address conductor 6 of Fig. 2 when the ramp waveform is applied to the row address conductor 5. Fig. 3 illustrates the existence of a threshold voltage Vt which the ramp voltage must exceed, even when the capacitor 1 is completely discharged, before the PNP transistor 2 and the NPN transistor 3 conduct. The point B on the ramp waveform indicates the ramp voltage level at which the transistors 2 and 3 will conduct when the capacitor 1 is completely discharged and the point C represents the

ramp voltage level at which the transisotrs 2 and 3 will conduct when the capacitor 1 holds charge resulting in an inter-plate voltage V_C. The point D on the ramp waveform represents the datum voltage V_{max} to which the capacitor 1 is charged prior to the light sensing operation. The voltage step GH on the column address waveform represents the condition signalling the switching on of the transistors 2 and 3 of Fig. 2. As is illustrated by Fig. 3, the time duration FG is a measure of the residual inter-plate capacitor voltage GH after exposure of the capacitor 1 to the light source the intensity level of which is being converted to an electrical value, and the time duration HK is a measure of the capacitor voltage drop JK which is an electrical value proportional to the intensity of the light source. The time durations FG and HK may be represented by the output value of a digital counter clocked at a uniform rate, and, assuming that the time range FL is represented by a count of one hundred and the time duration FG will then be represented by a count of forty, then the time duration HK will be represented by a count of sixty. By arranging for a counter to be preset to a count of one hundred and to count down for the time duration FG, the output count will be sixty, which is the correct count for the time duration HK. As will be evident from Fig. 3, the effect of the threshold

voltage V_t is to introduce a fixed error corresponding to the time delay EF when the count starts at a time corresponding to the point A, that is, at the start of the ramp waveform. The error is removed either by delaying the start-of-count by a time interval equal to EF or, when the count starts at the time A, adding to the final counted down value a count corresponding to the time interval EF.

Fig. 4 illustrates actual results from a test device for a high incident light level. In Fig. 4, the ramp waveform is the curve AD corresponding to the idealised curve AD of Fig. 3, and the column voltage is the curve EFGHJ corresponding to the idealised curve EFGHJ of Fig. 3, the period FG being the measure of the capacitor residual voltage as for the period FG of Fig. 3.

Fig. 5 illustrates another result from the test device, this being for a low incident light level. As is evident from Fig. 5, the capacitor residual voltage corresponding to the period FG is higher than it is for the situation represented by Fig. 4, since the capacitor residual voltage will vary as the inverse of the incident light level.

Fig. 6 illustrates the measured light sensitivity obtained from a test device for a range of irradiating light intensities for sampling times of 10mS (curve A), 40mS (curve B), and 1 second (curve C), with adjustment

of the light intensity axis scales for the curves A, B and C to present the curves closely enough together for the effects of varying the sampling periods to be evident. In total darkness, the test device showed a loss of 50% from its initial charge level over a period of about 3 seconds, and, as is evident from the curves A and B, shows good linearity under the realistic sampling times of 10mS and 40mS, with the expectation that sampling times in the range 10mS to 40mS will give results bounded by the curves A and B. At the excessive samping time of 1 second, there is some degradation due to loss of capacitor charge from causes other than intentional light irradiation. The light intensity axis scales are in inverse proportion to the sample time for the curves A, B and C, that is, the scaling is such that the total number of incident photons is the same for these curves.

The waveform applied to the test device of Fig. 6 to read it is ilustrated by Fig. 7. The waveform of Fig. 7 consists of a ramp portion AD of duration 25 µS followed by the period MA, the waveform ADMA being repeated. The sampling time MM is made 10mS in deriving the curve A of Fig. 6, MM is made 40mS in deriving the curve B of Fig. 6, and MM is made 1 second in deriving the curve C of Fig. 6.

Fig. 8 illustrates an arrangement for an array 101 of light-to-electrical energy transducers with the

external control circuits to operate it as an imager array. The imager array includes a row driver 102, separate n-bit column registers 103,104.... and m connected to respective column conductors 103c,104c ..... and mc and an n-bit down counter 106 arranged to pass its count to the n-bit registers 103,104..... and m along a data bus 107. A further set of n-bit registers 30,40... and p are connected in parallel with the registers 103,104.... and m and arranged to be selected for operation alternately with the registers 103,104.... and m which operate with alternate rows of the array 101. There is one row driver such as the row driver 102 for each of the rows of the array 101.

The operation of the imager array 101 of Fig. 8 takes place as a repeating cycle started by presetting the n-bit down counter 106 to the full-scale value for the system and triggering a ramp generator (not shown) which drives the row driver 102 at the same time as causing the counter 106 to start counting down under the control of pulses from a timing clock (not shown). As each cell in the addressed row switches to cause the row driver ramp voltage to appear at the associated column conductor, the current value of the counter 106 is loaded into the associated one of the registers 103,104 .... and m. The cycle continues until the counter 106 has been decremented to zero at which time the counter and the ramp generator are reset for the next

cycle during which the count data stored in each of the registers 103,104.... and m is read out on the output bus 108 . The next cycle is carried out with the next row driver 102 connected to the next row of transducer cells in the array 101 and the registers 30,40... and p operating to receive the output count from the counter 26. As with the registers 103,104.... m, each of the registers 30,40...p stores the output count it is receiving from the counter 106 when the column conductor to which it is connected is switched from zero voltage to the row driver voltage by the transducer cell being monitored. The registers 103,104.... m are brought back into operation for the next row while data is being transferred out from the registers 30,40....p, and so on, until all the rows have been scanned, and the whole cycle is repeated indefinetely.

The arrangement of Fig. 8 is therefore operable as an imager array in which each row read cycle is controlled by the n-bit binary down counter with a resolution of 2^n levels of the incident light intensity. Each row read cycle is started by presetting the counter to the full-scale value for the system and triggering a ramp generator (not shown), arranged to provide a ramp waveform of duration such that the counter will reach zero output when the ramp is at its maximum value, to start the ramp-up of the drive signal to the selected

row. The ramp generator (not shown) may provide a staircase waveform composed of 2^n discrete steps to correspond to the 2^n level resolution provided by the ramp or the ramp may be a straight line. As each cell in the addressed row changes state to effect the connection of its row conductor to its column conductor, the appearance of a non-zero voltage on the column conductor causes the current value of the counter to be loaded into the n-bit register or latch dedicated to the column conductor. When the counter has been decremented to zero by its reference timing clock, the ramp generator is reset to return the row drive voltage to zero. Data held in digital form in the registers or latches for each row are shifted out while the next row is being sampled and the results stored in a duplicate set of registers or latches connected also to the column conductors and the counter. One set of registers or latches is therefore used for the data from alternate rows of the array. Because the output data from the counter and the registers or latches are in digital form, that is, analogue to digital conversion is performed automatically as part of the sampling of the stored charge level for the imager array, the output data from the imager array are compatible with computer and digital transmission systems. A ramp duration of up to 64μS provides data at a rate corresponding to a television system of line scan rate providing 625 lines

per frame at 25 frames per second.

Fig. 9 illustrates an imager array block with cell redundancy, buffer amplifiers, and transfer gates, providing both fault tolerance and expansion capability. Referring to Fig. 9, the imager array block includes a transducer array 111 consisting of an array of picture element (pixel) units 112 each made up of two transducer cells 112a and 112b. The transducer cell 112a has its own row conductor 113a and column conductor 114a and the transducer cell 112b has its own row conductor 113b and column conductor 114b. The transducer cell 112a is representative of an upper set of transducer cells to which the row conductor 113a is common and the transducer cell 112b is representative of a lower set of transducer cells to which the row conductor 113b is common. Also, the transducer cell 112a is representative of a left-hand set of transducer cells to which the column conductor 114a is common and the transducer cell 112b is representative of a right-hand set of transducer cells to which the column conductor 114b is common. Outside the transducer array 1, a column conductor 114 is connected to a buffer amplifier 115 which drives the column conductor 114a within the array 111 and to a buffer amplifier 116 which drives the column conductor 114b within the array 111. On leaving the array 111, the column conductors 114a

and 114b are combined into a column conductor 110 by means of AND gates 117 and 118 and an OR gate 119. The AND gate 117 is connected also to a transfer control conductor 110 and the AND gate 118 is connected also to a transfer control conductor 120 . Also outside the array 111, a row driver conductor 17 and a row conductor 16 are connected to an AND gate 15 the output of which is connected to a buffer amplifier 14 which drives the row conductor 113a within the array 111 and to a buffer amplifier 13 which drives the row conductor 113b within the array 111. When the row conductors 113a and 113b leave the array 111 they are combined by means of AND gates 18 and 19 and an OR gate 20 to form a row conductor 21. The AND gate 18 is connected also to a transfer control conductor 23 and the AND gate 19 is connected also to a transfer control conductor 22.

The imager array block of Fig. 9 is suitable for connection with similar blocks to form a matrix of the blocks. The provision of the buffer amplifiers 115, 116, 13 and 14 facilitates the fabrication of matrices with indefinite numbers of rows and columns, and the provision of the transfer gates 117, 118 and 119 and 18, 19 and 20, facilitates the transfer of data through the blocks either along the column conductors 114 and 100 or along the row conductors 16 and 21. The provision of dual transducer cells 112a and 112b for each

picture element 112 with dual row conductors 113a and 113b and dual column conductors 114a and 114b facilitates the fabrication of fully functional imager arrays from array blocks having some defective components.

Referring to Fig. 9, each row of picture elements is provided with a pair of row conductors and each column of picture elements is provided with a pair of column conductors, each conductor of a pair being driven independently with the same signal at the input to a block, but only one conductor of a pair being sampled to provide the data to be taken from the block. The row and column transfer conductors of the block are so controlled as to select only one of the row or column conductors to provide the ouput signal to be sampled. The order of the row and column conductor pairs are reversed alternately, that is, the order of the row and column conductors is 1A-1B, 2B-2A, 3A-3B, 4B-4A and so on. The block is tolerant to fabrication defects including single cell defects, discontinuities in row and column conductors, short circuits between adjacent row conductors, short circuits between adjacent column and short circuits between adjacent row and column conductors. The provision of redundant cells and conductors does not lead to excessively large picture elements since each cell area is only 20 times the square of the minimum line width which may be achieved

by current fabrication processes.

Referring to Fig. 9, the signals from each block will be converted to digital form, as is explained above, and may be transferred from block to block and regenerated as necessary. Intermediate values may be derived from the signals obtained from adjacent conductors.

Fig. 10 is a more detailed representation of the transducer array block of Fig. 9. In Fig. 10, the transistors 101 to 104 perform the functions of the logic gates 13, 14 and 15 of Fig. 9, the transistors 105 and 106 perform the functions of the logic gates 117, 118 and 119 of Fig. 9, and the transistors 107 and 108 perform the functions of the logic gates 18, 19 and 20. The remainder of Fig. 10 corresponds more or less fully to Fig. 9.

An array of the tranducer cells, particularly an array comprising redundant cells and conductors, may be of indefinite size and may be large enough to occupy an entire semiconductor wafer. As has been described above, the transducer cells may be arranged as an imager array and the output signals are obtained directly in digital form, permitting the switching and regeneration of the signals within the array, particularly where the array is formed as a matrix of blocks.

Figs. 11b, and 11c illustrate, respectively, a section along a line Y-Y and a section

along a line X-X, of an integrated circuit implementation of the transducer cell of Fig. 1. as represented by Fig. 11a.

Fig. 11a illustrates that a region 6 extends fully across the memory cell structure in the y-direction, say, while regions 5,50,51,52,54 and 56 extend fully across the memory cell in the x-direction. The region 53, alone, is local to the transducer cell. The structure illustrated by Fig. 11a permits the fabrication of an array of transducer cells in which rows share the region 6 in the y-direction and columns share the regions which extend in the x-direction, providing simplified access to the transducer cells and permitting the fabrication of a transducer array having a repeating column and row structure.

Fig. 11c illustrates that the p^+ doped region 51, the region 52, the region 53, and the region 6 are stacked one above the other and confined on each side by a silicon dioxide wall 57.

The array of memory cells, described above, may occupy an entire semiconductor wafer.

Referring to Figs. 11a, 11b and 11c, a monolithic semiconductor structure providing the circuit arrangement of Fig. 1 includes a longitudinally extending bar 6 of N type silicon material (the column conductor 6 of Fig. 1) above which lies a bar of P type silicon material 53, above which, in turn, lies a bar of

N type silicon material 52 displaced towards one side of the P type bar 53. A layer 55 of silicon nitride covers the upper surface of the N type bar 52 and extends over the upper surface of the P type bar 53. A first transversely extending bar 5 of p^+ type silicon material (the row conductor 5 of Fig. 1) makes contact along the N type silicon bar 52 and creates a doped region 51 in the region 52, and a second transversely extending bar 50 of p^+ type silicon material makes contact along the P type silicon bar 53 creates a doped region 56 in the region 53. The bar 53 is terminated by an N^+ type silicon barrier 54 and the entire structure described above is formed on a P- type silicon substrate.

Referring still to Figs 11a, 11b and 11c, the transversely extending p^+ silicon bar 5 may be replaced by a metal bar and the doped region 51 produced by ion implantation. The transversely extending bar 50 may also be replaced by a metal bar and ion implantation used to provide the doped region 56.

In the structure represented by Figs. 11a, 11b and 11c, regions 52, 53 and 6 together form a vertical NPN transistor and the regions 51, 52 and 53 together form a vertical PNP transistor, the two transistors bearing to each other the relationship of the transistors 2 and 3 of Fig. 1. The silicon nitride layer 55 forms the dielectric of a capacitor having the regions 50 and 52 as its plate electrodes, the capacitor

being connected to the remainder of the circuit as shown for the capacitor 1 of Fig. 1. The resistor 4 is provided mainly by the silicon bulk material within the region 53 lying between the region 56 and the part of the region active as the base electrode of the transistor 3 and the collector electrode of the transistor 2 provided by the region 51.

In the arrangement represented by Figs. 11a, 11b and 11c, the three-dimensional stacking of the active devices yields a compact cell occupying some 65% of the area required by current 256K MOS cells. Also, the arrangement of the storage capacitor in relation to the parasitic collector-to-base capacitance of the NPN transistor structure yields a storage capacity equivalent to that of current 256K MOS cells in a smaller area.

The arrangement represented by Figs. 11a, 11b and 11c provides an inverted NPN transistor structure with a buried N-type emitter region 6, a uniformly doped epitaxial base region 53 with a polysilicon doped base contact, and a polysilicon doped collector which doubles as the N-type base region for the PNP transistor. The inverted NPN transistor structure is such that there should be a high injection of holes into the emitter region from the base region contact due to the p^+ /P/N structure, leading to poor emitter efficiency and low gain. The situtation is altered by the presence

of the resistive path between the region 56 and the active region of the NPN structure 5253/6 which acts against the region under the resistor contact becoming forward biassed with the result that there is no hole injection into the emitter and the NPN transistor exhibits high gain, as does the PNP transistor (which is not inverted). The resistive path referred to above is generally similar to the structure of a junction field effect transistor in which the regions 52 and 6 form gate electrodes and the region 53 forms the channel, conduction along the channel taking place under pinch-off. The combined PNP/NPN structure forms an efficient thyristor switch.

Figs. 12a, 12b and 12c illustrate a modification of the structure represented by Figs. 11a, 11b and 11c in which the region 56 is extended to provide a diode between the region 56 and the region 52. The capacitance of the diode junction provides the charge storage capacitor.

Claims

1. A light to electrical energy transducer cell including charge storage means which, when exposed in charged state a light, loses an amount of charge dependent on the quantity of light received by the charge storage means, switch means connected to the charge storage means arranged to facilitate charging of the charge storage means, the switch means being arranged also to be so controlled by the charge storage means and by the voltage level of a first control port as to assume a state indicative of the relative voltage levels of its control port and the charge storage means, and input and output means not connected to the charge storage means and preferably connected only to the switch means for charging the charge storage means and for measuring the voltage level of the charge storage means by varying the voltage level of the control port of the switch means to cause a change of state of the switch means.

2. A light to electrical energy transducer cell, as claimed in claim 1, wherein the charge storage means is connected between a second control port of the switch means and a reference point within the cell.

3. A light to electrical energy transducer cell, as claimed in claim 2, wherein a third control port of the switch means is connected to the reference point within the cell by way of a resistive means.

4. A light to electrical energy transducer cell, as claimed in claim 3, wherein input means is connected to the first control port of the switch means and an output means is connected to a fourth control port of the switch means.

5. A light to electrical energy transducer cell, as claimed in any one of claims 1 to 4, wherein the switch means is a PNPN device connected between the input and the output means, and the charge storage means is connected between the inner N- layer and an internal ground potential point of the cell.

6. A light to electrical energy transducer cell substantially as herein described with reference to, and as illustrated by, Fig. 1 of the accompanying drawings.

7. A light to electrical energy converter including a light to electrical signal transducer cell as claimed in any one of claims 1 to 6, and means connected to the input and output means for charging the charge storage means, and means for measuring the voltage level of the charge storage means.

8. A light to electrical energy converter, as claimed in claim 7, wherein the means for measuring the voltage level of the charge storage means inlcudes means arranged to detect a change of state of the switch means and to provide an output signal indicative of the time of the change of state of the switch means relative to the time at which the change would take place when the

charge storage means is at its initial voltage.

9. A light to electrical energy converter, as claimed in claim 8, wherein the means for measuring the voltage level of the charge storage means is arranged to provide a digital output.

10. A light to electrical energy converter, as claimed in claim 9, wherein the means for measuring the voltage level of the charge storage means includes a ramp generator arranged to vary the voltage level of a control port of the switch means which is arranged to switch as the ramp generator voltage approaches the charge storage means voltage, and a digital down-counter arranged to count during a period between the start of the ramp and the change of state of the switch means.

11. A light to electrical signal converter substantially as herein described with reference to, and as illustrated by, Figs. 2 and 3 of the accompanying drawings.

12. A light to electrical energy transducer block including a plurality of light to electrical signal transducer cells arranged in a matrix of rows and columns with respective row conductors arranged as the input means and respective column conductors arranged as the output means, and means shared by the signal transducer block for charging the charge storage means of the cells and for measuring the voltage levels of the cells.

13. A light to electrical energy transducer block, as claimed in claim 12, including multiple transducer cells forming the elements of the matrices, and associated multiple row and column conductors.

14. A light to electrical energy transducer block, as claimed in claim 12 or claim 13, inluding input and output buffer amplifiers and input and output transfer gates connected to the row and column conductors.

15. A light to electrical energy transducer block, as claimed in any one of claims 12 to 14, wherein the means for measuring the voltage levels of the cells includes means arranged to detect a change of state of each the switch means, one row at a time, and to provide an output signal indicative of the time of the change of state of each of the switch means, one row at a time, relative to the time at which the change would take place when the charge storage means of the cell is at its initial voltage, and means for storing the results from each of the cells one row at a time.

16. A light to electrical energy transducer block, as claimed in claim 14, wherein alternate rows of the block are connected to respective first and second sets of means for storing the results from the cells.

17. A light to electrical energy transducer block, as claimed in any one of claims 12 to 16, wherein the means for measuring the voltage levels of the cells is arranged to provide a digital output.

18. A light to electrical energy transducer block, as claimed in claim 17, wherein the means for measuring the voltage levels of the cells includes a ramp generator arranged to vary the voltage level of a control port of each of the switch means, one row at a time, which switch means are each arranged to switch as the ramp generator voltage approaches the voltage of its associated charge storage means, a digital down-counter arranged to count during the ramp, and means for storing the count reached for each cell, a row at a time, at the time of the change of state of its switch means.

19. A light to electrical energy transducer block substantially as herein described with reference to, and as illustrated by, Fig. 8, or Fig. 9, or Figs. 9 and 10, of the accompanying drawings.

20. A light to electrical energy transducer array comprising a plurality of transducer cells as claimed in any one of claims 1 to 6.

21. A light to electrical energy transducer array comprising a plurality of transducer blocks as claimed in any one of claims 12 to 19.

22. A method of converting energy from an electromagnetic energy source into an electrical signal including the steps of charging a charge storage means which, when exposed in a charged state to the electromagnetic energy, loses an amount of charge dependent on the quantity of the electromagnetic energy

received by the charge storage means, exposing the charge storage means to the electromagnetic energy, measuring the voltage level of the charge storage means by comparing it with a ramp voltage, and generating, as an output signal the difference between the voltage levels of the charge storage means before and after exposure to the electromagnetic energy.

23. A method of converting a light signal into an electrical signal as claimed in claim 22, wherein the output signal is generated as a count downwards from a value corresponding to the voltage level of the charge storage means before exposure to the electromagnetic energy, the count being halted when the ramp voltage reaches the voltage of the charge storage means after exposure to the electromagnetic energy.

24. A light to electrical energy transducer array as claimed in claim 20 or claim 21 formed in a semiconductor wafer.

25. A light to electrical energy transducer array including a monolithic structure having a plurality of charge storage means at one of its surfaces and an enclosure arranged to permit each of the charge storage means to receive light, each of the charge storage means being so arranged with switch means as to permit the sensing of the voltage level of the charge storage means by sensing the state of the switch means by means of signals applied to the switch means, and each of the

charge storage means being arranged, when exposed to light while charged, to lose an amount of charge dependent on the quantity of light received.

26. A light to electrical energy transducer array as claimed in claim 25, wherein the enclosure is arranged to permit only the charge storage means to receive light.

27. A light to electrical signal transducer array as claimed in claim 25 or 26, wherein the monolithic structure consists of a semiconductor material.

28. A light to electrical signal transducer array including a plurality of transducer cells substantially as herein described with reference to and as illustrated by Figs. 11a, 11b and 11c, or Figs. 12a, 12b or 12c, of the accompanying drawings.

29. Any new feature herein described or any new combination of hereindescribed features.

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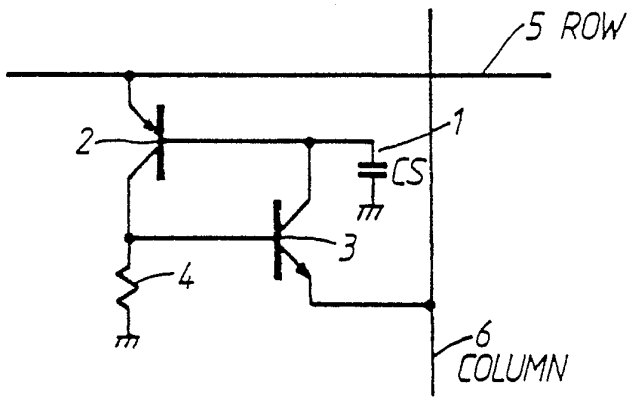


FIG.1.

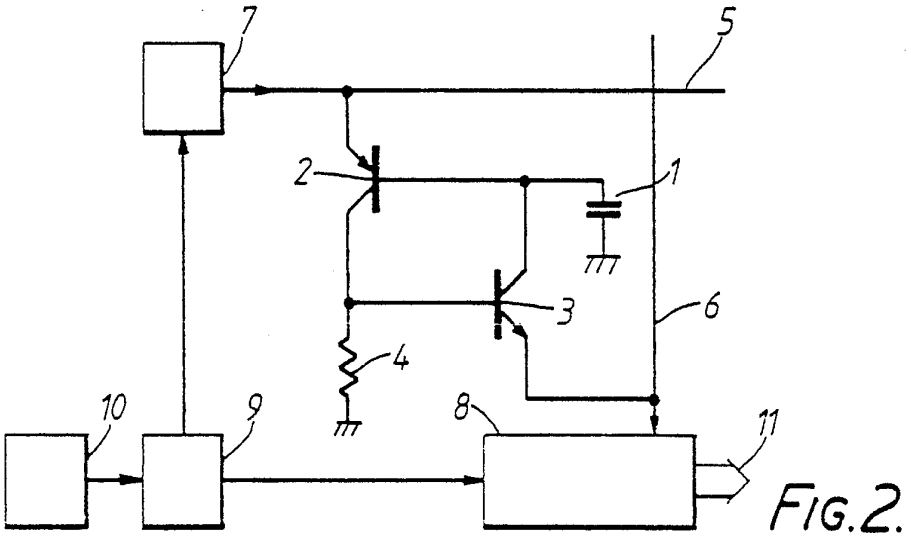


FIG.2.

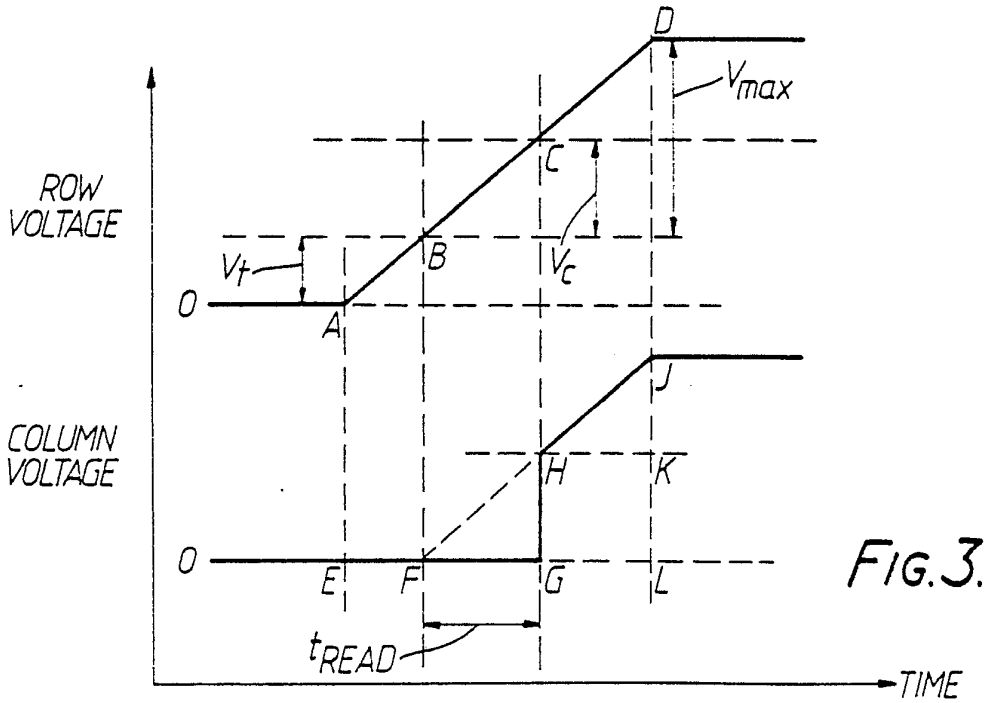


FIG.3.

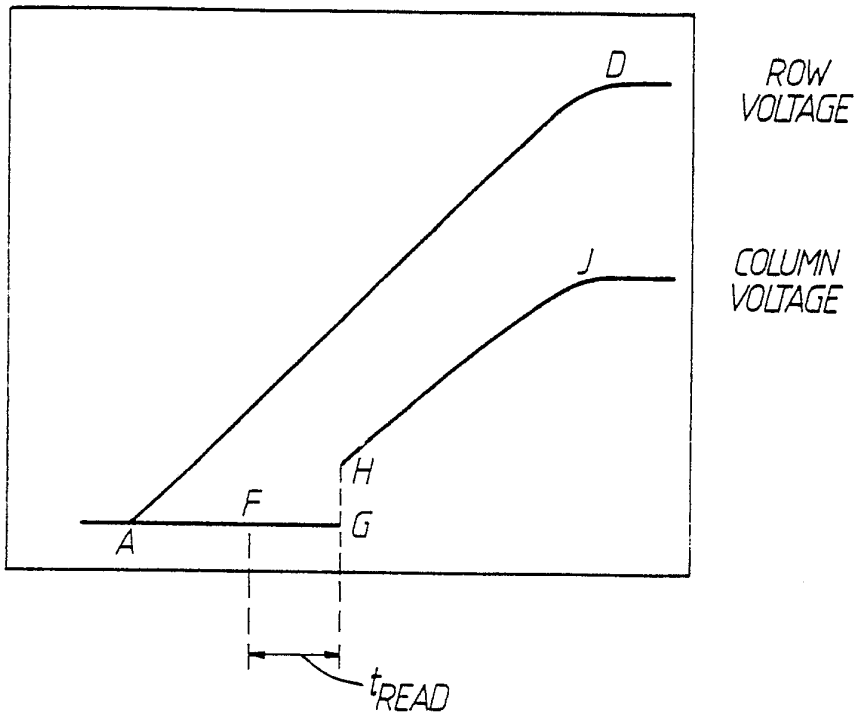

D
ROW VOLTAGE
J
COLUMN VOLTAGE
H
F
G
A
t_{READ}

FIG. 4.

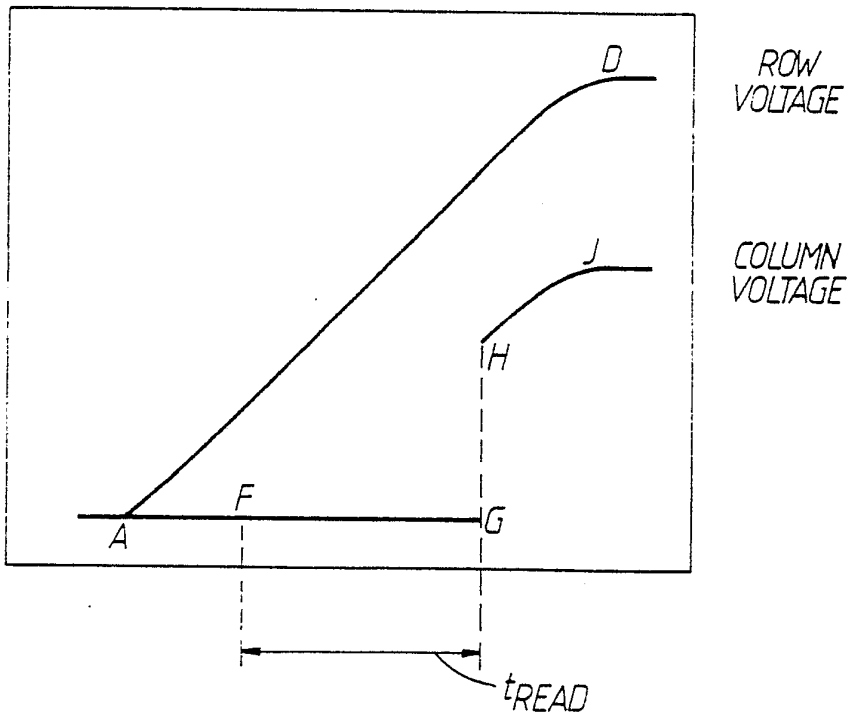

D
ROW VOLTAGE
J
COLUMN VOLTAGE
H
F
G
A
t_{READ}

FIG. 5.

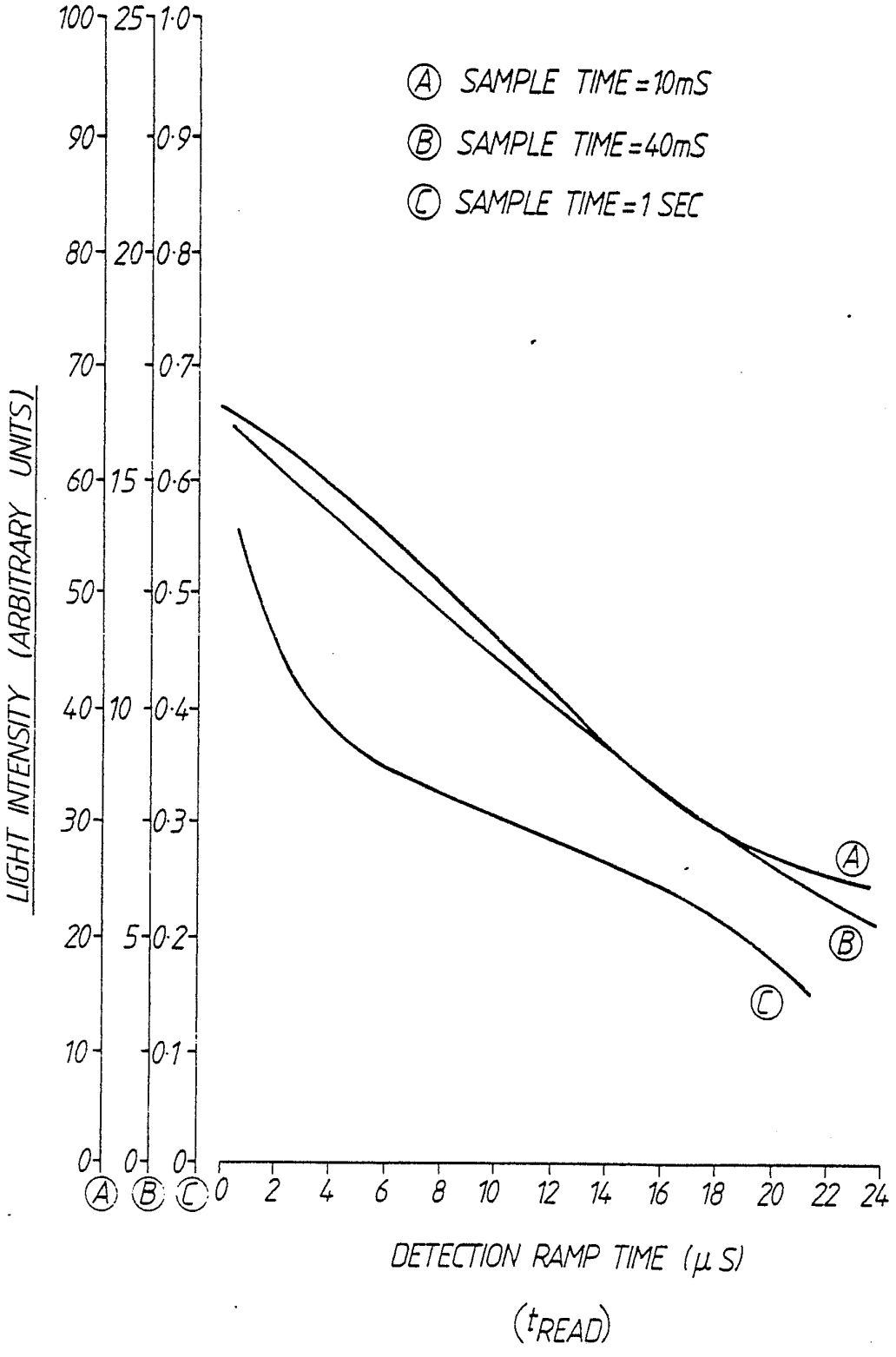

Ⓐ SAMPLE TIME = 10mS
Ⓑ SAMPLE TIME = 40mS
Ⓒ SAMPLE TIME = 1 SEC
LIGHT INTENSITY (ARBITRARY UNITS)
100 90 80 70 60 50 40 30 20 10 0
25 20 15 10 5 0
1·0 0·9 0·8 0·7 0·6 0·5 0·4 0·3 0·2 0·1 0
Ⓐ Ⓑ Ⓒ
0 2 4 6 8 10 12 14 16 18 20 22 24
DETECTION RAMP TIME (μS)
(t_{READ})

FIG.6.

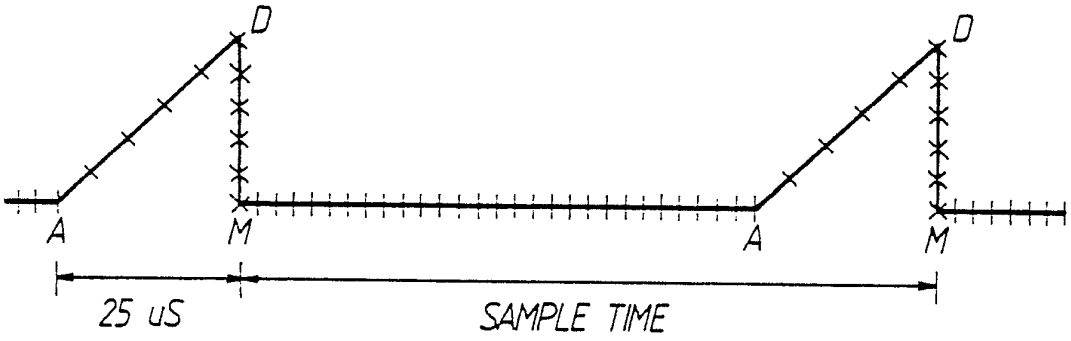

D
D
A
M
A
M
25 uS
SAMPLE TIME

FIG.7.

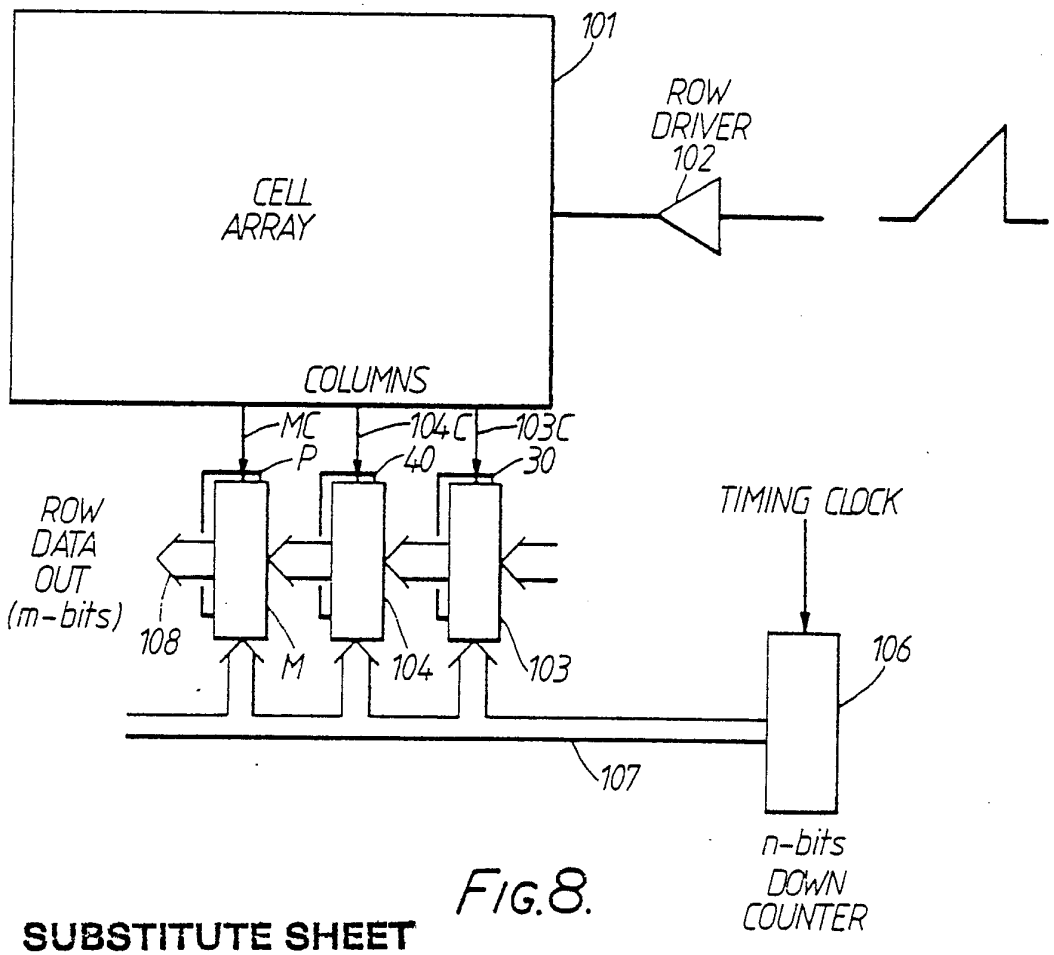

101
ROW DRIVER 102
CELL ARRAY
COLUMNS
MC P
104C 40
103C 30
ROW DATA OUT (m-bits)
TIMING CLOCK
108
M
104
103
106
107
n-bits DOWN COUNTER

FIG.8.

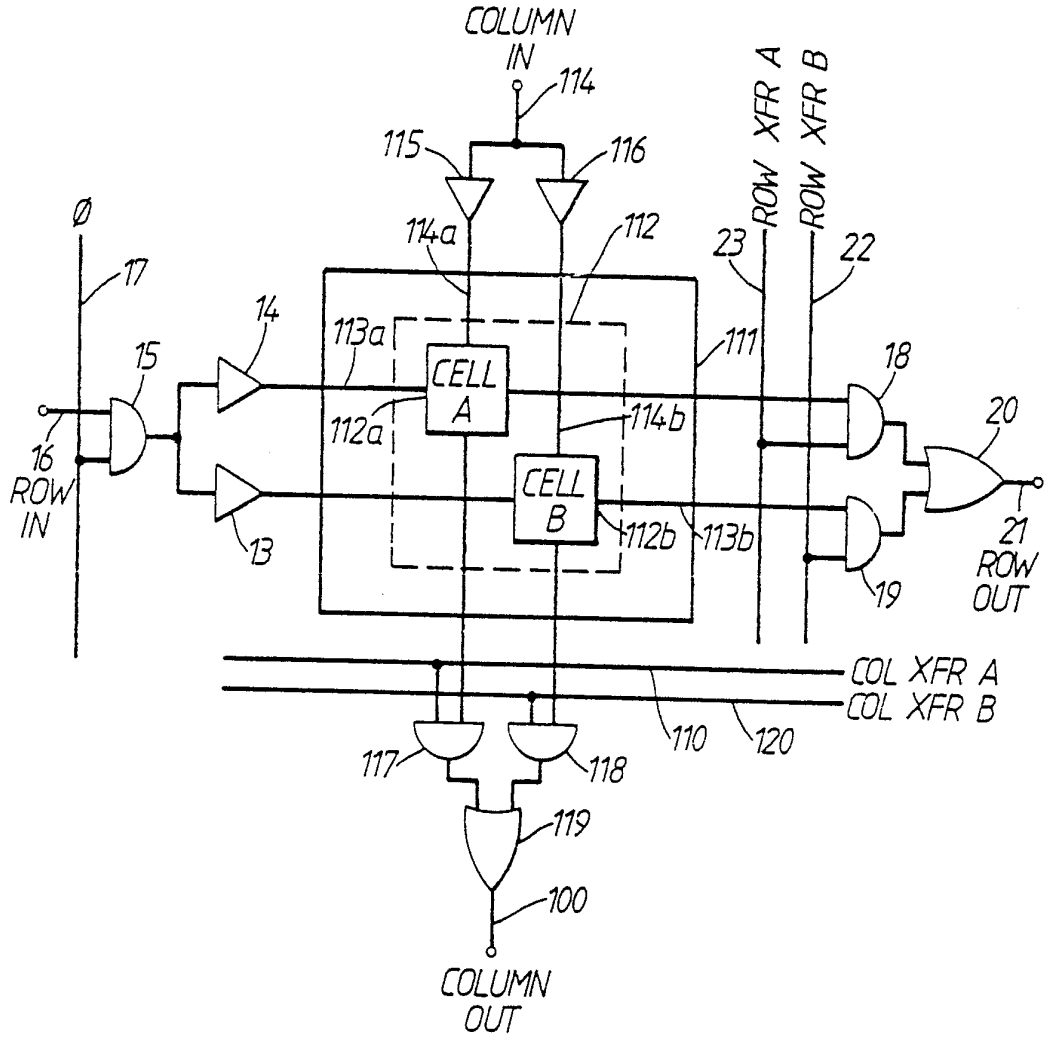

COLUMN IN
114
115
116
ROW XFR A
ROW XFR B
Ø
17
114a
112
23
22
14
113a
111
15
CELL A
18
20
16
ROW IN
112a
114b
CELL B
112b
113b
13
21
ROW OUT
19
COL XFR A
COL XFR B
110
120
117
118
119
100
COLUMN OUT

FIG.9.

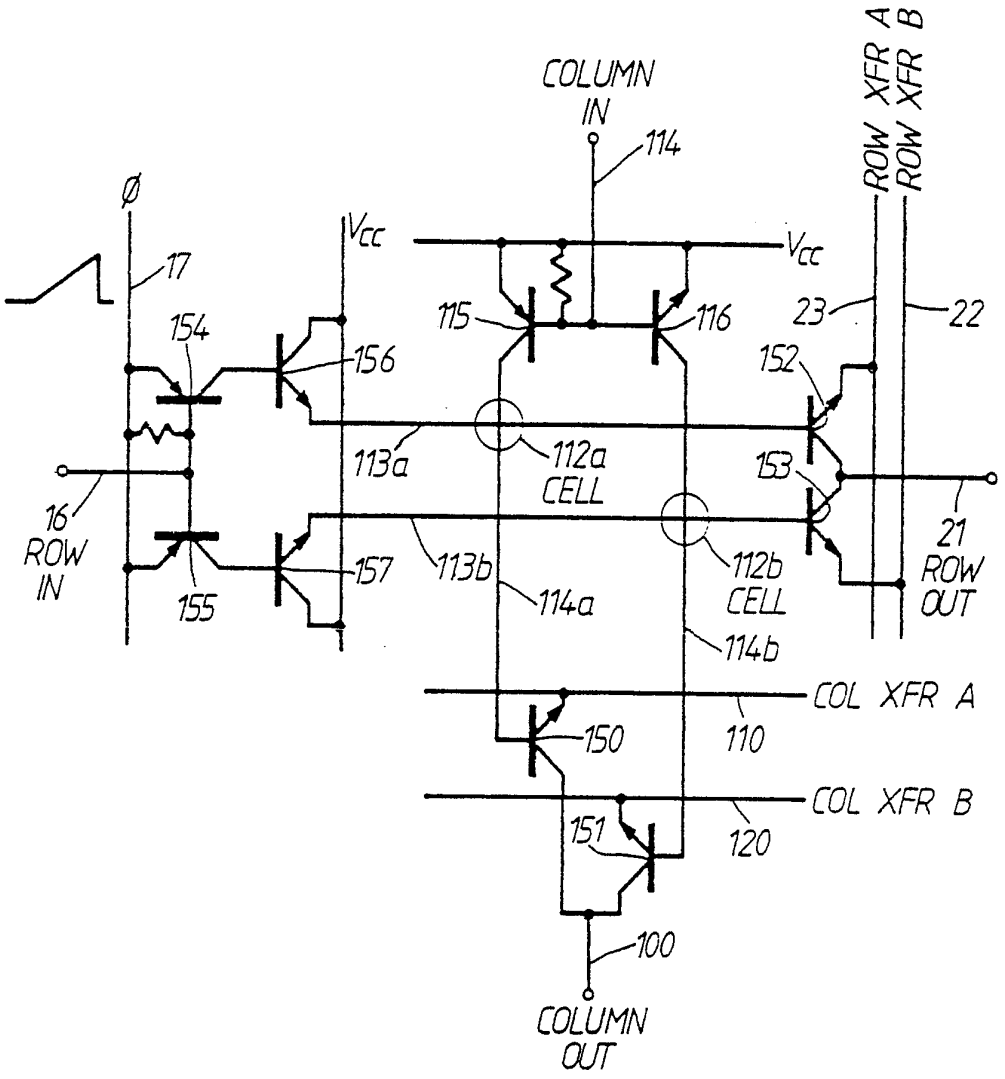

COLUMN IN
114
ROW XFR A
ROW XFR B
Ø
17
Vcc
Vcc
154
156
115
116
23
22
152
113a
112a CELL
153
16 ROW IN
155
157
113b
114a
112b CELL
21 ROW OUT
114b
COL XFR A
150
110
COL XFR B
151
120
100
COLUMN OUT

FIG.10.

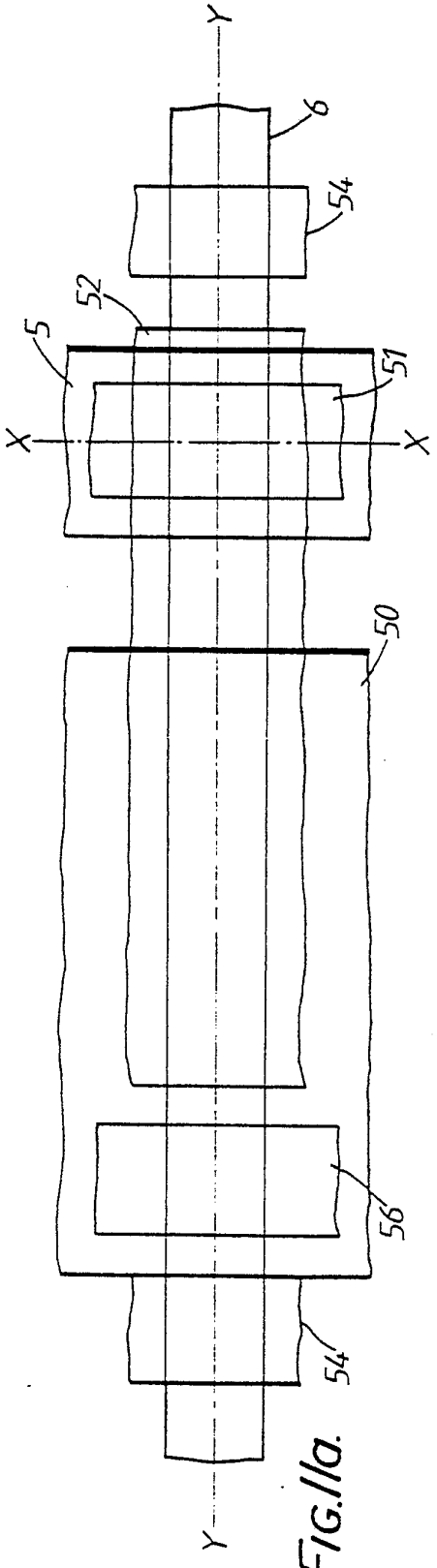


FIG.IIa.

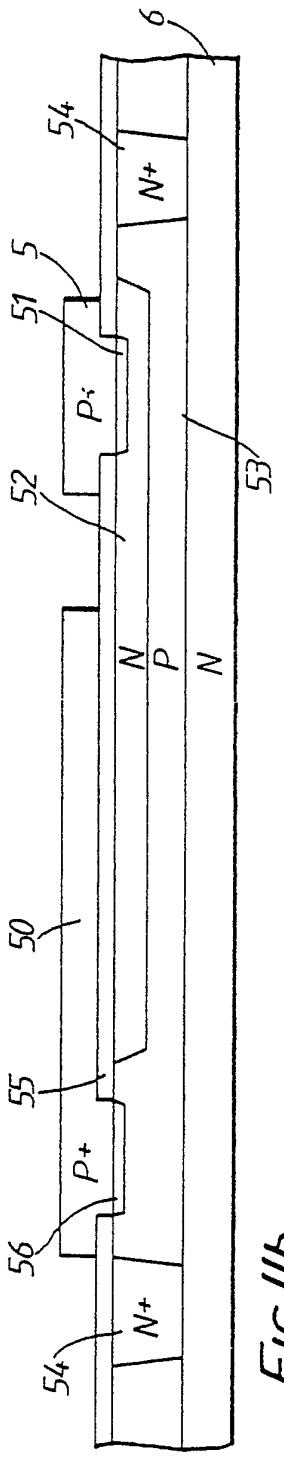


FIG.IIb.

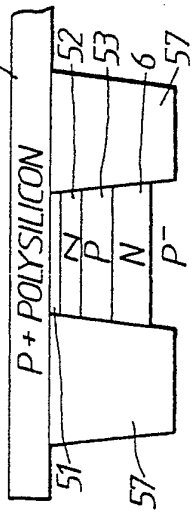


FIG.IIc.

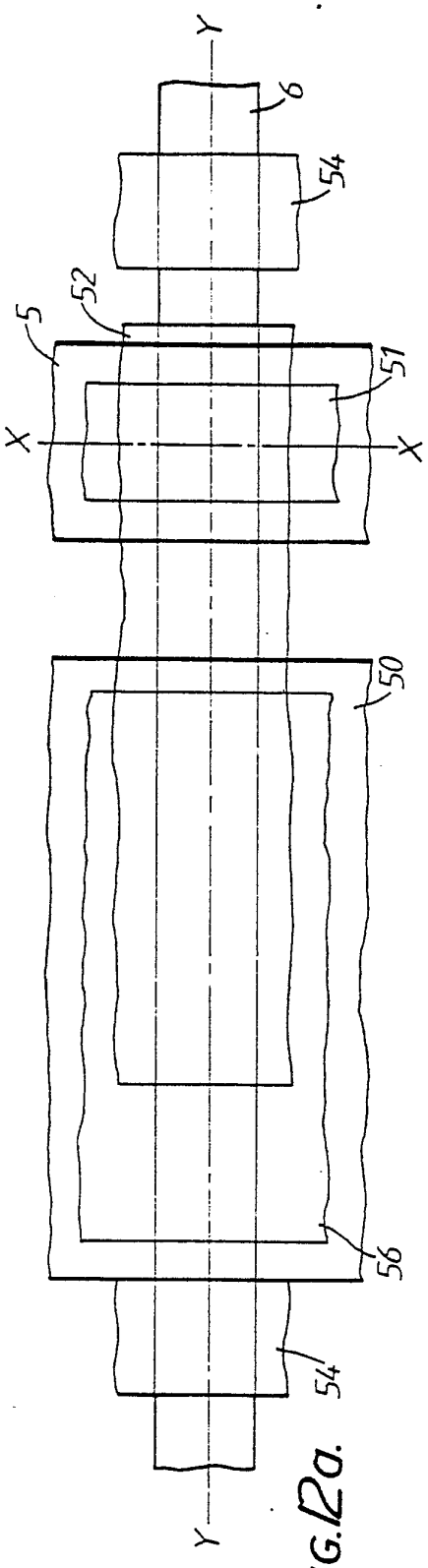


FIG.12a.

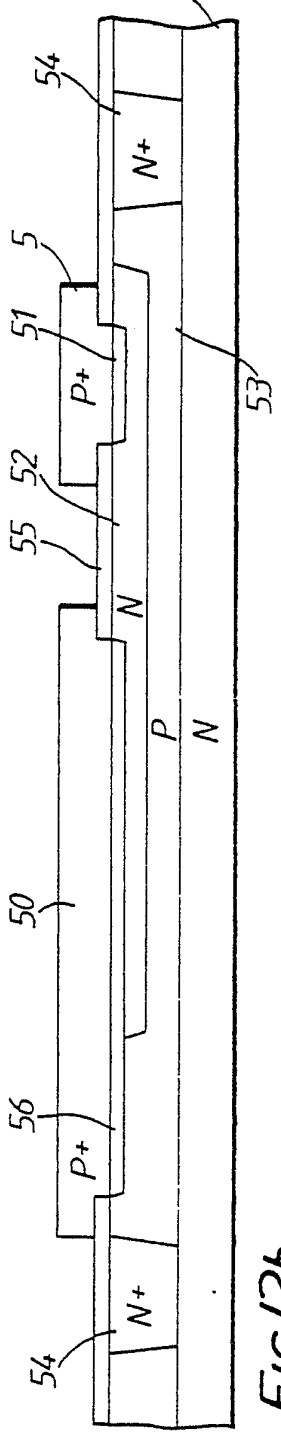


FIG.12b.

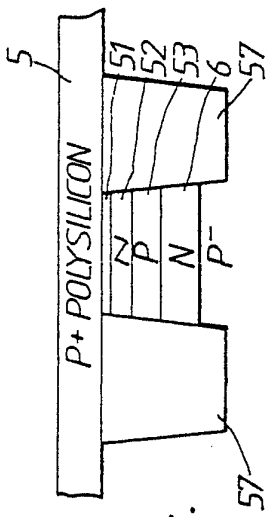


FIG.12c.

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 87/00146

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 04 N 3/15; G 11 C 27/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 04 N 3/15; H 04 N 5/335; G 11 C 27/00; G 11 C 27/02; G 11 C 11/34

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 3665196 (MACALL) 23 May 1972 see column 3, lines 35-64; figure 2 --	1,10,12, 18,22,25
A	US, A, 4181981 (EL-KAREH et al.) 1 January 1980 see column 3, line 3 - column 4, line 2; figure 3 --	1
A	US, A, 4242706 (McCORMACK et al.) 30 December 1980 see column 3, line 19 - column 4, line 5; figure 1	1,12,22

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* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
26th June 1987	23 JUL 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 87/00146 (SA 16361)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/07/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 3665196	23/05/72	NL-A-	7202307	24/08/72
		FR-A-	2126311	06/10/72
		DE-A-	2208344	14/09/72
		AU-A-	3905572	23/08/73
		BE-A-	779627	16/06/72
		SE-B-	366833	06/05/74
US-A- 4181981	01/01/80	EP-A,B	0003030	25/07/79
		JP-A-	54094843	26/07/79
US-A- 4242706	30/12/80	None		