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(54) **Gradation corrector**

Gradationskorrekturanordnung

Correcteur de gradation

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- **PATENT ABSTRACTS OF JAPAN vol. 15, no. 334 (E-1104) 26 August 1991 & JP-A-03 126 377**
- **COMPUTER VISION GRAPHICS AND IMAGE PROCESSING, vol.39, no.3, September 1987, DULUTH, MA US pages 355 - 368 PIZER ET AL. 'Adaptive Histogram Equalization and Its Variations'**

EP 0 501 728 B1

Description

BACKGROUND OF THE INVENTION

The present invention relates to a gradation corrector used in correcting the gradation of a video signal in a television receiver, a video tape recorder, a video camera, a video disk or the like.

In recent years, great importance has been attached to a gradation corrector in order to provide a more clear image which is required with the increase in size of a colour television receiver and the improvement in image quality thereof, and more especially, in order to expand the dynamic range of an image on a CRT by passing a video signal through a non-linear amplifier to correct the gradation of the video signal.

US-A-3,979,555 discloses a system for display improvement that builds up an intensity histogram from the video signal and then redistributes the intensity coding of the video signal so that there are an equal number of display elements or pixels at all display intensity levels. However, the system in US 3,979,555 does not determine a plurality of characteristic features of the intensity histogram nor does it particularly take into account the effect of noise on the signal.

Figure 4 shows a block diagram of a gradation corrector proposed precedently to the present application. In Figure 4, reference numeral 1 designates an A/D converter for converting an input luminance signal into a digital value. Numeral 2 designates a histogram memory for obtaining a luminance distribution of the input luminance signal. In general, the luminance level enters an address of the memory 2 and the frequency enters as data thereof. Numeral 3 designates a histogram operating circuit for computing histogram features such as mean value, mode value, minimum value, maximum value, deviation coefficient, white area, black area, etc of the input luminance signal from the data of the histogram memory 2 and computing control values inclusive of a limiter level, the value of addition, an accumulation start luminance level, an accumulation stop luminance level, the maximum luminance level and so on from the determined values to output the control values to a limiter/adder circuit 5, an accumulation control register circuit 6 and a normalization control register circuit 7. The limiter/adder circuit 5 is provided for processing the data of the histogram. Namely, on the basis of data transferred from the histogram operating circuit 3, the limiter/adder circuit 5 imposes a limitation on the data of the histogram so that it does not exceed a certain level and performs the operation of addition. In general, the data processing performed by the limiter/ adder circuit 5 is completed during a time when the address is accessed once. The accumulation start and stop luminance levels, at which the accumulation is to be started and stopped in determining a cumulative histogram, are supplied from the histogram operating circuit 3 to the accumulation control register circuit 6 which in turn controls a histogram accumulation circuit 8.

The histogram accumulation circuit 8 makes the accumulation of processed data from the histogram memory 2 on the basis of a control signal from the accumulation control register circuit 6. Numeral 9 designates a cumulative histogram memory for storing therein the result of accumulation by the histogram accumulation circuit 8. In general, the luminance level enters an address of the memory 9 and the frequency enters as data thereof. In normalizing data of the cumulative histogram to produce a look-up table, the maximum luminance level for an output luminance signal after normalization is supplied from the histogram operating circuit 3 to the normalization control register circuit 7 and the normalization control register circuit 7 controls a normalization coefficient in accordance with the value of the maximum luminance level. Numeral 10 designates a look-up table operating circuit which normalizes the data of the cumulative histogram memory 9 in accordance with an output of the normalization control register circuit 7. Numeral 11 designates a look-up table memory for storing therein the data normalized by the look-up table operating circuit 10. In general, the luminance level of the input signal enters an address of the memory 11 and the normalized data enters an data thereof. Numeral 12 designates a timing control circuit which makes the sequencing of various operations and the control for the memories. Numeral 13 designates a D/A converter by which output data corrected by use of the look-up table is converted into an analog value.

Next, explanation will be made of the operation of the gradation corrector having the above construction. Figs. 5A to 5F show operating waveforms of various parts.

First, an input luminance signal a is inputted to the A/D converter 1 and is converted thereby into a digital value which is in turn outputted as a converted input luminance signal b. The converted input luminance signal b is taken as a memory address of the histogram memory 2 and data at that address is processed by the limiter/adder circuit 5. By performing this operation during one vertical scanning interval, it is possible to obtain a histogram distribution of the input luminance signal a. The histogram distribution is shown in Fig. 5A.

Next, data of the histogram memory 2 including the histogram distribution is read by the histogram operating circuit 3 which in turn calculates the mean value, the mode value, the minimum value, the maximum value, the deviation coefficient, the white area, the black area, etc. of the input luminance signal. The histogram operating circuit 3 further determines control values inclusive of a limiter level, the value of addition, an accumulation calculation start luminance level, an accumulation calculation stop luminance level, the maximum luminance level after normalization and so on from the result of the above calculation and transfers the determined data to the limiter/adder circuit 5, the accumulation

control register circuit 6 and the normalization control register circuit 7.

Thereafter, the limiter/adder circuit 5 reads data from the histogram memory 2 to make a limiter (see Fig. 5B) and the operation of addition or the like for each read data on the basis of each data transferred from the histogram operating circuit 3 and outputs the result (or corrected histogram data c) to the histogram accumulation circuit 8 (see Fig. 5C). In the case where the value of addition is fixed, a curve obtained by the cumulative addition becomes nearer to a linear profile as the value of addition is larger and approaches to a histogram flatting process as the value of addition is smaller (see Figs. 5C and 5D).

On the basis of the accumulation start luminance level and the accumulation stop luminance level supplied from the accumulation control register circuit 6, the histogram accumulation circuit 8 calculates cumulative histogram data f from the corrected histogram data c in a range between the accumulation start and stop luminance levels and causes the cumulative histogram memory 9 to store the result of calculation.

Next, the look-up table operating circuit 10 reads the cumulative histogram data from the cumulative histogram memory 9 to determine a normalization coefficient so that the maximum value of the cumulative histogram data becomes the maximum output luminance level h supplied from the normalization control register circuit 7. The look-up table operating circuit 10 performs an operation on all the cumulative histogram data g by use of the determined normalization coefficient and causes the look-up table memory 11 to store the result i. If the maximum output luminance level is controlled, an operation such as an automatic contrast control (ACL) or an automatic brightness control (ABL) is possible. Such an operation is shown in Fig. 5E.

Thereafter, data in the look-up table memory 11 is read with the converted input luminance signal b being used as an address and the read data is outputted as a corrected output luminance signal j. Fig. 5F shows a histogram of the corrected output luminance signal j. The D/A converter 13 outputs the corrected output luminance signal j after conversion thereof into an analog signal k.

The timing control circuit 12 controls the operations of various circuits so that the operations of respective parts are performed at such timings as mentioned above. [For example, refer to Japanese Patent Application No. (Hei) 1-265393 (JP-A-3-126,377), entitled "Gradation Corrector", filed by the applicant of the present application.] The gradation corrector proposed in the preceding application JP-A-3-126,377 is of a same type as the above corrector shown in Fig. 4 and adapted to be capable of sufficiently effecting gradation correction on signals of bright levels and intermediate luminance levels as well as on those of black side, and yet capable of effecting gradation correction of higher fidelity and higher contrast, while capable of preventing over-extension of dynamic range. These gradation corrections are effected, as above noted, by adding or subtracting preselected values to or from the data of histogram, substituting preselected values for that of higher or lower than a certain value, thereby optimizing effects of histogram flatting processing, and by controlling range of histogram data to be accumulated or controlling the maximum of the normalized data. In an embodiment of the preceding application, the histogram operating circuit comprises an average luminance level computing circuit for computing from data of the histogram memory an average value of input luminance signal, a mode luminance level detection circuit for detecting a mode value, maximum and minimum detection circuits, a circuit for computing a deviation (dispersion) coefficient from data of the histogram memory, and a computing circuit for computing white and black areas. With these circuits the histogram operating circuit is adapted to further compute the control values such as limiter level, accumulation start/stop luminance level, etc. The average value of input luminance signal is computed from the histogram memory data and along the following equation (1).

$$\text{average value} = (\text{input luminance levels}) \times (\text{histogram values}) \div (\text{total number of picture elements}) \quad (1)$$

The mode value designates an input luminance signal level causing a maximum of histogram data. The maximum value detected by the detection circuit designates an input luminance level corresponding to an upper limit of the histogram distribution, and the detected minimum value designates an input luminance level corresponding to a lower limit of the histogram distribution. The black area designates picture elements of input signal luminance levels, for example, in a luminance range of 0 to 40% of the histogram distribution while the white area designates picture element of input signal luminance levels, for example, in a luminance range of more than 60% of the histogram distribution. The deviation coefficient may be calculated as a standard deviation or alternatively may be calculated simply along the following equation (2).

$$(\text{deviation coefficient}) =$$

[(maximum value) - (minimum value)] × constant

÷ (maximum value of histogram) (2)

The histogram operating circuit 3 of the gradation corrector shown in present Fig. 4 is substantially the same constitution and function as the preceding circuit just mentioned.

In the above type gradation correctors, however, since the minimum value of the histogram to be detected is an instantaneous value detected from the histogram in one vertical scanning interval, there is a problem that if many noises are included in a video signal, the minimum value detected has a great variation with the result that the corrected output luminance signal oscillates, which value may affect to such corrected output luminance signal more significantly than other histogram features.

SUMMARY OF THE INVENTION

Objects of the present invention made to solving the above-mentioned problem in the preceding correctors are to provide a gradation corrector which can make a smooth correction so that the minimum value to be detected is not affected by noises or the like and to provide a gradation corrector which can follow a change in video scene with no delay in response.

According to one aspect of the present invention, there is provided a gradation corrector comprising:

a histogram memory for storing a histogram of an input video luminance signal;
a histogram operating circuit connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;
a limiter/adder circuit connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the valve of addition;
an accumulation control register circuit and a normalization control register circuit each connected to an output of the histogram operating circuit;
a histogram accumulation circuit connected to the histogram memory and the accumulation control register circuit for making a cumulative addition of output data of the histogram memory;
a cumulative histogram memory for storing the result of cumulative addition;
a look-up table operating circuit connected to the cumulative histogram memory and the normalization control register circuit for normalizing data of the cumulative histogram memory; and
a look-up table memory for storing the result of normalization;
wherein the accumulation control register circuit is arranged to control the data range of the cumulative addition of the histogram accumulation circuit in response to the accumulation start level and accumulation stop level output from the histogram operating circuit;
the normalization control register circuit is arranged to receive the maximum luminance level output from the histogram operating circuit and to control the normalizing operation of the look-up table operating circuit so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit;
said histogram operating circuit including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a circuit arranged to receive an input video signal and for detecting a S/N ratio of said input video signal; and a clipping circuit connected to an output of the S/N ratio detecting circuit and an output of the histogram memory for clipping said output of the histogram memory and outputting a detected minimum value; a clipping level of the clipping circuit being controlled by the output of the S/N ratio detecting circuit.

With the above construction, it is possible to prevent a large variation of the minimum value to be detected, which variation may be caused from noises included in the video signal. As a result, it is possible to realize an excellent gradation corrector in which a corrected output signal does not oscillate.

According to another aspect of the present invention there is provided a gradation corrector comprising:

a histogram memory for storing a histogram of an input video luminance signal;
a histogram operating circuit connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;

a limiter/adder circuit connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the valve of addition;
an accumulation control register circuit and a normalization control register circuit each connected to an output of the histogram operating circuit;
a histogram accumulation circuit connected to the histogram memory and the accumulation control register circuit for making a cumulative addition of output data of the histogram memory;
a cumulative histogram memory for storing the result of cumulative addition;
a look-up table operating circuit connected to the cumulative histogram memory and the normalization control register circuit for normalizing data of the cumulative histogram memory; and
a look-up table memory for storing the result of normalization;
wherein the accumulation control register circuit is arranged to control the data range of the cumulative addition of the histogram accumulation circuit in response to the accumulation start level and accumulation stop level output from the histogram operating circuit;
the normalization control register circuit is arranged to receive the maximum luminance level output from the histogram operating circuit and to control the normalizing operation of the look-up table operating circuit so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit;
said histogram operating circuit including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a clipping circuit connected to an output of the histogram memory for clipping said output of the histogram memory and outputting a detected minimum value;
a circuit connected to an output of said clipping circuit for detecting a change in video scene;
a recursive filter circuit composed of an adder connected to the output of the clipping circuit and a circuit connected to an output and an input of the adder for multiplying the output of the adder by a certain coefficient K;
an output of the video scene change detecting circuit being connected to the multiplication circuit and the value of the coefficient K being controlled by said output of the video scene change detecting circuit. Thereby, a variation of a value to be detected, which may be caused from noises or the like, can be suppressed greatly in accordance with the degree of change in scene. As a result, it is possible to provide an excellent gradation corrector which can make a smooth correction.

According to a further aspect of the present invention there is provided a gradation corrector comprising:

a histogram memory for storing a histogram of an input video luminance signal;
a histogram operating circuit connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;
a limiter/adder circuit connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the valve of addition;
an accumulation control register circuit and a normalization control register circuit each connected to an output of the histogram operating circuit;
a histogram accumulation circuit connected to the histogram memory and the accumulation control register circuit for making a cumulative addition of output data of the histogram memory;
a cumulative histogram memory for storing the result of cumulative addition;
a look-up table operating circuit connected to the cumulative histogram memory and the normalization control register circuit for normalizing data of the cumulative histogram memory; and
a look-up table memory for storing the result of normalization;
wherein the accumulation control register circuit is arranged to control the data range of the cumulative addition of the histogram accumulation circuit in response to the accumulation start level and accumulation stop level output from the histogram operating circuit;
the normalization control register circuit is arranged to receive the maximum luminance level output from the histogram operating circuit and to control the normalizing operation of the look-up table operating circuit so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit;
said histogram operating circuit including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a clipping circuit connected to an output of the histogram memory for clipping said output of the histogram memory and outputting a detected minimum value;
a circuit connected to an output of said clipping circuit for detecting a change in video scene;

a recursive filter circuit composed of an adder connected to the output of the clipping circuit and a circuit connected to an output and an input of the adder for multiplying the output of the adder by a certain coefficient K; and
a two-input/one-output selector circuit connected to the output of the clipping circuit and the output of the recursive filter circuit for making a change-over between the output of the recursive filter circuit and the output of the clipping circuit in accordance with an output of the video scene change detecting circuit. Thereby, when the video scene has a sudden change, a delay in response owing to the recursive filter circuit can be avoided. As a result, it is possible to realize an excellent gradation corrector which can make a gradation correction following a change in video scene.

With the above-mentioned various constructions of the present invention,the following effects are provided. It is possible to prevent a variation of a detected value due to noises by detecting the S/N ratio of the input video signal and changing the clipping level of the clipping circuit for detection of the minimum value in accordance with the level or magnitude of the S/N ratio. Also, it is possible to make a smooth correction with the suppressed variation of the minimum value to be detected by additionally providing the recursive filter circuit and changing the feedback coefficient of the recursive filter circuit in accordance with the degree of a change in video scene. Further, in the case where the video scene has a sudden change, it is possible to avoid a delay in response by outputting an instantaneous value without being passed through the recursive filter circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of an essential portion of one embodiment of the present invention;
Fig. 2 shows a block diagram of an essential portion of another embodiment of the present invention;
Fig. 3 shows a block diagram of an essential portion of still another embodiment of the present invention;
Fig. 4 shows a block diagram of a gradation corrector; and
Figs. 5A to 5F show waveforms for explaining the operation of the gradation corrector shown in Fig. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The output signal e of the histogram operating circuit 3 shown in Fig. 4 representatively indicates signals of the control values such as limiter level, addition value, accumulation start/stop luminance levels. These control values are also calculated by the operating circuit 3 in dependence upon histogram features such as mean value, mode value, minimum value, etc. computed or detected in the circuit 3. Figs. 1 to 3 show in dashed blocks circuits for the detection of the minimum value of the histogram, which circuits are included in the respective histogram operating and circuits 3. The respective minimum value detection circuit results in controlling the output signal e of the circuit 3.

(Embodiment 1)

Fig. 1 shows a main part of one embodiment of the present invention. In the figure, reference numeral 2 designates a histogram memory which is the same as that used in the conventional gradation corrector. Numeral 50 designates an S/N detecting circuit which detects the level of noise included in a video signal. Numeral 51 designates a clipping circuit which clips a frequency which is not higher than a certain level to have a clipped level zero.

Explanation will now be made of the operation of the above construction. First, the level of noises in a video signal is detected by the S/N detecting circuit 50. Then, a clipping level of the clipping circuit 51 is changed in accordance with an output level of the S/N detecting circuit 51. More particularly, the clipping level is made large in the case where many noises are involved and small in the case where less noises are involved.

According to the present embodiment as described above, a large variation of the minimum value to be detected, which variation may be caused from noises included in the video signal, can be prevented by providing the S/N detecting circuit 50 and the clipping circuit 51 which is connected to the S/N detecting circuit 50 and the clipping level of which is controlled by an output of the S/N detecting circuit 50. As a result, it is possible to make a gradation correction with no oscillation of a corrected output signal.

(Embodiment 2)

Fig. 2 shows another embodiment of the present invention. In the figure, reference numerals 2 and 51 designate a histogram memory and a clipping circuit which are the same as those shown in Fig. 1. Numeral 52 designates a video scene change detecting circuit which detects the degree of change in video scene. Numeral 53 designates an adder and numeral 54 designates a xK circuit which multiplies feedback data by the weight K. The adder 53 and the xK circuit 54 form a recursive filter circuit.

Explanation will now be made of the operation of the above construction. First, a frequency not higher than a certain level is clipped to zero by the clipping circuit 51 and an output signal of the clipping circuit 51 is connected to the recursive filter circuit. Then, the weight K of a feedback coefficient of the recursive filter circuit is controlled by an output of the video scene change detecting circuit 52 or in accordance of the degree of change in video scene to the optimum value in a range where the minimum value to be detected does not oscillate. More especially, when the change in video scene is small, the value of K is made large.

According to the present embodiment as described above, a variation of a value to be detected, which may be caused from noises or the like, can be suppressed greatly by providing the video scene change detecting circuit 52, the adder 53 and the xK circuit 54 the feedback coefficient of which is controlled by an output of the video scene change detecting circuit 52. As a result, it is possible to make a smooth gradation correction.

(Embodiment 3)

Fig. 3 shows still another embodiment of the present invention. In the figure, reference numerals 2, 51, 52, 53 and 54 designate a histogram memory, a clipping circuit, a video scene change detecting circuit, an adder and a xK circuit which are the same as those shown in Fig. 2. Numeral 55 designates a two-input/one-output selector circuit which makes a change-over between an output of the clipping circuit 51 and an output of the recursive filter circuit in accordance with an output of the video scene change detecting circuit 52.

The operation of the above construction will now be explained. First, a frequency not higher than a certain level is clipped to zero by the clipping circuit 51 and an output of the clipping circuit 51 is connected to the recursive filter circuit. Then, the selector circuit 55 selects an output of the recursive filter circuit usually and the output of the clipping circuit 51 when a video scene has a sudden change.

According to the present embodiment as described above, a delay in response, which may be caused owing to the recursive filter circuit when the video scene has a sudden change, can be avoided by providing the video scene change detecting circuit 52, the adder 53, the xK circuit 54 and the selector circuit 55 which is controlled by an output of the video scene detecting circuit 52. As a result, it is possible to make a smooth gradation correction which follows a change in video scene.

Claims

1. A gradation corrector comprising:

a histogram memory (2) for storing a histogram of an input video luminance signal;
a histogram operating circuit (3) connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;
a limiter/adder circuit (5) connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the value of addition;
an accumulation control register circuit (6) and a normalization control register circuit (7) each connected to an output of the histogram operating circuit;
a histogram accumulation circuit (8) connected to the histogram memory (2) and the accumulation control register circuit (6) for making a cumulative addition of output data of the histogram memory (2);
a cumulative histogram memory (9) for storing the result of cumulative addition;
a look-up table operating circuit (10) connected to the cumulative histogram memory (9) and the normalization control register circuit (7) for normalizing data of the cumulative histogram memory; and
a look-up table memory (11) for storing the result of normalization;
wherein the accumulation control register circuit (6) is arranged to control the data range of the cumulative addition of the histogram accumulation circuit (8) in response to the accumulation start level and accumulation stop level output from the histogram operating circuit (3);
the normalization control register circuit (7) is arranged to receive the maximum luminance level output from the histogram operating circuit (3) and to control the normalizing operation of the look-up table operating circuit (10) so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit (7);
said histogram operating circuit (3) including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a circuit (50) arranged to receive an input video signal and for detecting a S/N ratio of said input video signal;

and a clipping circuit (51) connected to an output of the S/N ratio detecting circuit and an output of the histogram memory for clipping said output of the histogram memory (2) and outputting a detected minimum value; a clipping level of the clipping circuit being controlled by the output of the S/N ratio detecting circuit.

2. A gradation corrector comprising:

a histogram memory (2) for storing a histogram of an input video luminance signal;
a histogram operating circuit (3) connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;
a limiter/adder circuit (5) connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the value of addition;
an accumulation control register circuit (6) and a normalization control register circuit (7) each connected to an output of the histogram operating circuit;
a histogram accumulation circuit (8) connected to the histogram memory (2) and the accumulation control register circuit (6) for making a cumulative addition of output data of the histogram memory (2);
a cumulative histogram memory (9) for storing the result of cumulative addition;
a look-up table operating circuit (10) connected to the cumulative histogram memory (9) and the normalization control register circuit (7) for normalizing data of the cumulative histogram memory; and
a look-up table memory (11) for storing the result of normalization;
wherein the accumulation control register circuit (6) is arranged to control the data range of the cumulative addition of the histogram accumulation circuit (8) in response to the accumulation start level and accumulation stop level output from the histogram operating circuit (3);
the normalization control register circuit (7) is arranged to receive the maximum luminance level output from the histogram operating circuit (3) and to control the normalizing operation of the look-up table operating circuit (10) so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit (7);
said histogram operating circuit (3) including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a clipping circuit (51) connected to an output of the histogram memory (2) for clipping said output of the histogram memory (2) and outputting a detected minimum value;
a circuit (52) connected to an output of said clipping circuit (51) for detecting a change in video scene;
a recursive filter circuit composed of an adder (53) connected to the output of the clipping circuit (51) and a circuit (54) connected to an output and an input of the adder (53) for multiplying the output of the adder by a certain coefficient K;
an output of the video scene change detecting circuit (52) being connected to the multiplication circuit and the value of the coefficient K being controlled by said output of the video scene change detecting circuit.

3. A gradation corrector comprising:

a histogram memory (2) for storing a histogram of an input video luminance signal;
a histogram operating circuit (3) connected to the histogram memory for determining characteristic features of the histogram data in the histogram memory and for determining and outputting control values comprising a limiter level, a value of addition, an accumulation start level, an accumulation stop level and a maximum luminance level;
a limiter/adder circuit (5) connected to an output of the histogram operating circuit for limiting the data of the histogram memory in accordance with the limiter level and adding thereto the value of addition;
an accumulation control register circuit (6) and a normalization control register circuit (7) each connected to an output of the histogram operating circuit;
a histogram accumulation circuit (8) connected to the histogram memory (2) and the accumulation control register circuit (6) for making a cumulative addition of output data of the histogram memory (2);
a cumulative histogram memory (9) for storing the result of cumulative addition;
a look-up table operating circuit (10) connected to the cumulative histogram memory (9) and the normalization control register circuit (7) for normalizing data of the cumulative histogram memory; and
a look-up table memory (11) for storing the result of normalization;
wherein the accumulation control register circuit (6) is arranged to control the data range of the cumulative addition of the histogram accumulation circuit (8) in response to the accumulation start level and accumulation

stop level output from the histogram operating circuit (3);
the normalization control register circuit (7) is arranged to receive the maximum luminance level output from the histogram operating circuit (3) and to control the normalizing operation of the look-up table operating circuit (10) so that the maximum value of the cumulative histogram data after normalization is the maximum luminance level output from the normalization control register circuit (7);
said histogram operating circuit (3) including a circuit for detecting a minimum value of the histogram;
the minimum value detecting circuit comprising:
a clipping circuit (51) connected to an output of the histogram memory (2) for clipping said output of the histogram memory (2) and outputting a detected minimum value;
a circuit (52) connected to an output of said clipping circuit (51) for detecting a change in video scene;
a recursive filter circuit composed of an adder (53) connected to the output of the clipping circuit (51) and a circuit (54) connected to an output and an input of the adder (53) for multiplying the output of the adder by a certain coefficient K; and
a two-input/one-output selector circuit (55) connected to the output of the clipping circuit (51) and the output of the recursive filter circuit for making a change-over between the output of the recursive filter circuit and the output of the clipping circuit in accordance with an output of the video scene change detecting circuit.

Patentansprüche

1. Gradationskorrektureinrichtung mit:

einem Histogrammspeicher (2) zum Speichern eines Histogramms eines Eingangsvideoluminanzsignals;

einer mit dem Histogrammspeicher verbundenen Histogrammoperationsschaltung (3) zum Bestimmen von charakteristischen Eigenschaften der Histogrammdaten in dem Histogrammspeicher zum Bestimmen und Ausgeben von Steuerungswerten einschließlich eines Grenzpegels, eines Additionswerts, eines Akkumulationsstartpegels, eines Akkumulationsstoppegels und eines Maximalluminanzpegels;

einer mit einem Ausgang der Histogrammoperationsschaltung verbundenen Begrenzer-/Addiererschaltung (5) zum Begrenzen der Daten des Histogrammspeichers entsprechend dem Grenzpegel und Dazuaddieren des Additionswerts;

eine Akkumulationssteuerungsregisterschaltung (6) und eine Normalisierungssteuerungsregisterschaltung (7), die jeweils mit einem Ausgang der Histogrammoperationsschaltung verbunden sind;

einer mit dem Histogrammspeicher (2) und der Akkumulationssteuerungsregisterschaltung (6) verbundenen Histogrammakkumulationsschaltung (8) zum Ausführen einer kumulativen Addition der Ausgangsdaten des Histogrammspeichers (2);

einem kumulativen Histogrammspeicher (9) zum Speichern des Resultats der kumulativen Addition;

einer mit dem kumulativen Histogrammspeicher (9) und der Normalisierungssteuerungsregisterschaltung (7) verbundenen Look-Up-Tabellenoperationsschaltung (10) zum Normalisieren der Daten des kumulativen Histogrammspeichers; und

einem Look-Up-Tabellenspeicher (11) zum Speichern des Resultats der Normalisierung;

wobei die Akkumulationssteuerungsregisterschaltung (6) dazu ausgelegt ist, den Datenbereich der kumulativen Addition der Histogrammakkumulationsschaltung (8) ansprechend auf den Akkumulationsstartpegel und den Akkumulationsstoppegel, ausgegeben von der Histogrammoperationsschaltung (3), zu steuern;

die Normalisierungssteuerungsregisterschaltung (7) ausgelegt ist zum Empfangen des aus der Histogrammoperationsschaltung (3) ausgegebenen Maximalluminanzpegels und zum Steuern der Normalisierungsoperation der Look-Up-Tabellenoperationsschaltung (10) derart, daß der Maximalwert der Kumulativhistogrammdaten nach der Normalisierung der aus der Normalisierungssteuerungsregisterschaltung (7) ausgegebene Maximalluminanzpegel ist;

wobei die Histogrammoperationsschaltung (3) eine Schaltung zum Erfassen eines Minimalwerts des Histogramms aufweist;

wobei die Minimalwerterfassungsschaltung aufweist:

eine Schaltung (50) ausgelegt zum Empfangen eines Eingangsvideosignals und zum Erfassen eines Signalrauschverhältnisses des Eingangsvideosignals; und eine mit einem Ausgangs der Signalrauschverhältniserfassungsschaltung und einem Ausgang des Histogrammspeichers verbundene Abschneidschaltung (51) zum Abschneiden des Ausgangs des Histogrammspeichers (2) und Ausgeben eines erfaßten Minimalwerts; wobei ein Abschneidpegel der Abschneidschaltung durch den Ausgang der Signalrauschverhältniserfassungsschaltung gesteuert ist.

2. Gradationskorrektureinrichtung mit:

einem Histogrammspeicher (2) zum Speichern eines Histogramms eines Eingangsvideoluminanzsignals;

einer mit dem Histogrammspeicher verbundenen Histogrammoperationsschaltung (3) zum Bestimmen von charakteristischen Eigenschaften der Histogrammdaten in dem Histogrammspeicher zum Bestimmen und Ausgeben von Steuerungswerten einschließlich eines Grenzpegels, eines Additionswerts, eines Akkumulationsstartpegels, eines Akkumulationsstoppegels und eines Maximalluminanzpegels;

einer mit einem Ausgang der Histogrammoperationsschaltung verbundenen Begrenzer-/Addiererschaltung (5) zum Begrenzen der Daten des Histogrammspeichers entsprechend dem Grenzpegel und Dazuaddieren des Additionswerts;

eine Akkumulationssteuerungsregisterschaltung (6) und eine Normalisierungssteuerungsregisterschaltung (7), die jeweils mit einem Ausgang der Histogrammoperationsschaltung verbunden sind;

einer mit dem Histogrammspeicher (2) und der Akkumulationssteuerungsregisterschaltung (6) verbundenen Histogrammakkumulationsschaltung (8) zum Ausführen einer kumulativen Addition der Ausgangsdaten des Histogrammspeichers (2);

einem kumulativen Histogrammspeicher (9) zum Speichern des Resultats der kumulativen Addition;

einer mit dem kumulativen Histogrammspeicher (9) und der Normalisierungssteuerungsregisterschaltung (7) verbundenen Look-Up-Tabellenoperationsschaltung (10) zum Normalisieren der Daten des kumulativen Histogrammspeichers; und

einem Look-Up-Tabellenspeicher (11) zum Speichern des Resultats der Normalisierung;

wobei die Akkumulationssteuerungsregisterschaltung (6) dazu ausgelegt ist, den Datenbereich der kumulativen Addition der Histogrammakkumulationsschaltung (8) ansprechend auf den Akkumulationsstartpegel und den Akkumulationsstoppegel, ausgegeben von der Histogrammoperationsschaltung (3), zu steuern;

die Normalisierungssteuerungsregisterschaltung (7) ausgelegt ist zum Empfangen des aus der Histogrammoperationsschaltung (3) ausgegebenen Maximalluminanzpegels und zum Steuern der Normalisierungsoperation der Look-Up-Tabellenoperationsschaltung (10) derart, daß der Maximalwert der Kumulativhistogrammdaten nach der Normalisierung der aus der Normalisierungssteuerungsregisterschaltung (7) ausgegebene Maximalluminanzpegel ist;

wobei die Histogrammoperationsschaltung (3) eine Schaltung zum Erfassen eines Minimalwerts des Histogramms aufweist;

wobei die Minimalwerterfassungsschaltung aufweist:

eine mit einem Ausgang des Histogrammspeichers (2) verbundene Abschneidschaltung (51) zum Abschneiden des Ausgangs des Histogrammspeichers (2) und Ausgeben eines erfaßten Minimalwerts;

eine mit einem Ausgang der Abschneidschaltung (51) verbundenen Schaltung (52) zum Erfassen einer Videoszenenveränderung;

eine aus einem mit dem Ausgang der Abschneidschaltung (51) verbundenen Addierer (53) und einer mit einem Ausgang und einem Eingang des Addierers (53) verbundenen Schaltung (54) zum Multiplizieren des Ausgangs des Addierers mit einem bestimmen Koeffizienten K aufgebaute Rekursivfilterschaltung;

wobei ein Ausgang der Videoszenenveränderungserfassungsschaltung (52) mit der Multiplikationsschaltung verbunden ist und der Wert des Koeffizienten K durch den Ausgang der Videoszenenveränderungserfassungsschaltung gesteuert ist.

3. Gradationskorrektureinrichtung mit:

einem Histogrammspeicher (2) zum Speichern eines Histogramms eines Eingangsvideoluminanzsignals;

einer mit dem Histogrammspeicher verbundenen Histogrammoperationsschaltung (3) zum Bestimmen von charakteristischen Eigenschaften der Histogrammdaten in dem Histogrammspeicher zum Bestimmen und Ausgeben von Steuerungswerten einschließlich eines Grenzpegels, eines Additionswerts, eines Akkumulationsstartpegels, eines Akkumulationsstoppegels und eines Maximalluminanzpegels;

einer mit einem Ausgang der Histogrammoperationsschaltung verbundenen Begrenzer-/Addiererschaltung (5) zum Begrenzen der Daten des Histogrammspeichers entsprechend dem Grenzpegel und Dazuaddieren des Additionswerts;

eine Akkumulationssteuerungsregisterschaltung (6) und eine Normalisierungssteuerungsregisterschaltung (7), die jeweils mit einem Ausgang der Histogrammoperationsschaltung verbunden sind;

einer mit dem Histogrammspeicher (2) und der Akkumulationssteuerungsregisterschaltung (6) verbundenen Histogrammakkumulationsschaltung (8) zum Ausführen einer kumulativen Addition der Ausgangsdaten des Histogrammspeichers (2);

einem kumulativen Histogrammspeicher (9) zum Speichern des Resultats der kumulativen Addition;

einer mit dem kumulativen Histogrammspeicher (9) und der Normalisierungssteuerungsregisterschaltung (7) verbundenen Look-Up-Tabellenoperationsschaltung (10) zum Normalisieren der Daten des kumulativen Histogrammspeichers; und

einem Look-Up-Tabellenspeicher (11) zum Speichern des Resultats der Normalisierung;

wobei die Akkumulationssteuerungsregisterschaltung (6) dazu ausgelegt ist, den Datenbereich der kumulativen Addition der Histogrammakkumulationsschaltung (8) ansprechend auf den Akkumulationsstartpegel und den Akkumulationsstoppegel, ausgegeben von der Histogrammoperationsschaltung (3), zu steuern;

die Normalisierungssteuerungsregisterschaltung (7) ausgelegt ist zum Empfangen des aus der Histogrammoperationsschaltung (3) ausgegebenen Maximalluminanzpegels und zum Steuern der Normalisierungsoperation der Look-Up-Tabellenoperationsschaltung (10) derart, daß der Maximalwert der Kumulativhistogrammdaten nach der Normalisierung der aus der Normalisierungssteuerungsregisterschaltung (7) ausgegebene Maximalluminanzpegel ist;

wobei die Histogrammoperationsschaltung (3) eine Schaltung zum Erfassen eines Minimalwerts des Histogramms aufweist;

wobei die Minimalwerterfassungsschaltung aufweist:

eine mit einem Ausgang des Histogrammspeichers (2) verbundene Abschneidschaltung (51) zum Abschneiden des Ausgangs des Histogrammspeichers (2) und Ausgeben eines erfaßten Minimalwerts;

eine mit einem Ausgang der Abschneidschaltung (51) verbundene Schaltung (52) zum Erfassen einer Video-

szenenveränderung;

eine aus einem mit dem Ausgang der Abschneidschaltung (51) verbundenen Addierer (53) und einer mit einem Ausgang und einem Eingang des Addierers (53) verbundenen Schaltung (54) zum Multiplizieren des Ausgangs des Addierers mit einem bestimmen Koeffizienten K aufgebaute Rekursivfilterschaltung; und

eine mit dem Ausgang der Abschneidschaltung (51) und dem Ausgang der Rekursivfilterschaltung verbundene Zweieingangs/Einausgangsauswahlschaltung (55) zum Umschalten zwischen dem Ausgang der Rekursivfilterschaltung und dem Ausgang der Abschneidschaltung entsprechend einem Ausgang der Videoszenenveränderungserfassungsschaltung.

Revendications

1. Correcteur de gradation comprenant :

une mémoire d'histogramme (2) destinée à stocker l'histogramme d'un signal de luminance d'entrée vidéo ;
un circuit fonctionnel d'histogramme (3) connecté à la mémoire d'histogramme pour déterminer les particularités caractéristiques des données d'histogramme de la mémoire d'histogramme et pour déterminer et sortir des valeurs de commande comportant un niveau limiteur, une valeur d'addition, un niveau de démarrage d'accumulation, un niveau d'arrêt d'accumulation et un niveau maximal de luminance ;
un circuit limiteur/additionneur (5) connecté à une sortie du circuit fonctionnel d'histogramme destiné à limiter les données de la mémoire d'histogramme conformément au niveau limiteur et à additionner la valeur d'addition qui s'y trouve ;
un circuit enregistreur de commande d'accumulation (6) et un circuit enregistreur de commande de normalisation (7), chacun étant connecté à une sortie du circuit fonctionnel d'histogramme ;
un circuit d'accumulation d'histogramme (8) connecté à la mémoire d'histogramme (2) et au circuit enregistreur de commande d'accumulation (6) pour effectuer une addition cumulative des données de sortie de la mémoire d'histogramme (2) ;
une mémoire cumulative d'histogramme (9) destinée à stocker le résultat de l'addition cumulative ;
un circuit fonctionnel de table à consulter (10) connecté à la mémoire cumulative d'histogramme (9) et au circuit enregistreur de commande de normalisation (7) destiné à normaliser les données de la mémoire cumulative d'histogramme ; et
une mémoire de table à consulter (11) destinée à stocker le résultat de la normalisation ;
dans lequel le circuit enregistreur de commande d'accumulation (6) est aménagé pour commander la plage de données de l'addition cumulative du circuit d'accumulation d'histogramme (8) en réponse au niveau de démarrage d'accumulation et au niveau d'arrêt d'accumulation sorti du circuit de commande d'histogramme (3) ;
dans lequel le circuit enregistreur de commande de normalisation (7) est aménagé pour recevoir le niveau maximal de luminance reçu du circuit de commande d'histogramme (3) et pour commander l'opération de normalisation du circuit de commande de table à consulter (10) de sorte que la valeur maximale des données cumulatives d'histogramme après la normalisation correspond au niveau de luminance maximal sortis du circuit enregistreur de commande de normalisation (7) ;
ledit circuit de commande d'histogramme (3) comprenant un circuit destiné à détecter une valeur minimale de l'histogramme ;
le circuit de détection de valeur minimale comportant :
un circuit (50) aménagé pour recevoir un signal d'entrée vidéo et destiné à détecter le rapport S/N dudit signal d'entrée vidéo ; et un circuit écrêteur (51) connecté à une sortie du circuit de détection du rapport S/N et à une sortie de la mémoire d'histogramme destinée à ladite sortie de la mémoire d'histogramme (2) et à sortir une valeur minimale détectée ; le niveau écrêteur du circuit écrêteur étant commandé par la sortie du circuit de détection du rapport S/N.

2. Correcteur de gradation comprenant :

une mémoire d'histogramme destinée à stocker l'histogramme d'un signal de luminance d'entrée vidéo ;
un circuit fonctionnel d'histogramme (3) connecté à la mémoire d'histogramme destiné à déterminer les particularités caractéristiques des données d'histogramme qui se trouvent dans la mémoire d'histogramme et destiné à déterminer et à sortir des valeurs de commande comprenant un niveau limiteur, une valeur d'addition,

un niveau de démarrage d'accumulation, un niveau d'arrêt d'accumulation, et un niveau maximal de luminance ;
un circuit limiteur/additionneur (5) connecté à une sortie du circuit fonctionnel d'histogramme destiné à limiter les données de l'histogramme conformément au niveau limiteur et à additionner la valeur d'addition qui s'y trouve ;
un circuit enregistreur de commande d'accumulation (6) et un circuit enregistreur de commande de normalisation (7), chacun étant connecté à une sortie du circuit de commande d'histogramme ;
un circuit d'accumulation d'histogramme (8) connecté à la mémoire d'histogramme (2) et au circuit enregistreur de commande d'accumulation (6) destiné à effectuer l'addition cumulative des données sorties de la mémoire d'histogramme (2) ;
une mémoire cumulative d'histogramme (9) destinée à stocker le résultat de l'addition cumulative ;
un circuit fonctionnel de table à consulter (10) connecté à la mémoire cumulative d'histogramme (9) et au circuit enregistreur de commande de normalisation (7) pour normaliser les données de la mémoire cumulative d'histogramme ; et
une mémoire de table à consulter 11) destinée à stocker les résultats de la normalisation ;
dans lequel le circuit enregistreur de commande d'accumulation (6) est aménagé pour commander la plage de données de l'addition cumulative du circuit d'accumulation d'histogramme (8) en réponse au niveau de démarrage d'accumulation et au niveau d'arrêt d'accumulation sortis du circuit fonctionnel d'histogramme (3) ;
dans lequel le circuit enregistreur de commande de normalisation (7) est aménagé pour recevoir le niveau maximal de luminance sorti du circuit fonctionnel d'histogramme (3) et pour commander l'opération de normalisation du circuit fonctionnel de table à consulter (10) de sorte que la valeur maximale des données cumulatives d'histogramme après la normalisation corresponde au niveau maximal de luminance sorti du circuit enregistreur de commande de normalisation (7) ;
ledit circuit de commande d'histogramme (3) comprenant un circuit destiné à détecter la valeur minimale de l'histogramme ;
le circuit de détection de la valeur minimale comportant :
un circuit écrêteur (51) connecté à une sortie de la mémoire d'histogramme (2) destiné à écrêter ladite sortie de la mémoire d'histogramme (2) et à sortir une valeur minimale détectée ;
un circuit (52) connecté à une sortie dudit circuit écrêteur (51) destiné à détecter une modification de la séquence vidéo ;
un circuit récurent de filtrage constitué d'un additionneur (53) connecté à la sortie du circuit écrêteur (51) et d'un circuit (54) connecté à une sortie et à une entrée de l'additionneur (53) destiné à multiplier la sortie de l'additionneur par un certain coefficient K ;
une sortie du circuit de détection de modification de la séquence vidéo (52) étant connectée au circuit de multiplication et la valeur du coefficient K étant commandée par ladite sortie dudit circuit de détection de modification de séquence vidéo.

3. Correcteur de gradation comprenant :

une mémoire d'histogramme (2) destinée à stocker l'histogramme d'un signal de luminance d'entrée vidéo ;
un circuit fonctionnel d'histogramme (3) connecté à la mémoire d'histogramme destiné à déterminer les particularités caractéristiques des données d'histogramme qui se trouvent dans la mémoire d'histogramme et destiné à déterminer et à sortir des valeurs de commande comportant un niveau limiteur, une valeur d'addition, un niveau de démarrage d'accumulation, un niveau d'arrêt d'accumulation et un niveau maximal de luminance ;
un circuit limiteur/additionneur (5) connecté à une sortie du circuit fonctionnel d'histogramme destiné à limiter les données de la mémoire d'histogramme conformément au niveau limiteur et à additionner la valeur d'addition qui s'y trouve ;
un circuit enregistreur de commande d'accumulation (6) et un circuit enregistreur de commande de normalisation (7), chacun étant connecté à une sortie du circuit fonctionnel d'histogramme ;
un circuit d'accumulation d'histogramme (8) connecté à la mémoire d'histogramme (2) et au circuit enregistreur de commande d'accumulation (6) destiné à effectuer l'addition cumulative des données de sortie de la mémoire d'histogramme (2) ;
une mémoire cumulative d'histogramme (9) destinée à stocker le résultat de l'addition cumulative ;
un circuit fonctionnel de table à consulter (10) connecté à la mémoire cumulative d'histogramme (9) et au circuit enregistreur de commande de normalisation (7) destiné à normaliser les données de la mémoire cumulative d'histogramme ;
une mémoire de table à consulter destinée à stocker le résultat de la normalisation ;
dans lequel le circuit enregistreur de commande d'accumulation (6) est aménagé pour commander la plage

de données de l'addition cumulative du circuit d'accumulation d'histogramme (8) en réponse au niveau de démarrage d'accumulation et au niveau d'arrêt d'accumulation sorti du circuit fonctionnel d'histogramme (3) ;
dans lequel le circuit enregistreur de commande de normalisation (7) est aménagé pour recevoir le niveau maximal de luminance sorti du circuit fonctionnel d'histogramme (3) et pour commander l'opération de normalisation du circuit fonctionnel de table à consulter (10) de sorte que la valeur maximale des données cumulatives d'histogramme après la normalisation correspond au niveau maximal de luminance sorti du circuit enregistreur de commande de normalisation ;
ledit circuit fonctionnel d'histogramme (3) comprenant un circuit destiné à détecter la valeur minimale de l'histogramme ;
le circuit de détection de valeur minimale comportant :
un circuit écrêteur(51) connecté à une sortie de la mémoire d'histogramme (2) destiné à écrêter ladite sortie de la mémoire d'histogramme et à sortir une valeur minimale détectée ;
un circuit (52) connecté à une sortie dudit circuit écrêteur (51) destiné à détecter une modification de la séquence vidéo ;
un circuit récurent de filtrage constitué d'un additionneur (53) connecté à la sortie du circuit écrêteur (51) et d'un circuit (54) connecté à une sortie et à une entrée de l'additionneur (53) destiné à multiplier la sortie de l'additionneur par un certain coefficient K ; et
un circuit sélecteur à deux entrées/ une sortie (55) connectée à la sortie du circuit écrêteur (51) et à la sortie du circuit récurent de filtrage destinée à effectuer un échange entre la sortie du circuit récurent de filtrage et la sortie du circuit écrêteur conformément à une sortie du circuit de détection de modification de séquence vidéo.

FIG. 1

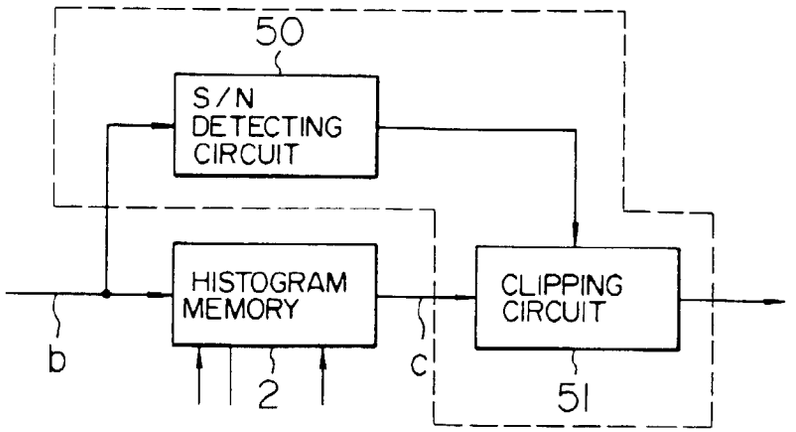

FIG. 2

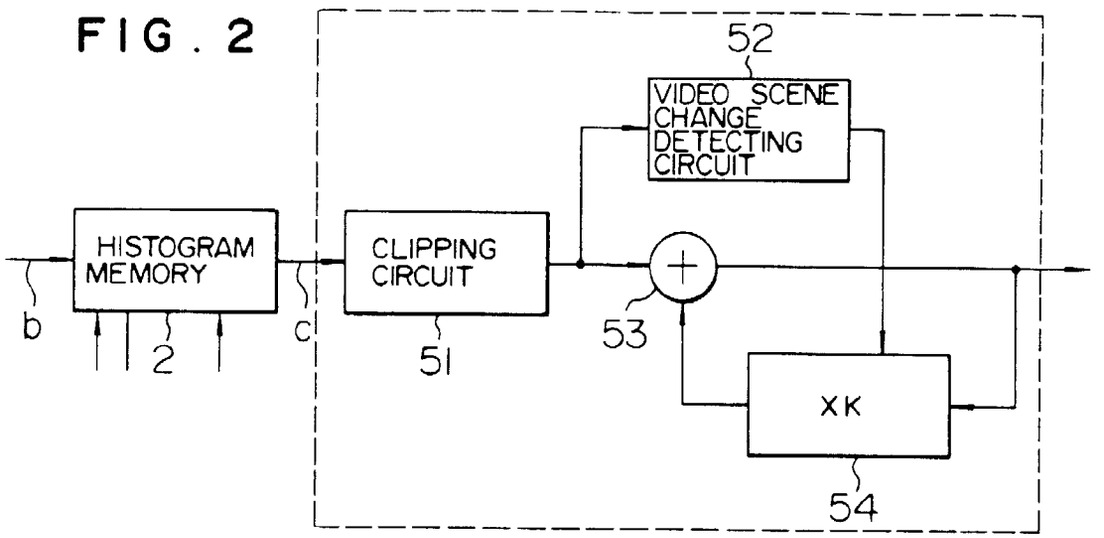

FIG. 3

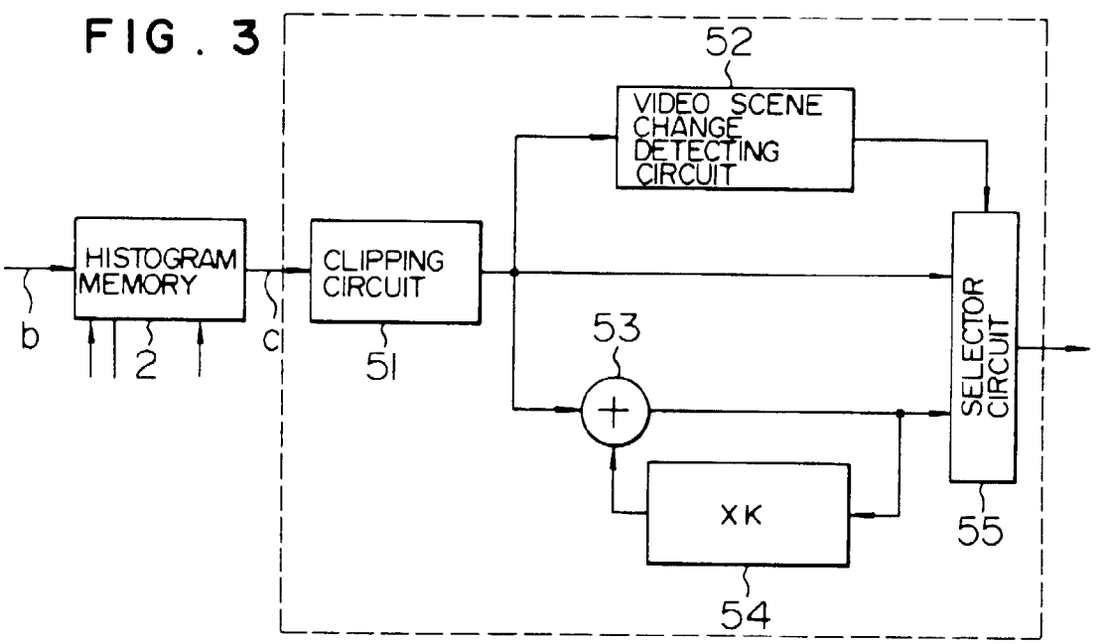

FIG. 4

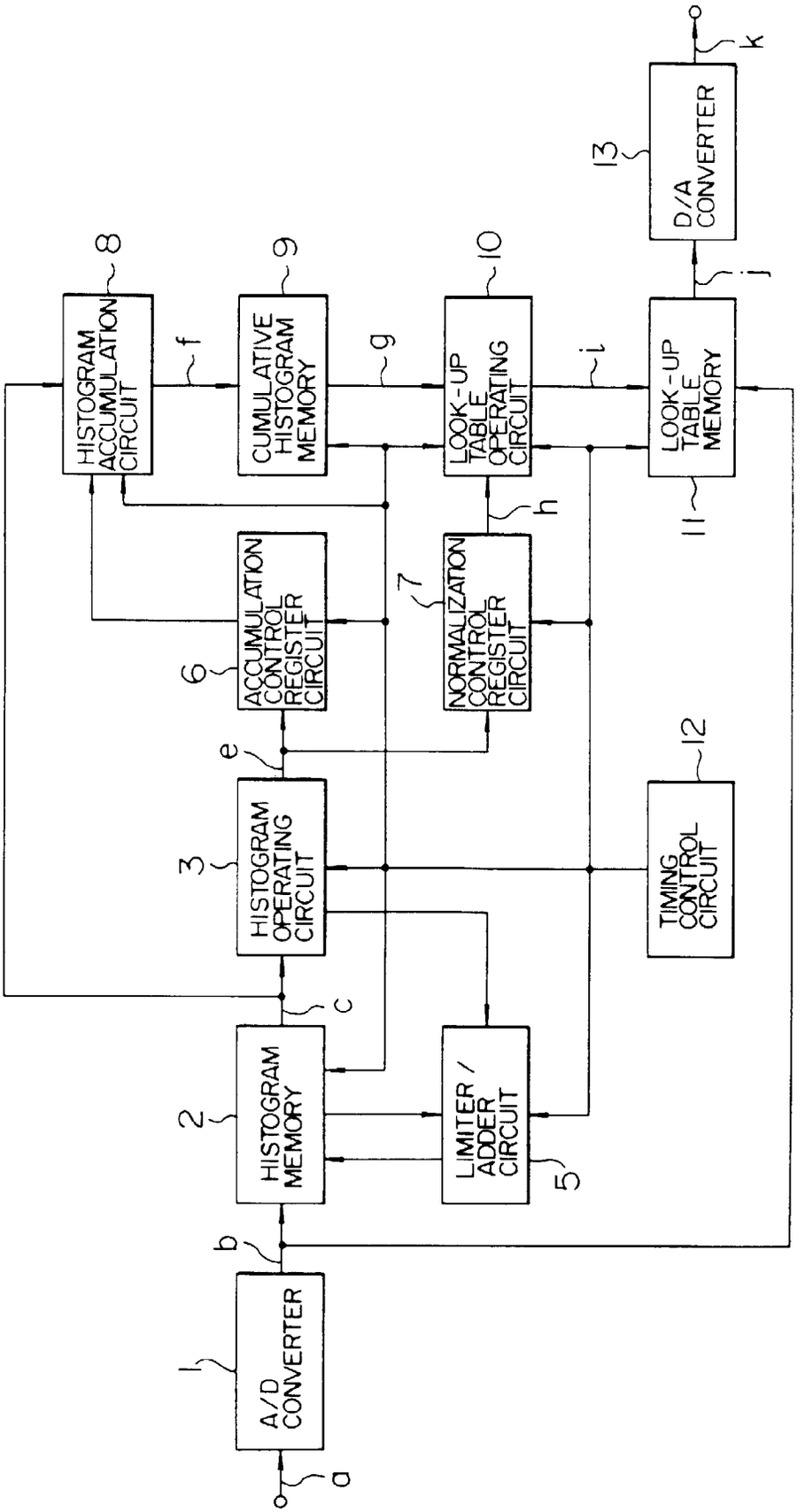
A/D CONVERTER
HISTOGRAM MEMORY
HISTOGRAM OPERATING CIRCUIT
ACCUMULATION CONTROL REGISTER CIRCUIT
NORMALIZATION CONTROL REGISTER CIRCUIT
HISTOGRAM ACCUMULATION CIRCUIT
CUMULATIVE HISTOGRAM MEMORY
LOOK-UP TABLE OPERATING CIRCUIT
LOOK-UP TABLE MEMORY
D/A CONVERTER
LIMITER / ADDER CIRCUIT
TIMING CONTROL CIRCUIT
1
2
3
5
6
7
8
9
10
11
12
13
a
b
c
e
f
g
h
i
j
k

FIG. 5A

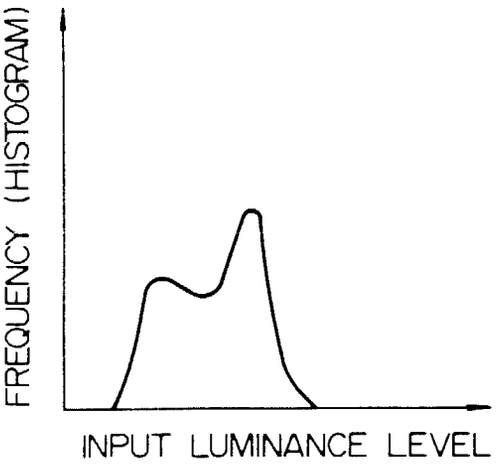

FIG. 5B

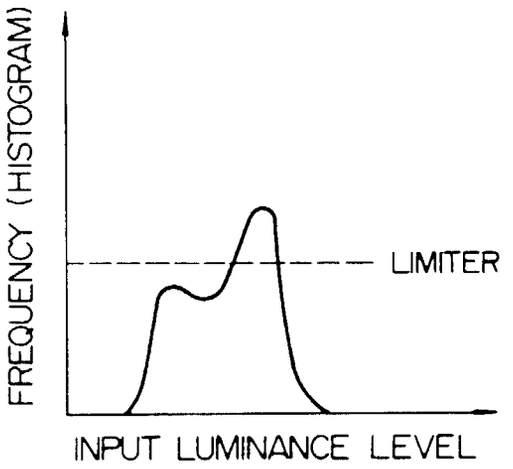

FIG. 5C

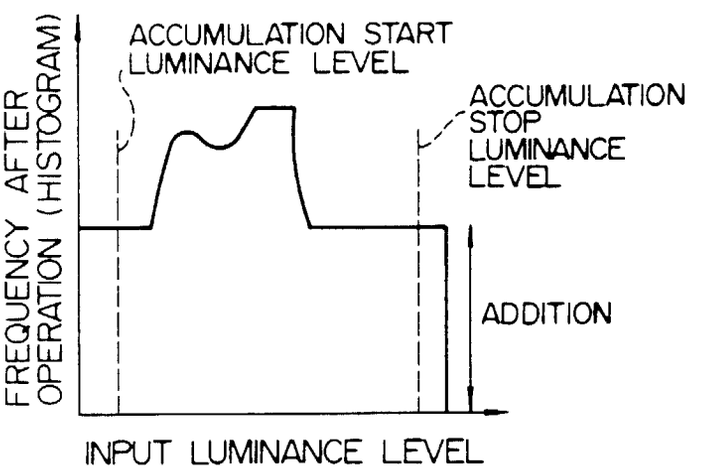

FIG. 5D

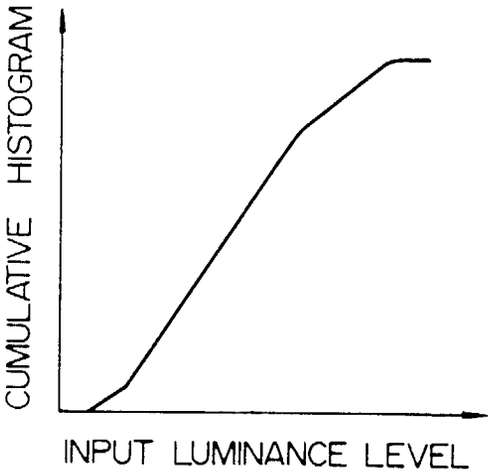

FIG. 5E

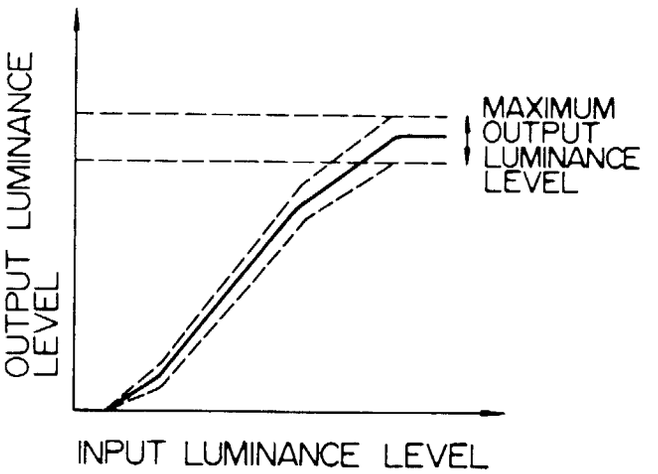

FIG. 5F