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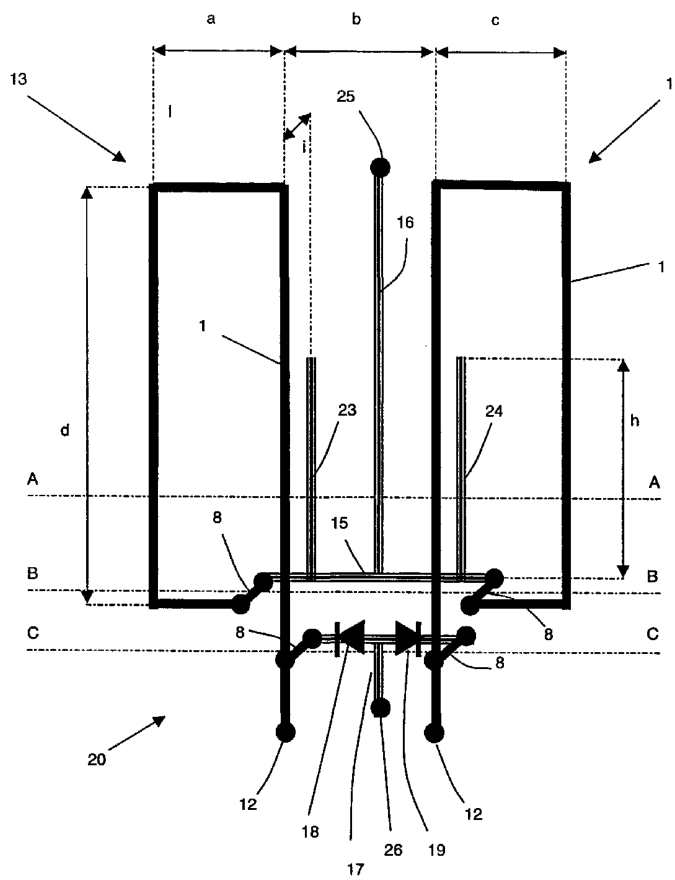

(57) Abstract: LC tank formed on a lossy substrate material having adjacent strips leading current in opposite directions and being arranged in such a way that substrate currents relating to individual strips (1) induced in the lossy substrate (3) are balancing out one another leading to high Q-values. According to one embodiment of the invention a pair of back to back coupled diodes (18, 19) are arranged between the input terminals of the tank and a pair of DC leads (16, 17) are arranged between the midpoint of the inductor structure and the midpoint between the diodes. The tank according to the invention can be implemented in MMIC devices using standard semiconductor substrates without any special treatment of the substrate being needed.

WO 01/88967 A1

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High-Q tank

Field of the invention

The present invention relates to a LC tank formed directly on a low resistivity substrate, such as a thin film substrate or a semiconductor substrate. More specifically, the invention relates to a tank formed on a low resistivity substrate, such as silicon, which is compliant for MMIC (Microwave Monolithic Integrated Circuit) production.

Background of the invention

LC tanks are used in a wide range of electronic circuits. One interesting use for tanks is in resonators, which form essential parts of microwave filters, oscillators etc. Some resonators should typically be tuneable, either because the application requires this functionality or in order to compensate for production tolerances.

The resonant frequency of a LC tank can be given as

$$f = \frac{1}{\sqrt{L \cdot C}},$$

where L is the inductance and C is the total capacitance.

Prior art document US-A-5 173 835 (D1) shows a tuneable tank comprising a voltage variable capacitor or varactor having at the base substrate a silicon wafer with a high resistivity semiconductor material on top of the substrate. An insulating layer of metal oxide having a dielectric constant greater than the dielectric constant of the semiconductor is formed on top of the high resistivity layer and a metal electrode is formed on the insulating layer. When applying a reverse bias voltage over the insulating layer, a depletion layer is created herein and the capacitive value changes such that the capacitor behaves like a variable width capacitor.

Document US-A-5 959 515 (D2) shows a tuneable LC tank having a spiral inductor provided on a dielectric substrate. An interdigitated double polysilicon capacitor and an interdigitated tuneable varactor capacitor are serially connected while subsequently forming a parallel connection with the inductor. By controlling a bias voltage over the tuneable varactor capacitor the capacitive value of the LC tank can be tuned. Although claimed in the above document, resonant frequencies above 1,0 GHz can hardly be accomplished because of high losses in the polysilicon capacitor and in the inductive part of the tank.

The losses for a given tank can be expressed by means of the Q-factor, which in a simple case may be regarded as the ratio of the conserved magnetic energy to the losses. Especially losses in the substrate reduce the Q-value of known devices.

Silicon, which has many excellent properties including a relatively low price, is not an ideal substrate material for LC tanks because of its lossy properties ranging in the area of 0,0001 - 20 Ωm. The relatively low resistance of the material leads to eddy currents being generated in the substrate, which then again lead to losses occurring in the inductor or tank.

Losses in tanks can be overcome by using semiconductor substrates such as GaAs or other high resistivity substrates having a resistivity $\rho > 100$ Ωm, but these substrate materials are relatively expensive.

At microwave frequencies, the total losses are given by ohmic resistance to the currents flowing in the strips and the dielectric losses in the surrounding dielectrics, such as the substrate. The losses and the overall performance of the inductance depend not only on the geometry and materials involved but also on the way the inductors are coupled in the actual application. These effects shall be dealt with briefly in the following by reference to appropriate models for an inductor structure having inherent capacities.

Fig. 1 shows a known simple loop structure being arranged on a dielectric or semiconductor substrate and having an optional ground plane being provided on the opposite side of the substrate. Fig. 2 is a cross-sectional view of the inductor shown on fig. 1.

Fig. 3 relates to a known meander structure, which requires a ground plane for the return current. Fig. 4 is a cross-sectional view of the inductor shown on fig. 3.

The terminals of the inductors can be coupled in various combinations. Fig. 5 , 6 and 7 depicts three main models corresponding to different ways of coupling the inductor and optionally arranging the ground plane for the plane inductors such as those shown in fig. 1 - 4.

In fig. 5 the inductor has a ground plane and is coupled as a two port, that is, the input terminals are formed between the terminal strip and the ground plane and the output port is formed between the terminal relating to the other end of the strip and the terminal of the adjacent ground plane.

In the fig. 5 configuration, return currents are flowing through the ground plane and a parasitic capacitance Cp and resistance Rp exist between the inductor strips and the ground plane. r_{strip} represents the losses in the strips and the losses in the ground plane. Additional ohmic losses (free carrier absorption) appear if the substrate is made of a semiconductor with free-charge carriers. These free carriers cause substrate currents between points of the strips having a potential difference (cf. fig. 2). The losses associated therewith are represented by the shunt loss resistance Rs. Cs is the parasitic capacitance due to the capacitive coupling between the strips and through the dielectric substrate. Finally, the losses relating to the parasitic currents, which are shown in fig. 1a with dotted arrows being of opposite direction to the main strip currents, are represented by the losses in r_{substr} in the model according to fig. 5.

Fig. 6 shows a one-port configuration, whereby the structure is provided with a ground plane on the backside of the substrate and whereby the output port has been shorted. The components correspond to those shown in fig. 5.

For the inductor shown in fig 7, no ground plane has been provided or none of the strip terminals have been grounded. In this case, there is no parasitic capacitance Cp and no parasitic resistance Rp.

It can be demonstrated that in many cases the circuit configurations shown on fig. 5 - 7 may be transformed to the more simplified circuit shown on fig. 8.

It should be noted that using the simplified equivalent of fig. 8 for the fig. 7 arrangement, R equals Rs, C equals Cs and r equals $r_{substr} + r_{strip}$. Correspondingly, it can be shown that the parameters of the simplified equivalent of fig. 8 can also be expressed by means of values calculated on the basis of the parameters given according to fig. 5 and 6.

According to prior art document "On-chip Spiral Inductors With Patterned Ground Shields for Si Based RFICs", by Yue et al, IEEE Journ. Solid State Circuits vol. 33, no. 5, pp. 743, 1998, D3) the Q-factor according to the above simplified embodiment may be given as:

$$Q=\frac{\omega L}{r}\cdot\frac{R}{R+r\left(1+\frac{\omega L}{r}\right)}\cdot\left(1-r^2\frac{C}{L}-\omega^2 LC\right)$$

In the above expression, R equals Rs, while r equals $r_{substr} + r_{strip}$.

Several proposals have been put forward in the past for reducing substrate currents in inductors on lossy substrates in order to increase the Q-value.

Many proposals are based on performing changes in the substrate so as to transform the resistances r and R. In document US-5,757,243 (D4) an inductor has been shown, whereby low and high resistivity layers are formed in the substrate by diffusion or other relevant techniques in order to reduce the substrate currents.

Prior art document "Reducing the substrate losses of RF Integrated Inductors", Mernyei et al., IEEE Microwave and Guided Wave Letters, Vol. 8, No 9, pp. 300, 1998 (D5), discloses a spiral planar inductor, which has been shown in fig. 9 and 10 of this patent application. The inductor according to the above document has a star shaped blocking structure, 2, embedded in the substrate, having layers denoted by reference numerals 4 - 7.

For the inductor according to prior art document D5 mentioned above, slots are provided in the low resistivity substrate under the inductor in order to reduce circumferential currents.

According to prior art document "Large suspended Inductors on Silicon and Their Use in a 2 µm CMOS RF amplifier", by J. Y. C. Chang, IEEE Electron Device Letters, Vol. 14, No. 5, pp. 246, May 1993 (D6) the silicon substrate underneath specific strips in the inductor structure has been removed by under-etching.

The above techniques, however, require additional masks and technological processes, are therefore costly to very costly, and are not practical for large-scale industrial application.

According to JP-A-06 224 042 (D7), a planar inductor has been disclosed comprising two magnetic wafers separated by a glass film, one wafer having slots in the shape of a meander, which enables the formation of a copper inductor being formed adjacent the glass film. The structure of the inductor according to this document has a set of input terminals being arranged close together. The inductor is claimed to provide enhanced high frequency characteristics and a high quality factor value. However, the wafers, which are made of nickel-zinc ferrite, have a high resistance factor. Moreover, the inductor does not appear suitable for the microwave range of above 300 MHz and substantial losses in this range are expected. The inductor according to D5 requires a complex manufacturing technique, which is incompatible with MMIC manufacture.

In prior art document "A Q-factor enhancement technique for MMIC inductors", by M. Danesh et al., IEEE MTT-S Digest, 5/1998 (D8) a square spiral microstrip inductor fabricated in a production silicon IC technology has been disclosed.

According to document D8, it has been shown that driving the microstrip structure differentially yields a significantly higher Q-factor as compared to driving the structure "single ended", i.e. connecting the source to one terminal while connecting the other terminal to ground.

Summary of the invention

One object of the present invention is to set forth a LC tank, which can be manufactured on a low resistivity substrate without any special preparation of the substrate being needed, the LC tank providing a reduced level of induced currents in the substrate and hence higher Q-values.

This object has been achieved by the subject matter defined by independent claim 1.

Further advantageous solutions are defined in the dependent claims, which provide for advantageous combinations of Q-values, inductance values and resistance values.

A further object is to accomplish a tuneable tank providing high Q-values at high frequencies.

This object has been accomplished by the subject matter defined by claim 7.

Among the further important advantages of the invention is that a tank of high mechanical stability has been provided.

Brief description of the drawings

Fig. 1 is a side view of a first known simple loop inductor,

Fig. 2 is an upper view of the first known loop inductor,

Fig. 3 and 4 shows a second known meander inductor,

Fig. 5 - 8 disclose known equivalent circuits for inductors in various coupling schemes,

Fig. 9 and 10 relates to a third structure known according to document (D5),

Fig. 11 and 12 is a schematic illustration of the balancing of substrate currents according to the invention,

Fig. 13 shows a LC tank comprising a varactor according to a first embodiment of the invention, the drawing showing two strip layers presented in an isometric view and diodes in a symbolic view,

Fig. 14 shows a cross-section along line A-A of fig. 13,

Fig. 15 shows a cross-section along line B-B of fig. 13,

Fig. 16 shows a cross-section along line C-C of fig. 13,

Fig. 17 shows an equivalent circuit of the tank according to fig. 13,

Fig. 18 shows another embodiment of a LC tank comprising according to the invention,

Fig. 19 shows a third embodiment of a LC tank according to the invention,

Fig. 20 shows a fourth embodiment of a LC tank according to the invention, and

Fig. 21 shows a fifth embodiment of a LC tank comprising according to the invention.

Detailed description of the preferred embodiments of the invention

For better understanding the invention we shall discuss the general definition of the Q-factor as set out above, namely as the ratio of the stored average energy to the average loss per time unit, the ratio being multiplied with the circular frequency.

The stored energy is given by the inductances and capacitances and may be represented as a sum of self-inductances and mutual inductances of the strips. As a first approximation, ignoring the energy stored in the capacitance, the stored energy in the inductance is proportional to $\sum(L_i + M_{ij})$, where L_i is the self inductance of the i-th strip and M_{ij} is the mutual inductance between strips i and j. For contra-directional currents, the mutual inductance is negative. The losses may be given by the resistances shown in the equivalent circuit of fig. 8. In particular, the losses due to the substrate currents can be expressed as: $P_{substr} = G_1 \cdot i_{substr}{}^2 \cdot r_{substr}$, where G_1 is a geometric factor given by the geometry of the strips and the current distribution in the substrate. Similarly, the losses in the strips are: $P_{str} = G_2 \cdot i_{str}{}^2 \cdot r_{str}$. The reduced current density in the semiconductor substrate and in the ground plane if available, results in lower microwave losses and higher Q-factor values being achieved for the inductor.

According to the present invention the substrate currents and hence the losses of the inductor are reduced by arranging the strips in such a way that the currents induced in the substrate balance one another.

Fig. 12 is a cross sectional schematic representation of an inductor structure relating to a preferred group of inductors according to the invention, whereby the direction of the currents induced in the substrate has been indicated (+ into / · out of the plane of the paper). It is seen that the currents in adjacent strips are of opposite direction.

In fig. 11, the current density in the substrate according to the lateral location has been shown for a given depth. The X-axis in fig. 11 correspond to the surface extension of the substrate shown in fig. 12 and the individual graphs I_{D1} in fig. 11 pertains to the substrate current density, which would occur for a given current magnitude, had the other strips not carried any current. The resultant current density I_{DT} relating to all the strips carrying the same given current magnitude has also been indicated.

From fig. 11 it appears that, the resultant current density is much lower than the current densities relating to the situation where strips are carrying the same current one at a time. This effect takes place because the currents in the substrate generate contra-directional magnetic fields around themselves. The magnetic fields in their turn induce contra-directional currents in the semiconductor substrate as shown in fig. 2. Since these currents are also contra-directional to one another, they partly balance out one another and the resultant substrate current is smaller than the individual substrate currents.

The most effective reduction of the resultant currents is achieved where the strips have identical cross-section, i.e. have the same width w and where the distance b_S between them is sufficiently small to optimise the Q value, i.e. where values of first and foremost r_{substr} , r_{strip} , and L but also Rp, Cs, Cp are optimised.

If the distance between the strips is chosen too small, the inductance L will suffer and the effective resistance r_{substr} will become to small leading to currents leaking between the strips. On the other hand, if the distance is chosen too high the distance between the induced adjacent magnetic fields will not affect one another, and thus not lead to a reduction of currents in the substrate.

To optimise the design of the coil for a given set of parameters such as frequency of interest, substrate thickness, substrate resistivity, strip conductivity and strip cross-section, one needs to change the strip separation, experimentally or numerically, until the currents in the lossy substrate balance one another and the maximum Q-factor is achieved.

Practical experiments show that the balancing of currents in the substrate is dominant for substrates having a resistivity of up to approximately 10 Ω·m.

Particular high Q-values are moreover found where the terminals of the inductor are arranged close together in relation to the wavelength intended for the inductor, i.e. where the distance between the terminals satisfies the following condition: $bt \leq \lambda/\left(10\sqrt{\varepsilon_{ef}}\right)$, where ε_{ef} is the effective dielectric constant of the substrate and λ is the wavelength corresponding to the operational frequency of the inductor. Moreover, good results are achieved where the inductor structure is coupled differentially, i.e. in a coupling where none of the input terminals are connected to the ground plane.

The strips, 1, according to the invention are forming at least a first loop, 13, having one or more segments of pair-wise disposed adjacent parallel legs of substantially the same length, being substantially aligned with one another.

Moreover, the adjacent strips are being arranged for carrying currents in opposite directions, such that currents induced in the lossy substrate from each respective leg in the segment balance each other.

In fig. 13, a first embodiment of the tank 20 has been shown. In fig. 14, 15 and 16 cross sections of the tank 20 according to lines A-A, B-B and C-C, respectively, have been shown. It should be understood that the above mentioned drawings are only schematic and that the true dimensions does not appear from the figures.

The tank 20 comprises four parallel strips 1 and other strips being orthogonal to and connected with the former through corner portions, the strips forming two loops 13 and 14 being symmetrical and connected with one another through a bridge portion 15, formed by a strip in a second strip layer 10. The strips 1 have a uniform width. Two input terminals 12 are formed as a prolongation of the two inner strips of the four parallel strips. The loops are elongate and square shaped. The confined area defined by each loop 13 or 14 and the bridge portion 15 has an aspect ratio d/a of about 3, where a=b=c, approximately.

In fig. 13, the vias are depicted at an oblique angle to bridge portion 15. In reality, the vias are arranged at right angles to the strips.

The bridge portion 15, comprises vias 8 which connect the strip of the bridge portion with the strips 1 of the respective loops 13 and 14. The bridge portion crosses the over- or underlying strip at a right angle. The strips 1 and the bridge portion forms the inductive part of the tank 20.

As will be understood from the structures according to the above figures, the balancing depends on the spacing a, b, and c between the strips in the respective loops and the substrate properties. Of interest is also the aspect ratio defined by the length, d, of the segments having parallel adjacent legs, to the separation distance or segment width, a, b and c. The aspect ratio is approximately d/a=3, where a, b and c are approximately equal. Tests show that good values are found where the aspect ratio of the loop is more than 2 to 1 or less than 1 to 2. Even better results are obtained when the aspect ratio is more than 3 to 1 or less than 1 to 3. Experimental tests can be used to estimate where the balancing effect has its optimum.

The high Q value is also believed to arise from the symmetry of the above structures and the central arrangement of the terminals in relation to the overall inductor structure.

It is noted that the adjacent legs corresponding to the legs of each respective loop, in each of the structures mentioned above, carries current in opposite directions whereby, currents are also balanced between these strips.

Respective cross-sections of a possible substrate / strip configuration for the tank structures according to the invention has been disclosed in fig. 14 - 16. In this exemplary embodiment, the substrate 3 comprises a first silicon dioxide layer 4 on top of a second dioxide layer 5, having a total width, i, of 45 µm thickness. Three conductive layers of gold, preferably, are provided, 1, 10 and 11, forming the respective strips having a thickness, t, of 1 µm. The width, W_1, of the strips 1 is 20 µm. The width, W_2, of the strips 11 are advantageously smaller than the width W_1. The first and second silicon dioxide layer are so-called lossy substrate layers and have a conductivity of 2,5 $(\Omega m)^{-1}$ and the lower silicon layer, 17, of 360 µm has a resistivity smaller than 100 Ohm cm .

As appears from fig. 14 and 15 a pair of capacitive strips 23 and 24 of length h and extending from bridge portion 15 in layer 11 are formed vertically under the strips 1. The capacitive strips 23 and 24 constitute together with the above strips 1, a shunt capacitance, which is dependent on the length h, the dielectric properties of layers 4 and 5 and the height i.

A pair of back to back coupled varactor diodes 18 and 19 are coupled between the input ports 12. The varactor diodes are integrated in the third silicon substrate by a p+ doped area [.....please correct and describe..]. Suitable vias 27 form the connection between a strip 10 and the diodes and the strips 1 through other vias 8.

A pair of bias leads 16, 17 serve for the connections between a DC bias source, $V_{bias}+$ and $V_{bias}-$, and the varactor diodes 18, 19 whereby the capacitive values of the varactor diodes can be regulated. The first bias lead 16 connects to a midpoint on the inductor structure, namely on the midpoint of the bridge 15. The second bias lead 17 connects to a mid-point between the diodes 18, 19 on strip 10.

In fig.17, an equivalent circuit of the coupling has been shown. C_var1 and C_var2 represent the tuneable capacitances of varactors 18 and 19 as given by the DC bias voltage. r is the total resistance constituted by the strip resistance r_strip and the substrate resistance r_substrate to the longitudinal substrate currents. C_t is the total capacitance represented by the capacitance between the capacitive leads 23 and 24 and the strips 1, and the inherent shunt capacitance C_p between the strips and the lossy substrate layer 6 . R_shuntp is the parasitic shunt resistance of the lossy substrate. The total inductance is constituted by the inductance of the loops 13 and 14 and the parasitic inductance given by strips 8, 15, 16, 23, 24. It includes also the inductive response of the longitudinal substrate currents.

As will be understood the resonance frequency can be approximated by the expression

$$f = \frac{1}{\sqrt{L\_t \cdot (C\_t + C\_var)}}$$

By suitable dimensioning of for instance the distance h and tuning the varactor diodes applying an appropriate DC bias voltage, the desired resonance frequency can be accomplished.

Since the capacitor leads 23 and 24 are arranged below the strips 1 of the inductor, the electrical field lines are mainly extending in the low loss dielectric layers 4 and 5, leading to a reduction of losses. The low width W_2 of the strips 23 and 24 in relation to the width of the loop strip 1 W_1 leads furthermore to a reduction of current crowding in the strips 1 leading to a more homogenous current distribution in the strips 1 arranged over the capacitive leads 23 and 24, which then again leads to a lower strip resistance in the parts of the associated strips.

It is seen that the tank is symmetrical about a line, along the bias leads 16 and 17, extending between the input terminals 12, please also confer fig. 14 - 16.

The tank according to the invention renders it possible to accomplish very high Q values. Practical tests show that Q-values over 20 can be accomplished for 20 GHz. The tank also provides low noise because of the reduced losses.

The advantages of the tank according to the invention are fully utilised if the input 12 terminals are coupled differentially, i.e. the input terminals have equal and opposite potentials relative to ground.

The third substrate layer 6 of the substrate 3 may constitute a ground plane. Also, an additional backside metal layer (not shown) may serve as a ground plane.

In case of a differential use of the input terminals, a virtual ground appears at the plane of symmetry (shown in figs. 14-16) on which the DC bias terminals 25 and 26 and the bias leads 16 and 17 are arranged. Since the impedance seen at the bias terminals appear to be zero since the voltage potential is zero, no matching or decoupling networks, such as low pass filters, are required. Thereby, the microwave high frequency and high Q performance is unaffected by the bias circuit.

In fig. 18, a second embodiment of a tank 28 according to the invention has been shown. The tank 28 is similar to the tank 20 explained in the foregoing except that varactors have not been provided. For applications where a tuneable tank is not necessary and the capacitance value can be accomplished with a desirable degree of precision, this embodiment can be used. In practice, it is often difficult to estimate the shunt capacitance, but for certain applications the above design may be suitable.

In fig. 19, a third embodiment 29 of the tank according to the invention has been shown which is also similar to the tank 20, but according to this embodiment no capacitor leads are provided. For applications where a sufficient capacitance value can be accomplished by the varactor diodes this embodiment may be appropriate.

In fig. 20, a fourth embodiment has been shown providing still higher capacitance values, by providing capacitor leads 23 and 24 which extends along a larger portion of the first and second loops 13 and 14 of the tank. According to this design, the capacitor leads extends from the first bias lead 16 near the first DC terminal 25.

In fig. 21 a fifth embodiment of the tank according to the invention has been shown, which comprises both varactor diodes 18 and 19 and capacitor leads 23 and 24, but where only a single loop has been provided.

It should be noted that the invention is not restricted to the substrate / strip configuration defined above. The invention would also be applicable to a substrate having several epitaxial layers. In addition, dielectric films could be provided to the extent that substrate currents would occur in a lossy part of the substrate. As long as currents can potentially be induced in a lossy substrate, the balancing of currents in the lossy part of the substrate can be effected according to the principles described above.

The tank structures according to the invention may therefore readily be applied in a wide range of MMIC applications such as balanced amplifiers, mixers, and voltage controlled oscillators and hence redefine the performance of such applications.

List of reference signs

1	strip
2	blocking structure
3	substrate
4	first layer
5	second layer
6	third layer
7	fourth layer
8	via
9	ground plane
10	second strip layer
11	third strip layer
12	input terminal
13	first loop
14	second loop
15	bridge portion
16	first bias lead
17	second bias lead
18	first diode
19	second diode
20	tank
21	third loop
22	fourth loop
23	first capacitor lead
24	second capacitor lead
25	first bias terminal
26	second bias terminal
27	via
28	second tank
29	third tank
30	fourth tank
31	fifth tank

Patent claims

1. Tank, comprising conductive strips (1) formed on a lossy dielectric or semiconductor substrate (3) having a resistivity of less than 10 Ω·m, the inductor having at least two input terminals (12) connected to the strips and being arranged close together in relation to the wavelength intended for the inductor,

   the strips (1) forming at least one loop (13, 14), having one or more segments of pair-wise disposed adjacent parallel legs of substantially the same length being substantially aligned with one another and being arranged for carrying currents in opposite directions, such that currents induced in the lossy substrate (3) from each respective leg in the segment balance each other, the loops accounting for an inductive value,

   the strips (1) of the at least one loop furthermore being arranged such that no two adjacent strips of the loop or loops are carrying current in the same direction,

   whereby the at least one loop is coupled in parallel with at least one capacitor (23, 24, 18, 19) formed in or on the substrate.

2. Tank according to claim 1, comprising a bridge portion (15), the loop (13, 14) and the bridge portion (15) defining a confined area as seen from above.

3. Tank according to claim 2, wherein the loop has an elongate substantially rectangular shape and wherein the aspect ratio of the loop, defined as the length (d), to the width (a, b, c) of the area formed by the loop (13, 14), is more than 2 to 1 or less than 1 to 2.

4. Tank according to claim 3, wherein the aspect ratio is more than 3 to 1 or less than 1 to 3.

5. Tank according to claims 2 - 4, comprising at least an additional second loop (13, 14) being substantially symmetrical to the first loop (13, 14) about an axis crossing the bridge portion (15).

6. Tank according to claims 2 - 5, wherein the tank is symmetrical about a line extending parallel with and between the input terminals (12) and parallel with the loop or loops (13, 14) formed by the strips (1).

7. Tank according to any of the claims 2 to 6, wherein the input terminals (12) connected to the strips (1) are being provided near the bridge portion (15).

8. Tank according to any preceding claim wherein the at least one capacitor is formed by a pair of back to back coupled varactor diodes (19, 20) arranged between the input terminals (12),

whereby the tuneable tank is being adapted to receive a DC bias voltage between a mid-point arranged between the diodes (18, 19) over a first bias lead (16) and a second bias lead (17) arranged on an opposing midpoint (V_bias+) on the tank.

9. Tank according to any preceding claim, wherein the capacitor is formed by a pair of capacitor leads (23, 24) arranged under the strips (1) forming the at least one inductive loop, the capacitor leads being arranged symmetrically to the strips (1) of the at least one loop.

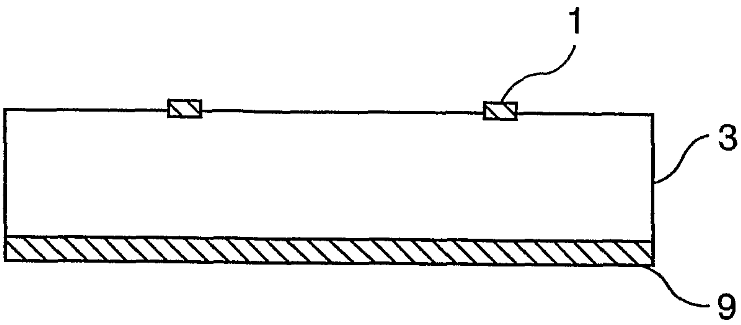

Fig. 1

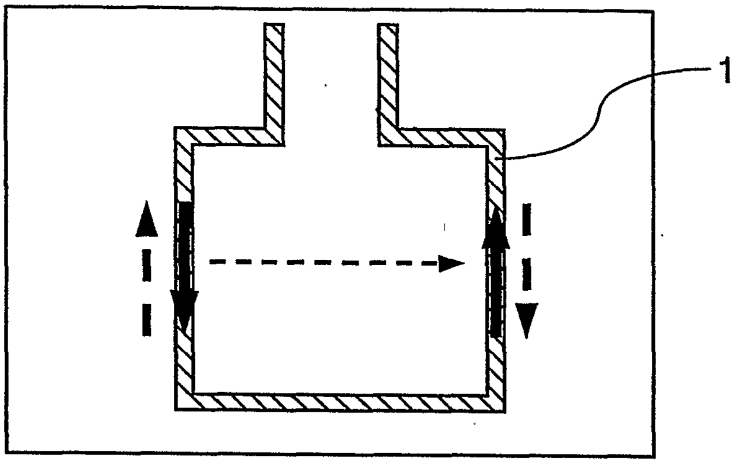

Fig. 2

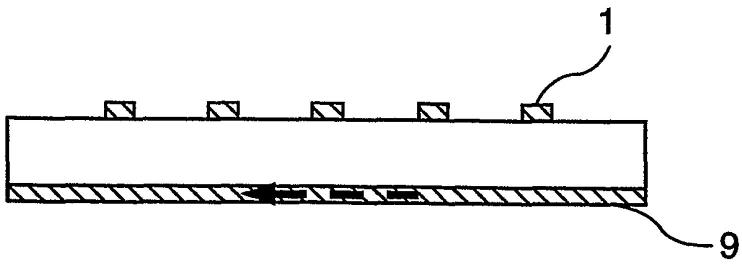

Fig. 3

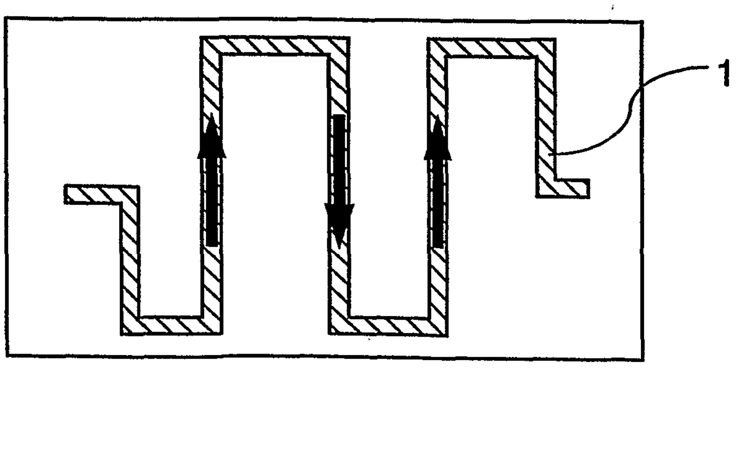

Fig. 4

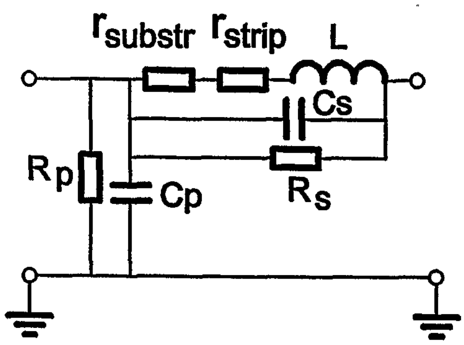

Fig. 5

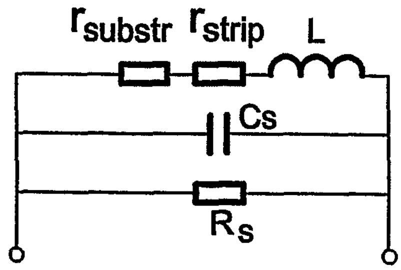

Fig. 7

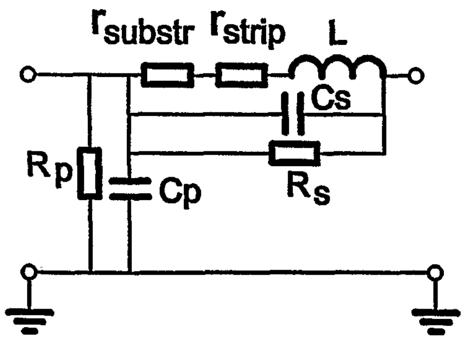

Fig. 6

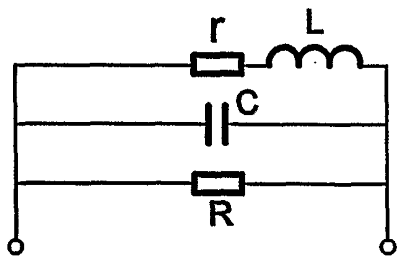

Fig. 8

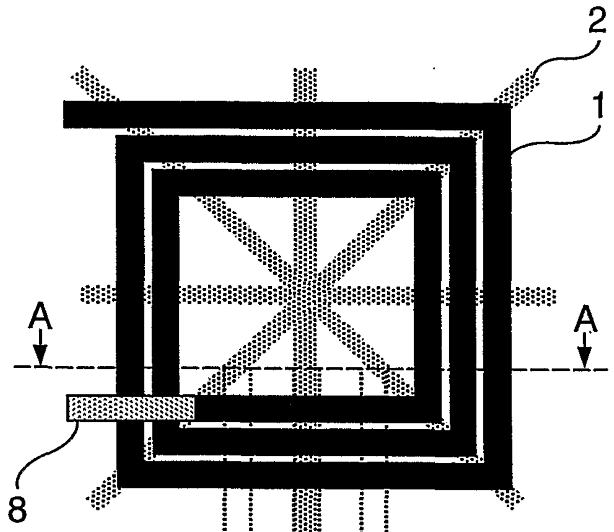

Fig. 9

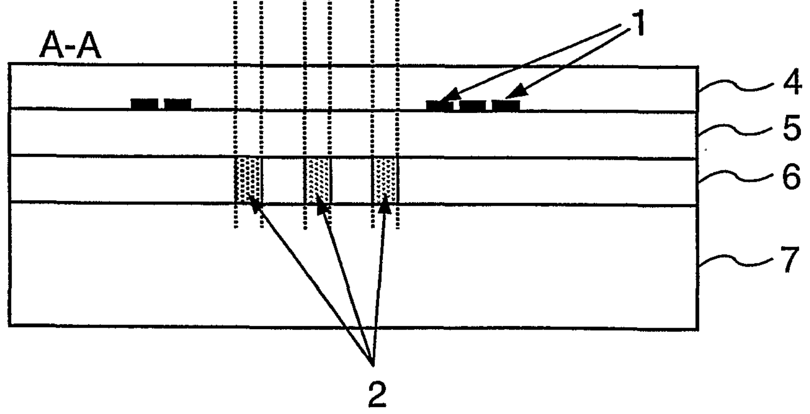

Fig. 10

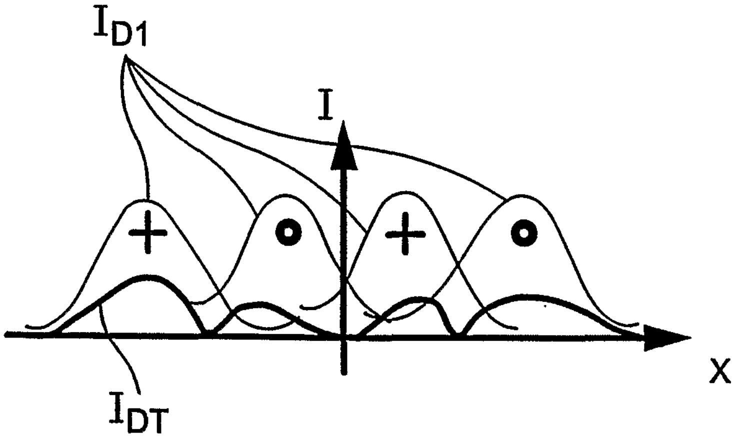

Fig. 11

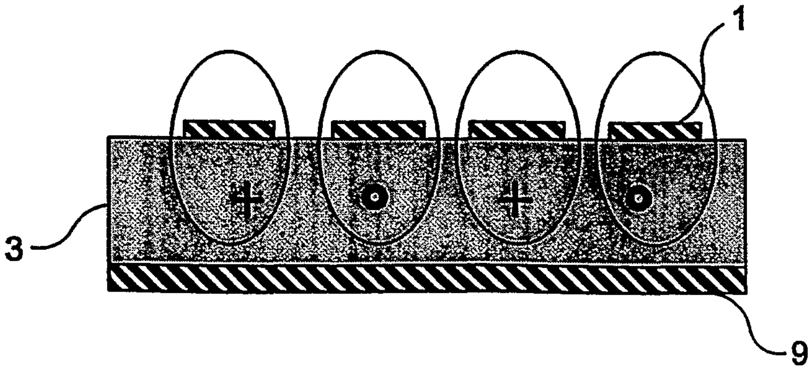

Fig. 12

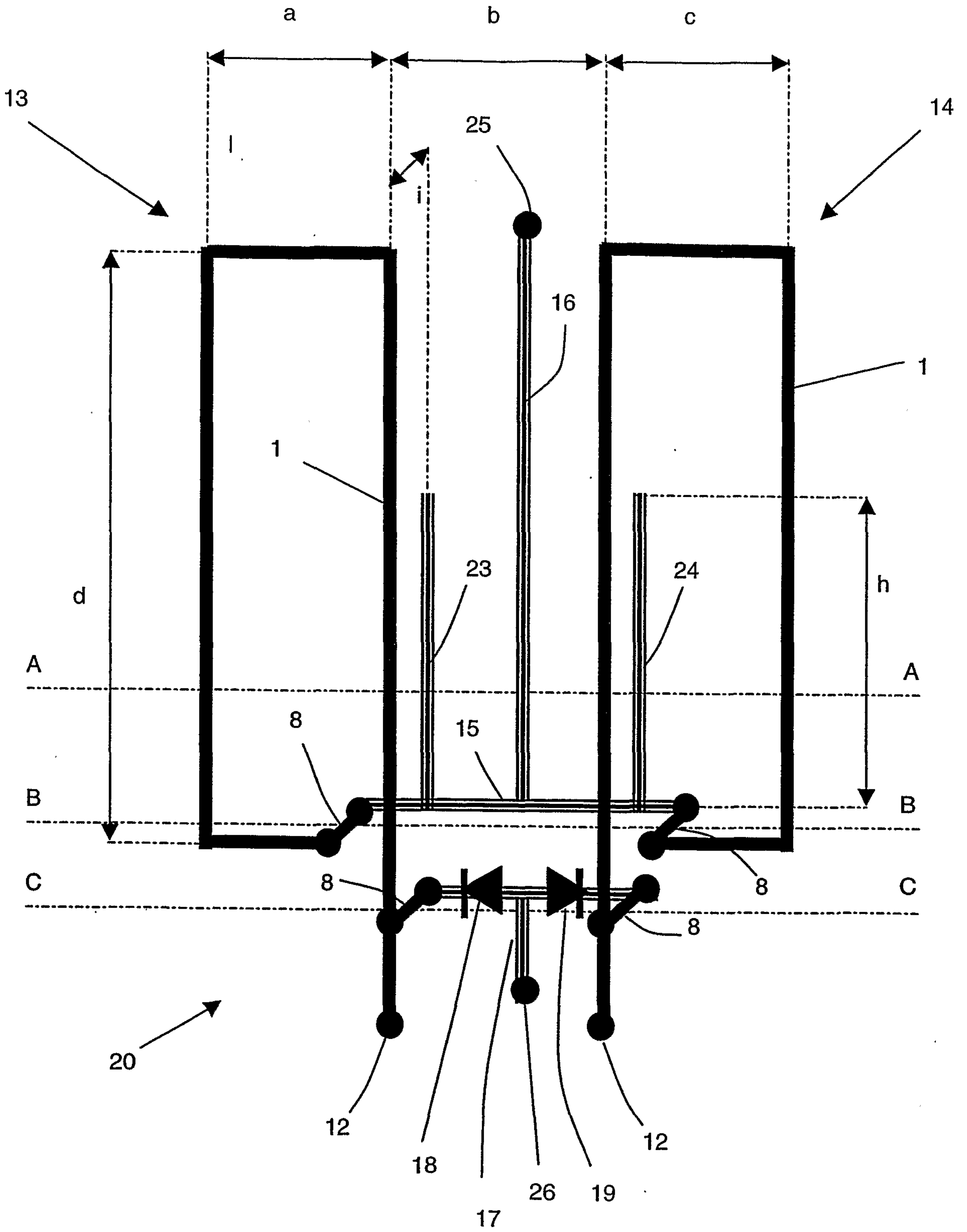

Fig. 13

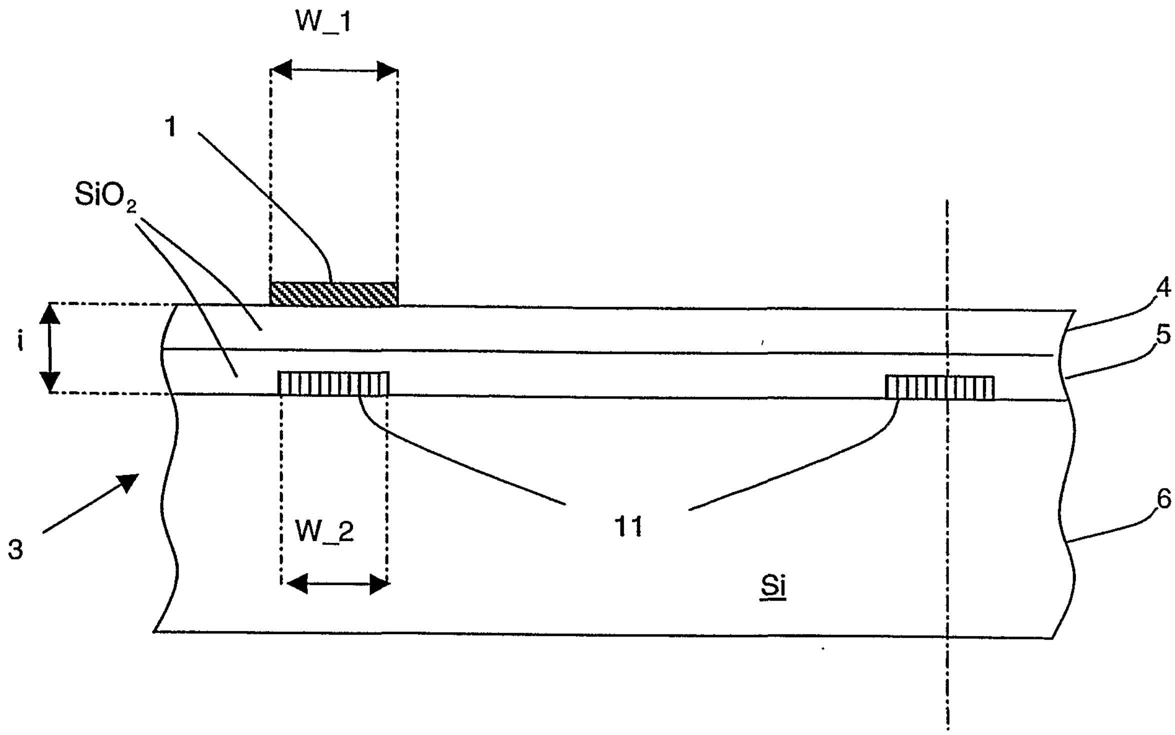

Fig. 14

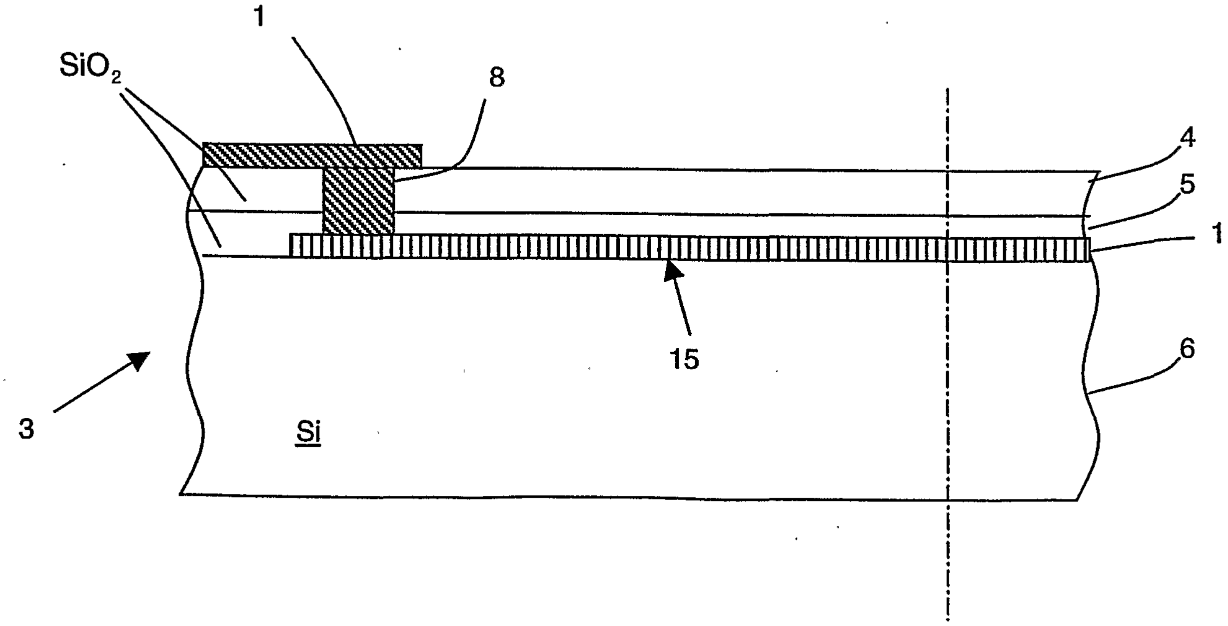

Fig. 15

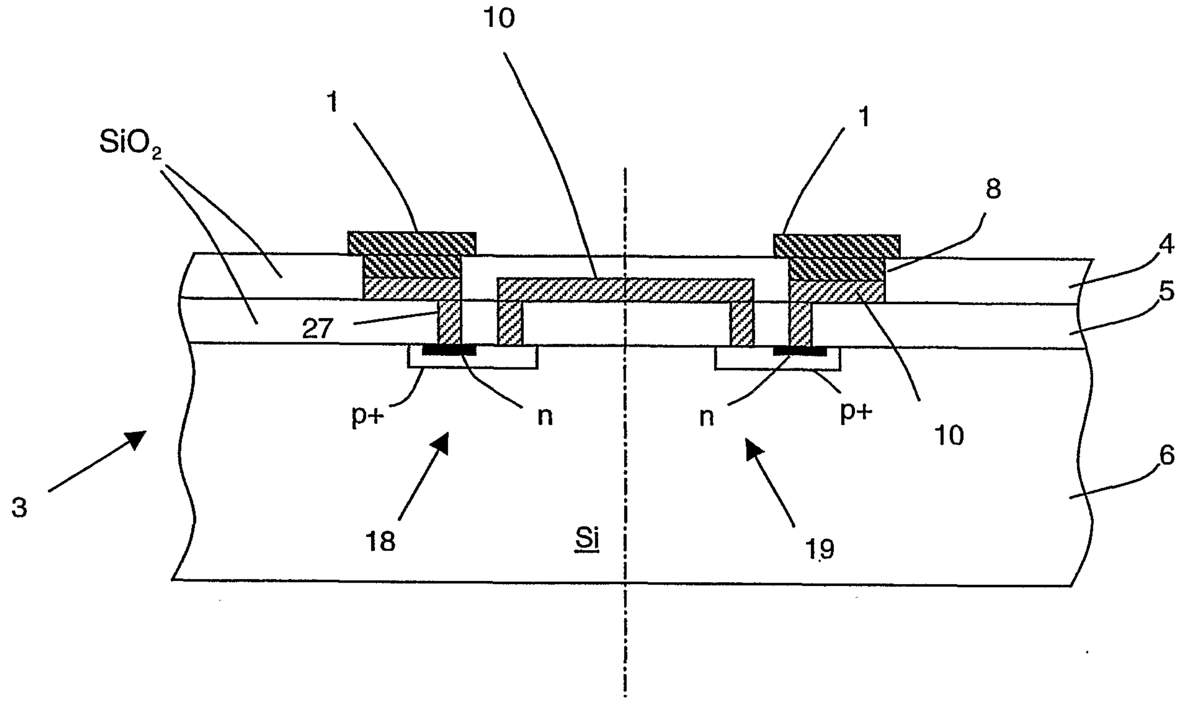
10
1
1
SiO_2
8
4
5
27
p+
n
n
p+
10
6
3
18
Si
19

Fig. 16

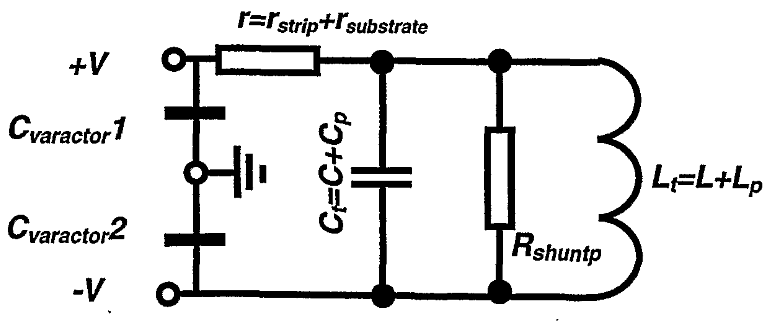
$r=r_{strip}+r_{substrate}$
+V
$C_{varactor}1$
$C_t=C+C_p$
$L_t=L+L_p$
$C_{varactor}2$
R_{shuntp}
-V

Fig. 17

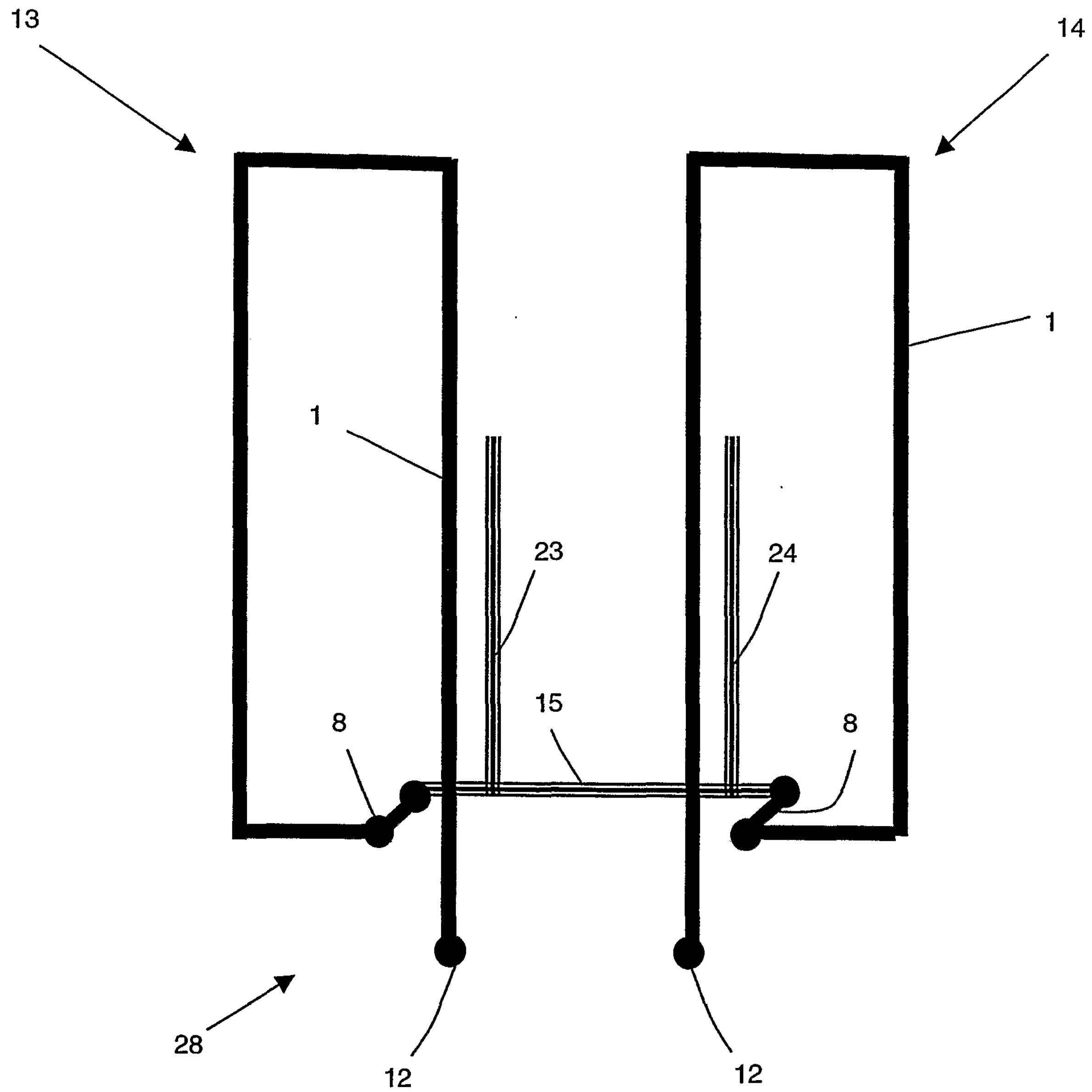

Fig. 18

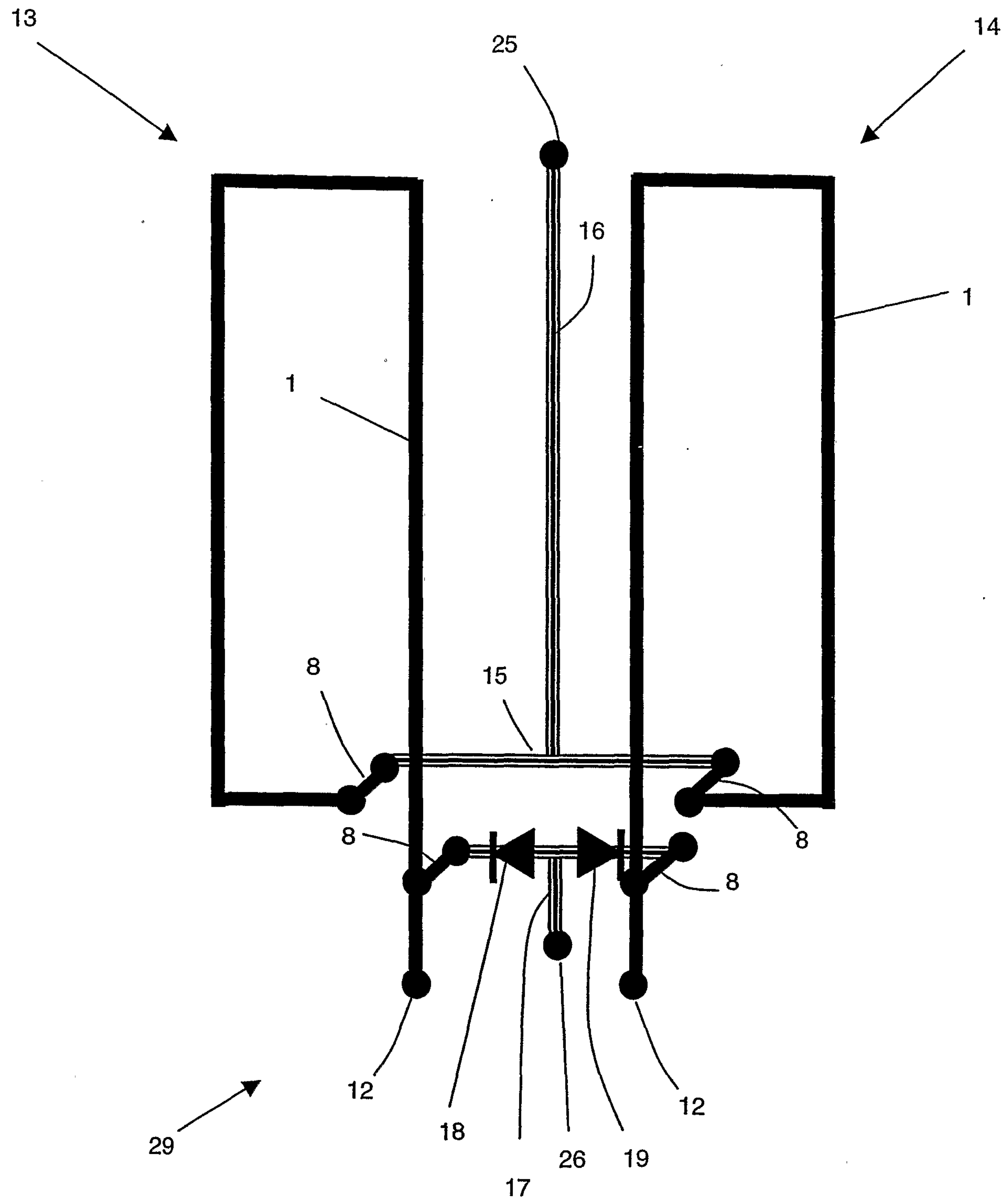

Fig. 19

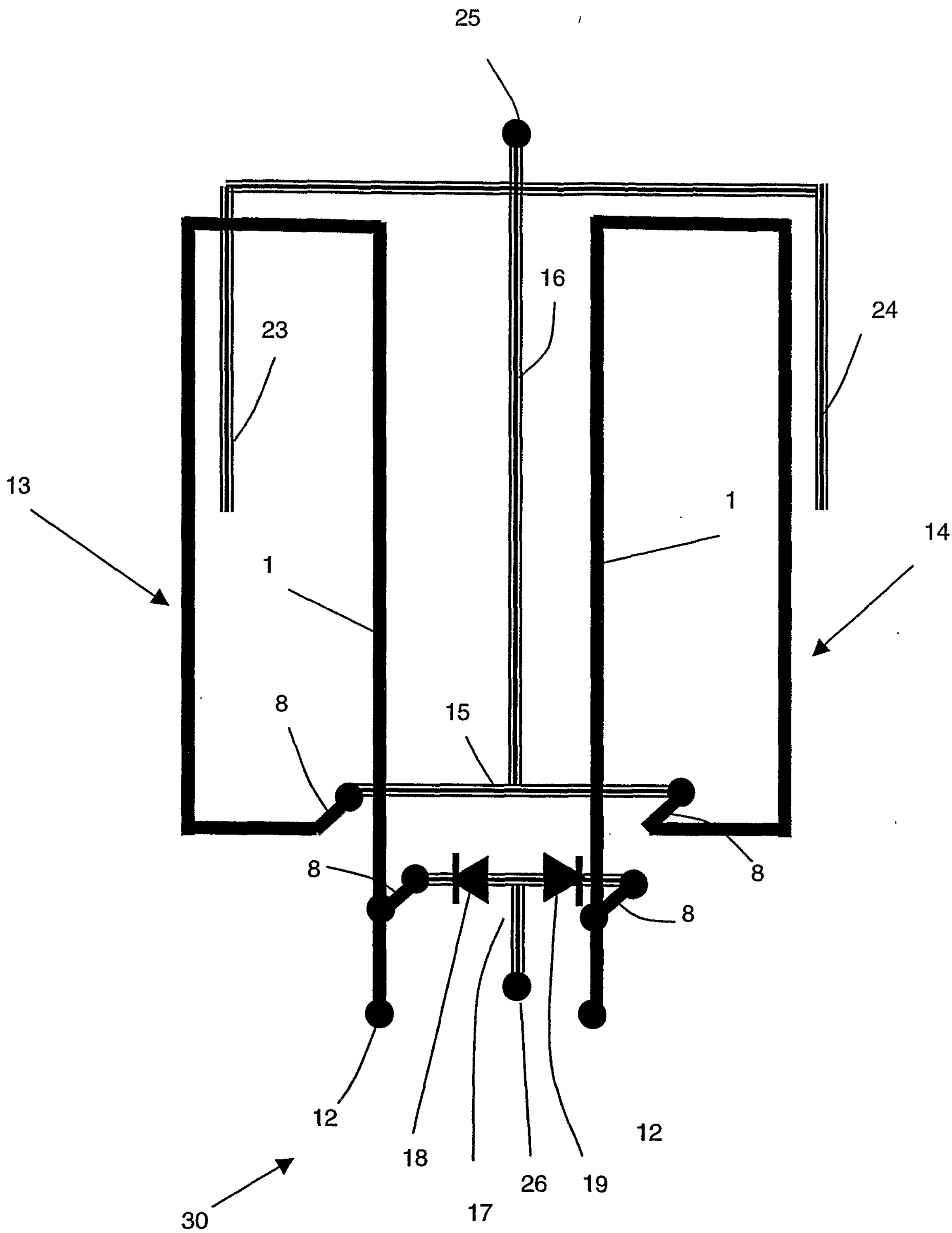

Fig. 20

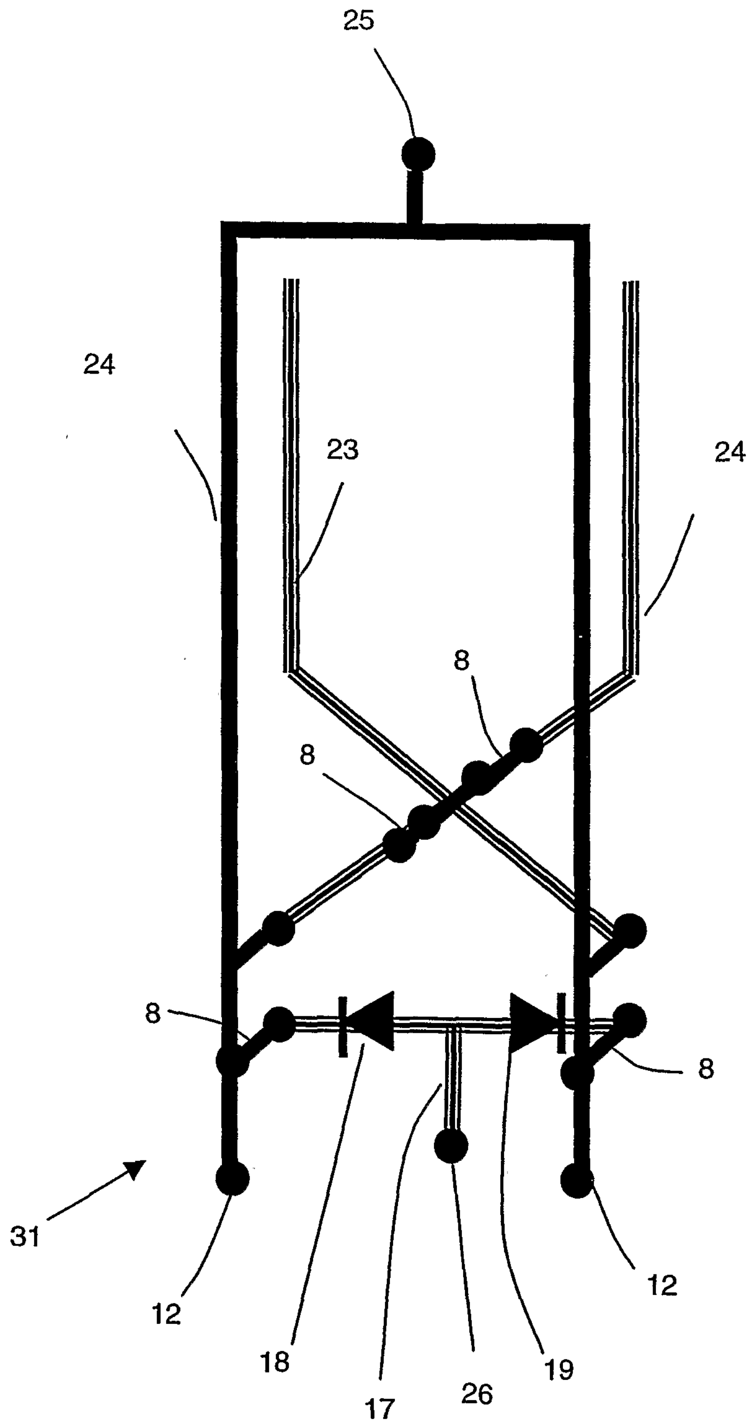

Fig. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/01045

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H01L 21/02, H03J 3/20
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03B, H01L, H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5959515 A (CORNETT ET AL), 28 Sept 1999 (28.09.99) --	1-9
A	US 5173835 A (CORNETT ET AL), 22 December 1992 (22.12.92) --	1-9
A	US 5844451 A (MURPHY), 1 December 1998 (01.12.98) --	1-9
A	US 5430895 A (HUUSKO), 4 July 1995 (04.07.95) -- --------	1-9

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2001	24 -08- 2001
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Per-Olof Warnbo/MN Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT
Information on patent family members

02/08/01

International application No.
PCT/SE 01/01045

Patent document cited in search report			Publication date	Patent family member(s)			Publication date
US	5959515	A	28/09/99	NONE			
US	5173835	A	22/12/92	EP	0608376	A	03/08/94
				JP	2853332	B	03/02/99
				JP	7500457	T	12/01/95
				KR	134980	B	15/05/98
				WO	9308578	A	29/04/93
US	5844451	A	01/12/98	NONE			
US	5430895	A	04/07/95	DE	69218104	D,T	11/09/97
				EP	0539133	A,B	28/04/93
				SE	0539133	T3	
				FI	93679	B,C	31/01/95
				FI	915006	A	24/04/93
				JP	5304028	A	16/11/93