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(54) **METHOD FOR FABRICATION OF
SEMICONDUCTOR DEVICE**

Publication Classification

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ABSTRACT

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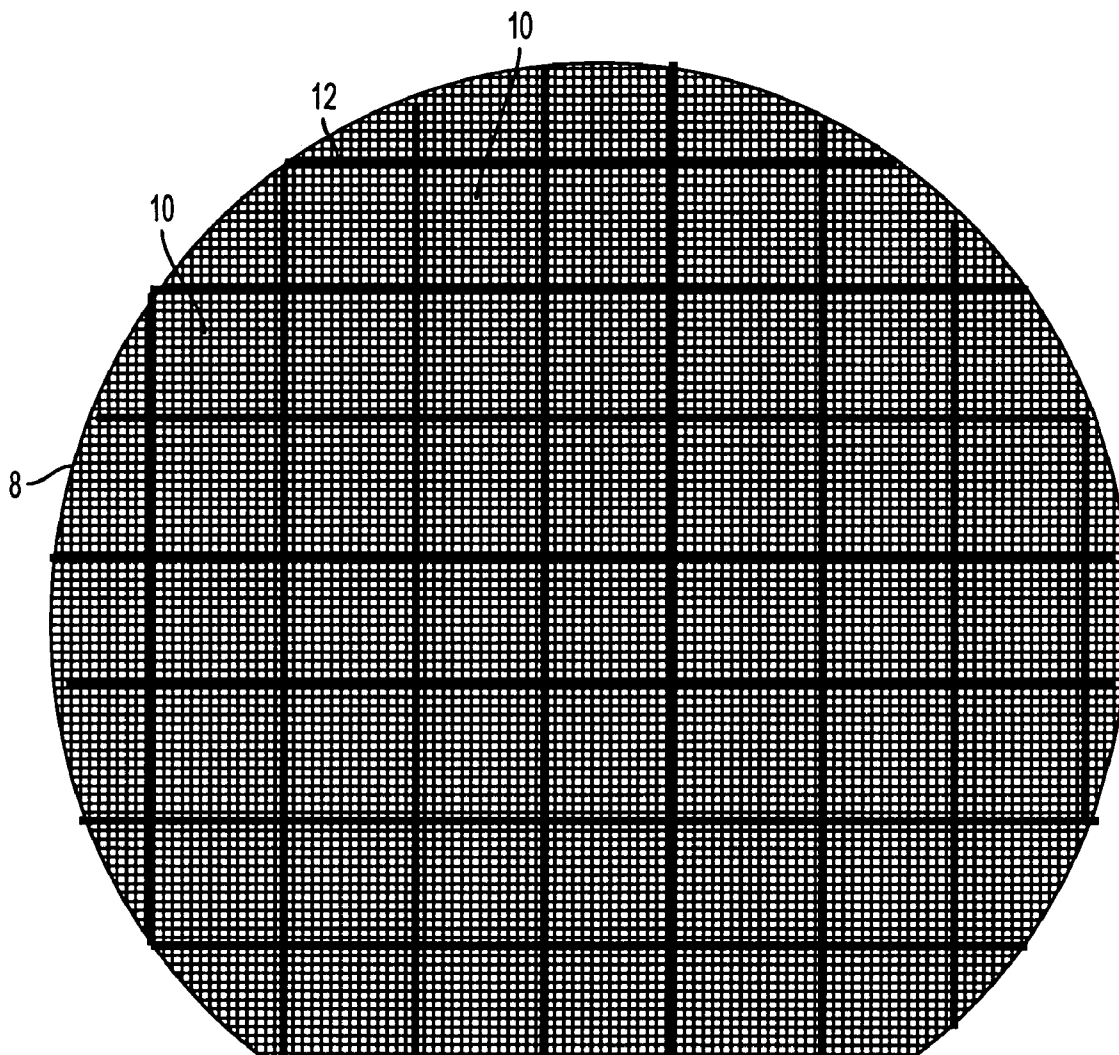
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(22) Filed: **Apr. 4, 2005**

Related U.S. Application Data

(62) Division of application No. 10/321,669, filed on Dec.
18, 2002.

A novel method is presented to provide ASICs with drastically reduced NRE and with volume flexibility. The invention includes a method of fabricating an integrated circuit, including the steps of: providing a semiconductor substrate, forming a borderless logic array including a plurality of Area I/Os and also including the step of forming redistribution layer for redistribution at least some of the Area I/Os for the purpose of the device packaging. The fabrication may utilize Direct Write e-Beam for customization. The customization step may include fabricating various types of devices at different volume from the same wafer.



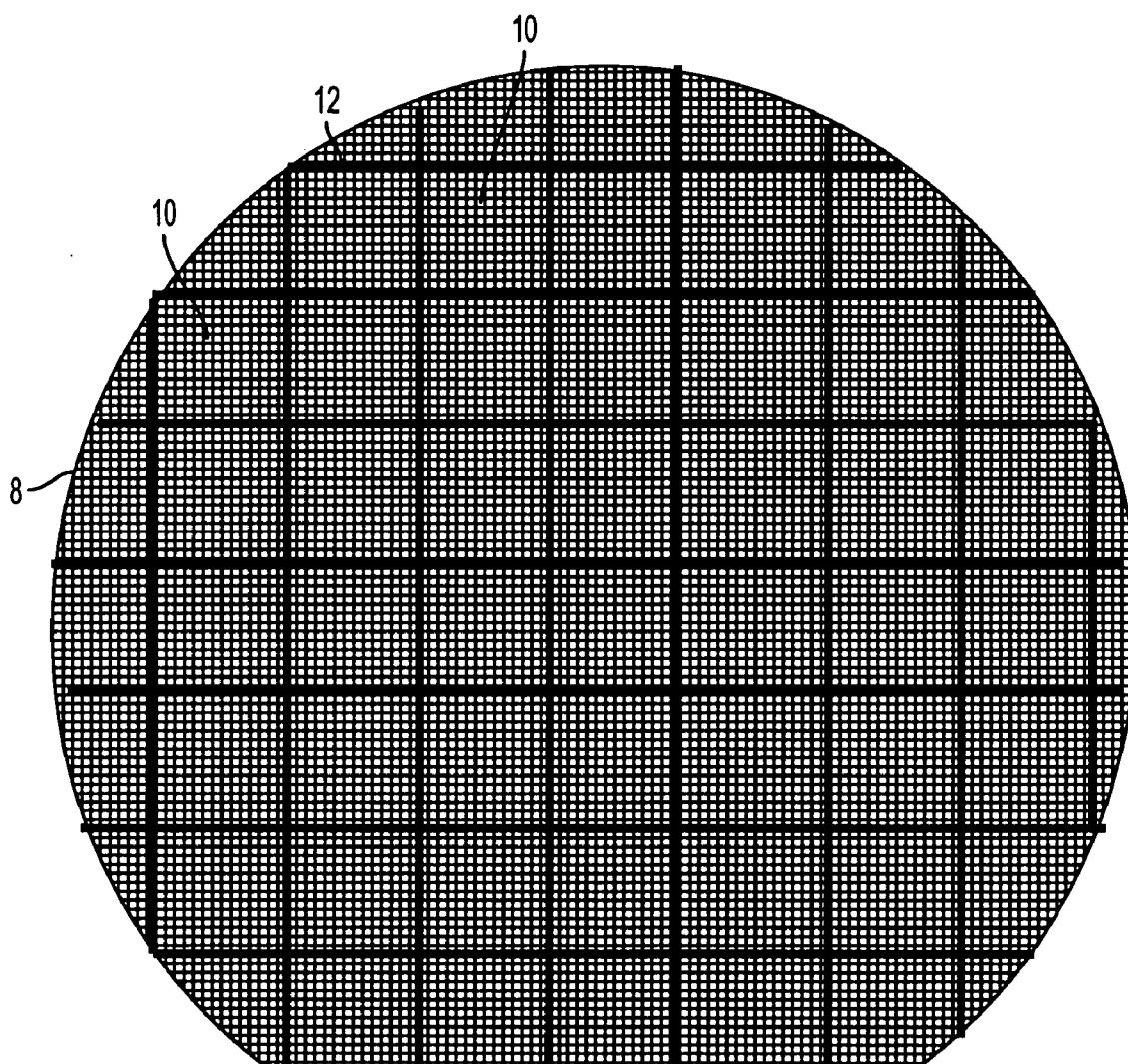
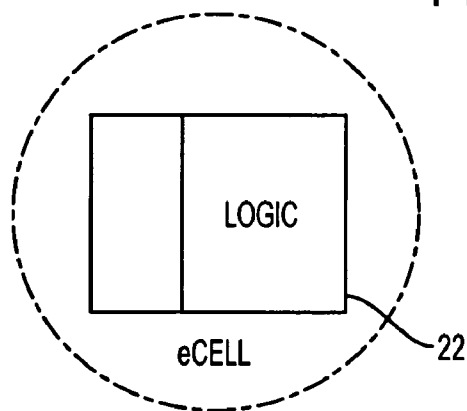
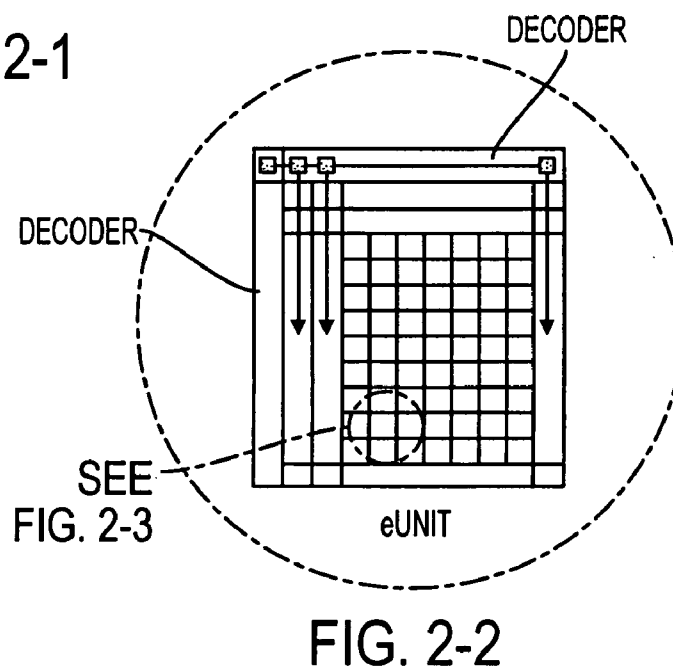
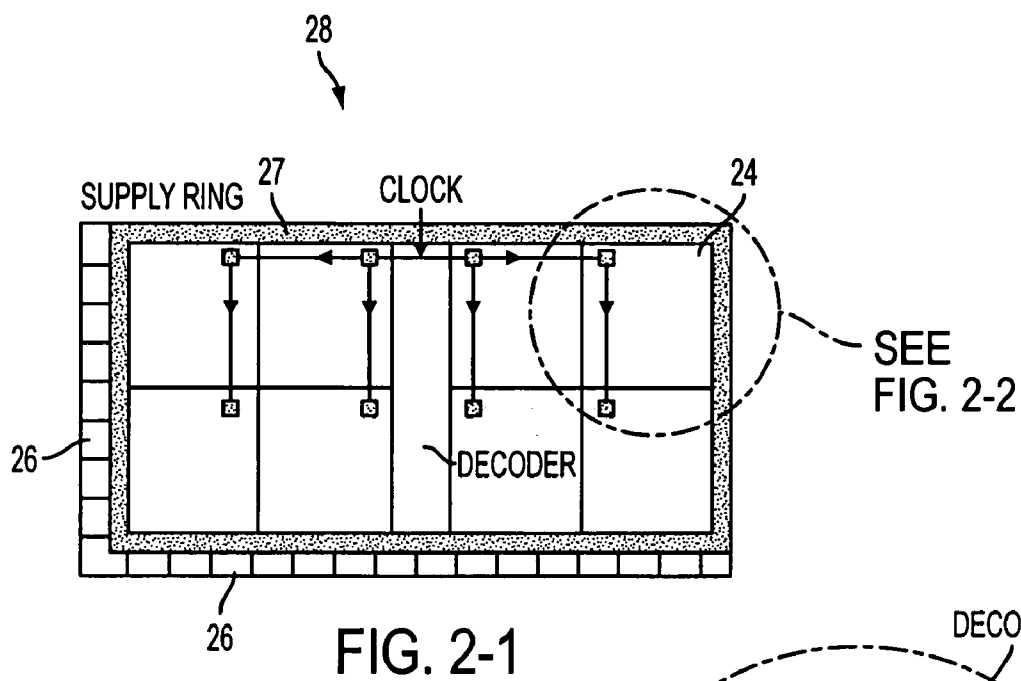


FIG. 1



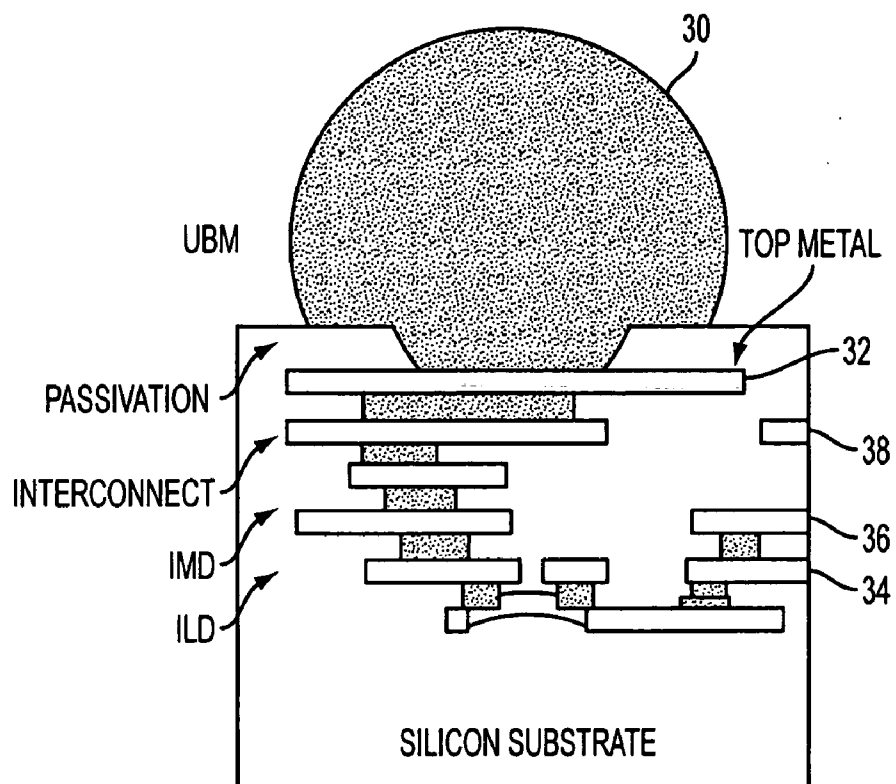


FIG. 3A

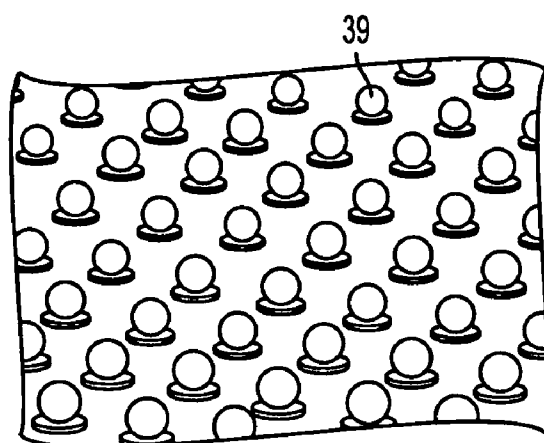


FIG. 3B

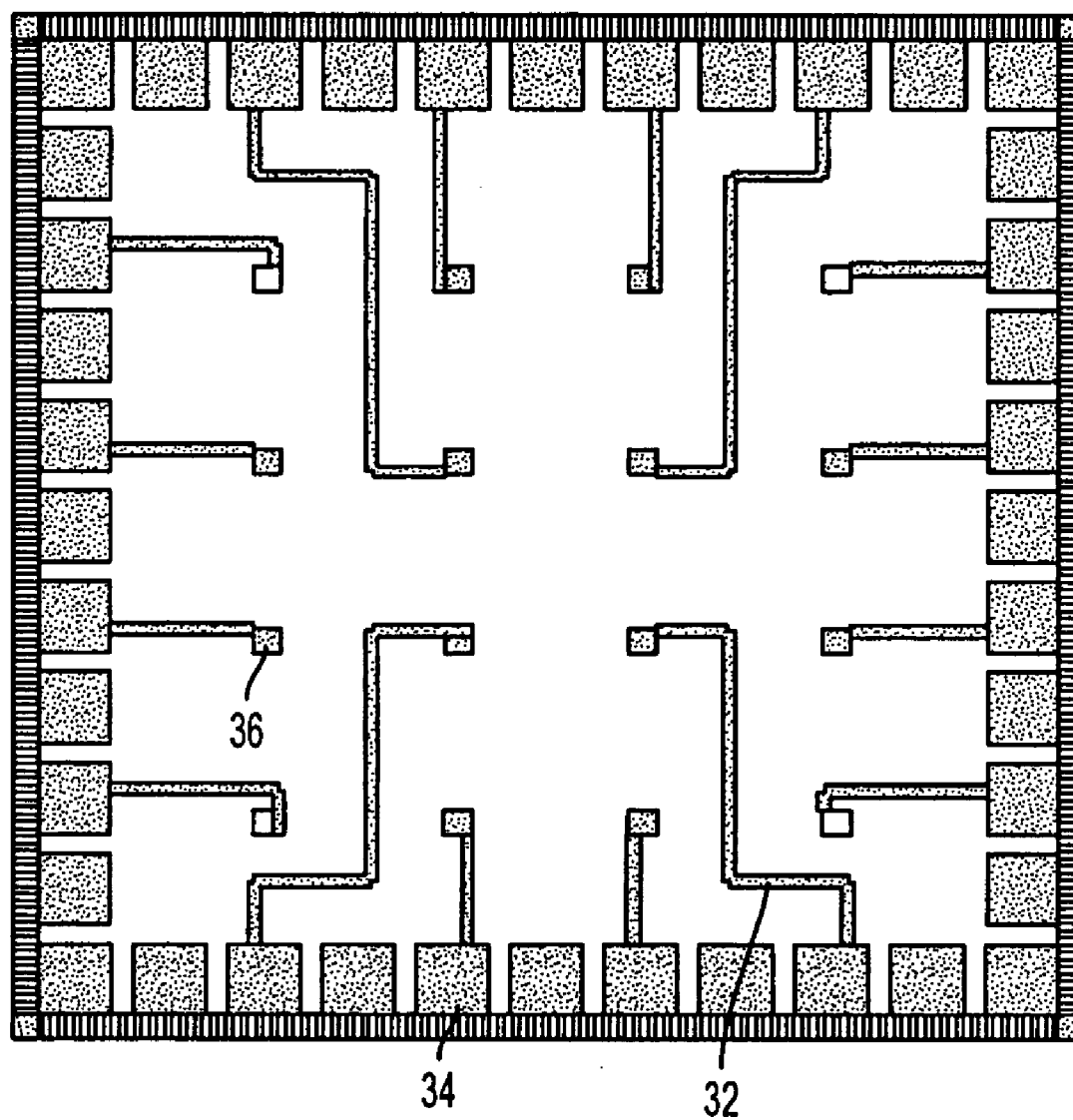


FIG. 3C

44

B	BUMP DIAMETER	150μm ± 10μm (IN WAFER)	70μm ± 10μm (IN WAFER)
C	Cu BUMP HEIGHT	20μm ± 3μm (IN WAFER)	10μm ± 3μm (IN WAFER)
D	BUMP ROOT DIAMETER	90μm	60μm
E	PASSIVATION HOLE SIZE	70μm	40μm
F	BUMP PITCH	200μm	120μm

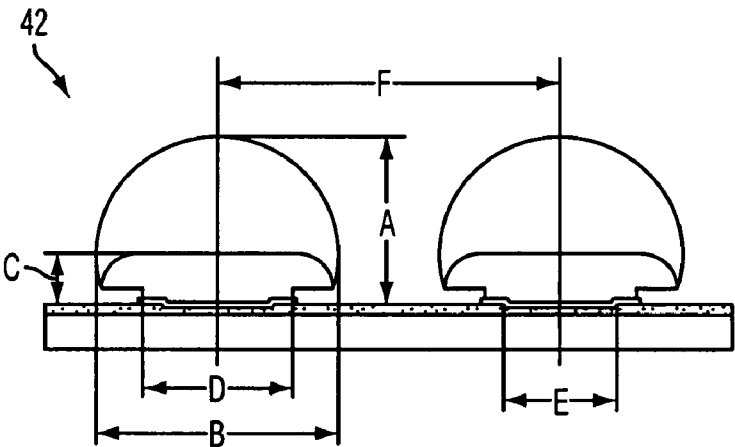


FIG. 4

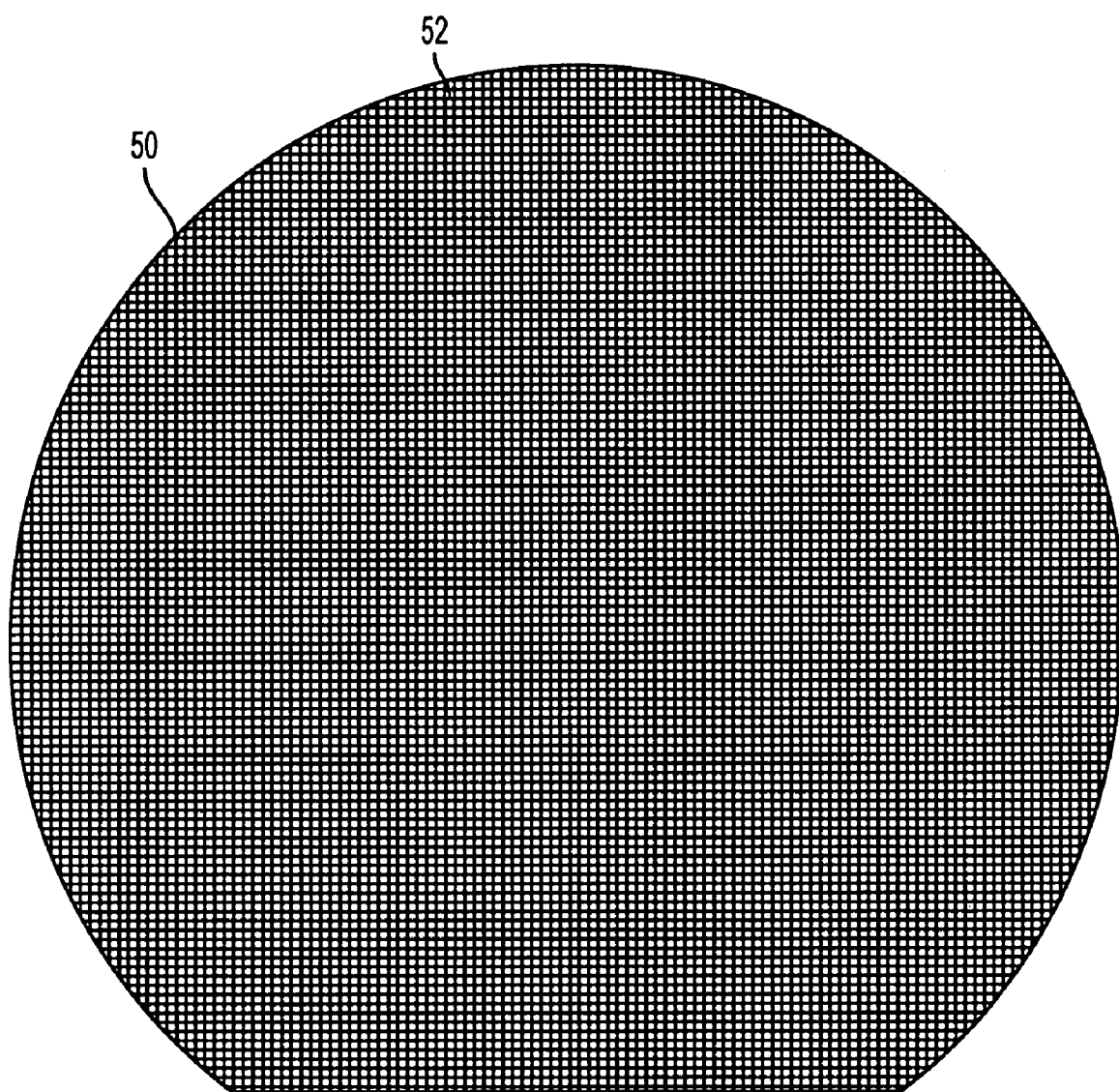


FIG. 5

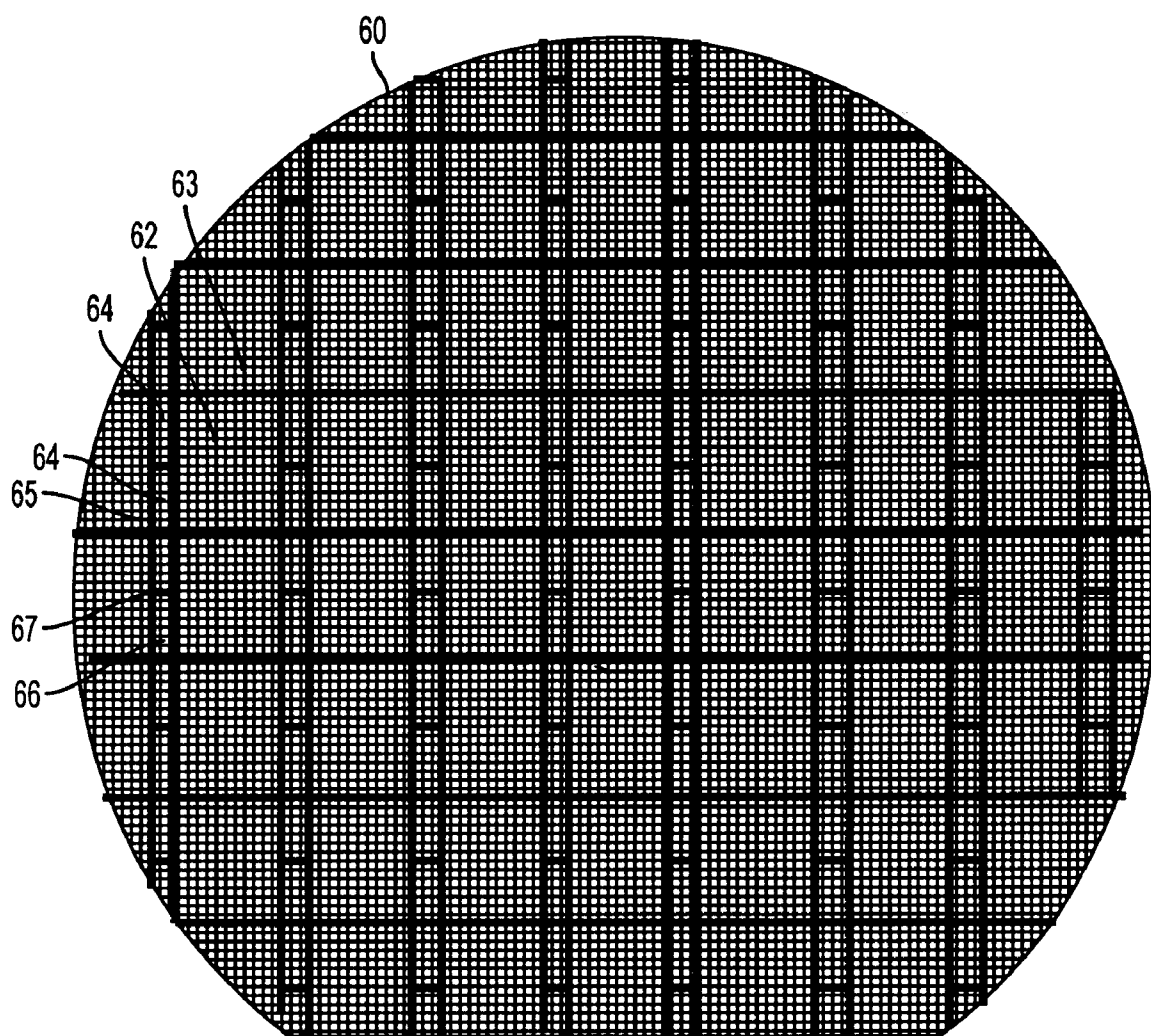


FIG. 6

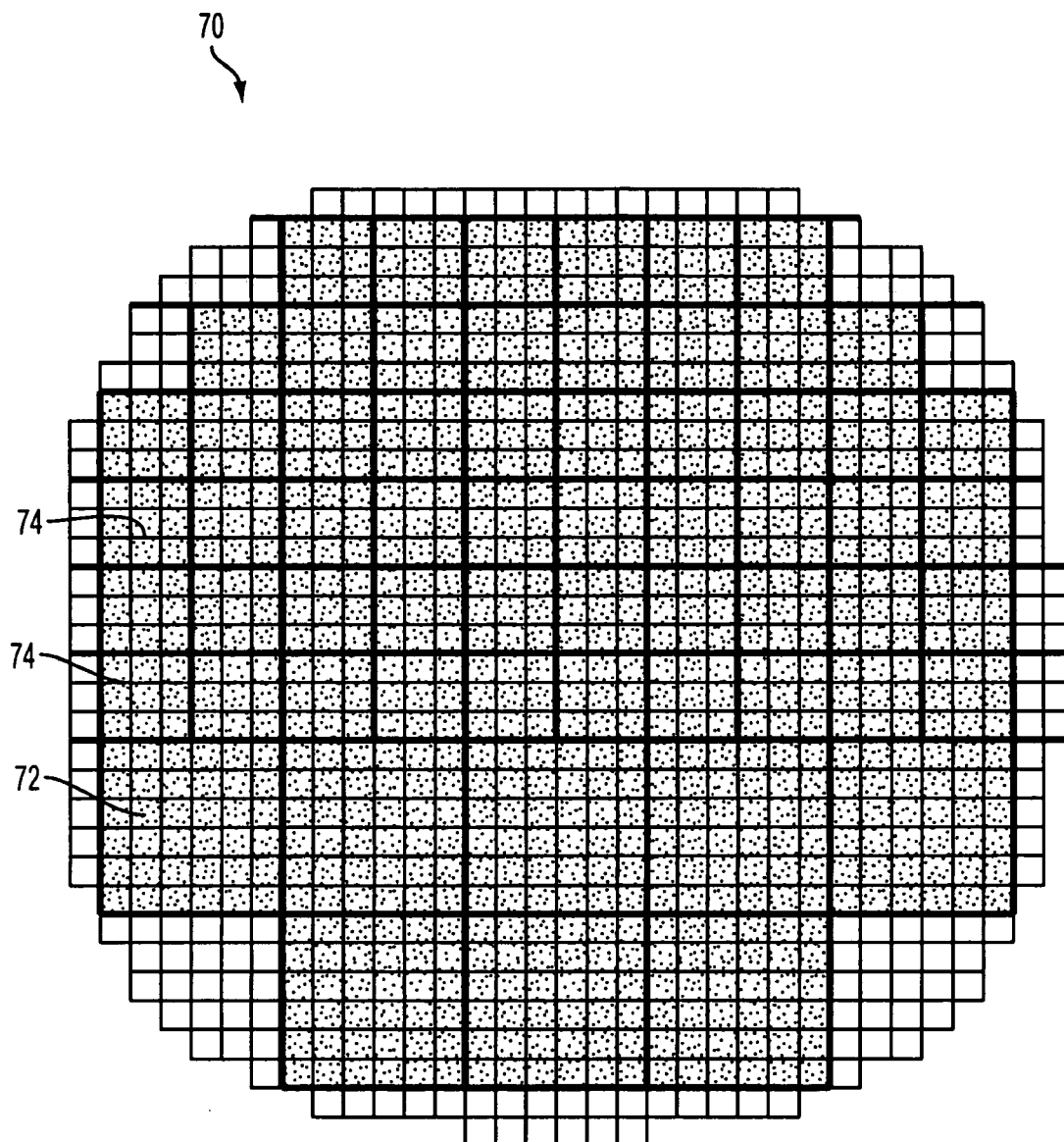


FIG. 7

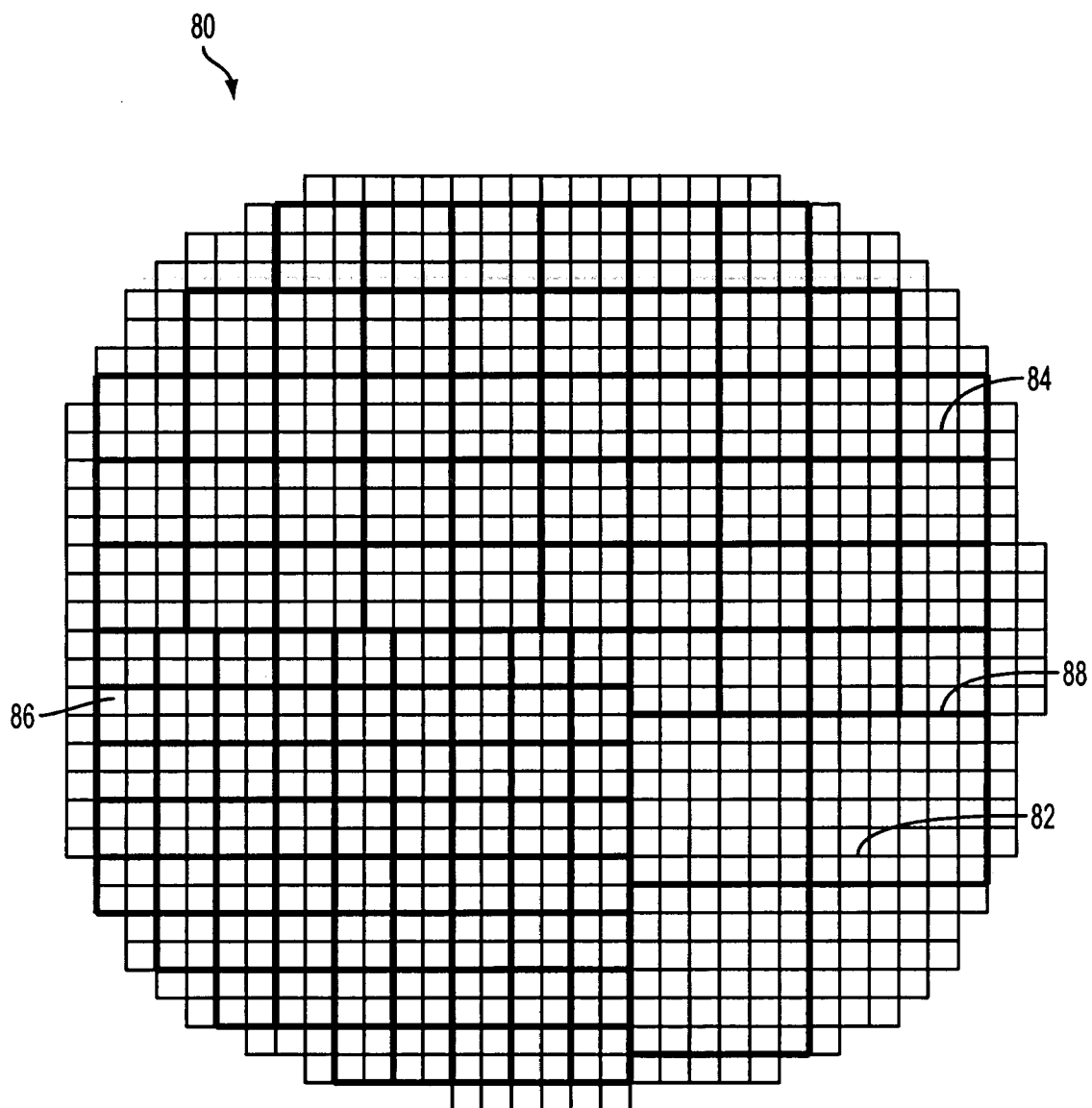


FIG. 8

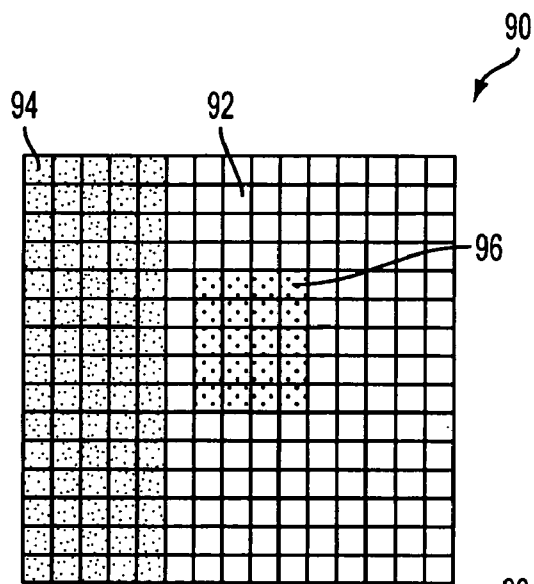


FIG. 9A

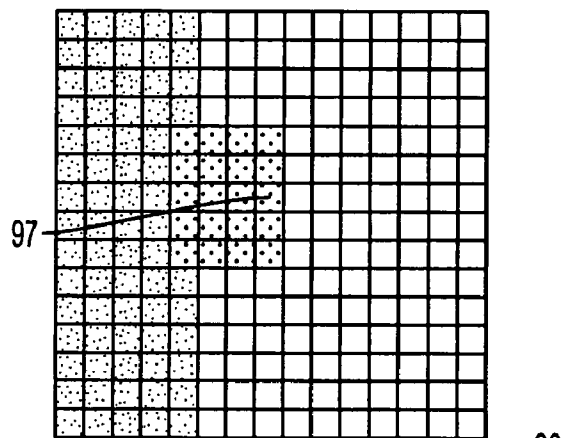


FIG. 9B

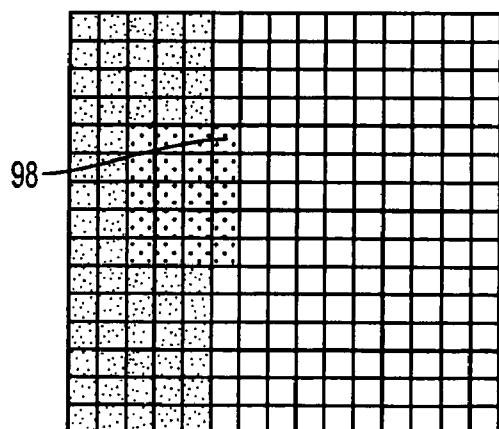


FIG. 9C

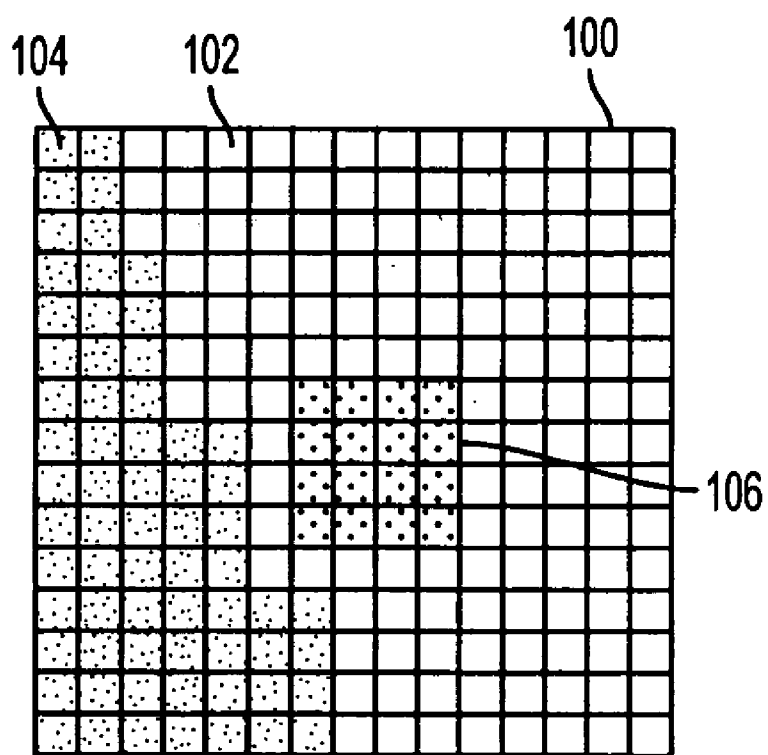


FIG. 10A

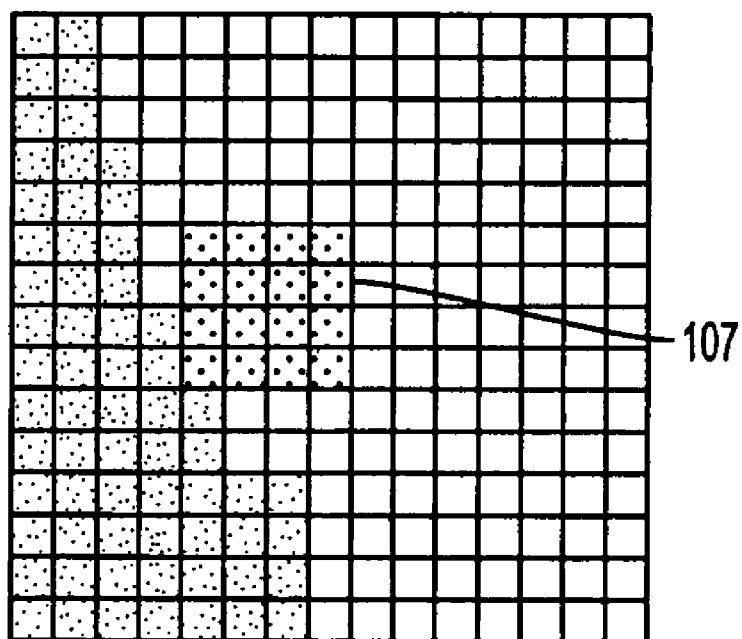


FIG. 10B

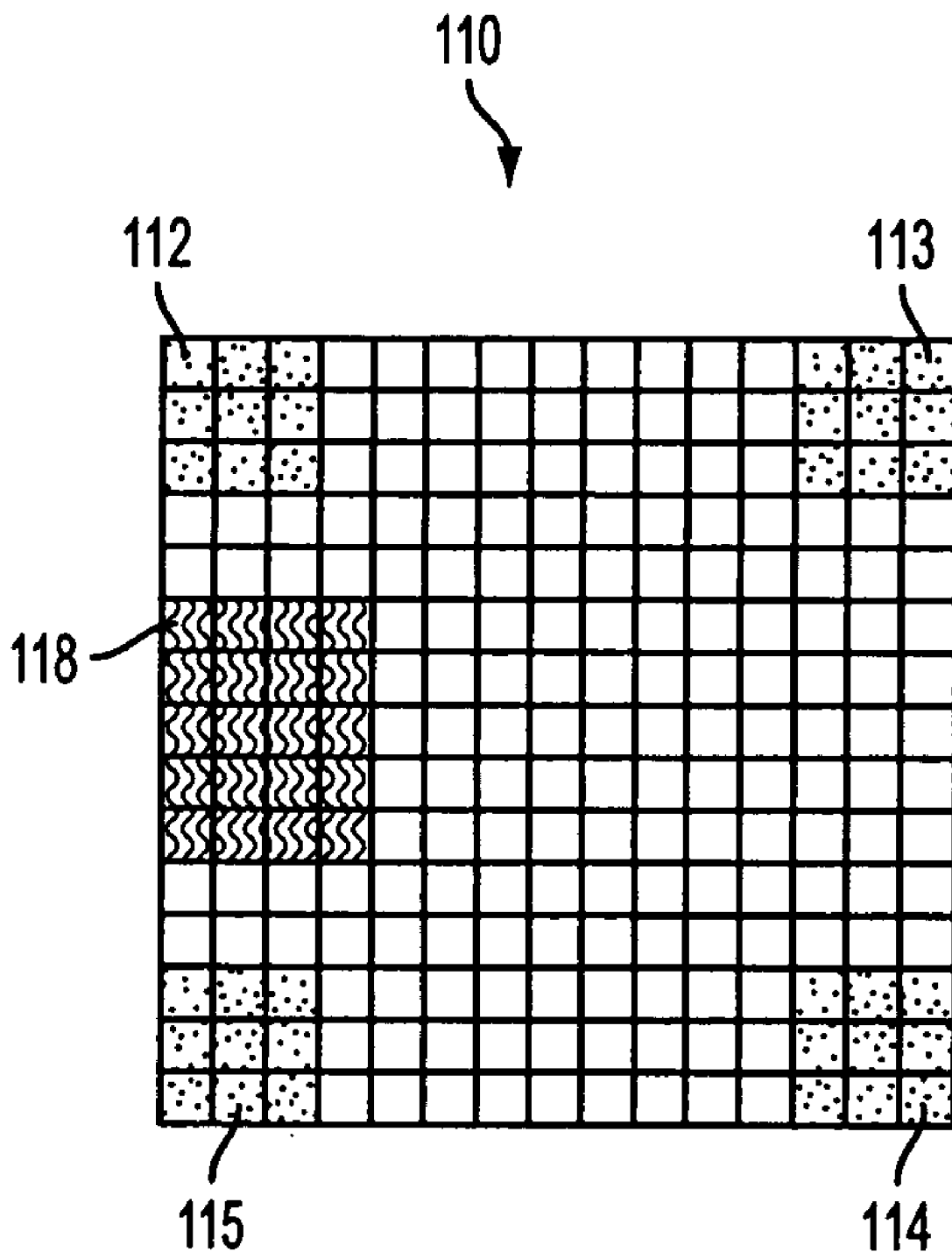


FIG. 11

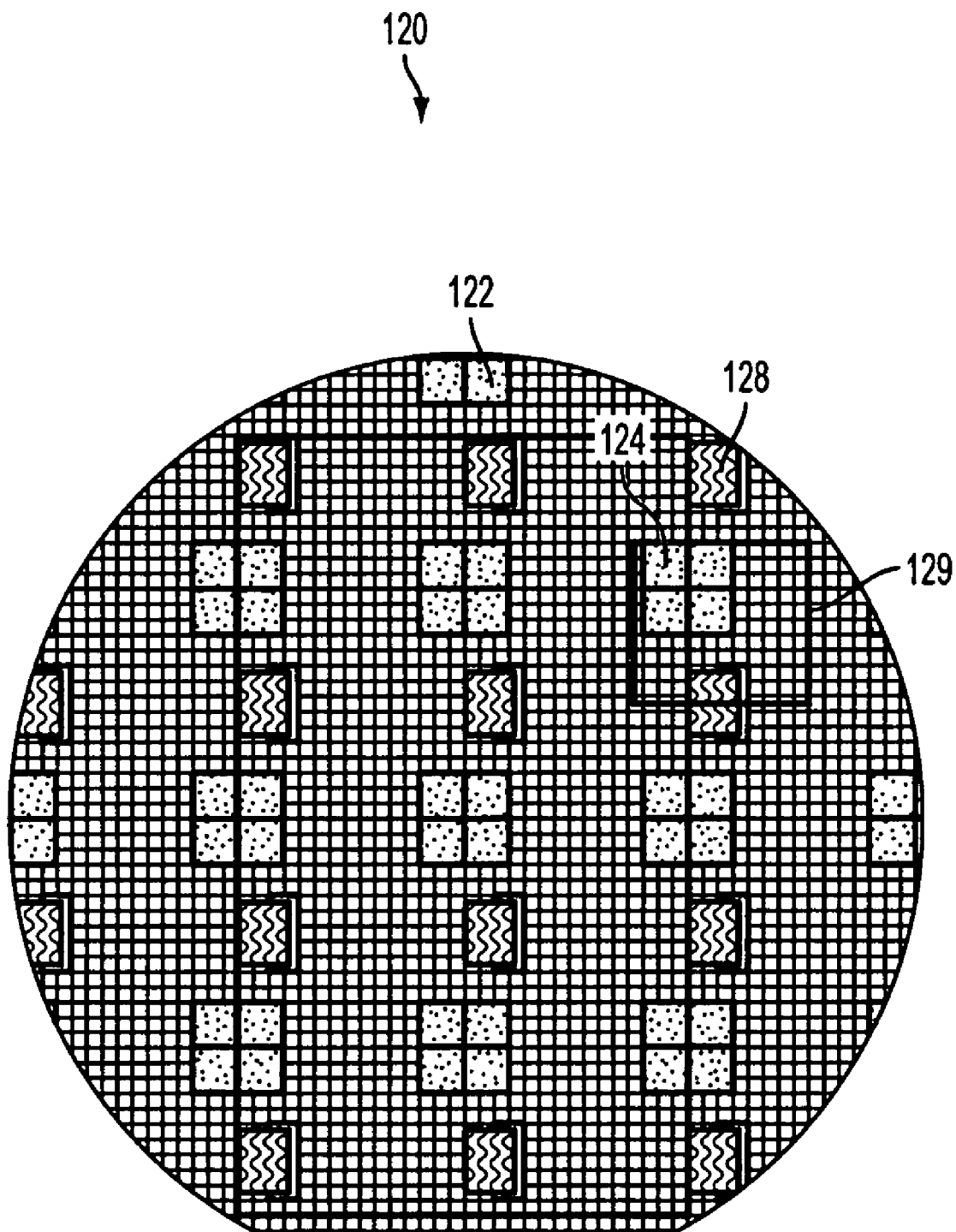


FIG. 12

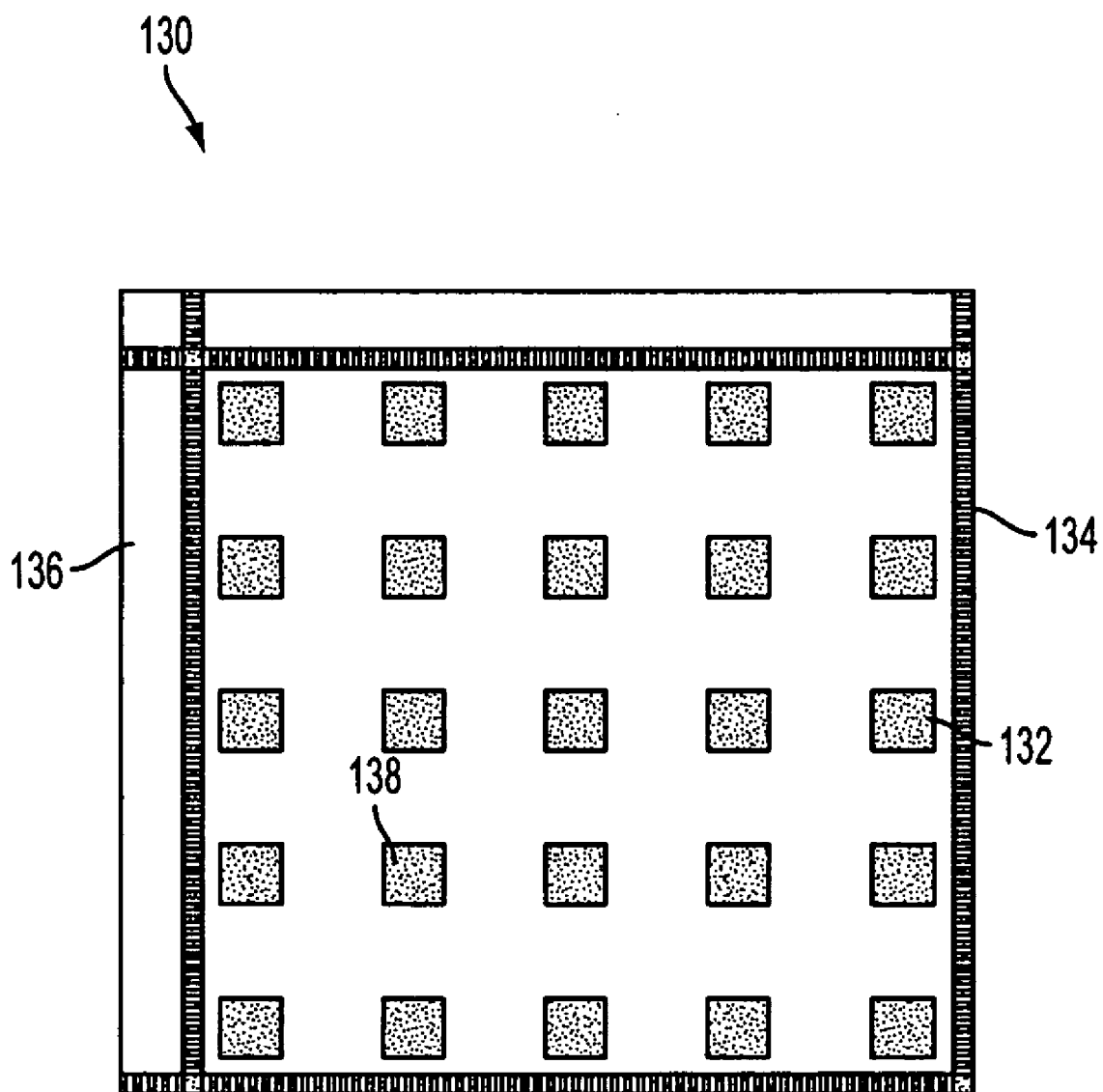


FIG. 13

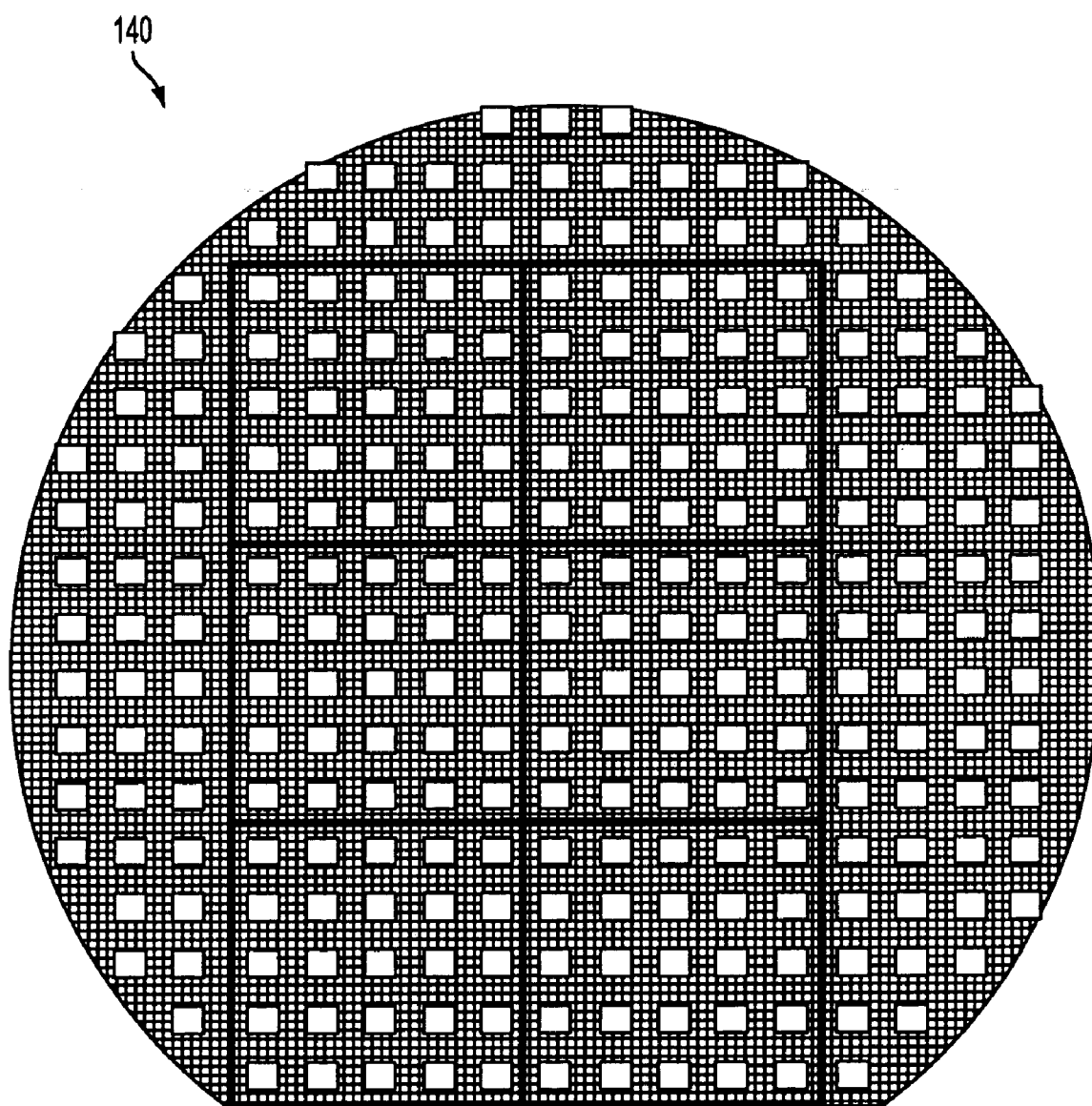
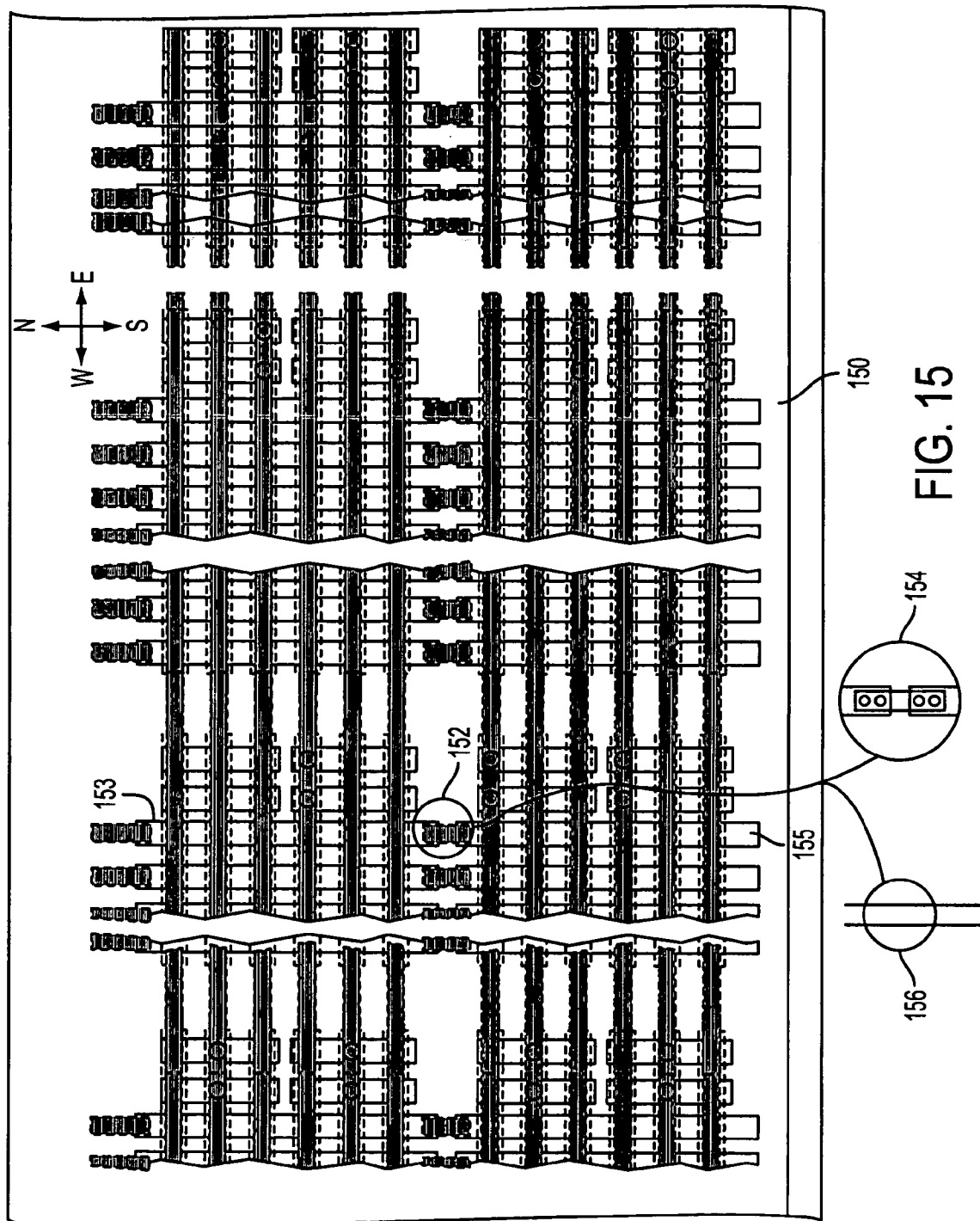


FIG. 14



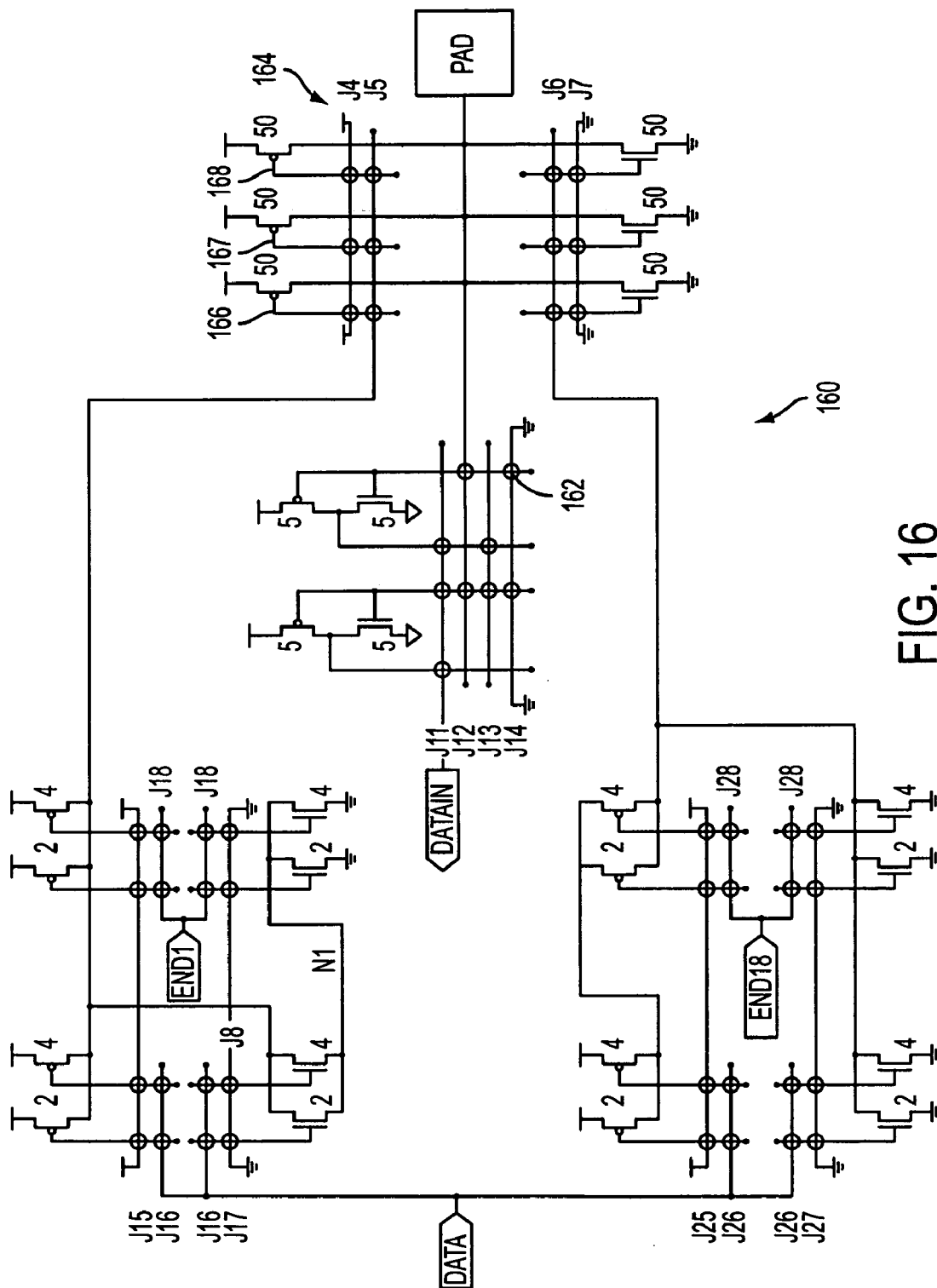


FIG. 16

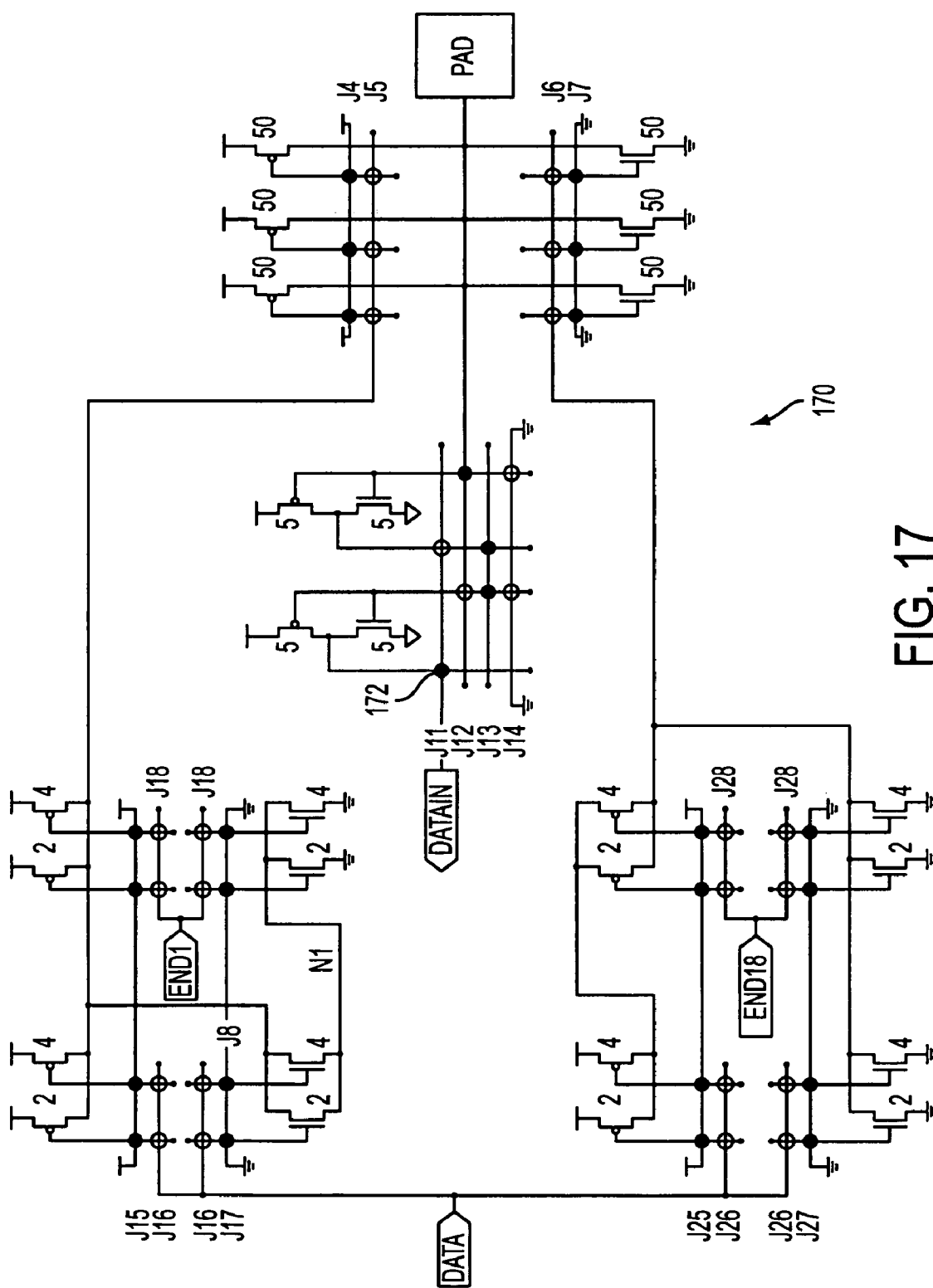


FIG. 17

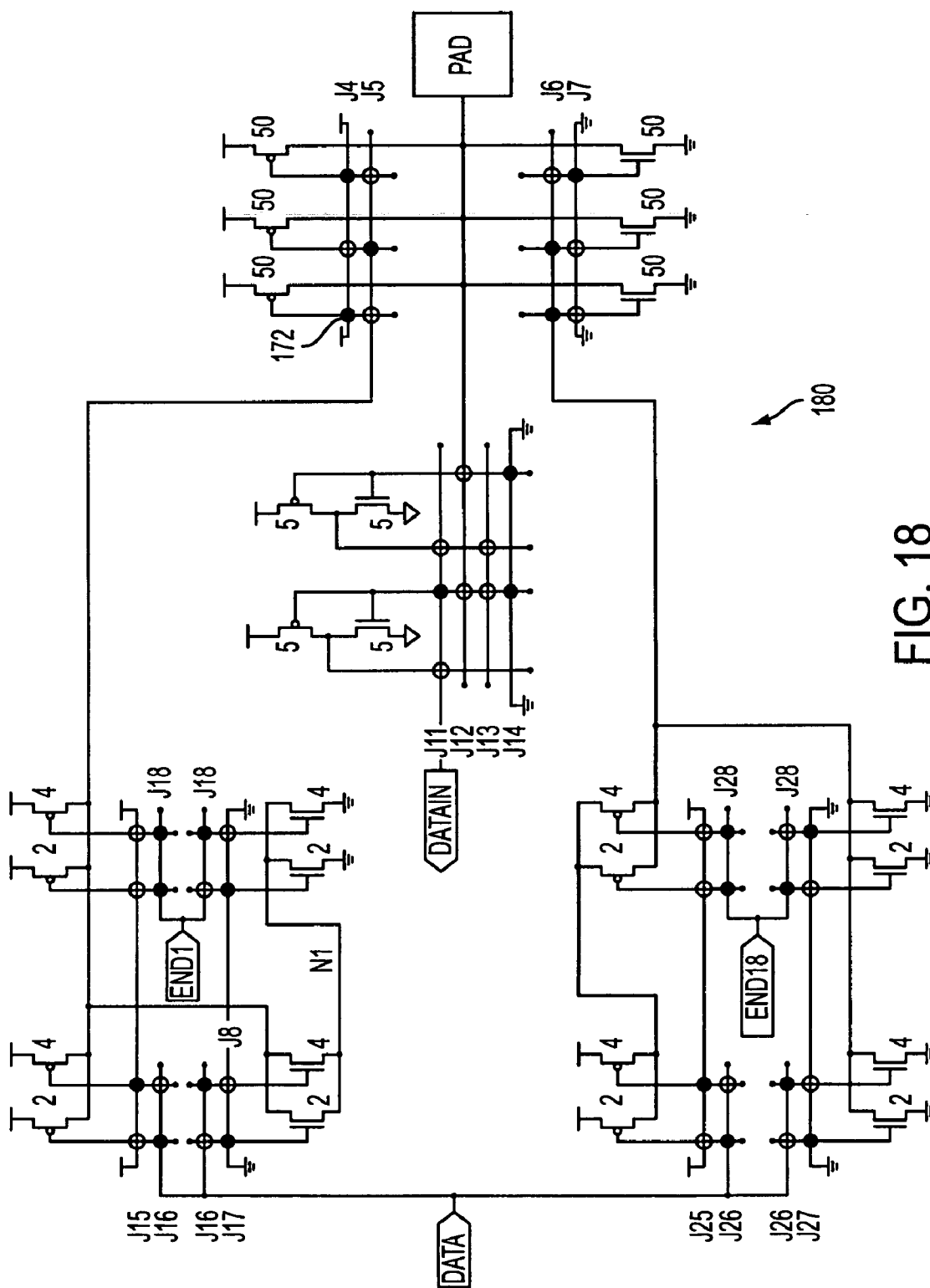


FIG. 18

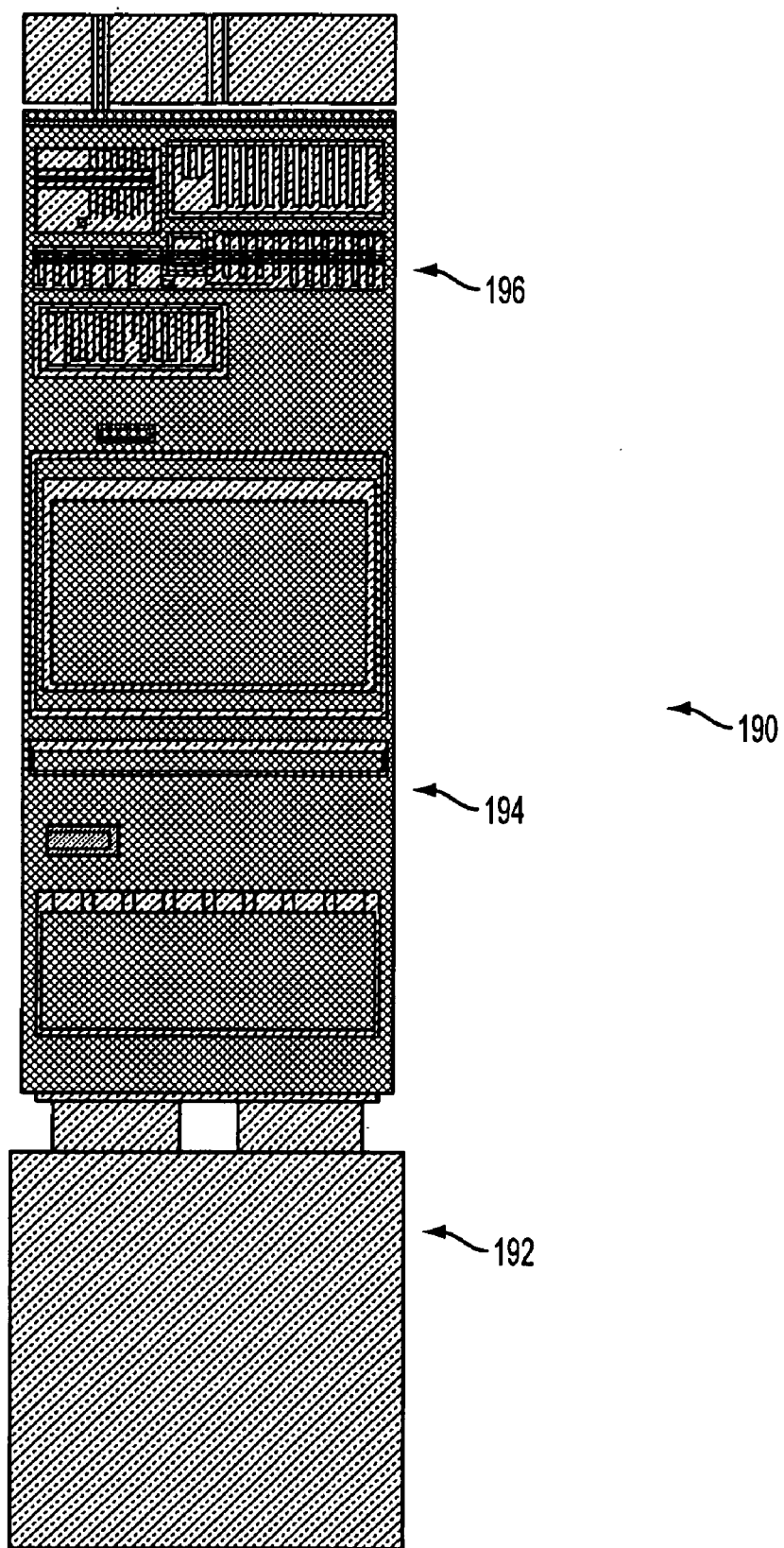


FIG. 19

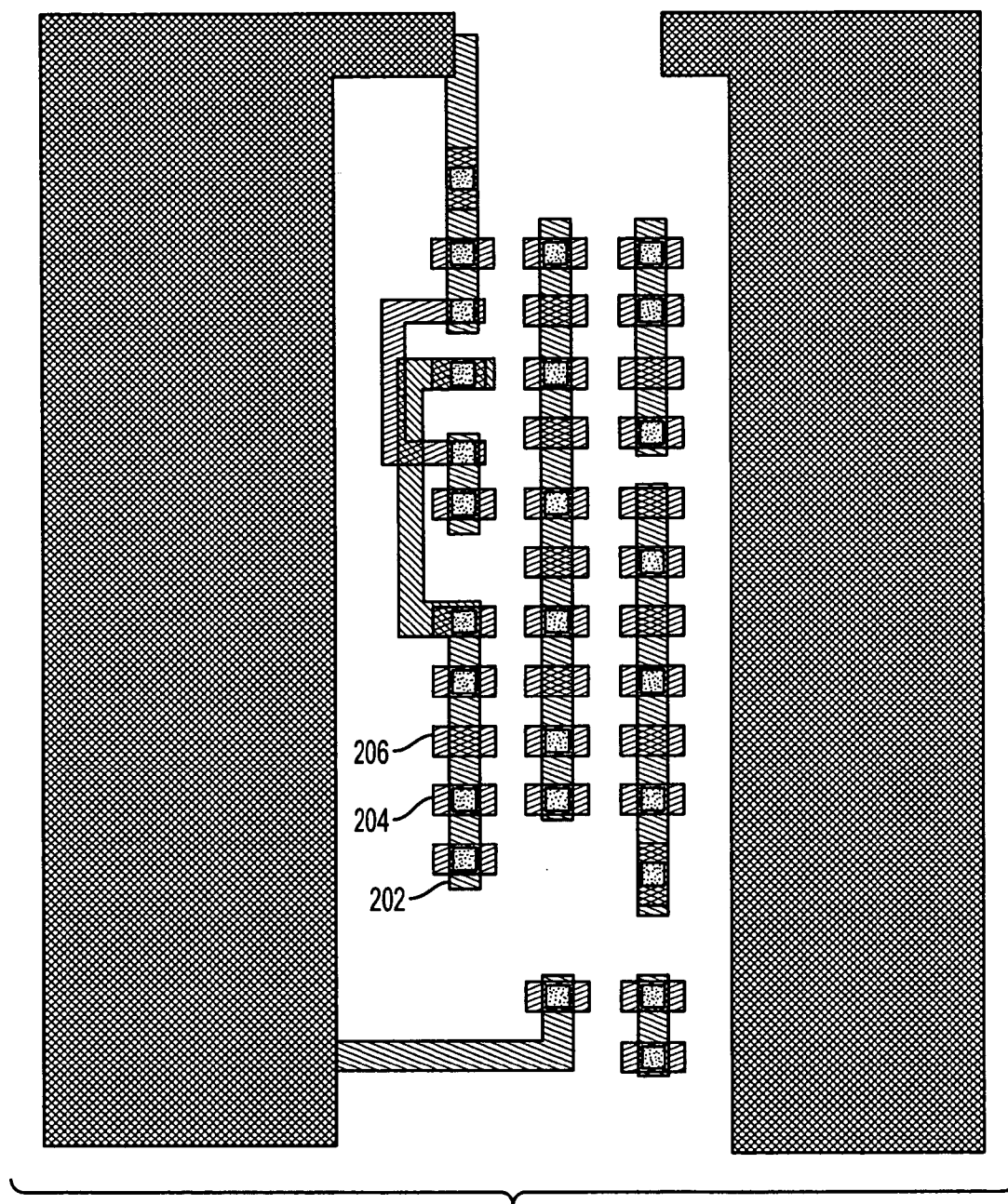
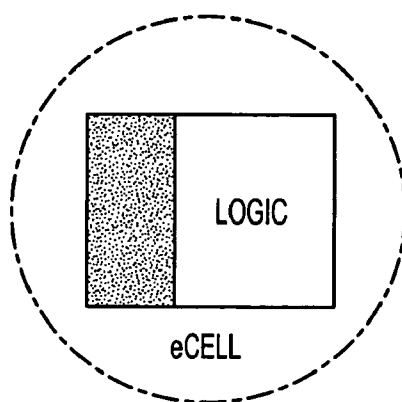
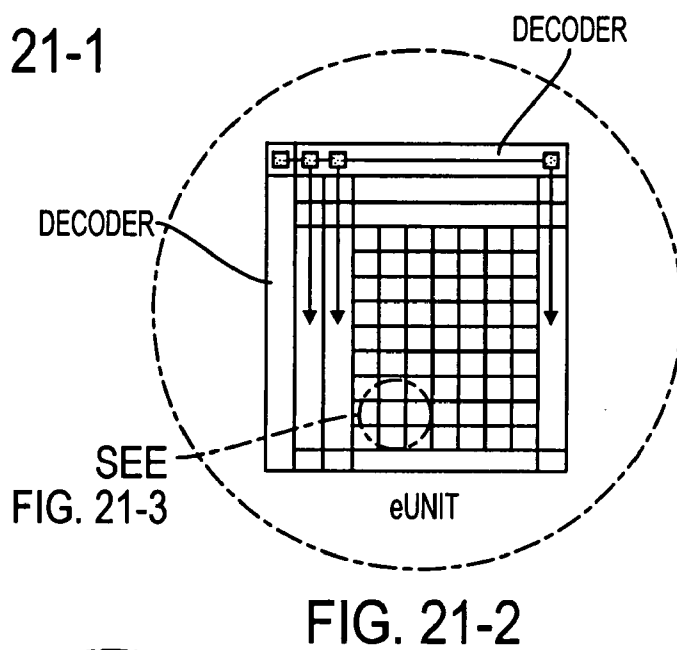
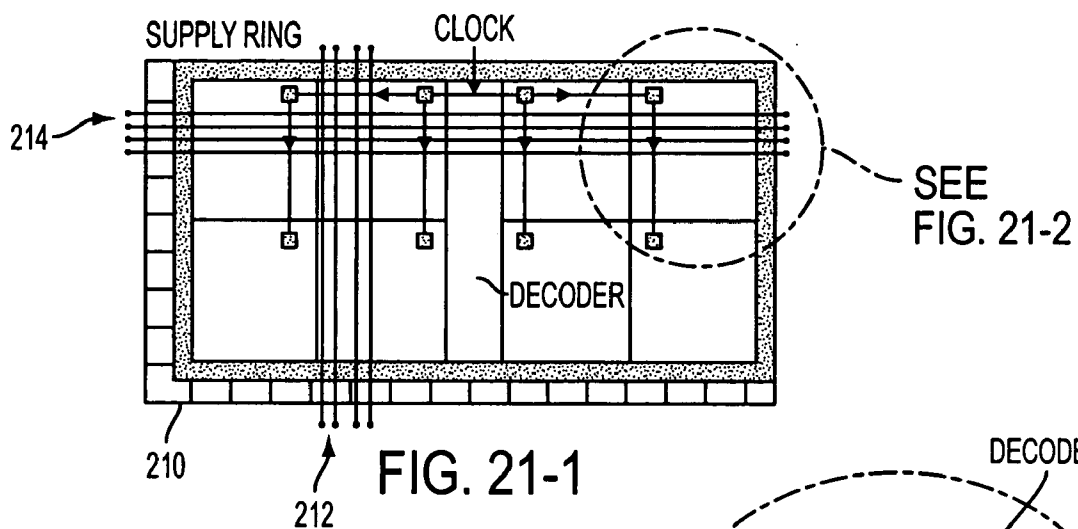


FIG. 20



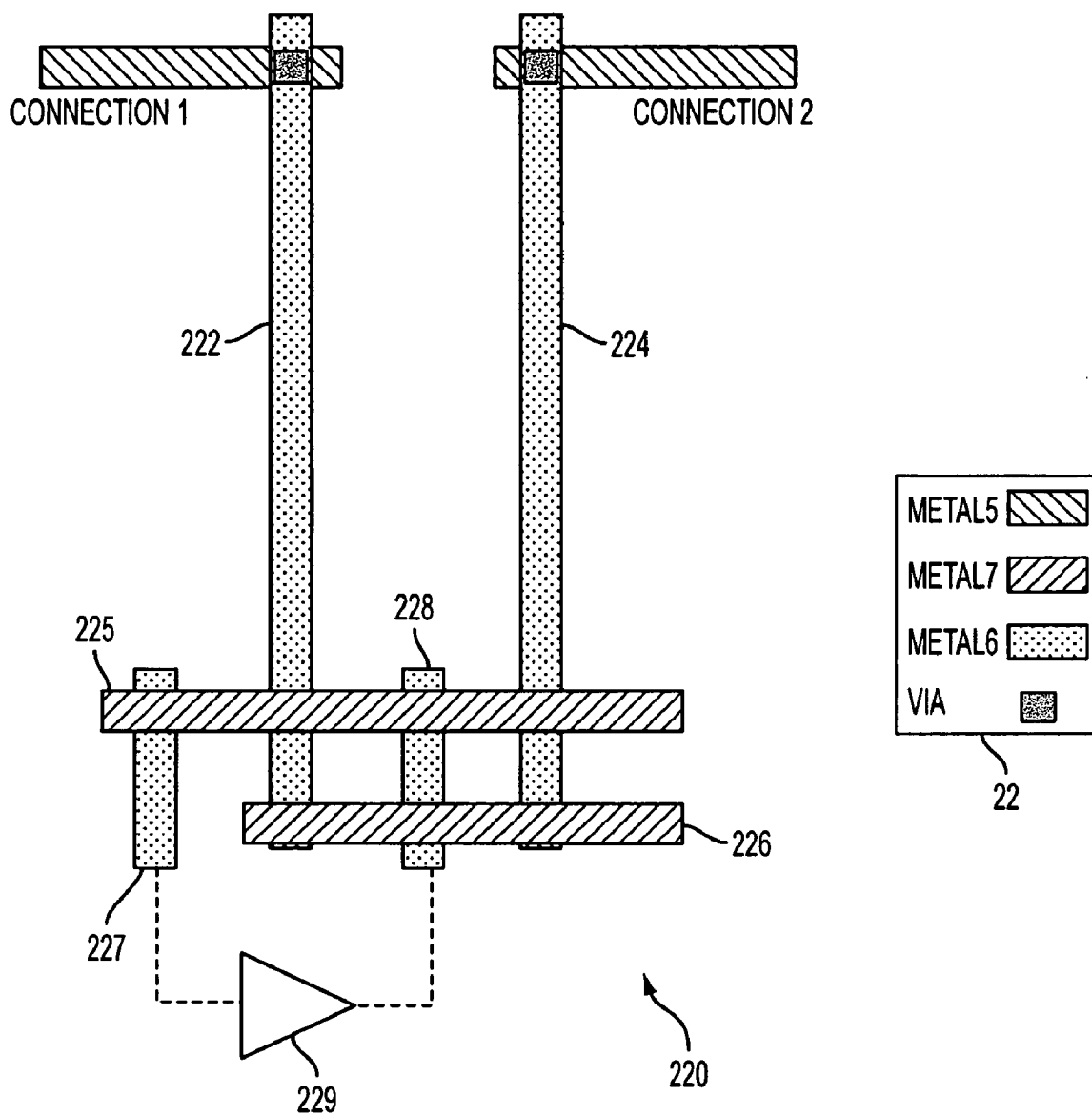


FIG. 22

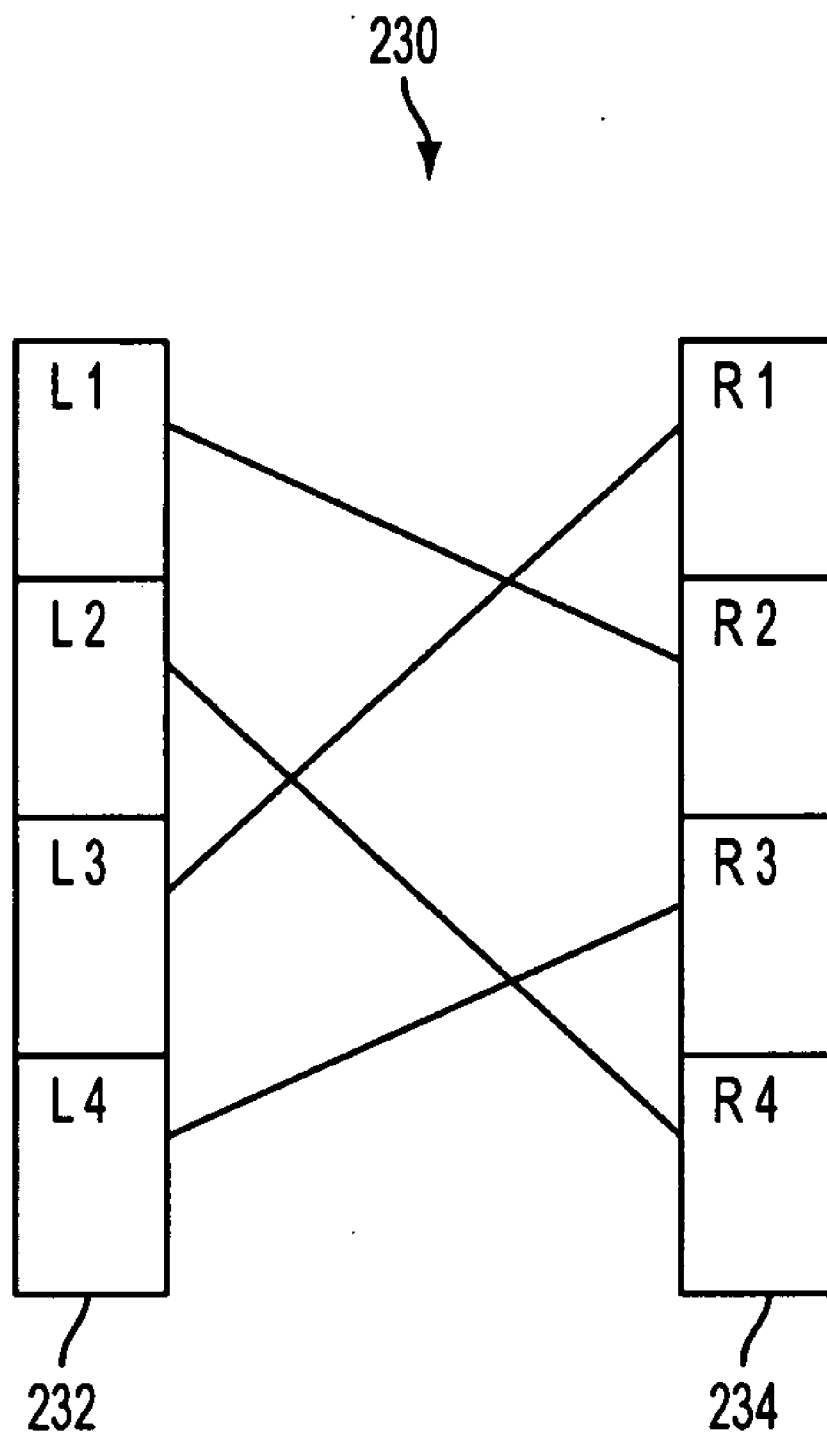


FIG. 23

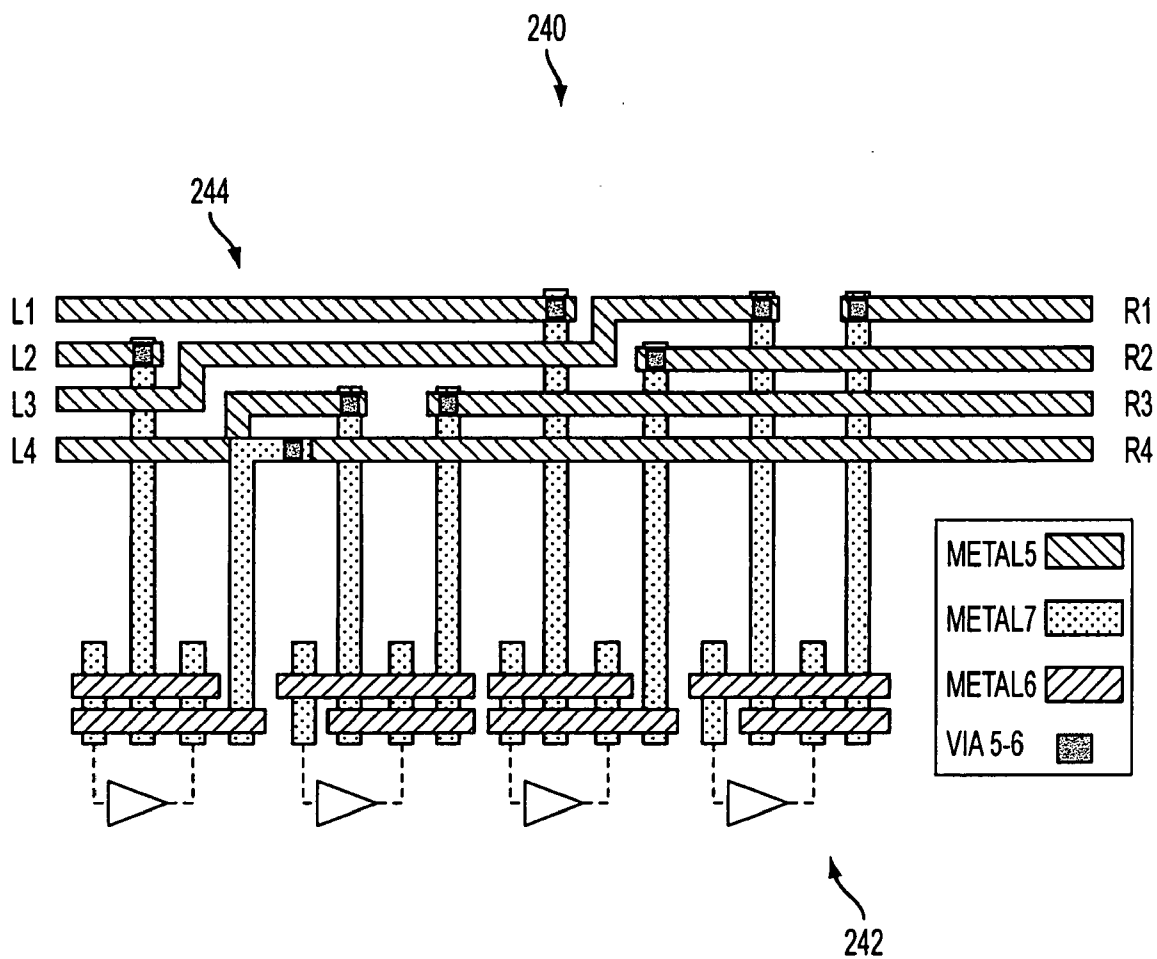


FIG. 24

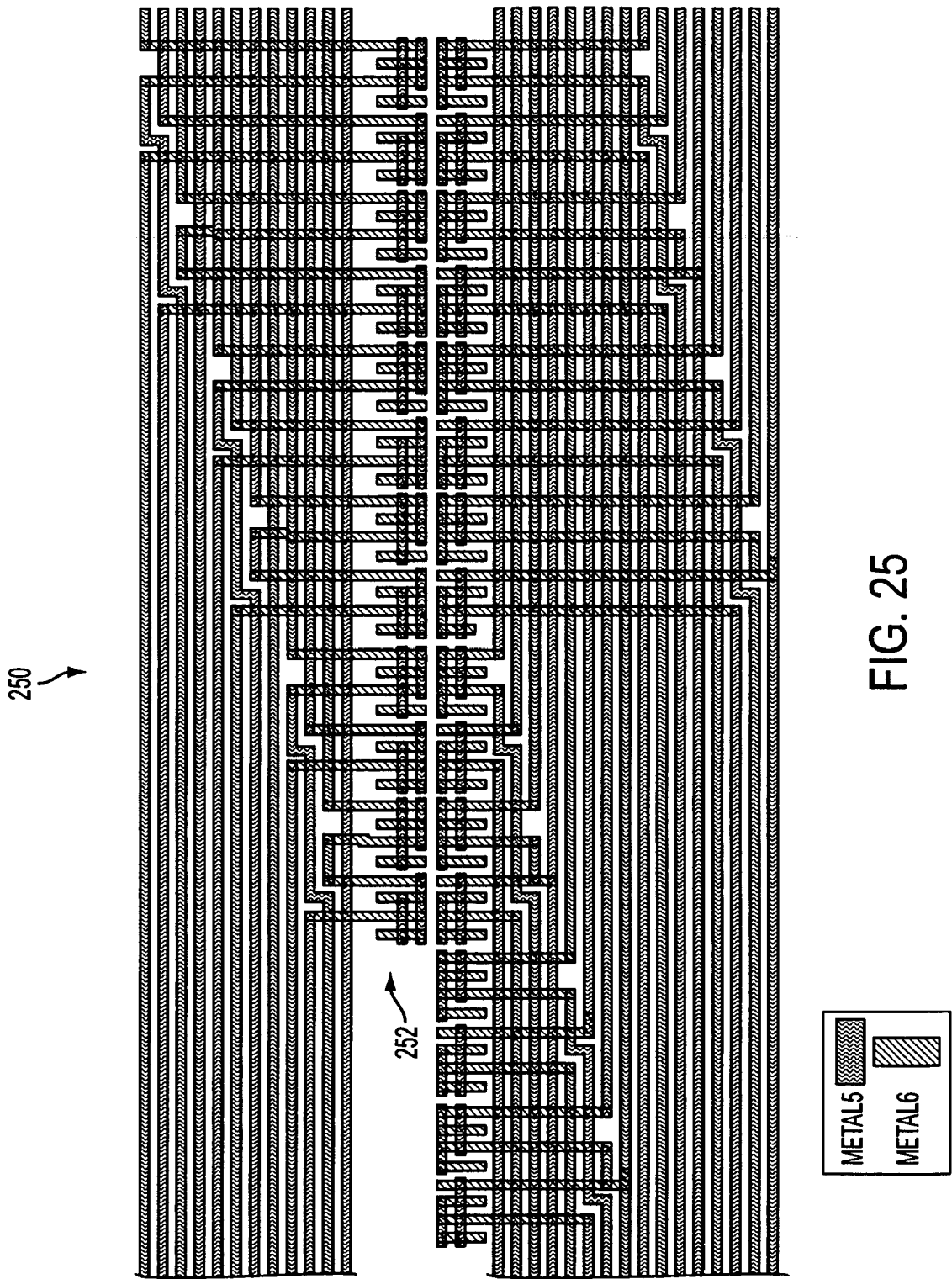


FIG. 25

METHOD FOR FABRICATION OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to logic arrays and fabrication method for custom integrated circuit

[0003] 2. Discussion of Background Art

[0004] Semiconductor manufacturing is known to improve device density in exponential manner over time, but such improvements do come with a price. The cost of mask set required for each new process technology has been increasing exponentially. In addition, the minimum fabrication quantity due to the increases of wafer size has also increased exponentially at the same time.

[0005] These changes represent an increasing challenge primarily to custom products, which tend to target smaller volume and less diverse market, therefore making the increased cost of product development and reduction of manufacturing flexibility very hard to accommodate.

[0006] Custom Integrated Circuits can be segmented into two groups. The first are devices that have all their layers custom made. The second group are devices that have at least some generic layers used across different custom products. Well known examples of the second kind are Gate Arrays, which use generic layers for all layers up to contact layer, and FPGAs which utilize generic layers for all their layers. This second group of custom integrated circuits is also sometimes called semi-custom devices due to their broader applicability. The generic layers in such devices are mostly a repeating pattern structure in array form.

[0007] The use of generic layers across multiple application provides saving for the individual custom product with respect to the cost of masks and economies of scale. In 1996 Chip Express of Santa Clara, Calif., introduced a logic array called CX2000 that utilized a base logic cell equivalent to about 4 logic gates. At a later time Lightspeed Semiconductor of Sunnyvale, Calif., introduced their 3G Modular Array product family. These more advanced logic arrays use generic layers, comprising mostly repeating pattern, also for some of the metal layers such as contact, Metal-1, Via-1 and Metal-2. These types of logic arrays are sometime called Module Arrays and require less custom layers. A very advanced Module Array technology was introduced by eASIC of San Jose, Calif., in September 2000.

[0008] That Module Arrays uses generic layers such as Metal-1 and Metal-2 to define the logic array, in conjunction with generic layers such as Metal-3 and Metal-4 to provide a generic connectivity fabric. The generic connectivity fabric comprises of repeating patterns and are also structured in array form. Such arrangement allows to further reduce the number of custom layers required for design customization. eASIC technology, as described in U.S. Pat. No. 6,331,790 is going further toward the goal minimizing the number of custom masks and requires only a single custom via mask.

[0009] The logic array technology is based on a generic fabric that is customized for a specific design during the customization stage. As designs tend to be highly variable in the amount of logic and memory each one needs, vendors of logic array create product families with a number of Master

Slices covering a range of logic and memory size options. Yet, it is always a challenge to come up with minimum set of Master Slices that will provide a good fit for maximal number of designs.

[0010] U.S. Pat. No. 4,733,288 issued to Sato Shinji Sato in March 1988, discloses a method "to provide a gate-array LSI chip which can be cut into a plurality of chips, each of the chips having a desired size and a desired number of gates in accordance with a circuit design." The prior art in the references cited presents few alternative methods to utilize generic structure for a different size of custom devices.

[0011] The array structure fits the objective of variable sizing. The difficulty to provide variable-sized devices is due to the need of providing I/O cells and associated pads to connect the device to the package.

[0012] U.S. Pat. No. 5,217,916 issued to Anderson et al. on Jun. 8, 1993, discloses a configurable gate array free of predefined boundaries-borderless-using transistor gate cells, of the same type of cells used for logic, to serve the input and output function. Accordingly, the input and output functions may be placed to surround the logic array sized for the specific application. This method presents a severe limitation on the I/O cell to use the same transistors as used for the logic and would not allow the use of higher operating voltage for the I/O.

[0013] It is also known in the art that I/O and pads do not need to be at the edge of the semiconductor device. Semiconductor devices could be using the flip chip or C-4 (controlled collapse chip connection) technology described in U.S. Pat. Nos. 3,401,126 and 3,429,040 by Miller that had been used for over 30 years in IBM's mainframe computer modules. In these approaches the bonding pads are deployed in an area array over the surface of the chip known as area bonding and may use I/O cells known as area I/O placed near the area pads. Flip Chip packaging is known in the art to use an additional final metal layer known as the redistribution layer, to allow proper distribution of the device I/O to the area pads.

SUMMARY OF THE INVENTION

[0014] The present invention seeks to provide a new method for semiconductor device fabrication that is highly desirable for custom products. The current invention suggests the use of direct-write e-Beam in conjunction with a continuous logic array. The continuous array utilizes area I/O with area pads to allow variable sizing of designs and placing them on a wafer with various numbers of repetitions. The current invention provides solution to the challenge of high cost of mask-set and low flexibility that exist in the currently-common method of semiconductor fabrication. An additional advantage of the invention that it reduces the high cost of manufacturing the many different mask sets required in order to provide acceptable range of master slices. The current invention improves upon the prior art in many respects, including the way the semiconductor device is structured and those related to methods of fabrication of semiconductor devices.

[0015] The prior art reflected the motivation to better fit the device size to the custom application and therefore saving on wasted silicon. The current invention reflects the motivation to save the cost of mask with respect to the

investment that would have been otherwise required to put in place proper set of master slices. The current invention also seeks to provide the ability to incorporate memory block in the custom device. The current invention provides a method to customize the device with respect the amount of logic and memory required.

[0016] The main point of the current invention is the use of area I/O to provide a continuous fabric that provides a continuous terrain of logic and I/O and also provides the ability to mix in continuous terrain of memory with islands of special functions like PLL and SERDES. The current invention shows that with area I/O and redistribution layer to connect the area I/O to area pads, many of the limitation of the prior art are overcome. A greater level of flexibility is therefore provided. The current invention also suggests to utilize Module Array, whereby additional layers such as Metal-1 and Metal-2 are generic and would be part of such borderless continuous terrain. Furthermore, the current invention also suggests the use of segmented routing whereby some of the connectivity layers are also generic and would be a part of the continuous terrain. In such fabric only few layers need to be customized while most of the layers are generic and consist primarily of a repeating pattern. A favorable embodiment of the current invention is a continuous terrain customizable by single custom via layer. Furthermore, the current invention suggests the use of direct-write e-Beam for those few custom layers. An added advantage of the current invention is the use of direct-write e-Beam on the continuous terrain to provide on the same wafer different product types, with different amount of product units of the various product types. The very large size of current wafer allows hundreds of device units, each of different type, built on a single wafer. Therefore the current invention allows to provide "on-demand" semiconductor device manufacturing, where one customers could get few units of one type of device for prototype work, while another may get few hundreds of devices for low volume production, all from a single wafer fabrication process.

[0017] To allow such level of flexibility with borderless terrain, the current invention suggests wafer level customization using equipment like direct-write e-Beam and dicing the wafer using highly flexible dicing using equipment like laser-based dicing. Such equipment allows mix and match of various die sizes on the wafer, as opposed to the saw dicing commonly used in the industry, which requires dicing along complete straight lines from one wafer edge to the other. An added advantage of the current invention's is the use of area pads and homogenous pad terrain so single probe card could be use for various devices.

[0018] The present invention also seeks to provide an improved semiconductor device including borderless logic array; area I/Os; and a redistribution layer for redistributing at least some of the area I/Os.

[0019] Preferably some of the pads are used to connect the semiconductor device to other devices and overlays at least a portion of the logic array or a portion of the area I/Os.

[0020] Preferably the semiconductor device also includes a borderless memory array. Preferably the logic array includes a module array. Preferably the logic array includes interconnections within the logic array, wherein the logic array interconnections include metal layers and via layers, and wherein at least one of the metal layers includes at least

one substantially repeating pattern for a portion used for the interconnections. And according to one embodiment of the invention, the logic array interconnection includes at least two of metal layers with substantially repeating patterns for portions used for interconnections. And according to another embodiment of the invention, the logic array interconnection includes at least three metal layers with substantially repeating patterns for portions used for the interconnections. Preferably the area I/Os are positioned in a non-surrounding fashion with respect to the logic array. Preferably, the logic array includes a repeating module, and wherein the area I/Os are positioned in a non-surrounding fashion with respect to at least one of the repeating module. Preferably at least one of the area I/Os is a configurable I/O.

[0021] There is thus provided in accordance with a preferred embodiment of the invention, a method of fabricating a semiconductor device, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os.

[0022] Preferably also including the step of: forming pads to connect the semiconductor device to other devices, and wherein at least one of the pads overlays at least a portion of the logic array or a portion of the area I/Os.

[0023] Preferably also including the steps of: placing and routing a specific design on the logic array; and marking marks for an edge of a used portion of the logic array according to the step of placing and routing.

[0024] Preferably the step of marking comprises photolithography, and also including a step of dicing the semiconductor substrate according to the marks.

[0025] Preferably the step of dicing includes laser dicing.

[0026] There is thus provided in accordance with another preferred embodiment of the invention, a method of fabricating an integrated circuit, comprising the step of: Providing a semiconductor substrate, forming a borderless logic array including a memory array, a plurality of area I/Os and also including the step of forming redistribution layer for redistribution at least some of the area I/Os for the purpose of the device packaging.

[0027] Preferably also including the steps of: placing and routing a specific design on the logic array and the memory array; and marking marks for an edge of a used portion of the logic array and the memory array according to the step of placing and routing.

[0028] Preferably the step of marking, includes photolithography, and also including a step of dicing the semiconductor substrate according to the marks.

[0029] Preferably the step of dicing includes laser dicing.

[0030] There is thus provided in accordance with another preferred embodiment of the invention, a method of fabricating an integrated circuit, comprising the step of: providing a semiconductor substrate, forming a borderless logic array including, a plurality of area I/Os and also including the step of forming redistribution layer for redistribution at least some of the area I/Os for the purpose of the device packaging and wherein the logic array includes a module array.

[0031] There is thus provided in accordance with another preferred embodiment of the invention, a method of fabricating an integrated circuit, comprising the step of: Providing a semiconductor substrate, forming a borderless logic array including a plurality of area I/Os and also including the step of forming redistribution layer for redistribution at least some of the area I/Os for the purpose of the device packaging, and wherein the logic array is interconnected by metal layers and via layers, and wherein at least one of the metal layers comprises at least one substantially repeating pattern for a portion used for interconnecting.

[0032] And according to one embodiment of the invention, at least two of the metal layers include substantially repeating patterns for portions used for interconnecting.

[0033] And according to another embodiment of the invention, at least three of the metal layers comprise substantially repeating patterns for portions used for the interconnecting.

[0034] There is thus provided in accordance with a preferred embodiment of the invention, a method of fabricating a semiconductor device, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os. And also includes the step of utilizing a direct write technique to customize the logic array.

[0035] Preferably the step of marking utilizes a direct write technique.

[0036] There is thus provided in accordance with a preferred embodiment of the invention, a method of fabricating a semiconductor device, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os, and wherein the step of forming a borderless logic array comprises the step of positioning the area I/Os in a non-surrounding fashion with respect to the logic array.

[0037] There is thus provided in accordance with another preferred embodiment of the invention, a method of fabricating a semiconductor device, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os, and wherein the logic array includes a repeating core, and wherein the step of forming a borderless logic array includes the step of positioning the area I/Os in a non-surrounding fashion with respect to at least one of the repeating core.

[0038] Preferably at least one of the area I/O is configurable I/O.

[0039] Preferably also including the step of: performing photolithography, wherein a reticle is projected over the semiconductor substrate, and wherein the used portion comprises elements from two projections.

[0040] There is thus provided in accordance with a preferred embodiment of the invention, a method of fabricating an integrated circuit wafer, comprising the steps of: providing a semiconductor substrate; forming a borderless logic

array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os.

[0041] Preferably also comprising the step of: forming pads to connect the semiconductor device to other devices, wherein at least one of the pads overlays at least a portion of the logic array or a portion of the area I/Os.

[0042] Preferably also including the steps of: placing and routing a specific design on the logic array; and marking marks for an edge of a used portion of the logic array according to the step of placing and routing.

[0043] Preferably the step of marking comprises photolithography, and also includes a step of dicing the semiconductor substrate according to the marks.

[0044] Preferably the step of dicing includes a step of laser dicing.

[0045] There is thus provided in accordance with a preferred embodiment of the invention, a method of fabricating an integrated circuit wafer, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a memory array, a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os.

[0046] Preferably also comprising the steps of: placing and routing a specific design on the logic array and the memory array; and marking marks for an edge of a used portion of the logic array and the memory array according to the step of placing and routing.

[0047] Preferably the step of marking comprises photolithography, and also comprising a step of dicing the semiconductor substrate according to the marks.

[0048] Preferably the step of dicing includes laser dicing.

[0049] Preferably the logic array includes a module array.

[0050] Preferably the logic array is interconnected by metal layers and via layers, and wherein at least one of the metal layers includes at least one substantially repeating pattern for a portion used for interconnecting.

[0051] Alternatively at least two of the metal layers include substantially repeating patterns for portions used for the interconnecting.

[0052] Preferably the step of placing and routing is done for a specific design called A' and also for another specific design called B', and wherein the location on the wafer in which design A' is placed is independent of the location on the wafer in which design B' is placed.

[0053] Alternatively the step of placing and routing is done for a specific design called A' and also for another specific design called B', and wherein a number of times that design A' is placed on the wafer is independent of a number of times that design B' is placed on the wafer.

[0054] Preferably the step of marking includes the step of utilizing a direct write technique.

[0055] Preferably the step of placing and routing is done for a specific design called A' and also for another specific design called B', and wherein a silicon area ratio of logic

array to memory array in design A' is substantially larger than a silicon area ratio of logic array to memory array in design B'.

[0056] Preferably the step of marking includes the step of utilizing a direct write technique.

[0057] Preferably also including the step of probing the wafer, wherein the step of probing utilizes the same wafer probe to test design A' and design B'.

[0058] Preferably also comprising the step of probing the wafer, wherein the step of probing utilizes the same wafer probe to test design A' and design B'.

[0059] Preferably also comprising the step of probing the wafer, wherein the step of probing utilizes the same wafer probe to test design A' and design B'.

[0060] Preferably also comprises the step of utilizing a direct write technique to customize the logic array.

[0061] Preferably the design A' and design B' are probed simultaneously.

[0062] Preferably design A' and design B' are probed simultaneously.

[0063] There is thus provided in accordance with additional preferred embodiment of the invention, a method of fabricating an integrated circuit wafer with improved yield, comprising the steps of: providing a semiconductor substrate; forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and forming a redistribution layer for redistributing at least some of the area I/Os, and further comprising the steps of: testing and marking modules on the logic array; placing specific designs on the logic array so as to avoid faulty modules; and customize the logic array according to placement of specific designs; testing and marking the specific designs; and dicing the logic array according to placement and marking of specific designs.

[0064] Preferably utilizing a direct write technique to customize the logic array.

[0065] Preferably having one or more pads dedicated to testing.

[0066] Preferably also including the step of using a probe card to independently test one or more modules simultaneously.

[0067] Preferably one or more of the pads dedicated to testing are not the area I/Os for the specific designs.

[0068] Preferably at least one of the area I/Os comprises a configurable I/O.

[0069] Preferably the configurable I/O comprises multiple copies of input, output, and pre-output cells, and wherein the semiconductor device further comprises connections between at least one of the input, output, and pre-output cells and area I/O pads to construct an area I/O.

BRIEF DESCRIPTION OF THE DRAWINGS

[0070] The present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

[0071] FIG. 1 is a drawing illustration of a wafer marked with reticle projections;

[0072] FIG. 2 is a drawing illustration of a repeating core;

[0073] FIG. 3A is a drawing illustration of a area pads;

[0074] FIG. 3B is a pictorial illustration of a area pads—soldering balls;

[0075] FIG. 4 is a detail drawing illustration of the area pads;

[0076] FIG. 5 is a drawing illustration of a wafer level borderless logic array;

[0077] FIG. 6 is a drawing illustration of a wafer shared between two applications utilizing reticle sharing;

[0078] FIG. 7 is a drawing illustration of a wafer shared between two applications;

[0079] FIG. 8 is a drawing illustration of a wafer shared between three applications;

[0080] FIG. 9A is a drawing illustration of a reticle fabric;

[0081] FIG. 9B is a drawing illustration of a reticle fabric;

[0082] FIG. 9C is a drawing illustration of a reticle fabric;

[0083] FIG. 10A is a drawing illustration of a reticle fabric;

[0084] FIG. 10B is a drawing illustration of a reticle fabric;

[0085] FIG. 11 is a drawing illustration of a reticle fabric;

[0086] FIG. 12 is a drawing illustration of a wafer marked with reticle projections;

[0087] FIG. 13 is a drawing illustration of a module;

[0088] FIG. 14 is a drawing illustration of a wafer comprise wafer level borderless logic array covered with Area Pads;

[0089] FIG. 15 is a drawing illustration of via customizable routing structure;

[0090] FIG. 16 is a drawing illustration of via customizable I/O;

[0091] FIG. 17 is a drawing illustration of via customizable I/O customized as input;

[0092] FIG. 18 is a drawing illustration of via customizable I/O customized as output;

[0093] FIG. 19 is a layout drawing illustration of via customizable I/O;

[0094] FIG. 20 is a layout drawing illustration of a small section of via customizable I/O;

[0095] FIG. 21 is a drawing illustration of very long tracks over a core;

[0096] FIG. 22 is a drawing illustration of a configurable buffer structure;

[0097] FIG. 23 is a drawing illustration of a simple “scramble box;”

[0098] FIG. 24 is a drawing illustration of “scramble box” layout; and

[0099] FIG. 25 is a drawing illustration of “scramble box” layout for 24 lines.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0100] The present invention is now described with reference to FIGS. 1-25, it being appreciated that the figures illustrate the subjects matter not to scale or to measure.

[0101] The current method of semiconductor fabrication is on lithography step for each layer. The dominating lithography technique of submicron process is called step and repeat. The layer pattern will be drawn into mask also called reticle. Such reticle may be projected over an area of about 20 mmx20 mm by the lithography tool called Stepper. Then the Stepper steps the wafer so the reticle would be projecting the same pattern on area next to it and so for. FIG. 1 illustrates a wafer 8 with marks 12 of reticle projections 10. With an 8-inch wafer, over 50 copies of the reticle will be typically stepped on one such wafer.

[0102] The current invention suggests the use of a much less common lithography technique called direct-write using e-Beam. Such could be done, for example, with direct-write e-Beam—Leica ZBA32 offered by Leica Microsystems Lithography GmbH Jena, Germany or F5112 offered by Advantest, Japan. Direct-write e-beam allows direct writing any pattern at any location over the wafer, without the use of a physical mask. Direct-write e-beam is not used in commercial fabrication of semiconductor devices due the low throughput and the implication of such on a single wafer cost. The current invention suggests the combination of reticle technique for the generic portion of logic array and the use of direct-write e-beam for the custom layers. A very good fit with this method is the logic array invented by eASIC, as only it provides a logic array that could be customized with single via layer. Via layer can be written much faster than metal layer with direct-write e-beam and would make such combination method commercially viable.

[0103] Such direct-write e-beam fabrication method are highly attractive for custom designs as previously described. Since single wafer may have room for hundreds of devices, the current invention seeks to allow multiple designs to be placed on one wafer and further, to allow each of these designs to be of different size and, even further, to allow placing different quantities of such designs on a single wafer, to support on one wafer the fabrication needs of both prototype volumes for some design and pre-production volumes for other designs.

[0104] While direct-write e-Beam is the most common technique, other direct-write lithography could be used. A laser mask write systems like Sigma 7000 from Micronic could be modified for such usage.

[0105] The current invention suggests a new architecture of logic array. This new architecture blends logic array with array of area I/O and array of area pads. Therefore it provides a continuous fabric instead of the master slice approach. Such fabric could comprise of a repeating structure—repeating core—as is illustrated in FIG. 2. The repeating core 28 comprises a set of area I/O 26 and then logic array 24 which is constructed from array of eCells 22. The area I/O may be constructed with thick oxide to allow them to operate at higher voltage appropriate to interface with the

element outside the device, while the logic array might be using thin oxide to operate at low voltage to reduce power consumption and allow higher performance and packing density. The area I/O might comprise elements that are common at boundary I/O such as ESD protection and latch-up protection. The area I/O could be configurable I/O that could be customized to the specific function by the custom layers used to customize the logic. The area I/O could include fixed function like input and output functions. The power supply to the core 28 and to the area 26 could be supplied from the same group of area pads.

[0106] FIG. 3 is a drawing and pictorial illustration of the area pads. FIG. 3A is a vertical cut drawing showing one area pad and the associated bump 30, and the layers underneath it including a thick layer 32 sometimes called redistribution layers and the underlying layers such as Metal-1 34, Metal-2 36 and Metal-4 38. FIG. 3B is a pictorial of section of the top surface of a device according to the current invention, with a regular array of area pads in the forms of bumps 39. FIG. 4 is a detailed drawing illustration of an area pads and sample sizes for such bumps. To maximize the number of pads per area, it is common to place the area pads in a regular array as can be seen in FIG. 3B. Consequently it is useful to have a top metal layer for pads redistribution, to allow area pads placement to be independent from area I/O placement.

[0107] This invention suggests a fabric of a repeating core which include logic, area I/O, and area pads. The minimum size of such core would be to fit single area pads like 3A. In most cases a larger size core would be more practical. The core 28 of FIG. 2 is about 1 mmx0.5 mm in 0.13 micron process. It would be quite possible to provide 4x2 area pads and the appropriate number of area I/O with it. Tilling such core to span a full wafer will allow a fabric of borderless logic array of about 20x40 cores 28 in one reticle. If the accuracy of the stepper is high enough, it would be conceivable that the borderless fabric could be extended up to wafer level. In such case it may require somewhat less dense lithography pitch for the routing structures, to allow spanning across reticle boundaries. The wafer level borderless fabric provides the highest level of flexibility and wafer utilization effectiveness. For the ease of description, the following detailed description of the additional preferred embodiments of this invention assumes wafer level borderless logic array. FIG. 5 is a drawing illustration of a wafer 50 comprising of wafer level borderless logic array of continuous tilling of cores 52.

[0108] The redistribution layer may also be a custom layer. It could therefore be custom designed to redistribute the area I/O to the edge pads in a specific design and therefore allow such custom design to be packaged using conventional bonding rather than Flip-chip. FIG. 3C illustrates the use of redistribution layer 32 to connect area I/O 36 to edge pads 34 so wire bonding could be used.

[0109] FIG. 6 is a drawing illustration of a wafer shared between two designs utilizing reticle sharing. FIG. 6 illustrates the existing art of reticle sharing wherein one reticle may include design A'62 which is placed and routed on the logic array and occupies a large portion of the reticle, and design B'64 that is smaller and could be placed two times within the reticle, so together with design A' the reticle

is fully utilized. Design A' edges are marked by marks **63** and **66** and design B' edges are marked by marks **65**, **66** and **67**.

[0110] It might be highly desirable to have these edges **63**, **65** marked by lithography and following process to allow proper dicing of the wafer. Such marking would be best done at the top or very close to the top layer and prior to the bump processing step. Such marking step is not usually required for logic array where the master slice are arranged for specific array size and the boundary pads, together with the space between devices, make it very visible where dicing should take place.

[0111] It is clear that conventional saw dicing would be proper for dicing the wafer **60** from design A' point of view. Yet the edge **67** would be left to be diced at a later stage to separate the two dies of design B'.

[0112] The current invention provides the ability to size each design independently and to mix different designs on single wafer. Constraining dicing along straight continuous lines places a strong limitation on the ability to share one wafer with multiple-sized designs. It is therefore suggested to use laser dicing for wafers fabricated according to the current invention. Laser dicing is being developed and offered by few companies such as DFL7160 made by Disco Corporation Tokyo, Japan, and Multidice made by NanoVia, LP of Londonderry, N.H. Thinning the back of the wafer may be required so laser dicing would allow for a full cut rather than just scribing.

[0113] In another embodiment of the current invention, a very flexible wafer sharing is suggested. Such wafer sharing provides much higher flexibility than reticle sharing. **FIG. 7** is a drawing illustration of a wafer shared between two applications taking advantage of the borderless array, together with the use of direct-write for wafer level lithography. It is therefore possible to mix different designs at various quantities on such wafer. **FIG. 7** illustrates design **72** placed for prototype stage, while another design **74** is placed many more times. Unlike the case with reticle sharing, the locations and the number of times one design is placed on a wafer has little bearing on the other design. An important advantage of this invention is that the location on the wafer in which one design is placed, is independent to the location on the wafer in which a second design is placed, other than the obvious limitation that it can not be placed in location already taken by the first design. More importantly, the number of times one design is placed is independent to the number of times the other design is placed.

[0114] **FIG. 8** is a drawing illustration of a wafer **80** shared between three applications. Design **82** has three sites on the wafer, which represent prototype level. Designs **84** and **86** have tens of locations assigned to them. It is clear that the location and the number of sites for design **86** are independent on those of design **82**. In addition it should be noted that many of the dicing lines **88** do not extend from one edge of the wafer **80** to the other edge. Dice lines **88** do not fit saw dicing, but rather require the use of a flexible dicing approach such as laser dicing.

[0115] Many logic arrays are now offering logic fabric with additional functional blocks such as memory blocks, processors or special elements like PLL. Typically the embedded memory takes the second largest portion of the

master slice area after the logic array. In general embedded memories are constructed as a small array of configurable memory blocks. The custom design may need certain amount of memory or some number of PLL and so forth. It is an increasing challenge to select the right master-slice combination, since designs with similar amounts of logic may require very different amounts of memory.

[0116] In yet another embodiment of the current invention, the continuous logic array fabric is comprised of a continuous logic array and continuous memory array of small memory blocks. It therefore now possible that a specific design will be placed on a section of such continuous fabric, sized to have exactly the desired amount of logic and the desired amount of memory.

[0117] **FIG. 9** is a drawing illustration of a reticle **90** fabric comprising of continuous logic array **92** and memory array **94**. **FIG. 9A** illustrates a custom design placed on such terrain as marked by the rectangle **96** to have no memory. **FIG. 9B** illustrates a custom design placed on such terrain as marked by the rectangle **97** to have some memory. **FIG. 9C** illustrates a custom design placed on such terrain as marked by the rectangle **98** to have a small amount of logic and all the rest memory. **FIG. 10A** is a drawing illustration of a reticle fabric **100** wherein the memory terrain **104** is shaped in a staircase manner. **FIG. 10B** illustrates that such staircase arrangement provides a higher level of flexibility with regards to the amount of memory blended into the rectangular markings of the custom design.

[0118] The advantage of continuous terrain is the ability to use one set of generic masks to cover many variations of product fabrics, with the ability to tailor the right amount of logic with the right amount of memory. The additional advantage is the ability to use one wafer run to make a flexible mix of custom products. It is usually highly desirable to utilize the silicon area as effectively as possible. Yet it may often happen that by tailoring the amount of logic and memory to the need of a specific design, the tiling efficiency is compromised. The number of devices on one wafer would be at least the number of times the reticle is stepped over the wafer. If high volume production is required then custom masks could be fabricated so volume production would be done at maximum silicon utilization.

[0119] **FIG. 11** is a drawing illustration of a reticle **110** of a logic array that in addition to array of logic fabric comprises additional functional logic elements like processor blocks **112**, **113**, **114**, **115** and memory array **118**. **FIG. 12** is a drawing illustration of a wafer **120** marked with reticle **110** projections. **FIG. 12** illustrates the use of the wafer terrain to carve out specific design **129** to include elements from four different reticle projections **124**—four processors—with a portion of the memory array **128**. By proper placing a specific design **129** on the wafer terrain, it is possible to optimize the silicon area and yet provide a different mix of elements from one generic fabric.

[0120] The construction of borderless logic array according to the current invention should include consideration for wafer dicing. The common way is to draw a scribe line indicating where the wafer will be scribed, to allow the dicing of the wafer into many individual dies. Typically a laser scribe can cut a 50 microns wide width, but it may be preferred to plan for scribing width between 75 to 100 microns wide. Preferably the continuous array is constructed

as array of modules. A preferred module is rectangular with each side sized between 0.5 to 2 mm. A module could be array of logic or array of memory or combination thereof, which may include other special function like PLL. A preferable location for scribe lines is the edge of such module. The location for potential scribe line may include transistors, which would not be powered if that scribe line is used for dicing. Alternatively it could be designed so only connectivity structures are placed in the scribe lines designated areas. **FIG. 13** is a drawing illustration of a module **130** with designated area for scribe line **136** and customizable connection **134** to the scribe line routing fabric (not shown). The customizable connection **134** allows disconnection from the routing fabric at the scribe lines area, if that potential scribe line is designated for dicing. The repeating module **130** comprises of pads **132** for the I/Os that are included in the module **130** and pads **138** for the supply powering the circuits within the module.

[0121] Yet another advantage of the current invention is the possible use of single Probe Card for multiple designs. **FIG. 14** is a drawing illustration of a wafer comprised of wafer level borderless logic array covered with Area Pads. The pads area of the wafer is uniform and is independent of the specific design size and placement. With such regularity, it is possible to construct single probe card to allow testing of the wafer by stepping over it. Under proper software control a single Probe Card could be used to test any device on the wafer **140**. Similarly, it is also contemplated that a single Probe Card may be used to simultaneously test multiple dies on the wafer, or with the proper test logic, test a die with more area pads than probes on the Probe Card.

[0122] The current invention is not limited to products that combine generic layers with custom layers. Rather it could be use to build a borderless FPGA product. A borderless FPGA wafer could than be diced to provide many options of gate count and block memory size from one base mask-set.

[0123] Another use of the current invention is to yield a very large device. Very large devices are subject to very low yield, which make them economically unviable. Under the current invention yield can be improved if the following procedure is applied:

[0124] (1) Test the substrate layers prior to the custom masks. This implies that each module is independently tested. To do this there need to be pads dedicated to some functions like clock, scan-in, scan-out, and test control. Probe technology exists to probe pads as small as 20x20 microns with minimal damage, though special alignment equipment will probably need to be integrated into existing standard Probers.

[0125] (2) Place the specific design so as to avoid faulty substrate cells. This requires a special placement program, to make the best use of the available wafer area given the outstanding orders of dies to manufacture. Presumably this also controls the designation of the direct write of the adapted for yield custom via patterns.

[0126] (3) Dice the wafer accordingly.

[0127] The resulting system should provide significant yield improvement over existing techniques. Rough analysis suggests that pre-testing and dynamic placement of die can

double the revenue per wafer over conventional techniques, if a sufficiently wide range of die sizes are required for production. It should also be noted that, as with the other techniques above, larger dies than are currently possible with existing stepper technology could be produced. In that case the described yield enhancement is crucial.

[0128] It is further contemplated that the dedicated pads needed for testing may or may not coincide with the area pads as shown in **FIG. 3c**. It is also contemplated that the pads necessary for testing may have the same configuration regardless of the type of module, such that the probe card may be configured to simultaneously probe any combinations of modules at a time.

[0129] In another embodiment, test, power, ground and clock logic may be tied together at the wafer level, such that a single probe of the wafer is sufficient to test all of the modules within the wafer. Subsequent customization and scribing then isolates the power, ground, test and clock logic to specific modules and dies, to reduce the need for special pads, and pre-customization test time.

[0130] **FIG. 15** is a drawing illustration of via layer customizable routing structure **150**. In some fabrication processes a via layer might have reduce yield. A variation of the structure **150**, that uses double via for the continuation bridges **154** instead of single via **152**, could be an effective solution. Via customizable routing fabric increases the use of vias primarily in the form of same direction connection utilizing small bridges. Therefore bridges employing double vias are an effective solution. It should be pointed out that double via bridges imply cost, by reducing the number tracks available for routing.

[0131] An alternative solution could be employed for volume production. It suggests that in addition to the custom via layer, the two metal layers could use custom mask that connect the segments **153**, **155** with the same metal layer **156**.

[0132] For volume production additional yield enhancement technique could be employed. For example, a software routine can inspect the custom design and replace any single via with a double via where possible. Having most of the patterns in an array form with a highly repetitive structure make it very friendly to employment of yield enhancements. It is possible to keep track of yield loss in production of specific designs that utilize the same logic array fabric. Any failure mechanism could then be reviewed for yield enhancement. The yield enhancement may involve changing the layout of the generic logic array and therefore replacing some of the generic masks.

[0133] Reference is now made to **FIGS. 16, 17, and 18** which illustrate another preferred embodiment of the current invention. These figures illustrate via-configurable I/O. Preferably the area I/O of the borderless logic array is configurable I/O. It is advantageous to many users to have flexibility of the I/O configuration, in addition to having flexibility of the logic. It is the purpose of this invention to utilize the same custom mask to configure both the core logic and the I/O. **FIG. 16** illustrates a simple via-configurable I/O **160**, where the potential via are marked by a circle **162**. Few vias are arranged to connect a line used as a jumper, and mark such as J4 **164** to the crossing line, preferably underneath **166** or **167** or **168**. Different types of

I/Os could be constructed by selecting some of the potential vias. FIG. 17 presents a configuration of the configurable I/O of FIG. 16 as an input cell 170. The selected vias are marked by black filled circle 172. FIG. 18 presents an alternative configuration as output cell 180.

[0134] FIG. 19 is a layout drawing illustration of via customizable I/O 190. The I/O comprises the main elements pads 192, high drive I/O section 194 and the I/O logic section 196 comprising the pre-I/O circuits.

[0135] FIG. 20 is a layout drawing illustration of a small section of the via customizable I/O. Illustrating a jumper 202 with via activated 204 and via not activated 206

[0136] In another embodiment I/O may be comprised of many input 163, output 165 or pre-output 161 cells such that most I/O types could be constructed by interconnecting to one or more of these cells by providing additional segments between cells for via programming. It is further contemplated that many more I/O cells 26 exist in each repeating core 28, FIG. 2, than area pads in each repeating core, to allow flexible programming of each repeating core's I/O pads.

[0137] In another embodiment of this current invention additional routing channels, called very long tracks, are introduced. Reference is now made to FIG. 21. FIG. 21 is a drawing illustration of very long tracks 212, 214 across a module 210. The very long tracks could go under or over the local routing fabric 150 to allow segmented routing of more than 4 metal layers. When many modules are tiled together to construct array of logic with over million gates, more than 4 layers of routing might be required. The current invention suggests the use of very long tracks in addition to the short tracks and long tracks described in U.S. Pat. No. 6,331,733. The very long tracks would have very few, or even no, contact within the module. The router software could assign the very long tracks to route between logic cells that are very far apart. At every end point or contact point of the very long track, short routing tracks would be used to connect it to the 4-metal routing fabric. This approach allows extension of the segmented routing architecture to as many metal layers as the fabrication process supports. It is further contemplated that very long tracks will include jumpers 154, an example of which is shown in FIG. 15, between each repeating core, to allow for scribing between repeating cores while maintaining reliable use of all segments. In addition, it is contemplated that some of these long lines may be used for power and ground distribution across modules within target dies.

[0138] In another embodiment of the current invention a "scramble box" is proposed for the routing connection between modules 190. The objective of such "scramble box" is to reduce cross talk between lines. By having such "scramble box" be part of the generic fabric the solution is provided in the fabric rather than by careful design of the customization layers. Preferably such a "scramble box" would include buffers to further simplify the customization. Reference is now made to FIG. 22. FIG. 22 is a drawing illustration of a configurable buffer structure. Numeral 220 illustrates a via configurable buffer structure. It includes a buffer 229 that has in the lower layers two Metal 7 jumpers 225, 226 and four Metal 6 connection lines. By selecting two or four vias the structure could be configured for:

[0139] (1) Buffer line 222 to line 224;

[0140] (2) Buffer line 224 to line 222;

[0141] (3) Connect line 222 with line 224 with no buffer and tie off the buffer;

[0142] (4) Leave lines 222 and 224 unconnected and tie off the buffer.

[0143] FIG. 23 is a drawing illustration of a simple "scramble box" in which four lines are coming into the "scramble box" 230 to one side 232 and coming out from the other side 234; each line is now next to a new line.

[0144] FIG. 24 is a drawing illustration of a "scramble box" layout. The four-lines "scramble box" 240 includes a configurable buffer structure 242.

[0145] FIG. 25 is a drawing illustration of a "scramble box" layout for 24 lines 250. It comprises six repetitions of the structure 240.

[0146] It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and sub-combinations of various features described hereinabove as well as modifications and variations which would occur to persons skilled in the art upon reading the foregoing description and which are not in the prior art.

1.-10. (canceled)

11. A method of fabricating a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and

forming a redistribution layer for redistributing at least some of said area I/Os.

12. A method according to claim 11 and also comprising the step of:

forming pads to connect said semiconductor device to other devices, wherein at least one of said pads overlays at least a portion of said logic array or a portion of the area I/Os.

13. A method according to claim 11 and also comprising the steps of:

placing and routing a specific design on said logic array; and

marking marks for an edge of a used portion of said logic array according to the step of placing and routing.

14. A method according to claim 13 and wherein said step of marking comprises photolithography, and also comprising a step of dicing said semiconductor substrate according to said marks.

15. A method according to claim 14 and wherein said step of dicing comprises laser dicing.

16. A method according to claim 11, further comprising the step of forming a memory array.

17. A method according to claim 16 and also comprising the steps of:

placing and routing a specific design on said logic array and said memory array; and

marking marks for an edge of a used portion of said logic array and said memory array according to the step of placing and routing.

18. A method according to claim 17 and wherein said step of marking comprises photolithography, and also comprising a step of dicing said semiconductor substrate according to said marks.

19. A method according to claim 18 and wherein said step of dicing comprises laser dicing.

20. A method according to claim 11 and wherein said logic array comprises a module array.

21. A method according to claim 16 and wherein said logic array comprises a module array.

22. A method according to claim 11, wherein said logic array is interconnected by metal layers and via layers, and wherein at least one of said metal layers comprises at least one substantially repeating pattern for a portion used for interconnecting.

23.-24. (canceled)

25. A method according to claim 11, further comprising the step of utilizing a direct write technique to customize said logic array.

26.-27. (canceled)

28. A method according to claim 11 and wherein said logic array comprises a repeating core, and wherein the step of forming a borderless logic array comprises the step of positioning said area I/Os in a non-surrounding fashion with respect to at least one of said repeating core.

29. A method according to claim 11, wherein said logic array comprises a repeating core, and wherein the step of forming a borderless logic array comprises the step of positioning said area I/Os within said core and wherein at least one of said area I/O is configurable I/O.

30.-55. (canceled)

56. A method of fabricating a semiconductor device with improved yield, comprising the method of claim 11, and further comprising the steps of:

testing and marking modules on said logic array;

placing specific designs on said logic array so as to avoid faulty modules;

customizing said logic array according to placement of specific designs;

testing and marking said specific designs; and

dicing said logic array according to placement and marking of specific designs.

57. A method according to claim 56, further comprising the step of utilizing a direct write technique to customize said logic array.

58.-62. (canceled)

63. A method of fabricating a semiconductor device, comprising:

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate, wherein said logic array comprises a repeating core, and wherein at least one of said area I/Os is a configurable I/O, said configurable I/O comprising at least one metal layer that is the same for the various I/O configurations.

64. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate; and

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate, wherein said logic array comprises configurable logic, and wherein said configurable logic comprises at least one metal layer that is the same for multiple logic configurations to which the configurable logic may be configured.

65. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate; and

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate, wherein said logic array comprises a configurable memory array, and wherein said configurable memory array comprises at least one metal layer that is the same for multiple memory array configurations to which the configurable memory array may be configured.

66. A method of fabricating a customizable semiconductor device, comprising:

providing a semiconductor substrate;

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and

utilizing a direct write technique to customize said semiconductor device.

67. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate;

forming a borderless logic array, including a plurality of area I/Os, on the semiconductor substrate; and

creating marks to guide a dicing process.

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