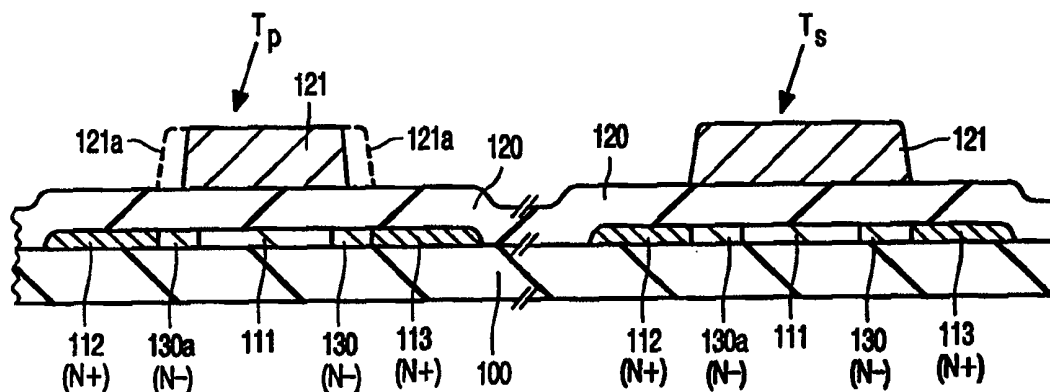




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(54) Title: ELECTRONIC DEVICES COMPRISING THIN-FILM TRANSISTORS



(57) Abstract

A large-area electronic device, such as an AMLCD, has switching TFTs (T_p) in a matrix and circuit TFTs (T_s) in a peripheral drive circuit. Both the TFTs (T_p , T_s) comprise a field-relief region (130) which has a lower doping concentration (N⁻) than their drain region (113) and which is present between their channel region (111) and the drain region (113). This field-relief region (130), at least over most of its length, overlaps with the gate (121) in the circuit TFTs (T_s) so as to reduce series resistance in the field-relief region (130) by conductivity modulation with the gate (121). However, the drain region (113) in the switching TFTs (T_p) is offset from overlap with their gate (121) by at least most of the length of their field-relief region (130). This field-relief offset permits the switching TFTs (T_p) to have a lower leakage current than the circuit TFTs (T_s).

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DESCRIPTION

ELECTRONIC DEVICES COMPRISING THIN-FILM TRANSISTORS.

5 This invention relates to electronic devices including thin-film transistors (hereinafter termed "TFTs") on a substrate, for example a glass or insulating polymer substrate. The device may be, for example, an active-matrix liquid-crystal display or other flat panel display, or any other type of large area electronic device with TFTs in a matrix and in a drive circuit, for example, a thin-
10 film data store or an image sensor. The invention also relates to methods of manufacturing such an electronic device.

 For many years there has been much interest in developing thin-film circuits with TFTs on glass and/or on other inexpensive insulating substrates, for large area electronics applications. Such TFTs fabricated with amorphous or
15 polycrystalline semiconductor films may form the switching elements of a cell matrix, for example, in a flat panel display as described in United States Patent US-A-5,130,829 (Our Ref: PHB 33646). A more recent development involves the fabrication and integration of circuits from TFTs (often using polycrystalline silicon) as, for example, integrated drive circuits for such a cell matrix. Thus, for
20 example, published European Patent Application EP-A-0 629 003 (corresponding United States Patent Application 08/639277: Our Ref: PHB 33845) describes such an electronic device comprising on a substrate a switching matrix of thin-film switching transistors and a peripheral drive circuit located outside the matrix and comprising thin-film circuit transistors which are
25 coupled to the switching TFTs of the matrix. The whole contents of US-A-5,130,829 and EP-A-0 629 003 are hereby incorporated herein as reference material.

 Unfortunately, undesirable field-induced effects occur in the transistor characteristics of such TFTs, especially those fabricated with polycrystalline
30 silicon formed using low temperature processes. Several instability mechanisms occur, for example, bias-induced state creation in the

polycrystalline silicon, and hot carrier induced state creation and carrier trapping. Another effect which occurs is a drain field-enhanced increase in leakage current. The degradation of the transistor characteristics (for example, off-state leakage current, threshold voltage and on-state current) can seriously limit the use of such TFTs in such circuits.

One way of reducing such effects in TFTs is by means of a field-relief region having a lower doping concentration of the one conductivity type than the drain region. The TFT comprises an insulated gate adjacent to a crystalline semiconductor film for controlling a conduction channel of one conductivity type in the semiconductor film between source and drain regions of the one conductivity type. The field relief region is present between the conduction channel and drain region of the TFT.

The article "Characteristics of Offset-Structure Polycrystalline-Silicon Thin-Film Transistors" by K. Tanaka et al. in IEEE Electron Devices Letters Vol.9 No.1, January 1988, describes one form of such a TFT wherein the drain region is offset from the gate by at least most of the field relief region. The resulting TFT has a reduced leakage current, as compared with a non-offset TFT structure without any field-relief region. The paper WS3/1 "Influence of Drain Field on Poly-Si TFT Behaviour" by J. R. Ayres et al. in the Proceedings of the Active Matrix Workshop (published by SID -The Society for Information Display) held with the 16th International Display Research Conference, Birmingham England, 30 September 1996, discloses another form wherein at least most of the field relief region overlaps with the gate. The whole contents of this article and this paper are hereby incorporated herein as reference material.

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It is an aim of the present invention to optimise (or at least to improve) the TFT operating characteristics in both the switching matrix and peripheral drive circuit of such flat panel displays and other electronic devices.

According to the present invention there is provided an electronic device as set out in Claim 1. In this device at least most of the field relief region overlaps with the gate in at least some of the circuit TFTs of the peripheral drive

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circuit, so as to reduce series resistance in their field relief region by conductivity modulation with the gate; whereas the drain region in the switching TFTs of the matrix is offset from overlap with the gate by at least most of their field relief region so as to provide the switching TFTs with a lower leakage current than the circuit TFTs with gate overlap. This advantageous mixture of gate-overlap and gate-offset TFTs with field relief regions permits the switching TFTs of the matrix to provide a low leakage for pixels (or other matrix cell types) in the off-state and to be stable at high drain bias, while permitting circuit TFTs of the drive circuit to have low series resistance in the on-state and to be stable at high drain bias.

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10 The gate-overlap TFT structure with low series resistance is particularly advantageous for circuit TFTs which transmit analog signals, for example sampling TFTs in sample-and-hold functions in the drive circuit.

Furthermore, the circuit TFTs of the peripheral drive circuit and the switching TFTs of the matrix may be fabricated using the same process steps and masks, at least when the regions of one type or both types of the TFTs are not defined in a self-aligned manner with respect to their gates. Different element layout geometries for (for example) the gate mask pattern and/or doping pattern can be used in the matrix area (to provide the gate-offset TFTs), as compared with the peripheral drive circuit area (to provide gate-overlap TFTs). Thus, for example, the source and drain regions of the gate-offset switching TFTs may have the same doping concentration as the source and drain regions of the circuit TFTs with gate overlap. The field relief regions of the gate-offset switching TFTs (when not self aligned with their gate) may, for example, have the same doping concentration as the field relief regions of the circuit TFTs with gate overlap. Some of the TFTs fabricated in the peripheral drive circuit (for example using the same process steps and masks) may be provided without gate overlap and/or without a field relief region when these features are not needed nor desirable in terms of the circuit functions of these particular circuit TFTs.

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30 The TFTs of the peripheral drive circuit and of the switching matrix may be fabricated using known technologies and process steps. Thus, for example,

the TFTs may be both of top-gate configuration or of bottom-gate configuration. The source and drain regions and field-relief region may be doped regions of the one conductivity type present in the semiconductor film, and/or they may be doped regions of one or more additional semiconductor films adjacent to the said semiconductor film. Gate-aligned processes may be used in order to reduce parasitic effects. Thus, for example, at least some of the circuit TFTs may have their field relief region substantially entirely overlapping with the gate, and the gate of these TFTs and/or of other circuit TFTs may have an edge which is substantially aligned with an edge of the drain region.

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These and other features of the present invention, and their advantages, are illustrated specifically in embodiments of the invention now to be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

15 Figure 1 is a circuit diagram (partly in block form) of a large area electronic device (such as a flat panel display) comprising on a substrate a switching matrix and a peripheral drive circuit;

Figure 2 is a circuit diagram of a sample-and-hold circuit in the drive circuit of the device of Figure 1;

20 Figures 3 to 6 are cross-sectional views of a variety of TFT structures which may be used in such a device in accordance with the invention, in which the left-hand section of each drawing relates to the switching matrix and the right-hand section relates to the peripheral drive circuit;

Figure 7 is a typical comparative plot of drain current I_D against gate voltage V_g , for gate-offset field-relief TFTs (curve A) of the switching matrix and gate-overlap field-relief TFTs (curve B) of the peripheral drive circuit; and

Figure 8 is a cross-sectional view of another type of TFT structure which may be used in a part of the peripheral drive circuit of Figure 1, for example together with the Figure 4 matrix and circuit TFTs in a device in accordance with the invention.

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It should be noted that the drawings are diagrammatic. Relative

dimensions and proportions of parts of the cross-section views and circuit layout have been shown exaggerated or reduced in size for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in the different embodiments.

5

Apart from the formation of its switching and circuit TFTs in accordance with the present invention, the electronic device may be of known type and construction. Thus, by way of a specific example, The device illustrated in Figures 1 and 2 may be similar to the active matrix liquid crystal display (AMLCD) panel of EP-A-0 629 003. Indeed these Figures are derived from Figures 1 and 2 of EP-A-0 629 003, corresponding and similar features being indicated by the same reference signs as in EP-A-0 629 003. Thus, only a brief overview of this device is now given before focusing on specific characteristic features of the present invention, and the reader is directed to the disclosure in EP-A-0 629 003 (and the background in US-A-5,130,829) for more details of this type of device.

In the Figure 1 device an electrically insulating substrate 100 carries a switching matrix 22 of switching TFTs T_p and also carries peripheral drive circuits 12,21 which are located outside the matrix 22 and which comprise switching TFTs, for example T_s and T_2 which are coupled directly or indirectly to the switching TFTs T_p of the matrix. In the present description and drawings, the switching TFTs are designated T_p , rather than 29 as in EP-A-0 629 003. The matrix 22 comprises cells 33 (for example, pixel cells of a liquid-crystal display) organised in rows and columns. The substrate 100 may be, for example, a glass back panel of the display. The matrix 22 has thin-film row lines 24 connected to a row drive circuit 21 for addressing rows of the matrix 22. The matrix 22 also has thin film column lines 26 connected to a column drive circuit 12 for supplying sampled signals to cells 33 in the addressed row. These lines 24 and 26 and drive circuits 12 and 21 are integrated in thin-film technology on the same substrate 100 as the matrix 22.

Figures 3 to 6 illustrate specific examples of thin-film transistor structures

for the switching TFTs T_p of the matrix 22 and for the circuit TFTs T_s of the drive circuit 12. The TFTs T_p and T_s each comprise an insulated gate 121 adjacent to a transistor body 110 of a crystalline semiconductor film. The semiconductor film is typically of polycrystalline silicon. The gate 121 is coupled to the body
5 110 across a gate dielectric film 120 so as to control a conduction channel of one conductivity type in a region 111 of the semiconductor film between source and drain regions 112 and 113, respectively, also of the one conductivity type. Typically the TFTs T_p and T_s are N-channel, the source and drain regions 112 and 113 being of the N-type conductivity. Typically the polysilicon film may have
10 a thickness of about 40 nm and has no deliberate doping in the region 111. The region 111 is effectively intrinsic in conductivity or very slightly n-type in some polycrystalline forms. Its conductivity state is determined by the high density of trapping states in the polycrystalline film. These trapping states result in the Fermi level being pinned near the middle of the energy band gap. The source
15 and drain regions 112 and 113 are highly doped with, for example, phosphorus or arsenic, and so are designated N+ in Figures 3 to 6. Typically the doping level in the source and drain regions 112 and 113 may be, for example, 10^{16} cm^{-2} or more.

Both the TFTs T_p and T_s also comprise a field-relief region 130 which has
20 a lower doping concentration (designated N-) of the one conductivity type than the drain region 113 and which is present between the channel region 111 and the drain region 113. Typically the doping level of the field-relief region 130 is less than $5 \times 10^{13} \text{ cm}^{-2}$, and may be of the order of 10^{12} cm^{-2} . In accordance with the present invention, the field-relief region 130 (at least over most of its length)
25 overlaps with the gate 121 in the circuit TFTs T_s so as to reduce series resistance in the field-relief region 130 by conductivity modulation with the gate 121, whereas the drain region 113 in the switching TFTs T_p is offset from overlap with their gate 121 by at least most of the length of their field-relief region 130. The field-relief offset in accordance with the present invention
30 permits these switching TFTs T_p to have a lower leakage current than the circuit TFTs T_s .

In this description, the expression "gate-overlap TFTs" is used for TFTs in which at least most of the field-relief region 130 overlaps with the gate 121, whereas the expression "gate-offset TFTs" is used for TFTs in which the drain region 113 is offset from overlap with the gate 121 by the field-relief region 130.

5 The optimum length of the field-relief region 130 for both the gate-offset TFTs T_p and the gate-overlap TFTs T_s depends, inter alia, on the length of the channel region 111, the gate and maximum drain operating voltages, the current levels through the TFT, and whether various regions are formed with self-aligned techniques. In a typical specific example, the length of the field-relief region 130 may be in the range of about $1\mu\text{m}$ (micrometre) to $3\mu\text{m}$ in TFTs T_p and T_s which are fabricated with present day technology for an AMLCD and which have a length in the range of $5\mu\text{m}$ to $10\mu\text{m}$ for their channel region 111. When regions are self-aligned with the gate, then the length of the field-relief region may be typically about $1\mu\text{m}$ or less. The source and drain regions 112 and 112 of the gate-offset switching TFTs T_p may have the same doping concentration as the source and drain regions of the gate-overlap circuit TFTs T_s . The field-relief regions of the gate-offset switching TFTs T_p may also have the same doping concentration (or at least the same order of magnitude) as the field-relief regions of the gate-overlap circuit TFTs T_s .

20 The drive circuit 12 for the column lines 26 comprises a shift register 13 which addresses sequentially individual sample-and-hold circuits 10 for each column line 26. The present invention permits the provision of a high performance individual sample-and-hold circuit 10 for each column line 26, by constructing the circuit 10 with gate-overlap TFTs T_s and T_2 . Depending upon 25 the capacitance of the column line 26, each circuit 10 may include a discrete storage capacitor C_s (as illustrated in Figure 2) or the capacitance of the line 26 itself may provide the charge-storage means of the sample-and-hold circuit 10. Figure 2 shows the same circuit configuration for the circuit 10 as in EP-A-0 629 003. Thus, the circuit 10 may additionally comprise a compensating TFT T_2 which is of a similar TFT structure to the sampling transistor T_s . These TFTs T_s and T_2 may each additionally comprise a minority-carrier injector 119 in 30

accordance with the teaching in EP-A-0 629 003. However, the circuit 10 may be constructed without the compensating TFT T_2 ; and instead of incorporating such an injector 119, a similar effect can be achieved by coupling a P-channel TFT in parallel with this N-channel TFT T_S . No injector 119 (and no compensating TFT T_2) is shown in Figures 3 to 6.

Figure 7 shows typical comparative characteristics for a gate-offset TFT (curve A) and a gate-overlap TFT (curve B) in both the on-state and the off-state. In the on-state (positive V_g for N-channel TFTs) the gate-overlap TFT has a lower series resistance and so passes a higher drain current for a given gate voltage value V_g . Thus, a gate-overlap TFT structure (instead of a gate-offset TFT structure) is beneficial for the transmission TFTs T_S (and T_2) in the circuit 10 for fast charging of the capacitor C_S to the analog video input signal. In the off-state (negative V_g for N-channel TFTs), the gate-offset TFT has a lower leakage current as shown by curve A. Thus, the use of a gate-offset TFT structure (instead of a gate-overlap TFT structure) is beneficial for the pixel switching TFTs T_P of the matrix 22. The magnitude of the different values of on-state current and leakage current for curves A and B depends on the particular TFT configurations (Figures 3 to 6) adopted for T_P and T_S and on their region dimensions. By way of example, the difference in on-state current between curves A and B may be a factor of two, for example at V_g of +15 volts, whereas the difference in the field-induced increase of leakage current between curves A and B may be an order of magnitude (i.e. a factor of ten, or more), for example at V_g of -10 volts. The Applicants find that the series resistance of the gate-offset field-relief region 130 is not a significant problem for the switching TFTs T_P of the matrix 22, but it would be a problem for the transmission TFTs T_S of the circuit 10. Both the gate-offset TFTs T_P and the gate-overlap TFTs T_S have good stability at high drain bias, due to the presence of their respective field-relief regions 130.

Both the gate-offset TFT T_P and the gate-overlap TFT T_S may be fabricated using many common process steps and masks, but with different element layout geometries. Known technologies and processes may be used.

Thus, for example, both Figures 3 and 4 illustrate top-gate configurations for the TFTs T_p and T_s . In this case the gate 121 of both TFTs T_p and T_s is provided on a gate-dielectric film 120 on the semiconductor film of the transistor body 110.

5 Figure 3 illustrates an embodiment in which there is a slight overlap between the gate 121 of T_s and its source and drain regions 112 and 113 and a slight overlap between the gate 121 of T_p and its source 112 and field-relief region 130. Thus, these TFTs do not have a self-aligned structure. In this case, the source and drain regions 112 and 113 and the respective field-relief regions
10 130 can be implanted in the semiconductor film of the transistor body 110, before the insulated gate structure 120,121 is provided on the semiconductor film.

 Figure 4 illustrates a modified embodiment with symmetrical TFT structures, each of which has similar low-doped regions at both its source and
15 drain ends of the channel region 111. Thus, in the Figure 4 embodiment, additional field-relief regions 130a are present between the source region 112 and channel region 111 of each TFT T_p and T_s . In this case the gate-overlap TFT T_s has symmetrical characteristics between its source and drain, and so too does the gate-offset TFT T_p . The TFTs T_s have their field-relief region 130
20 substantially entirely overlapping with the gate 121, and the gate 121 has an edge substantially aligned with an edge of the drain region 113. This TFT structure for T_s has a reduced gate-drain capacitance. The gate-source capacitance is also reduced by the edge of the source region 112 being substantially aligned with the edge of the gate 121. A similar self-aligned
25 structure is first formed for the TFT T_p of Figure 4, except in this case the field-relief regions 130 and 130a have their source and drain edges subsequently offset from the edges of the gate 121 by etching back these edges of the gate 121 (as illustrated by the broken outline 121a in in Figure 4). This etch back can be carried out while masking the matrix 22.

30 Figure 5 illustrates a symmetrical TFT arrangement, but in a bottom-gate configuration for the TFTs T_p and T_s . In this case, the semiconductor film which

provides the transistor body 110 is present on a gate-dielectric film 120 which extends over the gate 121 on the substrate 100. In the Figure 5 embodiment, the field-relief regions 130 and 130a and the source and drain regions 112 and 113 of each TFT T_p and T_s are implanted in the semiconductor film deposited on the insulated gate structure 120, 121.

In the embodiments of Figures 3 to 5 the source and drain regions 112 and 113 and field-relief region 130 are doped regions of one conductivity type present in the same semiconductor film. Figure 6 illustrates an embodiment in which the source and drain regions 112 and 113 and the field relief region 130 are doped regions of additional semiconductor films adjacent to the semiconductor film which provides the channel region 111. By way of example, this multiple semiconductor film embodiment is shown as a modification of the bottom-gate configuration of Figure 5. In this example the field-relief regions 130 (and 130a) are formed from a lightly doped N-type semiconductor film deposited on the undoped semiconductor film which provides the channel region 111. The source and drain regions 112 and 113 are formed from a highly doped N-type semiconductor film which is deposited on the lightly doped film. The lateral extent of the source and drain regions 112 and 113 and the field-relief regions 130 (and 130a) are defined using known photolithographic and etching techniques.

The gate-overlap TFT structures illustrated in Figures 3 to 6 are particularly advantageous for transistors such as T_s and T_2 which transmit analog signals in the drive circuit. Most of the TFTs of other parts 13, 20 and 23 of the peripheral drive circuits are digital switching transistors. These other TFTs may be fabricated with a gate-overlap structure similar to that of T_s or even (if series resistance is less problematic) a gate-offset structure similar to that of T_p for some of these other circuit TFTs. Furthermore the transistor structure T13 of Figure 8 may be used for circuit TFTs requiring only a low voltage operation. The TFT T13 of Figure 8 has no field-relief region 130, and its source and drain regions 112 and 113 have their channel edges aligned with the edges of the gate 121, so providing a fast switching characteristic. Figure 8

illustrates an N-channel TFT structure compatible with the TFT structures of Figure 4. The circuit blocks 13, 20 and 23 may be formed entirely with N-channel TFTs, or they may be formed with complementary P-channel and N-channel TFTs.

5 In the switching TFT T_p of Figure 4, the regions 130a and 130 are formed in the same doping step as the regions 130a and 130 of the circuit TFT T_s . However, the regions 130 (and optional regions 130a) of switching TFTs T_p may be formed in a later doping step from the regions 130 (and optional regions 130a) of the circuit TFT T_s . Thus, for example, the regions 130 of TFTs T_s may first be implanted, and then the source and drain regions of both TFTs T_s and T_p may be implanted using the gate electrodes 121 as masks so as to be self-aligned with the gate electrodes 121. The gate electrodes 121 of TFTs T_p can then be etched back (for example as in Figure 4), and then the regions 130 and 130a of these TFTs T_p can be implanted using their gate electrodes 121 as
10 masks so as to be self-aligned with the gate electrodes 121.
15

Figure 1 illustrates a flat panel display. The present invention may be employed with other matrix devices which are designed for a quite different function, for example a data store having a matrix of TFTs T_p for addressing an array of thin-film data storage elements (for example thin-film capacitors or
20 memory-type TFTs). In this different type of device in accordance with the present invention, the matrix TFTs T_p have a gate-offset field-relief structure whereas at least some of the circuit TFTs T_s have a gate-overlap field-relief structure, for example with TFT structures as in Figures 3 to 6. Such gate-offset and gate-overlap TFT structures may be used in accordance with the present
25 invention in another form of matrix device, for example an image sensor having a matrix 22 of cells 33 each comprising a thin-film image-sensing element (for example a photodiode) addressed by a gate-offset TFT T_p via row lines 24. The TFTs T_p (which switch each imaging pixel 33) may have a transistor structure as illustrated in the left hand section of Figures 3 to 6. The photodiode signal may
30 be output to peripheral sensing circuitry 13' of the image sensor, via a sample-and-hold circuit 10' which acts as an integrator for a signal. Such a circuit 10' for

an image sensor may be constructed with a gate-overlap TFT T_s , for example as illustrated in the right hand sections of Figures 3 to 6.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications
5 may involve equivalent and other features which are already known in the design, manufacture and use of electronic devices comprising TFTs and other semiconductor devices and component parts thereof and which may be used instead of or in addition to features already described herein.

Although Claims have been formulated in this Application to particular
10 combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the
15 same technical problems as does the present invention. Although the dependency of subsidiary Claims has been limited in the interests of meeting the requirements and reducing the fees for multiple-Claim-dependency in some countries, it should be understood that technical features included in any one Claim may be used in combination with technical features of any one of the
20 other Claims. Particularly, but not exclusively, the following combinations are potentially important: features of Claim 4 may be used in combination with any one of the Claims 1 to 3; and features of Claims 7, 8 and 9 may be used in combination with any one of the Claims dependent on Claim 1.

The Applicants hereby give notice that new Claims may be formulated
25 to any such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. An electronic device comprising on a substrate a switching matrix of thin-film switching transistors and a peripheral drive circuit comprising thin-film circuit transistors which are coupled to the switching transistors of the matrix, wherein the thin-film switching transistors and circuit transistors both comprise an insulated gate adjacent to a crystalline semiconductor film for controlling a conduction channel of one conductivity type in the semiconductor film between source and drain regions of the one conductivity type, a field-relief region having a lower doping concentration of the one conductivity type than the drain region being present between the conduction channel and the drain region, and wherein at least most of the field relief region overlaps with the gate in at least some of the circuit transistors so as to reduce series resistance in the field relief region by conductivity modulation with the gate, and wherein the drain region in the switching transistors of the matrix is offset from overlap with the gate by at least most of the field relief region so as to provide the switching transistors with a lower leakage current than the circuit transistors with gate overlap.

2. A device as claimed in Claim 1, wherein the thin-film switching transistors and circuit transistors are both of top-gate configuration having their gate on a gate-dielectric film on the said semiconductor film.

3. A device as claimed in Claim 1, wherein the thin-film switching transistors and circuit transistors are both of bottom-gate configuration having their semiconductor film on a gate-dielectric film which is present over the gate on the substrate.

4. A device as claimed in Claim 1, wherein the source and drain regions of the switching transistors have the same doping concentration as the source and drain regions of the circuit transistors with gate overlap.

5. A device as claimed in Claim 4, wherein the source and drain regions and field-relief region are doped regions of the one conductivity type present in the semiconductor film.

5 6. A device as claimed in Claim 4, wherein the source and drain regions and field-relief region are doped regions of one or more additional semiconductor films adjacent to the said semiconductor film.

7. A device as claimed in Claim 4, wherein the field relief regions of
10 the switching transistors have the same doping concentration as the field relief regions of the circuit transistors with gate overlap.

8. A device as claimed in Claim 1, wherein at least some of the circuit transistors have their field relief region substantially entirely overlapping
15 with the gate which has an edge substantially aligned with an edge of the drain region.

9. A device as claimed in Claim 1, wherein at least some of the circuit transistors with gate overlap are transmitting transistors which transmit
20 analog signals in the drive circuit.

10. A device as claimed in Claim 9, wherein at least some of the transmitting transistors with gate overlap are sampling transistors in sample-and-hold circuits and have charge-storage means coupled to their drain region
25 for storing the analog signals.

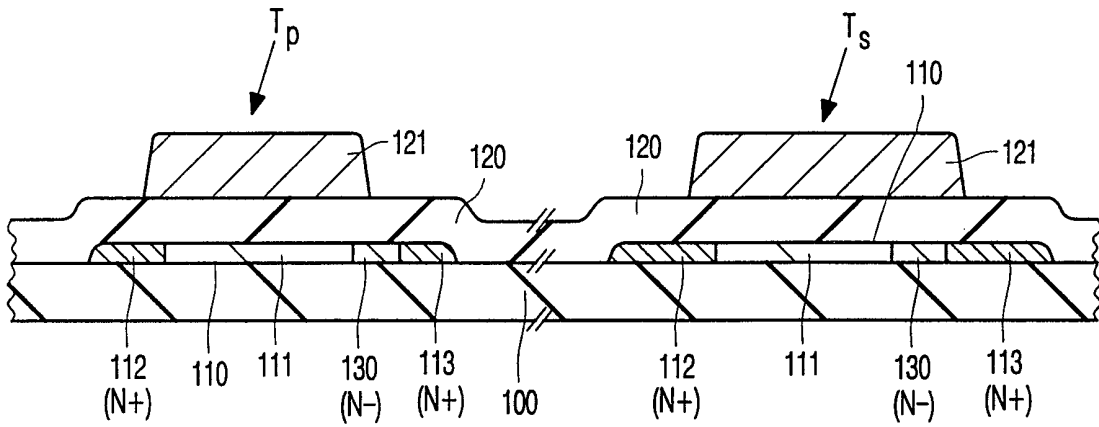


FIG. 3

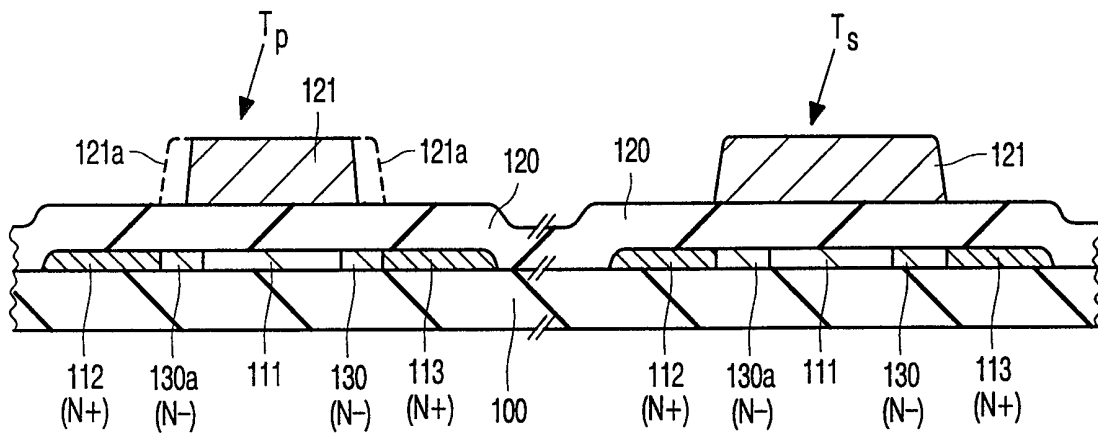


FIG. 4

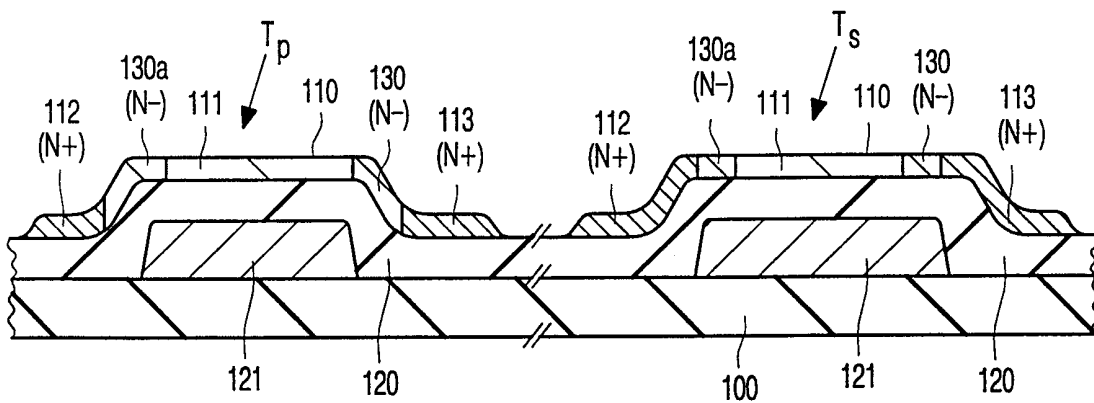


FIG. 5

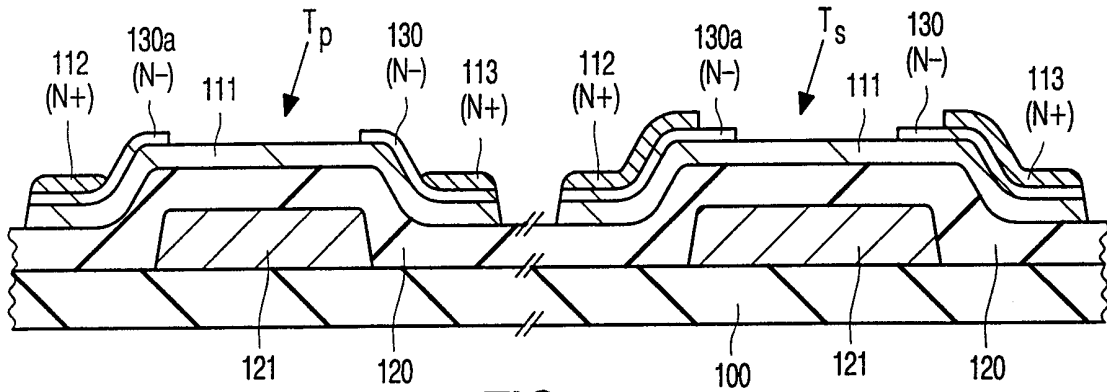


FIG. 6

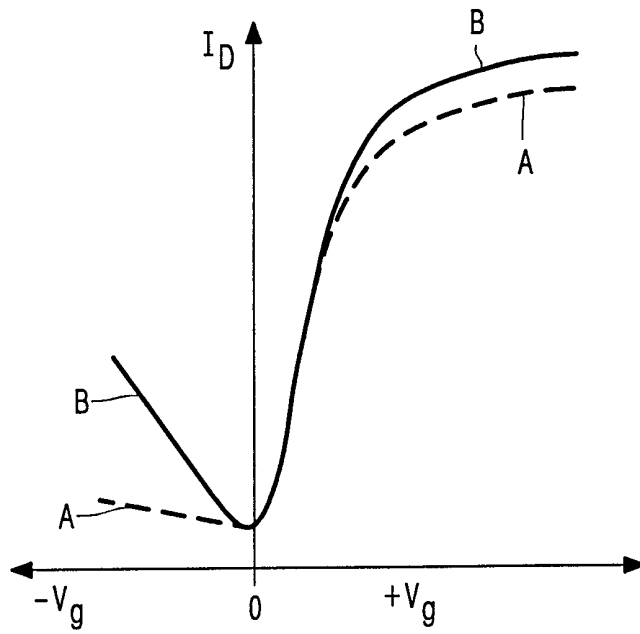


FIG. 7

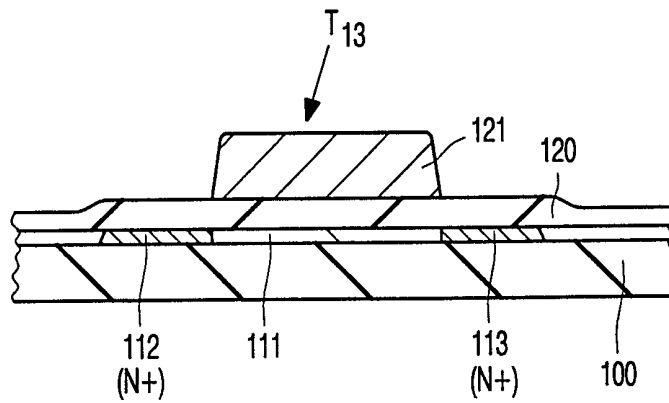


FIG. 8