

United States Patent

[11] 3,615,949

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 [73] Assignee **The United States of America as**
represented by the Secretary of the Navy

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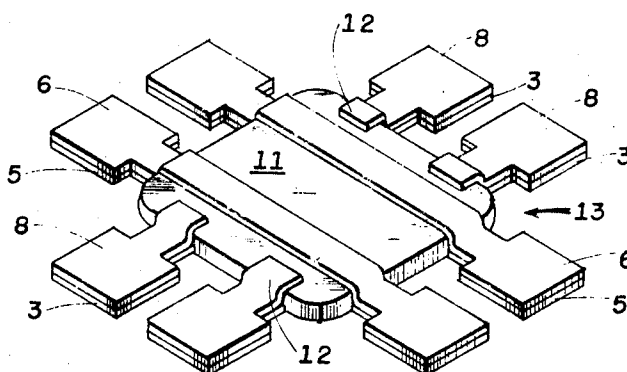
[54] CROSSOVER FOR LARGE SCALE ARRAYS 6 Claims, 10 Drawing Figs.

[52] U.S. Cl..... **156/3,**
156/17, 29/625, 117/217, 317/101, 174/68.5
 [51] Int. Cl..... **H05k 1/00,**
H05k 3/06
 [50] Field of Search..... **156/3, 17;**
29/625; 174/68.5; 117/217; 317/101 CX

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ABSTRACT: The subject invention relates to a method for providing crossovers in microelectronic circuitry. More particularly, the subject invention contemplates the fabrication of crossovers by deposition of insulative material on a conductor at the point of crossover and subsequent deposition of a crossing conductor over the insulative "bridge." Additional advantages other than the elimination of point-to-point wiring methods include improved circuit reliability; room temperature circuit assembly; decreased manufacturing time; increased unit density; "flip-chip" utilization; and reduction of stray capacitance.



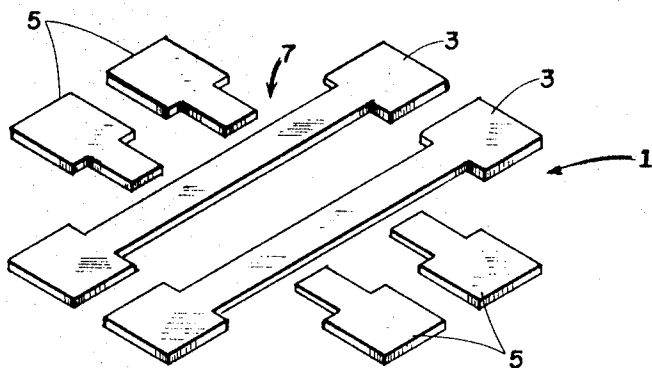


FIG. 1

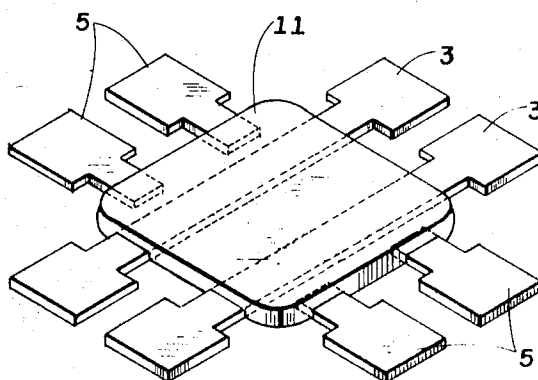


FIG. 2

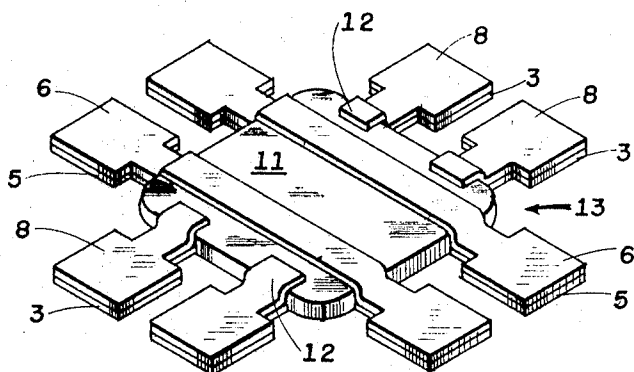


FIG. 3

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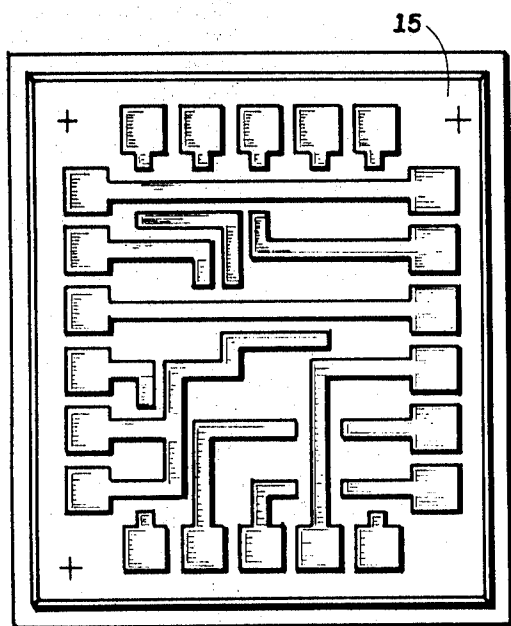


FIG. 4a

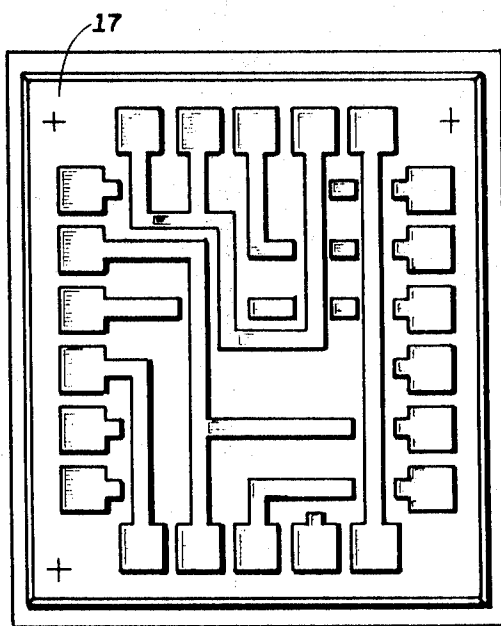


FIG. 4b

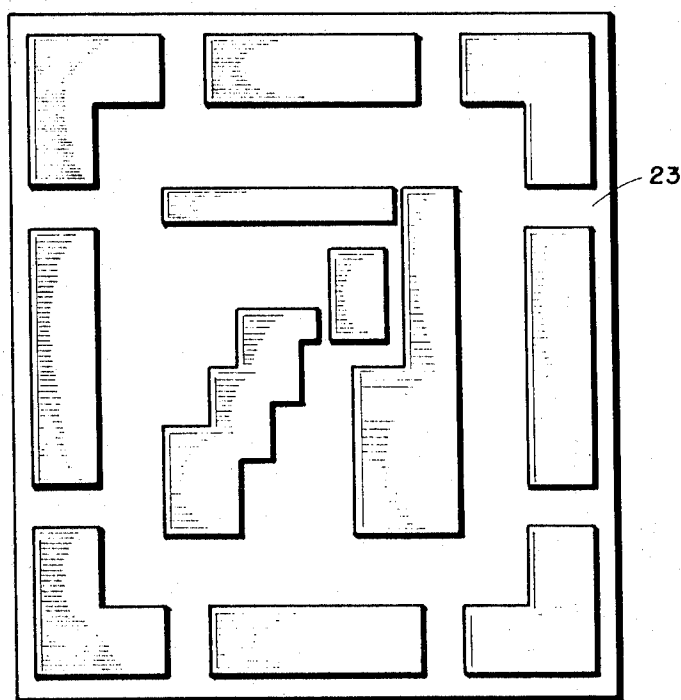


FIG. 5

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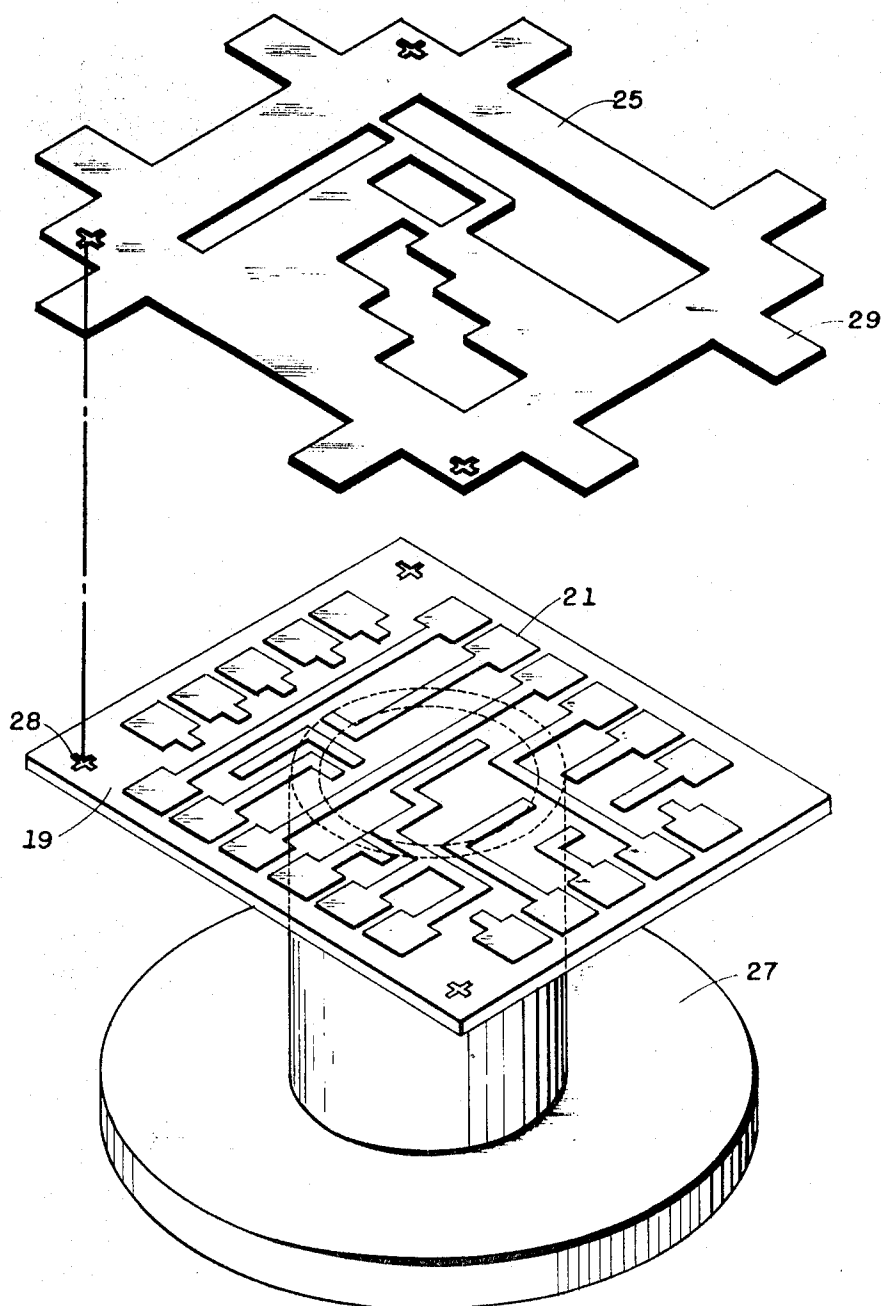


FIG. 6

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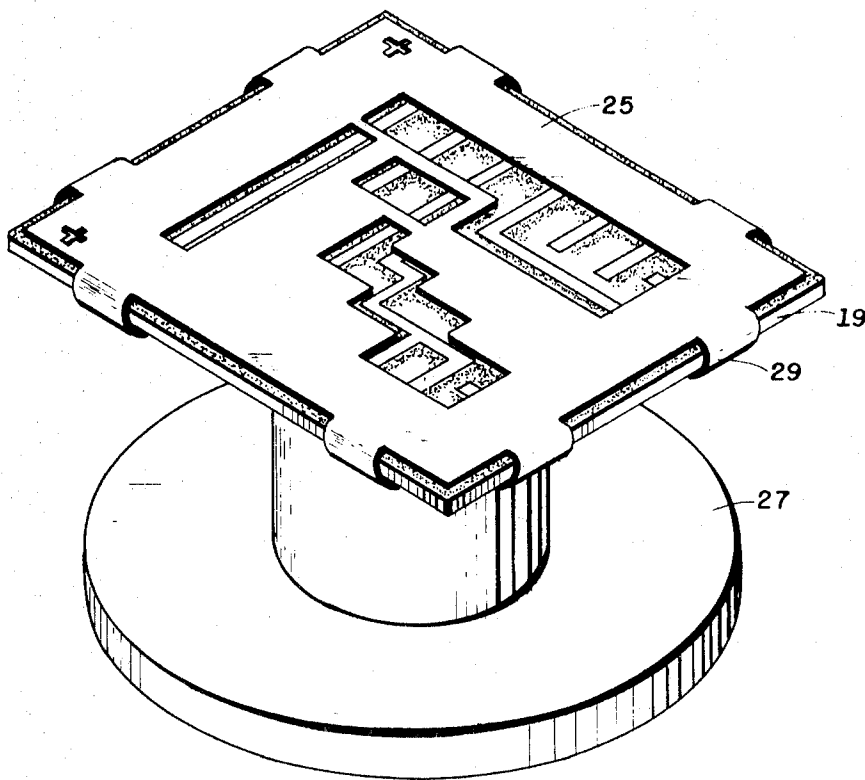


FIG. 7

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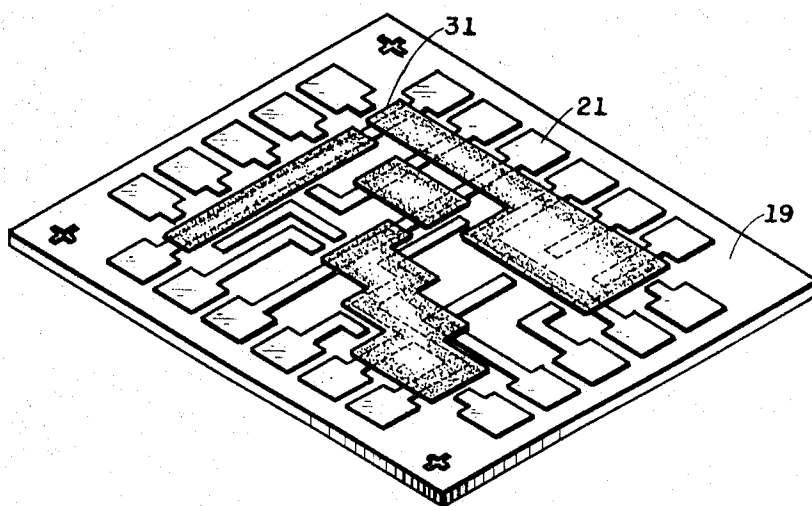


FIG. 8

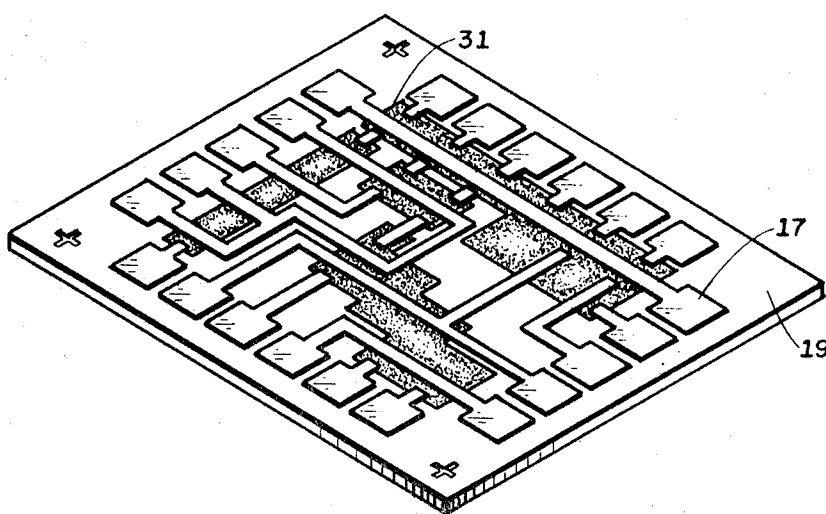


FIG. 9

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CROSSOVER FOR LARGE SCALE ARRAYS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method for fabricating improved crossovers for microelectronic circuits. The invention also includes the article of manufacture provided by the method itself, i.e., the improved crossover useful in densely-packaged integrated circuits.

2. Description of the Prior Art

Prior art crossover techniques have included point-to-point wiring and interlayer connections. The former method requires twice the connections, and the manufacturing time is more than doubled. Additionally, the possibility of technician error in forming point-to-point connections reduces the reliability of the method. Utilization of interlayer connections requires depositing conductors on separate substrates, a problem eliminated by the present invention. Improvement exhibited by the present invention over the prior art also includes doubling the density of units accommodatable in microelectronic packages and greatly reducing stray capacitance.

SUMMARY

The problem of circuit crossovers complicates any array design. According to the present invention, crossovers are accomplished by depositing an insulator on the conductor at the point of crossover. The crossing conductor is deposited over the insulator. The entire process is accomplished by three deposition steps. The present method also includes a novel masking technique developed to facilitate the process. The present method offers numerous advantages including design simplicity, quick reaction time, and low cost.

Accordingly, it is an object of the present invention to provide a simple, highly reliable method of producing crossovers for microelectronic circuits.

It is another object of the invention to provide a low-cost crossover useful in integrated circuitry and which substantially reduces fabrication time.

It is a further object of the invention to provide a reliable circuit crossover which permits increased unit density.

Further objects and attendant advantages of the present invention will become more fully appreciated in light of the following detailed description of the preferred method and article of manufacture thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an enlarged perspective view of a simplified first conductor pattern which comprises the first step in the fabrication of a conductor crossover;

FIG. 2 is an enlarged perspective view of the second major step employed to produce a conductor crossover, i.e., the provision of an insulative pad over the first conductor pattern;

FIG. 3 depicts the conductor crossover which has been completed by provision of a simplified second conductor pattern superimposed on the first conductor pattern and insulative pad;

FIGS. 4a and 4b are plan views of typical first and second conductor pattern photo masks used to produce conductor patterns;

FIG. 5 is a plan view of a mask pattern used for depositing insulative material on the patterned substrate;

FIG. 6 is a perspective view showing a first step in the procedure employed to deposit insulative material on the patterned substrate;

FIG. 7 is a perspective depicting the patterned substrate fitted with a deposition mask prior to deposition of insulative material onto the substrate;

FIG. 8 depicts a patterned substrate onto which insulative material has been deposited at points of conductor crossover; and

FIG. 9 is a perspective of a finished microcircuit array having crossing conductors mutually insulated according to the present invention.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

A simplified step-by-step illustration of the present method is provided in FIGS. 1, 2, and 3. In these views the substrate has been omitted and the conductors and insulating pad greatly enlarged, for the sake of clarity. FIG. 1 depicts a first conductor pattern shown generally at 1 and which, in practice, is formed on a suitable substrate. The first conductor pattern 1 is prepared using conventional layout techniques with conductors 3 and 5 lying in the same plane. Where a crossover is to occur, such as at 7 and 9, the conductors 5 are interrupted on either side of the conductors 3, or on either side of what would be the intersection of the conductors 3 and 5 if opposing conductors 5 were joined. The manner of interrupting the conductors 5 is therefore pictured in FIG. 1, the two conductors 3 being continuous and the two crossing conductors 5 being interrupted.

FIG. 2 illustrates the design of a dielectric pad 11 which is deposited over the four conductor crossover pattern of FIG. 1. The pad 11 must be large enough to cover the central portions of the continuous conductors 3 and overlap the confronting end portions of the conductor elements 5.

A second conductor pattern, shown at 13 in FIG. 3, is disposed over the pad 11 and is a duplicate of the first conductor pattern 1 with a single exception, i.e., conductors 6 which correspond to and overlap the conductors 5 of the first pattern 1, are continuous on the second pattern 13 continuous conductors 8 which correspond to and overlap the conductors 3 of the first pattern 1, are interrupted on the second pattern 13. Extensions 12 of the conductors 8, which are deposited as part of the second conductor pattern 13, overlap confronting edge portions of the dielectric pad 11 on either side of the conductors 6. These extensions 12 are included in the deposition of conductor pattern 13 in order to protect the conductors 3 of the first conductor pattern 1. That is, if the extensions 12 did not extend beyond the edges of the pad 11, portions of the conductors 3 of the first conductor pattern would be removed during the etching of the second conductor pattern 13. Provision of the extensions 12 comprise an important feature of the invention. As can be seen, the method described eliminates interlayer connections, such as plated through holes, and results in higher reliability than conventional interconnect patterns.

FIGS. 4a and 4b illustrate typical examples of the artwork necessary to produce a common crossover pattern. Conductor pattern photo masks 15 and 17 are utilized for developing the desired patterns on the aluminized substrate.

Any number of metal conductor deposition techniques, such as silk screen, evaporation through a mask, or evaporation followed by photolithographic etching, may be used to apply a metallic conductive layer to a suitable substrate. The photolithographic process is preferably used with the present invention due to achievement thereby of greater size reductions and resistor tolerances.

FIG. 6 shows a substrate 19 with a first conductor pattern shown generally at 21 having been etched on the surface of the substrate. The metal deposition and etching process used to produce the substrate 19 and pattern 21 are well known in the art; however, a brief description of a preferred manner of producing the patterned substrate follows.

Substrate materials suitable to the practice of the present invention using the photolithographic process include: Corning 0211 Microsheet glass, Corning 7059 Glass, and Al-Si-Mag 772 Unglazed Alumina with 8 microinch as-fired finish. The Alumina proves to be the most difficult material to work with because of surface roughness.

The first deposition applied to the substrate 19 is a 12,000 A. layer of aluminum. The aluminized substrate is stored in a vacuum desiccator at 70° C. in order to protect the aluminum surface from dirt and oxidation.

A layer of photoresist is applied to the substrate 19 as soon as practical after the metallization. A positive photoresist such as Shipley AZ 1350 has provided excellent results with glass substrates. A negative photoresist, such as Kodak KMER, is preferable on the rough surface of Alumina. The first conductor pattern mask 15 shown in FIG. 4a is placed over the substrate 19 to develop the photoresist.

Etching of the aluminum conductor pattern is accomplished with a phosphoric acid etch stock solution (540 ml. deionized water, 120 ml. nitric acid, 2400 ml. phosphoric acid) at 70° F. A typical etching rate of 1,000 Å. per minute can be expected, thus, etching of the first conductor pattern should be complete in 12 minutes. Before removing the photoresist, the substrate should be thoroughly inspected to verify the completion of etching.

A dielectric material, preferably silicon monoxide, is employed as the insulator at the crossovers. Since silicon monoxide is not easily deposited in the presence of aluminum conductors without destroying the conductors, the insulative pads which separate the crossing conductors are deposited through a mask. A novel masking technique is herein described using the mask pattern 23 shown in FIG. 5. A "Kovar" metal sheet of either 0.001 or 0.002 inch thickness, depending on the size and complexity of the mask, is used to fabricate a mask 25, shown in FIG. 6. Chemical milling is used to produce the pattern in the mask. Using KMER as a photoresist on the Kovar sheet, the photoresist is exposed and developed using the mask pattern 23 and the mask is etched in ferric chloride, 36° to 42° Baume. The etch time is 5 minutes for the 0.002 inch thickness and 2 minutes for the 0.001 inch thickness Kovar mask 25, it should be stored in a vacuum desiccator.

Mask alignment is illustrated in FIG. 6. The mask 25 is placed over the patterned substrate 19 which has been preferably located on a vacuum pedestal 27. The mask 25 is aligned with the aid of the alignment crosses 28 etched in the corners of the mask 25 and substrate 19. A stereo microscope may be used to insure proper alignment. The mask 25 is held in place while tabs 29 are bent around the edges of the substrate 19 as shown in FIG. 7, which shows the metal mask 25 in proper registration and fastened to the substrate 19.

In the 30° C. to 400° C. temperature range, the expansion coefficient of the substrate materials used is greater than that of "Kovar." As a result, when the substrate 19 is raised to the 250° C. temperature normally used during the silicon monoxide deposition, it will expand more than the mask 25, thereby pulling the mask more snugly in contact with said substrate. When using other masking techniques, the mask tends to sag when heated.

The assembled substrate 19 and mask 25 is placed in a conventional vacuum deposition chamber (not shown) with the mask facing a silicon monoxide evaporation source contained in said chamber. Upward evaporation with a mask-to-source distance of approximately 12 inches is a convenient workable arrangement. As previously mentioned, the system is held at 250° C. during the evaporation. A thickness of 18,000 Å. provides a satisfactory insulating pad. FIG. 8 illustrates silicon monoxide pads 31 deposited over the patterned substrate 19. After the silicon monoxide evaporation is complete, the substrate assembly is removed from the vacuum system and the metal mask 25 is removed from the substrate 19. The mask may be stored as previously described for reuse.

The substrate 19 is then returned to the aluminum evaporation system and a layer of aluminum 12,000 Å. thick is evaporated over the entire surface. Photoresist is applied over this aluminum layer and is exposed with the second conductor pattern mask 17 properly aligned over the first conductor pattern 15. After development, the aluminum is etched. FIG. 9 illustrates the appearance of the substrate 19 after the second conductor pattern 17 has been etched. The conductor circuit is 24,000 Å. thick everywhere except at the crossovers where it is half that value.

The crossovers produced by the present method have been evaluated to determine their effect on high frequency or high

impedance circuits. The capacitance of a typical crossover using 0.005 inch width lines is less than one picofarad; the electrical resistance of a crossover exceeds 10 megohms. The breakdown voltage exceeds 200 volts. In circuits incorporating elements such as rhenium resistors, a silicon monoxide layer may be deposited over these elements in order to passivate the elements. This passivation layer is deposited concurrently with the crossover layer.

Although vacuum evaporation and subtractive etching processes have been described in using the present method, there are no obvious reasons why the present method would not be equally successful if executed by either a silk screen thick film process or an evaporation through masks process.

It is believed apparent that the practice and use of the present invention are not confined to the specific teachings related herein. The invention is not to be limited to the particular description provided herein, said description being given as a guide to the use of the invention and not as a limitation to the scope thereof.

I claim:

1. A method for fabricating crossovers useful in microelectronic circuitry comprising the steps of depositing a conductive metallic layer on a substrate; removing portions of the metallic layer to produce a first conductor pattern on the substrate to define a continuous first conductor and an interrupted second conductor with portions on either side of the first conductor; placing a patterned mask etched from a thin metal sheet over the substrate and first conductor pattern; holding the mask in place along the perimeter of the mask whereby said mask will contact the substrate assembly snugly on application of a thermal influence; depositing a layer of dielectric material through the patterned mask at points of conductor crossing; depositing a second conductive metallic layer over the first conductor pattern and dielectric layer; and, removing portions of the second metallic layer to produce a second conductor pattern, whereby the first conductor is continuous below the dielectric layer and interrupted on either side of the second conductor above the dielectric layer and the second crossing conductor is interrupted on either side of the first conductor below the dielectric layer and continuous above the dielectric layer.

2. The method for producing the microcircuit array of claim 1 wherein the first conductor which is interrupted above the dielectric layer is provided with extensions which overlap portions of the dielectric layer on either side of the second conductor.

3. The method of claim 1 wherein the first-mentioned conductive metallic layer is comprised of a substance selected from the group consisting of aluminum, gold, copper, and nickel.

4. The method of claim 3 wherein the second conductive metallic layer is comprised of a substance selected from the group consisting of aluminum, gold, copper, and nickel.

5. The method of claim 4 wherein the layer of dielectric material is comprised of a substance selected from the group consisting of silicon oxide, silicon dioxide, and quartz.

6. The method of forming crossovers in a microcircuit hybrid array which consists of the steps of depositing a layer of aluminum on a substrate, applying a layer of photoresist to the aluminized substrate, developing portions of the photoresist through a conductor pattern mask,

- etching the layer of aluminum to produce a metallic conductor pattern on the substrate, said conductor pattern at points of conductor crossover having first conductors continuous through the points of conductor crossing and second conductors interrupted on either side of the points of conductor crossing, stripping the remaining photoresist from the patterned substrate,

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depositing layers of insulative material at the points on the metallic conductor pattern where conductor crossovers are required,

depositing a second layer of aluminum over the patterned substrate,

applying a layer of photoresist to said substrate,

developing portions of the photoresist through a second conductor pattern mask,

etching the second aluminum layer to produce a second conductor pattern superimposed over the first conductor pattern and insulative layers,

said second conductor pattern at points of conductor cros-

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sover having continuous conductors surmounting the insulative layers and joining the interrupted second conductors of the first conductor pattern, thereby causing said second conductors of the first conductor pattern to be continuous above the insulative layers for producing conductor crossovers, the first conductors of the crossover being continuous below the insulative layers and the second conductors of said crossovers being continuous above the insulative layers, and stripping the remaining photoresist to produce a finished array.

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