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(54) SEMICONDUCTOR SUBSTRATE AND LITHOGRAPHIC MASK PROCESSING

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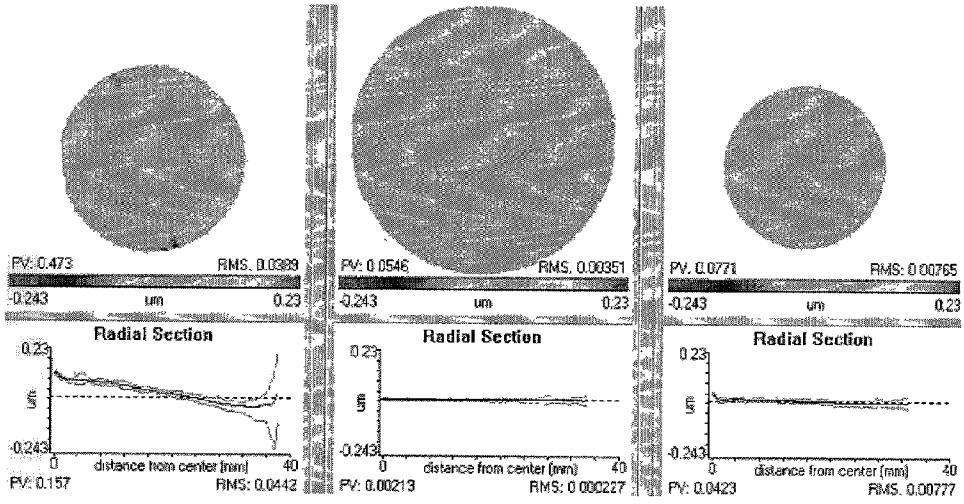
(57) **ABSTRACT**

A system and method for semiconductor processing using magnetorheological finishing (MRF) includes polishing of semiconductor substrates, ceramic bodies and glass lithography masks, to a high degree of flatness by the abrasive action of a magnetorheological fluid flowing in a magnetic field.



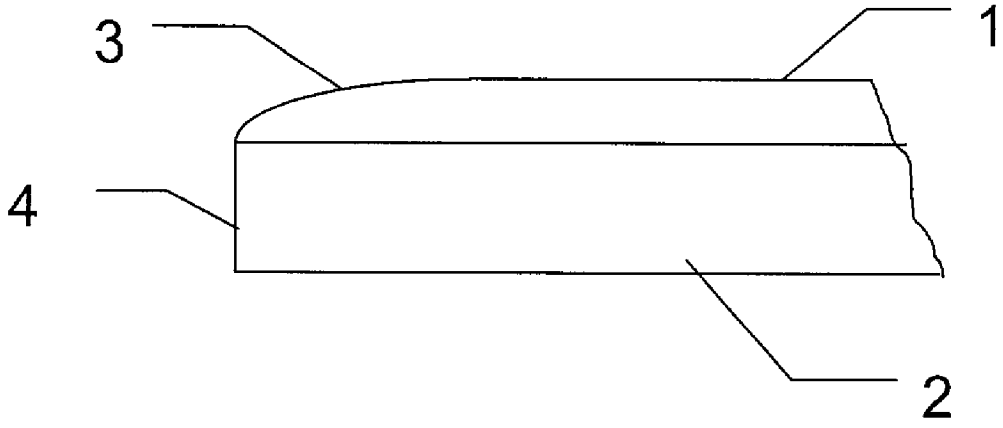


FIG. 1

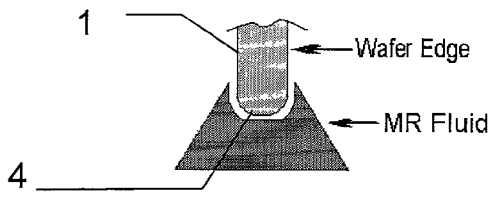

1
Wafer Edge
MR Fluid
4

FIG. 2

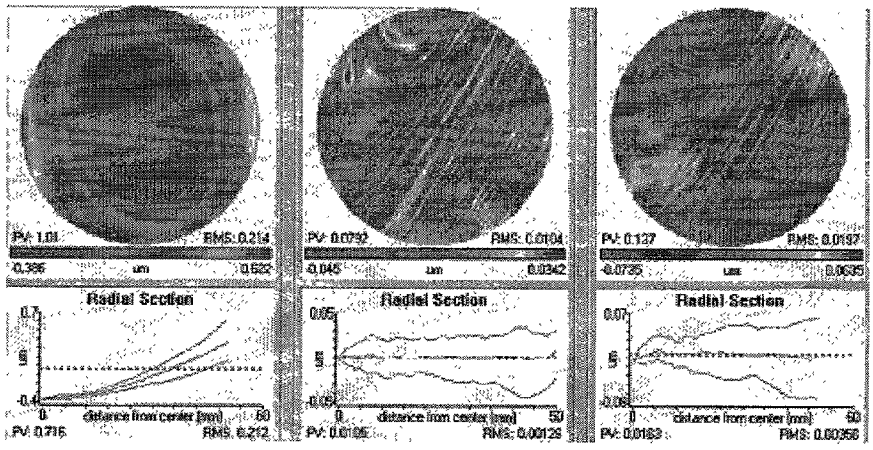

Radial Section
Radial Section
Radial Section

FIG. 3

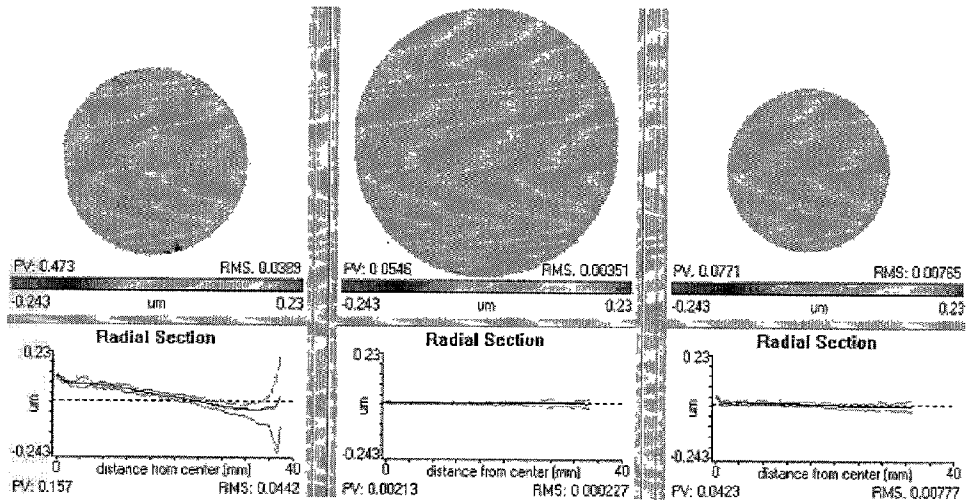
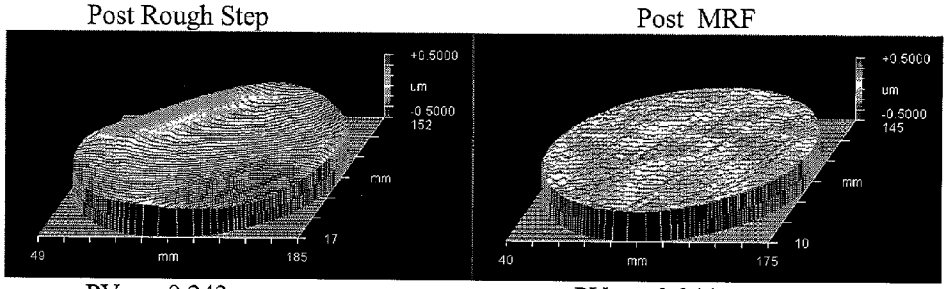
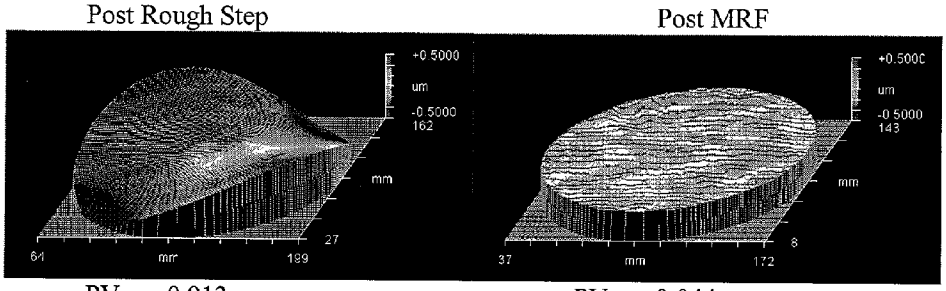

PV: 0.473
RMS: 0.0389
-0.243
um
0.23
Radial Section
0.23
um
-0.243
0
distance from center (mm)
40
PV: 0.157
RMS: 0.0442
PV: 0.0546
RMS: 0.00351
-0.243
um
0.23
Radial Section
0.23
um
-0.243
0
distance from center (mm)
40
PV: 0.00213
RMS: 0.000227
PV: 0.0771
RMS: 0.00765
-0.243
um
0.23
Radial Section
0.23
um
-0.243
0
distance from center (mm)
40
PV: 0.0423
RMS: 0.00777

FIG. 4



PV = 0.243 μm PV = 0.044 μm

FIG. 5



PV = 0.913 μm PV = 0.044 μm

FIG. 6

SEMICONDUCTOR SUBSTRATE AND LITHOGRAPHIC MASK PROCESSING

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of provisional application Serial No. 60/255,040 filed Dec. 11, 2000.

FIELD OF THE INVENTION

[0002] This invention relates, generally, to polishing systems and methods to obtain a substantially flat surface profile and, more particularly, to polishing systems and processes using Magnetorheological finishing, MRF.

BACKGROUND OF THE INVENTION

[0003] The increasing need to form planar surfaces in semiconductor device fabrication has led to the development of process technology known as chemical-mechanical-polishing (CMP). In the CMP process, semiconductor substrates are rotated against a polishing pad in the presence of a chemical slurry. As each substrate is rotated against the polishing pad, the force of the polishing pad in conjunction with the action of the polishing slurry polishes away the surface of the substrate. In the slurry, chemical compounds undergo a chemical reaction with the semiconductor substrate to enhance the rate of removal.

[0004] A common requirement of all CMP processes is that the substrate be uniformly polished. Uniform polishing can be difficult because, typically, there is a strong dependence of the polish removal rate on localized variations in the surface topography of the substrate. For example, the polishing rate at the center of substrate may differ from the polishing rate at the edge of the substrate. Uniform polishing of the entire surface of the substrate is important, because semiconductor manufacturers seek to use as much of each substrate as possible in order to maximize the number of integrated circuit devices, IC devices, that can be built on a useable area of the surface of each substrate.

[0005] The useable area of a semiconductor substrate is reduced by an unusable region along an edge of the substrate, at a perimeter of the surface, referred to as the edge exclusion area. Prior to the invention, the edge exclusion area was 2 mm-3 mm wide, as measured diametrically from the perimeter of the substrate surface. The edge exclusion area defines a boundary or perimeter that encircles the useable area available for fabrication of IC devices thereon. The useable area is known as the FQA, flatness quality area, which is manufactured by polishing a major surface of a bare silicon wafer to provide a flat planar surface on the wafer, followed by, successive layers of materials that are deposited onto the surface of the wafer, constructed with a damascene architecture of circuit interconnects and conducting vias, and then planarized by respective CMP operations. The planarized layers of damascene architecture are of nonuniform planarity or flatness, particularly at the unusable edge region of the substrate, which contributes further to the edge exclusion area. There has been a need to reduce the edge exclusion area, which would increase the FQA on the wafer for supporting an increased number of manufactured IC devices.

[0006] The unusable edge region along the edge of a substrate surface is partly due to nonuniform edge polishing of the cylindrical perimeter of a bare silicon wafer, further referred to as, a silicon substrate or semiconductor substrate. Prior to the invention, edge polishing was a time consuming process, since the edge regions on both sides of a bare silicon wafer must be polished, one side at a time.

[0007] Further, the unusable edge regions along the edge of a substrate is partly due to nonuniform polishing of a surface of the silicon wafer in preparation for manufacture of IC devices thereon. First, the surface of the wafer undergoes a rough polishing operation. Rough polishing intends to provide the wafer surface with a desired global planarity or global flatness. However, as disclosed by **FIG. 1**, such rough polishing causes an edge effect, on an edge region at the perimeter of a major surface **1** of the wafer **2**, that is disclosed as a roll off **3**. IC devices can not be fabricated on the roll off **3**, because the roll off **3** is not flat and coplanar with the central region of the surface **1**, and further, the roll off **3** extends below the elevation of the central region of the surface **1**. It would be desirable to lower the surface **1** to a lower elevation while maintaining its desired planarity, thus, substantially removing the roll off **3**, and desirably increasing the total useable area of the surface **1** on which IC devices can be fabricated.

[0008] The roll off **3** contributes to the unusable edge region along an edge of the substrate. During fabrication of multilayer circuit interconnects and conducting vias for IC devices, successive layers of materials are deposited onto the prepared surface **1** of the wafer **2**. The materials which deposit onto the roll off **3**, are unusable. Further, the cumulative build up of the successive layers on the roll off **3** increase the prominence of the roll off **3**.

[0009] After rough polishing, the wafer **2** is subjected to an intermediate step of polishing that provides a useable area of the surface **1** with a desired local flatness and nanotopography. Nanotopography is expressed by, a manufacturing specification of nanometer scale surface height variations of the surface **1** within a unit distance of millimeter scale. The intermediate step of polishing improves the smoothness or texture of the surface **1**. Further, the intermediate step of polishing, prior to the invention, was capable of introducing further roll off, enhanced dopant striations and a degraded global flatness that was obtained by the previous rough polishing operation.

[0010] The wafer **2** undergoes a final step of polishing, which further improves the smoothness of the surface **1** in conformance with a manufacturing specification of Angstrom scale RMS roughness of the surface **1** within a unit distance of millimeter scale. The appearance of the surface **1** changes from a haze covered surface **1** to a surface **1** that is smooth, planar and haze free with a reflective finish.

[0011] Other devices and materials, such as ceramic bodies for use as magnetic heads and glass reticles used in lithography are also subject to non-uniform polishing, so as to have a similar edge effect as that illustrated in **FIG. 1**. The performance of magnetic heads and glass reticles is reduced due to the edge effect from CMP processing. For example, optical distortion, refraction and other deleterious optical effects can be encountered by a glass reticle because of non-uniform flatness near the edge of the exposure field of the reticle.

[0012] Magnetorheological Finishing (MRF) has been recently developed for shaping optical components to mea-

surement levels well below the capabilities of current methods (e.g., lapping, grinding, polishing). Some of the major advantages of an MRF system include: less than 50 nm (0.5 microns) peak-to-valley flatness capability, conformal polishing media, and deterministic polishing on a variety of materials. **FIGS. 5 and 6** illustrate the

[0013] An MRF system is a computer numerically controlled (CNC) polishing tool that can be used to remove sub-surface damage and improve surface features on a variety of materials. MRF systems are described in, for example, U.S. Pat. Nos. 5,616,066 and 5,971,835 and 6,106,380, which are incorporated by reference herein.

[0014] The MRF system is designed to improve the shape of a previously polished workpiece to metrology levels of measurement well below the capabilities of current methods, such as lapping, grinding and polishing. The polishing media includes a magnetorheological fluid for MRF that mimics a fixed abrasive polishing pad as it comes in contact with the workpiece. The MRF system incorporates the flow of a polishing fluid onto a substrate to be polished. The substrate and polishing fluid are positioned within a magnetic field having a form field shaped by mathematical modeling. The fluid contains a slurry of abrasive particles and ferromagnetic particles, which are aligned by the magnetic field.

SUMMARY OF THE INVENTION

[0015] Many of the MRF benefits to the optics industry can be applied to the flatness processing of bare silicon wafers in the semiconductor industry. According to the invention an optimized MRF system for polishing bare silicon wafers can significantly reduce defects of global flatness scale and defects of site flatness scale, reduce edge polishing cycle time, and can planarize and polish the surface **1**. Additionally, MRF technology can be applied to the polishing of appliances, such as glass reticles and blank glass masks, and ceramic magnetic heads, to provide uniform flatness across the entire working surface of appliance.

[0016] According to an embodiment of the invention, a process for shaping a semiconductor wafer comprises; positioning a silicon wafer having a surface in a fixturing device; contacting the surface with a magnetorheological fluid in the presence of a magnetic field; and shaping the surface of the silicon wafer to a predetermined degree of flatness.

[0017] According to another embodiment of the invention, a process for shaping a perimeter surface of a semiconductor wafer comprises; positioning a silicon wafer having a perimeter surface in a fixturing device, wherein the wafer has opposing surfaces; contacting at least the perimeter surface of the silicon wafer with a magnetorheological fluid in the presence of a magnetic field; and simultaneously shaping the opposing surfaces and the perimeter surface to a predetermined degree of flatness.

[0018] According to another embodiment of the invention, an MRF system is used to polish a surface of a bare silicon wafer, while maintaining its desired planarity, to substantially remove its roll off, and desirably increase the FQA on which IC devices can be fabricated.

[0019] Embodiments of the invention will now be described by way of example with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] **FIG. 1** illustrates a partial cross-sectional view of a semiconductor substrate in the form of a rough polished wafer, for example, a wafer of silicon;

[0021] **FIG. 2** is a schematic diagram of an edge polishing technique in accordance with the invention;

[0022] **FIG. 3** illustrates experimental results for polishing a glass substrate carried out in accordance with the invention using an MRF system;

[0023] **FIG. 4** illustrates experimental results obtained subsequent to the invention by using an MRF system for polishing a semiconductor substrate;

[0024] **FIG. 5** illustrates experimental results for polishing an amorphous glass substrate carried out in accordance with the invention using an MRF system; and

[0025] **FIG. 6** illustrates experimental results for polishing a crystalline glass substrate carried out in accordance with the invention using an MRF system.

DETAILED DESCRIPTION

[0026] In accordance with one embodiment of the invention, a semiconductor wafer **2** is shaped to a flatness of surface **1** substantially the same degree as that of a glass substrate using an MRF system. High end, prime silicon manufacturers are capable of consistently producing 200 mm wafers with global and site flatness levels to 0.50 μm and 0.20 μm, respectively. A typical site size is 25×25 mm. In contrast to CMP processing, an MRF system is capable of achieving less than about 0.05 μm global flatness, with even lower site flatness. To carry out the process, a wafer fixturing device is attached to the MRF system. The method used to hold or fix a wafer **2** during any polishing or finishing step is critical to achieve the desired shape or finish. In accordance with the invention, a fixturing device that can be used for positioning a semiconductor substrate or wafer **2** in an MRF system includes, a vacuum plate (grooved or porous plate, ceramic or metal), an electrostatic chuck, a clamp mount, a template assembly mount and the like. Also, a semiconductor substrate or wafer **2** can be wax mounted to an appropriate support surface. An MRF process is then carried out to form a uniformly flat surface across the entire surface of the substrate or wafer **2**.

[0027] The process includes, positioning a substrate or wafer **2** having a surface in a fixturing device and contacting the surface **1** with a magnetorheological fluid in the presence of a magnetic field. The magnetorheological fluid imparts abrasive action on the wafer **2** by flowing in the magnetic field, such that relative motion of the surface **1** and the fluid polishes and shapes the surface **1** with a predetermined site flatness having a nanometer scale topography. Conveying successive portions of the surface **1** in contact with the fluid distributes the polishing and shaping operations onto successive portions of the surface **1**. Alternatively, the entire surface **1** to be polished is in contact with the fluid. The fluid is subjected to a magnetic field having a form field that is mathematically configured to conform the fluid while the fluid polishes and shapes the surface **1** being polished.

[0028] In an embodiment of the invention, an MRF system is used to edge polish a bare silicon wafer **2**, simultaneously polishing a cylindrical perimeter surface **4** and the edge

regional areas on opposing surfaces, including the surface **1**, on respective sides of the bare silicon wafer **2**, which reduces the manufacturing time for attaining an edge polished silicon wafer **2**, as well as, increases the FQA by minimization of the edge effect due to edge polishing. Further, a bare silicon wafer **2** that has been edge polished by MRF has a perimeter surface **4** of increased strength to resist breaking off of fragments of particulate material. Further, the surface **4** has a smooth polished finish to reduce contamination-related defects. The conformal polishing media in an MRF system is used to polish the complete substrate edge (both sides and the perimeter surface **4**) at one time with good finishing control.

[**0029**] As disclosed by **FIG. 2**, according to an embodiment of the invention, a bare silicon wafer **2**, i.e. semiconductor substrate, is positioned with the cylindrical perimeter surface **4** and the adjoining, edge regions on opposing surfaces on the wafer **2** being contacted by a magnetorheological fluid during an MRF process. By simultaneously polishing the edge regions on opposing surfaces and the perimeter surface **4** of the wafer **2**, the entire edge of the substrate or wafer **2** is polished at a controlled material removal rate, with a minimized manufacturing time duration. The wafer **2** is rotated about its central axis to convey successive portions of the wafer **2** into contact with the fluid, which distributes the polishing and flattening operations over the successive portions of the wafer **2**. Alternatively, the entire periphery of the wafer **2** can be immersed in contact with the fluid, while conforming the fluid by a magnetic field that is mathematically shaped to polish and conform the perimeter surface **4** and the edge regions that are polished by the MRF system.

[**0030**] According to an embodiment of the invention, an MRF system is used to edge polish a bare silicon wafer **2**, simultaneously polishing the cylindrical perimeter surface **4** and the edge regional areas on the surfaces **1** on both sides of the bare silicon wafer **2**, which reduces the manufacturing time for attaining an edge polished silicon wafer **2**.

[**0031**] In accordance with another embodiment of the invention, an MRF system and operation supplements the rough polish operation by replacing the intermediate polish operation used prior to the invention to prepare a bare silicon wafer **2** for manufacture of IC devices thereon. Prior to the invention, the intermediate polishing operation tended to produce a surface **1** with waviness, ripples or undulations having spatial wavelengths ranging from about 0.5 mm to about 20 mm, which comprise nanometer scale waviness detrimental to the desired smoothness of the FQA of the surface **1** on which IC devices are manufactured. The MRF operation in place of the intermediate polishing operation does not introduce nanometer scale defects in the surface **1** in the form of waviness, and, instead, smoothes the surface **1** by minimizing nanometer scale waviness. Further, the MRF operation in place of the intermediate polishing operation substantially eliminates roll off **3**, and improves the site flatness of the surface **1**. By substantially eliminating the roll off **3**, the FQA is maximized to increase the number of IC devices that can be manufactured on the surface **1**. The MRF operation increases the FQA of the surface **1** substantially to as near the perimeter surface **4** of the wafer **2** as can be measured by existing metrology, for example, by capacitance gauge metrology. Improving the site flatness, as measured by standard site flatness metrology, reduces the occurrence of nonplanar or rough surface areas, thus improving the yield of IC devices. As a further benefit, the MRF operation leaves a surface texture of nanometer scale height variations that tailors the surface **1** for removal of the surface texture to a smooth finish by a final polishing operation.

[**0032**] Based on the experimental data using a glass sample described below, and shown in **FIG. 3**, the MRF system benefits a semiconductor substrate polishing process by replacing the traditional intermediate polishing operation with an MRF flattening operation that does not create or enhance nanotopography surface features in the substrate.

[**0033**] In accordance with a further embodiment of the invention, the flatness of a semiconductor substrate or wafer **1** is improved using the MRF system to shape a substrate carrier plate (polishing plate) of apparatus for performing rough polishing of a wafer **2**, to compensate for the shape induced during a typical rough polishing process. The polishing plate is typically made of a ceramic or metal material. In accordance with the invention, an MRF system is programmed to shape the carrier plate to match the desired substrate shape. This technique can be used with wax or free-mount (template assembly) fixturing.

[**0034**] In accordance with a still further embodiment of the invention, an MRF system is used to polish large glass sample materials, such as blank lithographic masks, and in particular lithographic masks used in ultra-violet (UV) lithography, to extremely flat tolerances. Reflective masks, such as those used for enhanced extreme Ultra-Violet (EUV) lithography must meet a much higher standard of flatness than conventional transmissive masks. In a preferred embodiment, a blank glass mask is polished to a TIR measurement, i.e. a peak to valley flatness of no more than about 0.050 μm. In comparison, conventional grinding, shaping, and polishing systems will not meet this standard, which typically provides about a TIR measurement of flatness on the order of about 500 nm. In accordance with the invention, using an MRF system, a blank glass mask can be prepared having a satisfactory Angstrom scale surface roughness. An additional benefit of glass mask processing using an MRF system is that the surface can remain free of polishing induced defects, which will result in fewer defects in subsequent coatings applied to the mask.

EXAMPLE 1

[**0035**] A glass sample was pre-measured for flatness, polished, and post-measured using a Q22 MRF system commercially available from QED Technologies, Rochester, New York, and a Zygo GPI interferometer. The glass sample was placed in the system, and a polish site size of about 100 mm diameter was polished for about 30 minutes.

[**0036**] The results from the test are illustrated in **FIG. 3**. From left to right, the plots of **FIG. 3** show the pre-polish flatness, the computer predicted values, and the actual post-polish flatness. Based on the data the following conclusions can be made: (1) the peak-to-valley flatness was reduced from the original value of about 1.01 μm to about 0.14 μm; (2) the RMS measurement of flatness was reduced from the original value of about 0.214 μm to about 0.020 μm.

EXAMPLE 2

[**0037**] A sample of amorphous glass was rough step polished and was measured by apparatus, similarly as was

the glass sample of EXAMPLE 1. As shown in **FIG. 5**, following rough step polish, the sample had a peak to valley flatness, PV=0.243 μm. The sample was polished by an MRF system which improved the peak to valley flatness, PV=0.044 μm.

EXAMPLE 3

[**0038**] A sample of crystalline glass was rough step polished and was measured by apparatus, similarly as was the glass sample of EXAMPLE 1. As shown in **FIG. 6**, following rough step polish, the sample had a peak to valley flatness, PV=0.913 μm. The sample was polished by an MRF system which improved the peak to valley flatness, PV=0.044 μm.

[**0039**] According to the invention an MRF system is used to polish a surface of a bare silicon wafer, while maintaining its desired planarity, to substantially remove its roll off, and desirably increase the FQA on which IC devices can be fabricated.

[**0040**] Although an embodiment of the invention is disclosed herein, other embodiments and modifications are intended to be covered by the spirit and scope of the appended claims.

What is claimed is:

1. A process for shaping a semiconductor wafer comprising:

positioning a silicon wafer having a surface in a fixturing device;

contacting the surface with a magnetorheological fluid in the presence of a magnetic field; and

shaping the surface of the silicon wafer to a predetermined degree of flatness.

2. The process of claim 1, wherein positioning a silicon wafer having a surface in a fixturing device comprises positioning a silicon wafer in a vacuum stage, an electrostatic chuck, a clamp mount, a template assembly mount and a wax mount stage.

3. The process of claim 1, wherein positioning a silicon wafer comprises positioning a prime silicon wafer.

4. The process of claim 1, wherein shaping the surface of the silicon wafer comprises flattening the surface to a peak to valley flatness of less than about 0.05 micrometers.

5. A process for shaping a perimeter surface of a semiconductor wafer comprising:

positioning a silicon wafer having a perimeter surface in a fixturing device,

wherein the wafer has opposing surfaces;

contacting at least the perimeter surface of the silicon wafer with a magnetorheological fluid in the presence of a magnetic field; and

simultaneously shaping the opposing surfaces and the perimeter surface to a predetermined degree of flatness.

6. The process of claim 5, wherein simultaneously shaping the opposing surfaces of the perimeter surface comprises rotating at least the perimeter surface of the silicon wafer through the magnetorheological fluid in the presence of the magnetic field.

7. A process for preparing a substrate comprising:

rough polishing a surface of the substrate using an abrasive polishing agent to create a spatial wavelength in the surface of the substrate;

positioning the substrate in a fixturing device;

contacting the surface with a magnetorheological fluid in the presence of a magnetic field; and

shaping the surface to a predetermined degree of flatness, such that the spatial wavelength of the surface is substantially preserved.

8. The process of claim 7, wherein positioning a silicon wafer having a surface in a fixturing device comprises positioning a silicon wafer in a vacuum plate, an electrostatic chuck, a clamp mount, a template assembly mount and a wax mount stage.

9. The process of claim 7, wherein the process for preparing a substrate comprises preparing a substrate selected from the group consisting of a semiconductor substrate, a glass substrate, and a ceramic substrate.

10. A process for shaping a substrate carrier plate comprising:

positioning a substrate carrier plate having a workpiece surface in a fixturing device;

contacting the workpiece surface with a magnetorheological fluid in the presence of a magnetic field; and

shaping the workpiece surface to a predetermined degree of flatness.

11. The process of claim 10, wherein shaping the workpiece surface comprises shaping the workpiece surface to substantially match the surface of a substrate to be placed on the workpiece surface prior to carrying out a polishing process.

12. The process of claim 11, wherein positioning a substrate carrier plate having a workpiece surface in a fixturing device comprises positioning the substrate carrier plate in a fixturing device selected from the group consisting of a template assembly mount and a wax mount stage.

13. A process for a glass lithographic mask comprising:

positioning a glass lithographic mask having a surface in a fixturing device;

contacting the surface with a magnetorheological fluid in the presence of a magnetic field; and

shaping the surface of the glass lithographic mask to a predetermined degree of flatness.

14. The process of claim 13, wherein positioning a glass lithographic mask comprises positioning an ultra-violet lithographic mask.

15. The process of claim 13, wherein shaping the surface of the glass lithographic mask comprises shaping the surface to a peak to valley flatness of no more than about 0.05 micrometers.

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