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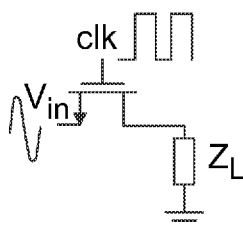


FIG. 14A

(57) Abstract: A circuit comprising a differential transmission line and eight switches provides non-reciprocal signal flow. In some embodiments, the circuit can be driven by four local oscillator signals using a boosting circuit. The circuit can be used to form a gyrator. The circuit can be used to form a circulator. The circuit can be used to form three-port circulator than can provide direction signal flow between a transmitter and an antenna and from the antenna to a receiver. The three-port circulator can be used to implement a full duplex transceiver that uses a single antenna for transmitting and receiving.

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## MAGNETIC-FREE NON-RECIPROCAL CIRCUITS BASED ON SUB-HARMONIC SPATIO-TEMPORAL CONDUCTANCE MODULATION

### Cross Reference to Related Application

[0001] This application claims the benefit of United States Provisional Patent Application No. 62/794,597, filed January 19, 2019, which is hereby incorporated by reference herein in its entirety.

### Statement Regarding Government Funded Research

[0002] This invention was made with government support under HR0011-17-2-0007 awarded by DOD/DARPA. The government has certain rights in the invention.

### Background

[0003] Full-duplex communications, in which a transmitter and a receiver of a transceiver operate simultaneously on the same frequency band, is drawing significant interest for emerging 5G communication networks due to its potential to double network capacity compared to half-duplex communications. Additionally, there are several efforts underway to include simultaneous transmit and receive functionality in the next generation phased array radar systems, especially in commercial automotive radars which can be an enabler technology for future connected or driverless cars. However, one of the biggest challenges from an implementation perspective is the antenna interface.

[0004] One way in which an antenna interface for a full-duplex transceiver can be implemented is using a non-reciprocal circulator. Reciprocity in electronics is a fundamental property of linear systems and materials described by symmetric and time-independent permittivity and permeability tensors. Non-reciprocity causes signals to travel in only one direction. For example, non-reciprocity in a circulator causes signals to travel in only one direction through the circulator. This directional signal flow enables full-duplex wireless communications because signals from the transmitter are only directed toward the antenna (and not the receiver) and received signals at the antenna are only directed toward the receiver (and

not the transmitter). Moreover, the receiver is isolated from signals from the transmitter, preventing desensitization and possible breakdown of the receiver due to the high-power transmitted signal.

**[0005]** Conventionally, non-reciprocal circulators have been implemented using ferrite materials, which are materials that lose their reciprocity under the application of an external magnetic field. However, ferrite materials cannot be integrated into CMOS IC technology. Furthermore, the need for an external magnet renders ferrite-based circulators bulky and expensive.

**[0006]** Accordingly, new mechanisms for implementing non-reciprocity in circuits is desirable.

### **Summary**

**[0007]** In accordance with some embodiments, magnetic-free non-reciprocal circuits based on sub-harmonic spatio-temporal conductance modulation are provided. In some embodiments, circuits are provided, the circuits comprising: a first differential transmission line having: a first end having a first connection and a second connection; and a second end having a third connection and a fourth connection; a first switch having a first side, a second side, and a control, wherein the first side of the first switch is connected to the first connection; a second switch having a first side, a second side, and a control, wherein the first side of the second switch is connected to the first connection; a third switch having a first side, a second side, and a control, wherein the first side of the third switch is connected to the second connection and the second side of the third switch is connected to the second side of the first switch and a first node; a fourth switch having a first side, a second side, and a control, wherein the first side of the fourth switch is connected to the second connection and the second side of the fourth switch is connected to the second side of the second switch and a second node; a fifth switch having a first side, a second side, and a control, wherein the first side of the fifth switch is connected to the third connection; a sixth switch having a first side, a second side, and a control, wherein the first side of the sixth switch is connected to the third connection; a seventh switch having a first side, a second side, and a control, wherein the first side of the seventh switch is connected to the fourth connection and the second side of the seventh switch is connected to the second side of

the fifth switch and a third node; an eighth switch having a first side, a second side, and a control, wherein the first side of the eighth switch is connected to the fourth connection and the second side of the eighth switch is connected to the second side of the sixth switch and a fourth node; and at least one boosting circuit that, in response to a modulation signal drives the control of at least one of the control of the first switch, the control of the second switch, the control of the third switch, the control of the fourth switch, the control of the fifth switch, the control of the sixth switch, the control of the seventh switch, and the control of the eighth switch with a drive signal.

### **Brief Description of the Drawings**

**[0008]** FIGS. 1A, 1B, 1C, and 1D are example illustrations of how a non-reciprocal phase shift can be implemented in accordance with some embodiments.

**[0009]** FIGS. 2A, 2B, 2C, and 2D are example illustrations of how non-reciprocal amplitude (an isolator) can be implemented in some embodiments.

**[0010]** FIG. 3 is an example of a circulator architecture in accordance with some embodiments.

**[0011]** FIGS. 4A, 4B, and 4C is an example of the operation of switch groups in accordance with some embodiments.

**[0012]** FIG. 5 is an example of a schematic of a circulator in accordance with some embodiments.

**[0013]** FIG. 6 is an example of a schematic of a circulator including a 1-stage lattice filter in accordance with some embodiments.

**[0014]** FIG. 7 is an example of schematic of a non-reciprocal circuit element in accordance with some embodiments.

**[0015]** FIGS. 8A, 8B, and 8C are examples of the operation of the element of FIG. 7 with a signal propagating from left to right in accordance with some embodiments.

**[0016]** FIGS. 9A, 9B, and 9C are examples of the operation of the element of FIG. 7 with a signal propagating from right to left in accordance with some embodiments.

**[0017]** FIG. 10 is an example illustration of forward and reverse insertion phases across frequency normalized to a modulation clock frequency in accordance with some embodiments.

**[0018]** FIG. 11 is an example illustration of adverse effects on the operation of a non-reciprocal circuit element when operating with a non-50% duty cycle local oscillator in accordance with some embodiments.

**[0019]** FIG. 12A is an example of a block diagram of a non-reciprocal circulator in accordance with some embodiments.

**[0020]** FIG. 12B is an example of a block diagram of a three port non-reciprocal circulator in accordance with some embodiments.

**[0021]** FIG. 13 is an example of a block diagram and circuit diagrams of a local oscillator path in accordance with some embodiments.

**[0022]** FIGS. 14A and 14B illustrate an example of a problem that can occur when an input signal at a passive mixer approaches the amplitude of a modulator signal in accordance with some embodiments.

**[0023]** FIG. 15 illustrates an example of a boosting circuit and a timing diagram for same in accordance with some embodiments.

**[0024]** FIG. 16 illustrates an example of the operation of a boosting circuit in accordance with some embodiments.

**[0025]** FIG. 17 also illustrates an example of the operation of a boosting circuit in accordance with some embodiments.

**[0026]** FIG. 18 illustrates an example of an implementation of a boosting circuit in accordance with some embodiments.

**[0027]** FIG. 19 illustrates an example of the cancellation of reflections in a gyrator with an impedance mismatch in accordance with some embodiments.

**[0028]** FIG. 20 illustrates an example of S11 parameters for a gyrator with an impedance mismatch in accordance with some embodiments.

**[0029]** FIG. 21 illustrates an example of S21 parameters for a gyrator with an impedance mismatch in accordance with some embodiments.

**[0030]** FIG. 22 illustrates an example of table showing Q values for a gyrator with impedance mismatches at different frequencies in accordance with some embodiments.

**[0031]** FIG. 23 illustrates another example of the cancellation of reflections in a gyrator with an impedance mismatch in accordance with some embodiments.

[0032] FIG. 24 illustrates another example of S21 parameters for a gyrator with an impedance mismatch in accordance with some embodiments.

### **Detailed Description**

[0033] FIGS. 1A, 1B, 1C, and 1D show an example of how a non-reciprocal phase shift can be implemented in some embodiments.

[0034] Turning to FIG. 1A, it can be seen that a signal  $\cos(\omega_{in}t)$  can be injected at nodes A. This is represented in graph 101 of FIG. 1B. As shown in FIG. 1A, the switch groups can then be switched by the following signals:  $\cos(\omega_{mt})$ ;  $\cos(\omega_{mt}+\Phi)$ ;  $\sin(\omega_{mt})$ ; and  $\sin(\omega_{mt}+\Phi)$ , where  $\Phi$  is  $90^\circ$ .  $\Phi_1$  and  $\Phi_2$  shown in FIGS. 1A and 1B relate to  $\Phi$  according to the following equation:  $2\Phi=180^\circ=\Phi_1-\Phi_2$  (or equivalently,  $2*Td*\omega_m/\pi=1$  where  $Td$  is the delay of the transmission lines). As a result of the switching at the switch groups closest to nodes A, the input signal is commutated and two mixing products appear after the commutation on each transmission line at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ . These signals then flow through the top and bottom transmission lines (which provide  $-\Phi_1$  and  $-\Phi_2$  phase shifts at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively). The mixing tones flowing through the top transmission line appear at node B<sub>1F</sub> with total phase shifts of  $-\Phi_1$  and  $-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. The mixing tones flowing through the bottom line appear at node B<sub>2F</sub> with total phase shifts of  $-\Phi_1+90^\circ$  and  $-\Phi_2-90^\circ$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. This is shown in graph 102 of FIG. 1B. The phase shifted signals are then commutated again at  $\omega_m$ , by the switch groups closest to nodes C, but with a phase shift of  $\Phi$ . For each of the four signals in graph 102, two mixing products appear after the commutation at nodes C (for a total of eight signals). As shown in graph 103 of FIG. 1B, the mixing products appear at  $\omega_{in}-2\omega_m$ ,  $\omega_{in}$ , and  $\omega_{in}+2\omega_m$  with phase shifts as shown in the following table:

Row	Signal in Graph 102	Mixing Product	Resulting Frequency	Resulting Phase Shift
1	$\omega_{in}-\omega_m, -\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1$
2	$\omega_{in}-\omega_m, -\Phi_1$	2	$\omega_{in}$	$\Phi-\Phi_1$
3	$\omega_{in}+\omega_m, -\Phi_2$	1	$\omega_{in}$	$-\Phi-\Phi_2 = \Phi-\Phi_1$
4	$\omega_{in}+\omega_m, -\Phi_2$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2$
5	$\omega_{in}-\omega_m, -\Phi_1+90^\circ$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1+180^\circ$
6	$\omega_{in}-\omega_m, -\Phi_1+90^\circ$	2	$\omega_{in}$	$\Phi-\Phi_1$
7	$\omega_{in}+\omega_m, -\Phi_2-90^\circ$	1	$\omega_{in}$	$-\Phi-\Phi_2 = \Phi-\Phi_1$
8	$\omega_{in}+\omega_m, -\Phi_2-90^\circ$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2-180^\circ$

**[0035]** As can be seen, the signals at  $\omega_{in}-2\omega_m$  and  $\omega_{in}+2\omega_m$  (in rows 1 and 5 and rows 4 and 8, respectively) are  $180^\circ$  out of phase and thus cancel out. Also, the signals at  $\omega_{in}$  (in rows 2, 3, 6, and 7) all have the same phase, and thus add up into a single signal with a phase shift of  $\Phi-\Phi_1$ , or  $90^\circ-\Phi_1$ . This is shown in graph 104 of FIG. 1B.

**[0036]** Turning to FIG. 1C, it can be seen that a signal  $\cos(\omega_{in}t)$  can be injected at nodes C. This is represented in graph 111 of FIG. 1D. As shown in FIG. 1C, the switch groups are switched by the following signals:  $\cos(\omega_m t)$ ;  $\cos(\omega_m t+\Phi)$ ;  $\sin(\omega_m t)$ ; and  $\sin(\omega_m t+\Phi)$ , where  $\Phi$  is  $90^\circ$ .  $\Phi_1$  and  $\Phi_2$  shown in FIGS. 1C and 1D relate to  $\Phi$  according to the following equation:  $2\Phi=180^\circ=\Phi_1-\Phi_2$  (or equivalently,  $2\cdot T_d\cdot\omega_m/\pi=1$  where  $T_d$  is the delay of the transmission lines). As a result of the switching at the switch groups closest to nodes C, the input signal is commutated and two mixing products appear after the commutation on each transmission line at  $\omega_{in}-\omega_m$  (with phase shifts of  $-\Phi$ ) and  $\omega_{in}+\omega_m$  (with phase shifts of  $\Phi$ ). These signals then flow through the top and bottom transmission lines (which provide  $-\Phi_1$  and  $-\Phi_2$  phase shifts at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively). The mixing tones flowing through the top transmission line appear at node  $B_{1R}$  with total phase shifts of  $-\Phi-\Phi_1$  and  $\Phi-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. The mixing tones flowing through the bottom line appear at node  $B_{2R}$  with total phase shifts of  $90^\circ-\Phi-\Phi_1$  and  $-90^\circ+\Phi-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. This is shown in graph 112 of FIG. 1D. The phase shifted signals are then commutated again at  $\omega_m$ , by the switch groups closest to nodes A. For each of the four signals in graph 112, two mixing products appear after the commutation at nodes A (for a total of eight signals). As shown in graph 113 of FIG. 1D, the

mixing products appear at  $\omega_{in}-2\omega_m$ ,  $\omega_{in}$ , and  $\omega_{in}+2\omega_m$  with phase shifts as shown in the following table:

Row	Signal in Graph 112	Mixing Product	Resulting Frequency	Resulting Phase Shift
1	$\omega_{in}-\omega_m, -\Phi-\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1$
2	$\omega_{in}-\omega_m, -\Phi-\Phi_1$	2	$\omega_{in}$	$-\Phi-\Phi_1$
3	$\omega_{in}+\omega_m, \Phi-\Phi_2$	1	$\omega_{in}$	$\Phi-\Phi_2 = -\Phi-\Phi_1$
4	$\omega_{in}+\omega_m, \Phi-\Phi_2$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2$
5	$\omega_{in}-\omega_m, 90^\circ-\Phi-\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1+180^\circ$
6	$\omega_{in}-\omega_m, 90^\circ-\Phi-\Phi_1$	2	$\omega_{in}$	$-\Phi-\Phi_1$
7	$\omega_{in}+\omega_m, \Phi-\Phi_2-90^\circ$	1	$\omega_{in}$	$\Phi-\Phi_2 = -\Phi-\Phi_1$
8	$\omega_{in}+\omega_m, \Phi-\Phi_2-90^\circ$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2-180^\circ$

[0037] As can be seen, the signals at  $\omega_{in}-2\omega_m$  and  $\omega_{in}+2\omega_m$  (in rows 1 and 5 and rows 4 and 8, respectively) are  $180^\circ$  out of phase and thus cancel out. Also, the signals at  $\omega_{in}$  (in rows 2, 3, 6, and 7) all have the same phase, and thus add up into a single signal with a phase shift of  $-\Phi-\Phi_1$ , or  $-90^\circ-\Phi_1$ . This is shown in graph 114 of FIG. 1D.

[0038] As can be seen in FIG. 1C and 1D, the signals at  $\omega_{in}$  incur different phase shifts in the forward and reverse direction ( $\Phi-\Phi_1$  and  $-\Phi-\Phi_1$ , respectively), demonstrating the phase non-reciprocity.

[0039] The scattering parameter matrix of the configuration shown in FIGS. 1A, 1B, 1C, and 1D can be represented by  $[S]$  as follows:

$$[S] = \begin{bmatrix} 0 & e^{j(-\phi-\phi_1)} \\ e^{j(\phi-\phi_1)} & 0 \end{bmatrix}$$

where:  $j$  is the square root of  $-1$ . The  $-\phi$  in the term on the top right corner and  $+\phi$  in the term on the bottom left corner show that the phase is non-reciprocal.

[0040] FIGS. 2A, 2B, 2C, and 2D show an example of how non-reciprocal amplitude (an isolator) can be implemented in some embodiments.

[0041] Turning to FIG. 2A, it can be seen that a signal  $\cos(\omega_{in}t)$  can be injected at nodes A. This is represented in graph 201 of FIG. 2B. As shown in FIG. 2A, the switch groups can then be switched by the following signals:  $\cos(\omega_{mt})$ ;  $\cos(\omega_{mt}+\Phi)$ ;  $\sin(\omega_{mt})$ ; and  $\sin(\omega_{mt}+\Phi)$ , where  $\Phi$  is  $45^\circ$ .  $\Phi_1$  and  $\Phi_2$  shown in FIGS. 2A and 2B relate to  $\Phi$  according to the following equation:  $2\Phi=90^\circ=\Phi_1-\Phi_2$  (or equivalently,  $4 * T_d * \omega_m / \pi = 1$  where  $T_d$  is the delay of the transmission lines). As a result of the switching at the switch groups closest to nodes A, the input signal is commutated and two mixing products appear after the commutation on each transmission line at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ . These signals then flow through the top and bottom transmission lines (which provide  $-\Phi_1$  and  $-\Phi_2$  phase shifts at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively). The mixing tones flowing through the top transmission line appear at node B<sub>1F</sub> with total phase shifts of  $-\Phi_1$  and  $-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. The mixing tones flowing through the bottom line appear at node B<sub>2F</sub> with total phase shifts of  $-\Phi_1+90^\circ$  and  $-\Phi_2-90^\circ$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. This is shown in graph 202 of FIG. 2B. The phase shifted signals are then commutated again at  $\omega_m$ , by the switch groups closest to nodes C, but with a phase shift of  $\Phi$ . For each of the four signals in graph 202, two mixing products appear after the commutation at nodes C (for a total of eight signals). As shown in graph 203 of FIG. 2B, the mixing products appear at  $\omega_{in}-2\omega_m$ ,  $\omega_{in}$ , and  $\omega_{in}+2\omega_m$  with phase shifts as shown in the following table:

Row	Signal in Graph 202	Mixing Product	Resulting Frequency	Resulting Phase Shift
1	$\omega_{in}-\omega_m, -\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1$
2	$\omega_{in}-\omega_m, -\Phi_1$	2	$\omega_{in}$	$\Phi-\Phi_1=45^\circ-\Phi_1$
3	$\omega_{in}+\omega_m, -\Phi_2$	1	$\omega_{in}$	$-\Phi-\Phi_2 = \Phi-\Phi_1=45^\circ-\Phi_1$
4	$\omega_{in}+\omega_m, -\Phi_2$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2$
5	$\omega_{in}-\omega_m, -\Phi_1+90^\circ$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1-180^\circ$
6	$\omega_{in}-\omega_m, -\Phi_1+90^\circ$	2	$\omega_{in}$	$\Phi-\Phi_1=45^\circ-\Phi_1$
7	$\omega_{in}+\omega_m, -\Phi_2-90^\circ$	1	$\omega_{in}$	$-\Phi-\Phi_2 = \Phi-\Phi_1=45^\circ-\Phi_1$
8	$\omega_{in}+\omega_m, -\Phi_2-90^\circ$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2-180^\circ$

**[0042]** As can be seen, the signals at  $\omega_{in}-2\omega_m$  and  $\omega_{in}+2\omega_m$  (in rows 1 and 5 and rows 4 and 8, respectively) are 180° out of phase and thus cancel out. Also, the signals at  $\omega_{in}$  (in rows 2, 3, 6, and 7) all have the same phase, and thus add up into a single signal with a phase shift of  $\Phi-\Phi_1$ , or 45°-  $\Phi_1$ . This is shown in graph 204 of FIG. 2B.

**[0043]** Turning to FIG. 2C, it can be seen that a signal  $\cos(\omega_{in}t)$  can be injected at nodes C. This is represented in graph 211 of FIG. 2D. As shown in FIG. 2C, the switch groups can then be switched by the following signals:  $\cos(\omega_{mt})$ ;  $\cos(\omega_{mt}+\Phi)$ ;  $\sin(\omega_{mt})$ ; and  $\sin(\omega_{mt}+\Phi)$ , where  $\Phi$  is 45°.  $\Phi_1$  and  $\Phi_2$  shown in FIGS. 2C and 2D relate to  $\Phi$  according to the following equation:  $2\Phi=90^\circ=\Phi_1-\Phi_2$  (or equivalently,  $4*T_d*\omega_m/\pi=1$  where  $T_d$  is the delay of the transmission lines). As a result of the switching at the switch groups closest to nodes C, the input signal is commutated and two mixing products appear after the commutation on each transmission line at  $\omega_{in}-\omega_m$  (with phase shifts of  $-\Phi$ ) and  $\omega_{in}+\omega_m$  (with phase shifts of  $\Phi$ ). These signals then flow through the top and bottom transmission lines (which provides  $-\Phi_1$  and  $-\Phi_2$  phase shifts at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively). The mixing tones flowing through the top transmission line appear at node B1R with total phase shifts of  $-\Phi-\Phi_1$  and  $\Phi-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. The mixing tones flowing through the bottom line appear at node B2R with total phase shifts of  $90^\circ-\Phi-\Phi_1$  and  $-90^\circ+\Phi-\Phi_2$  at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$ , respectively. This is shown in graph 212 of FIG. 2D. The phase shifted signals are then commutated again at  $\omega_m$ , by the switch groups closest to nodes A. For each of the four signals in graph 212, two mixing products appear after the commutation at nodes A (for a total of eight signals). As shown in graph 213 of FIG. 2D, the mixing products appear at  $\omega_{in}-2\omega_m$ ,  $\omega_{in}$ , and  $\omega_{in}+2\omega_m$  with phase shifts as shown in the following table:

Row	Signal in Graph 212	Mixing Product	Resulting Frequency	Resulting Phase Shift
1	$\omega_{in}-\omega_m, -\Phi-\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1$
2	$\omega_{in}-\omega_m, -\Phi-\Phi_1$	2	$\omega_{in}$	$-\Phi-\Phi_1$
3	$\omega_{in}+\omega_m, \Phi-\Phi_2$	1	$\omega_{in}$	$\Phi-\Phi_2 = -\Phi-\Phi_1$
4	$\omega_{in}+\omega_m, \Phi-\Phi_2$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2$
5	$\omega_{in}-\omega_m, 90^\circ-\Phi-$ $\Phi_1$	1	$\omega_{in}-2\omega_m$	$-\Phi-\Phi_1-180^\circ$
6	$\omega_{in}-\omega_m, 90^\circ-\Phi-$ $\Phi_1$	2	$\omega_{in}$	$-\Phi-\Phi_1$
7	$\omega_{in}+\omega_m, \Phi-\Phi_2-$ $90^\circ$	1	$\omega_{in}$	$\Phi-\Phi_2 = -\Phi-\Phi_1$
8	$\omega_{in}+\omega_m, \Phi-\Phi_2-$ $90^\circ$	2	$\omega_{in}+2\omega_m$	$\Phi-\Phi_2-180^\circ$

**[0044]** As can be seen, the signals at  $\omega_{in}-2\omega_m$ ,  $\omega_{in}$ , and  $\omega_{in}+2\omega_m$  (in rows 1 and 5, rows 2, 3, 6, and 7, and rows 4 and 8, respectively) are  $180^\circ$  out of phase and thus cancel out. This is shown in graph 214 of FIG. 2D.

**[0045]** As can be seen in FIG. 2C and 2D, the signal at  $\omega_{in}$  can only pass in the forward direction while it is completely attenuated in the reverse direction, showing amplitude non-reciprocity.

**[0046]** FIGS. 2A, 2B, 2C, and 2D describe an isolator configuration, where signals can travel in one direction but not the reverse direction. An isolator is like one arm of a circulator. It is useful because it can be placed between a power amplifier and its antenna, and it will protect the power amplifier from back reflections at the antenna.

**[0047]** Another use of the structures of FIGS 1A, 1B, 2A, and 2B is a 2D lattice of such structures which can have a programmable signal propagation based on the phase shifts of the different switches.

**[0048]** In FIGS. 1A, 1B, 2A, and 2B, mixing products at  $\omega_{in}-\omega_m$  and  $\omega_{in}+\omega_m$  have been shown for simplicity, but, in reality, square-wave commutation can produce mixing products at offsets equal to all odd multiples of  $\omega_m$ .

**[0049]** Turning to FIG. 3, an example 300 of a circulator architecture in accordance with some embodiments is shown. As illustrated, circulator 300 includes an antenna port 301, a transmitter port 302, a receiver port 304, a non-reciprocal phase component 306, and transmission lines 308, 310, and 312. Within non-reciprocal phase component 306, there are passive mixers 314, 316, 318, and 320, and transmission lines 322 and 324.

**[0050]** As shown in FIG. 3, values of signals and components in non-reciprocal phase component 306 may depend on an input frequency ( $\omega_{in}$ ) and a modulation frequency ( $\omega_m$ ).  $\omega_{in}$  represents the frequency of operation of the circulator.  $\omega_m$  represents the frequency at which the mixers are modulated. Any suitable frequencies can be used for  $\omega_{in}$  and  $\omega_m$ , in some embodiments. For example, in some embodiments, RF/millimeter-wave/Terahertz frequencies can be used. In some embodiments,  $\omega_{in}$  and  $\omega_m$  may be required to be sized relative to each other. For example, in some embodiments, the mixing signals at  $\omega_{in}+\omega_m$  and  $\omega_{in}-\omega_m$  should be  $180^\circ$  out of phase or equivalently the following equation may be required to be met:  $2\omega_m T_d=180^\circ$ , where  $T_d$  is the group delay. More particularly, for example, in some embodiments,  $\omega_{in}$  can be 28 GHz and  $\omega_m$  can be 9.33 GHz.

**[0051]** Each of the transmission lines in FIG. 3 is illustrated as having a “length” that is based on a given frequency. For example, transmission lines 308, 310, and 312 are illustrated as having a length equal to  $\lambda/4$ , where  $\lambda$  is the wavelength for a frequency of  $\omega_{in}$ . As another example, transmission lines 322 and 324 are illustrated as providing  $180^\circ$  phase difference between the signals at  $\omega_{in}+\omega_m$  and  $\omega_{in}-\omega_m$  or equivalently a group delay of  $T_d=1/4(\omega_m/2\pi)$ .

**[0052]** Transmission lines 308, 310, 312, 322, and 324 can be implemented in any suitable manner. For example, in some embodiments, one or more of the transmission lines can be implemented as C-L-C pi-type lumped sections. In some other embodiments, they may be implemented as truly distributed transmission lines.

**[0053]** The passive mixers can be driven by signals as shown in FIG. 3, in some embodiments. For example, in some embodiments, mixer 314 can be driven by a signal  $\cos(\omega_m t)$ , mixer 316 can be driven by a signal  $\cos(\omega_m t + \Phi)$ , mixer 318 can be driven by a signal  $\sin(\omega_m t)$ , and mixer 320 can be driven by a signal  $\sin(\omega_m t + \Phi)$ , where  $\Phi$  is  $90^\circ$  for  $T_d=1/4(\omega_m/2\pi)$ .

**[0054]** In some embodiments, mixers 314, 316, 318, and 320 shown in FIG. 3 can be implemented with switch groups 414, 416, 418, and 420, respectively, as illustrated in FIG. 4A.

As shown in FIG. 4B, the switch groups in FIG. 4A can each include four switches 402, 404, 406, and 408, in some embodiments.

**[0055]** The switches in the switch groups can be implemented in any suitable manner. For example, in some embodiments, the switches can be implemented using NMOS transistors, PMOS transistors, both NMOS and PMOS transistors, or any other suitable transistor or any other switch technology.

**[0056]** Switch groups 414, 416, 418, and 420 can be controlled by local oscillator signals LO1, LO2, LO1Q, and LO2Q, respectively, as shown in FIG. 4A, in some embodiments. A timing diagram showing an example of these signals with respect to each other is shown in FIG. 4C. In this diagram,  $f_{LO}$  is equal to  $\omega_m/2\pi$ . When a local oscillator (e.g., LO1, LO2, LO1Q, or LO2Q) is HIGH, switches 402 and 408 in the corresponding switch group are CLOSED and switches 404 and 406 in the corresponding switch group are OPEN. When a local oscillator (e.g., LO1, LO2, LO1Q, or LO2Q) is LOW, switches 404 and 406 in the corresponding switch group are OPEN and switches 402 and 408 in the corresponding switch group are CLOSED.

**[0057]** Turning to FIG. 5, an example of a schematic of a circulator that can be implemented in accordance with some embodiments is shown. This circulator is generally in the same architecture as shown in FIG. 3, except that transmission line 308 is split in half and part is placed adjacent to the receiver nodes.

**[0058]** The differential nature of the circulator can reduce the LO feedthrough and improve power handling. The fully-balanced I/Q quads can be designed using  $2 \times 16 \mu\text{m}/40\text{nm}$  floating-body transistors. The placement of the gyrator in a symmetric fashion between the TX and RX ports can be used to enable switch parasitics to be absorbed into the lumped capacitance of the  $\lambda/8$  sections on either side. Artificial (quasi-distributed) transmission lines with inductor Q of 20 can be used in the gyrator, using four stages of lumped  $\pi$ -type C-L-C sections with a Bragg frequency of 83.9GHz. The  $\lambda/4$  transmission lines between the TX and ANT and ANT and RX ports can be implemented using differential conductor-backed coplanar waveguides. As shown, baluns can be included at the TX, ANT and RX ports to enable single-ended measurements, and separate test structures can be included to de-embed the response of the baluns.

**[0059]** Turning to FIG. 6, an example of the architecture of FIG. 3 using 1-stage lattice filters instead of transmission lines 322 and 324 (FIG. 3) is shown. Any suitable filters can be used. For example, in some embodiments, film bulk acoustic resonator (FBAR) filters, surface

acoustic wave (SAW) filters, bulk acoustic wave (BAW) filters, and/or any other suitable filters can be used. By implementing large delays using SAW or BAW filters, the clock frequency can be even further reduced. This can be exploited to design even-higher-linearity circulators through the use of high-voltage technologies and high-linearity switch design techniques.

**[0060]** The circuits described herein can be implemented in any suitable technology in some embodiments. For example, in some embodiments, these circuits can be implemented in any semiconductor technology such as silicon, Gallium Nitride (GaN), Indium phosphide (InP), Gallium arsenide (GaAs), etc. More particularly, for example, in some embodiments, the circuits can be implemented in IBM 45nm SOI CMOS process.

**[0061]** In FIG. 1, the phase shift provided by the non-reciprocal phase component,  $\Phi - \Phi_1$ , can be tuned by changing the clock phase,  $\Phi$ . The frequency at which TX-to-RX isolation is achieved depends on  $\Phi - \Phi_1$ , so by tuning  $\Phi$ , the isolation frequency can be tuned.

**[0062]** Turning to FIG. 7, another example of some embodiments is shown. As illustrated, a spatio-temporal conductivity modulation concept in accordance with some embodiments can include two sets of switches implemented in a fully-balanced fashion on either end of a differential transmission line delay. The switches can be modulated between short and open circuit states through periodic square pulses with a 50% duty cycle. As shown, the transmission line provides a delay equal to one quarter of the modulation period ( $T_m/4$ ), and the modulation of the right switches is delayed with respect to those on the left by the same amount ( $T_m/4$ ). Adding this delay between the two sets of switches allows incident signals from different directions to follow different paths, breaking reciprocity.

**[0063]** FIGS. 8A, 8B, and 8C depict an example of signal propagation in the forward direction (from left, or port 1, to right, or port 2) in accordance with some embodiments. As shown in FIG. 8A, during the first half-period of the modulation clock, when LO1+ is high, the incident signal goes into the transmission line, gets delayed by the transmission line delay of  $T_m/4$ , and reaches to the second set of switches. At this instant, LO2+ is high, so that the signal directly passes to the output. A similar explanation holds also for the second half-period of the modulation clock (shown in FIG. 8B): the signal goes into the transmission line with a sign flip, gets delayed by  $T_m/4$ , and the sign flip is recovered by the second set of switches. In other words, signals traveling in the forward direction experience no polarity inversion in the first half cycle, and two polarity inversions negate each other occur in the second half cycle. Thus,

effectively, in the forward direction, signals pass through the structure without any loss and experience a delay of one quarter of the modulation period. This can be described by the time domain equation:

$$v_2^-(t) = v_1^+ \left( t - \frac{T_m}{4} \right)$$

where  $v_1^+$  and  $v_2^-$  are the incident and transmitted signals at ports 1 and 2, respectively.

**[0064]** Alternatively, this structure can be modeled by multiplication, delay and multiplication as depicted in FIG. 8C. Here, the fully-balanced switching operation is modeled as multiplication by a 50% duty cycle clock,  $m(t)$ , flipping between +1 and -1. Thus, the output signal can be written as:

$$v_2^-(t) = v_1^+ \left( t - \frac{T_m}{4} \right) m \left( t - \frac{T_m}{4} \right) m \left( t - \frac{T_m}{4} \right) = v_1^+ \left( t - \frac{T_m}{4} \right) \quad (1)$$

which takes advantage of the fact that  $m \left( t - \frac{T_m}{4} \right) m \left( t - \frac{T_m}{4} \right) = +1$  for a binary (-1, +1) signal.

**[0065]** The signal propagation in the backward direction (from right to left) is shown in FIGS. 9A, 9B, and 9C. As shown in FIG. 9A, during the first half-period of the modulation clock, when LO2+ is high, the signal goes into the transmission line and gets delayed by  $T_m/4$ , and the second set of switches flips the signal sign. Similarly, during the second half-period of the modulation clock (LO2- is high), the signal goes into the transmission line with a sign flip, gets delayed by  $T_m/4$  and reaches the output as LO1+ is high. In brief, signals traveling from right to left experience a transmission line delay of  $T_m/4$  and a polarity inversion in both half cycles. This can be described by:

$$v_1^-(t) = -v_2^+ \left( t - \frac{T_m}{4} \right)$$

where  $v_2^+$  and  $v_1^-$  are the incident and transmitted signals at ports 1 and 2, respectively.

**[0066]** An analysis based on the signal flow diagram in FIG. 9C gives

$$v_1^-(t) = v_2^+ \left( t - \frac{T_m}{4} \right) m \left( t - \frac{T_m}{2} \right) m(t) = -v_2^+ \left( t - \frac{T_m}{4} \right) \quad (2)$$

which takes advantage of  $m(t-T_m/2)m(t) = -1$  for a binary (-1, +1) 50% duty-cycle signal.

**[0067]** From (1) and (2), the resultant S-parameters can be written as

$$S_{21}(\omega_{in}) = e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} \quad (3)$$

$$S_{12}(\omega_{in}) = -e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} \quad (4)$$

where  $\omega_{in}$  and  $\omega_m$  are the signal and modulation frequencies, respectively. It should be noted  $S_{11}=S_{22}=0$  since there is a pair of switches which connects the transmission line to the input and output at any instant in both half cycles. As can be seen from (3) and (4), this generalized spatio-temporal conductivity modulation technique is ideally lossless and breaks phase reciprocity over a theoretically infinite bandwidth. More importantly, it operates as an ideal passive lossless gyrator -- a basic non-reciprocal component that provides a non-reciprocal phase difference of  $\pi$  and can be used as a building block to construct arbitrarily complex non-reciprocal networks -- over theoretically infinite bandwidth. In practice, the insertion loss would be limited by ohmic losses in the switches and transmission line, and bandwidth by dispersion effects in the transmission line, particularly if it is implemented in a quasi-distributed fashion to absorb the capacitive parasitics of the switches.

**[0068]** FIG. 10 shows an example of an illustration of forward and reverse insertion phases ( $\angle S_{21}$  and  $\angle S_{12}$ , respectively) across frequency normalized to the modulation clock frequency. As can be seen, the spatio-temporal conductivity modulation provides a phase shift of  $\pm 90$  degrees at the odd multiples of the modulation frequency, namely  $\omega_{in}=(2n-1)\omega_m$ , where  $n$  is a positive integer. Using higher odd multiples reduces the clock frequency, which eases clock generation and distribution, at the expense of a longer transmission line which introduces more loss and larger form factor. In some embodiments, an operating to modulation frequency ratio of  $3(\omega_m=\omega_{in}/3=8.33\text{GHz})$  can be used to optimize this trade-off.

**[0069]** In some embodiments, duty cycle impairment in the modulation clock can have an adverse effect on operation in the reverse direction. For example, let us assume a deviation from ideal 50% duty cycle by  $\Delta T_m$ . The forward direction remains unaffected, since  $m(t-T_m/4)m(t-T_m/4)$  continues to be +1, but in the reverse direction,  $m(t-T_m/2)m(t)$  will give a pulse train with a pulse width of  $\Delta T$  and period of  $T_m/2$  as depicted in FIG. 11. Thus, deviation from 50% duty cycle would result in loss in the reverse direction, as some portion of the power would be transferred to mixing frequencies due to the  $2\omega_m$  content in  $m(t-T_m/2)m(t)$ .  $S_{12}$  at the operating frequency becomes

$$S_{12}(\omega_{in}) = \left(-1 + \frac{4\Delta T_m}{T_m}\right) e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} \quad (5)$$

**[0070]** As shown in FIG. 12A, a non-reciprocal phase shift element (gyrator) can be embedded within a  $3\lambda/4$  transmission line ring to realize a non-reciprocal circulator in accordance with some embodiments. In the clockwise direction, the -270 degree phase shift of the transmission line adds to the -90 degree phase shift through the gyrator, enabling wave propagation ( $-270 + -90 = -360$ ). In the counter-clockwise direction, the -270 degree phase shift of the transmission line adds to the +90 degree phase shift of the gyrator, suppressing wave propagation ( $-270 + +90 = -180$ ).

**[0071]** A three-port circulator can be realized in some embodiments by introducing three ports  $\lambda/4$  apart from each other as shown in FIG. 12B. The gyrator can be placed symmetrically between the TX and RX ports in some embodiments. The S-parameters of the circulator at  $\omega_{in} = 3\omega_m$  can be derived to be:

$$\begin{pmatrix} 0 & 0 & -1 \\ -j & 0 & 0 \\ 0 & -j & 0 \end{pmatrix}$$

where TX is port 1, ANT is port 2, and RX is port 3.

**[0072]** FIG. 13 shows an example of a block diagram and circuit diagrams of an 8.33GHz LO path in accordance with some embodiments. As illustrated, the four quadrature clock signals driving the switches can be generated from two input differential sinusoidal signals at 8.33GHz. A two-stage poly-phase filter (phase imbalance  $< 2$  degrees for up to 15% variation in R and C values) can be used to generate the 8.33GHz quadrature signals with 0/90/180/270 degree phase relationship. After the poly-phase filter, a three stage self-biased CMOS buffer chain with inductive peaking in the final stage can be used to generate the square wave clock signals for the switches. Independently controlled NMOS varactors (implemented using  $4 \times 40\mu\text{m}/40\text{nm}$  floating-body devices) can be placed at the differential LO inputs to compensate for I/Q imbalance of the poly-phase filter. This provides an I/Q calibration range of  $\pm 10$  degrees that can be used to optimize the circulator performance.

**[0073]** Turning to FIG. 14A, a switch that can be used in the passive mixers described above (e.g., any one or more of switches 402, 404, 406, and 408 of FIG. 4B) is illustrated. As shown,

the switch may have a clock (clk) at its gate and an input signal ( $V_{in}$ ) at its source. An impedance  $Z_L$  may be present at the switch's drain.

**[0074]** A passive mixer compresses when the RF swing on the source/drain of the transistor becomes comparable to the modulation signal at the gate. For a large enough RF swing, the mixer is modulated by the RF signal rather than the modulation signal resulting in false switching and hence compression.

**[0075]** As shown in FIG. 14B, when  $V_{in}$  (represented by the sine wave shown) gets large, for given high and low voltage levels ( $V_{HIGH}$  and  $V_{LOW}$ , respectively) of the clock, the difference between the high voltage level and the input signal divided by two can be less than the threshold voltage of the switch, and the difference between the input signal divided by two and the low voltage level can be greater than the threshold voltage of the switch. This can cause improper behavior of the switch.

**[0076]** In accordance with some embodiments mechanisms for clock boosting are provided that can address this problem. These mechanisms produce a larger modulation signal thereby enabling mixers to handle higher RF power.

**[0077]** Turning to FIG. 15, an example of a mechanism for clock boosting in accordance with some embodiments is illustrated. As shown, this mechanism includes an inverter at the left, eight switches numbered 1-8, capacitors C1 and C2, and a switch at the right (which is part of a passive mixer). In some embodiments, the inverter need not be added to an existing design and the signal LO provided at the output of the inverter can be provided by any suitable component of a circuit that has been designed to drive a passive mixer's switch.

**[0078]** During operation, when the output (LO) of the driving inverter (the driver) is high ( $+V_{DD}$ ), the output of the driver is level shifted using a pre-charged capacitor (C1, which is charged to  $+V_{DD}$ ) to create a high output level of  $+2V_{DD}$  as shown in the timing diagram on the right of FIG. 15. When the output of the driving inverter is low (0 Volts), the output of the driver is level shifted using a pre-charged capacitor (C2, which is charged to  $-V_{DD}$ ) to create a low output level of  $-V_{DD}$ . Hence, the output swing of the driving inverter is boosted to create a 3x higher modulation swing. That is, as shown in the timing diagram on the right of FIG. 15, the signal driving the gate of the switch transitions between  $-V_{DD}$  and  $+2V_{DD}$  instead of between 0 and  $V_{DD}$ .

[0079] The function performed by the circuit of FIG. 15 can be represented by the following equation:

$$V_{gate}(t) = LO(t) + V_{C1}(t) * \left( \frac{LO(t)}{V_{dd}} \right) + V_{C2}(t) * \left( \frac{LOb(t)}{V_{dd}} \right)$$

[0080] In the timing diagram, the voltages  $V_{C1}$  and  $V_{C2}$  across capacitors C1 and C2 are shown as being constant even though slight variations in these voltages may occur due to parasitic in the path between the driver and the gate. Although + and - symbols are shown in the figure to provide a reference for voltage measurements, these symbols do not denote that the capacitors are or need to be polarized.

[0081] FIGS. 16 and 17 further illustrate the operation of the circuit shown in FIG. 15 in accordance with some embodiments. As shown in FIG. 16, when the output of the driver is high (e.g., +Vdd), switch 1, 2, 7, and 8 are closed, and switches 3, 4, 5, and 6 are open. This causes the voltage across capacitor C1 (+Vdd) to be added to the signal (+Vdd) at the output of the driver to produce +2Vdd at the gate of the switch (represented in FIG. 16 by  $C_{load}$ ). At the same time, capacitor C2 is charged to -Vdd. As shown in FIG. 17, when the output of the driver is low (e.g., 0V), switch 1, 2, 7, and 8 are open, and switches 3, 4, 5, and 6 are closed. This causes the voltage across capacitor C2 (-Vdd) to be added to the signal (0V) at the output of the driver to produce -Vdd at the gate of the switch (represented in FIG. 17 by  $C_{load}$ ). At the same time, capacitor C1 is charged to +Vdd.

[0082] For purposes of illustration, it can be assumed that the switches of FIGS. 15, 16, and 17 are implemented using NMOS transistors, such that when a high signal is applied at the gate of the switch, the switch is closed and such that when a low signal is applied at the gate of the switch, the switch is opened.

[0083] Turning to FIG. 18, an example of an implementation of the circuit of FIG. 15 in accordance with some embodiments is shown. As illustrated, switches 1, 2, 7, and 8 can be implemented using PMOS transistors and switches 3, 4, 5, and 6 can be implemented using NMOS transistors. As also illustrated, the gates of transistors 1, 3, 5, and 7 can be driven by signal LO, the gates of transistors 2 and 6 can be driven by signal  $LO_{CPN}$ , and the gates of transistors 4 and 8 can be driven by signal  $LO_{CPP}$ .  $LO_{CPN}$  and  $LO_{CPP}$  (and  $\overline{LO}_{CPN}$  and  $\overline{LO}_{CPP}$ ) can be generated by a level shift circuit shown in the right of FIG. 18. Mathematically,  $LO_{CPN}$ ,  $LO_{CPP}$ ,  $\overline{LO}_{CPN}$ , and  $\overline{LO}_{CPP}$  can be represented as:

$$LO\_CPN = -V_{dd} + LO$$

$$\overline{LO}_{CPN} = -V_{dd} + \overline{LO};$$

$$LO\_CPP = +V_{dd} + LO; \text{ and}$$

$$\overline{LO}_{CPP} = +V_{dd} + \overline{LO}$$

**[0084]** Theoretically, a 3x higher swing can be achieved by increasing the supply voltage and increasing the power consumption by 9x. However, using the technique of clock boosting only the last transistor experiences the higher swing, so the total power consumption will be increased only by a factor of 4-5. In addition, owing to the limit of  $2V_{DD}$  for the long-term reliability, supply voltage of a conventional driver cannot be increased to  $3V_{DD}$ . On the other hand, it is important to notice that despite of achieving a  $3xV_{DD}$  swing, none of the CMOS transistor cross the long-term reliability limit of  $2xV_{DD}$ . This clock boosting technique can be used to drive any of the passive mixers described above.

**[0085]** As described above in connection with FIG. 3, the transmission line should be quarter wave at the modulation frequency. Thus, while having a lower modulation frequency implies lower clocking power consumption, a lower modulation frequency means a longer transmission line and the area associated with it. While the electrical length of a lumped LC transmission line can be increased by increasing only the capacitance of the line with negligible increase in the area, doing so also changes the impedance of the transmission line.

**[0086]** When the gyrator is operated in an environment of  $Z_o$ , it is intuitive to use a transmission line with impedance  $Z_o$  so that there will be perfect matching. Typically, when we have an interface with  $Z_o$  on one side and other impedance  $Z_g$  on another side there will a mismatch.

**[0087]** As illustrated in FIGS. 18-24, the matching of the gyrator structure at the odd multiples of the modulation frequency will not be compromised by using a different impedance "Zg" for the transmission line in the gyrator. This happens in a very counter-intuitive way. As shown in FIGS. 19 and 23, when there is an impedance mismatch at odd multiples of the modulation frequency, multiple reflections at port 1 (between the  $Z_o$  and  $Z_g$  interface) and port 2 (between the  $Z_g$  and  $Z_o$  interface) add up in a destructive way leading to a perfect matching.

**[0088]** The  $S_{11}$  parameter of the gyrator in FIG. 19 can be represented as:

$$S_{11} = -\Gamma - \Gamma(1 + \Gamma)(1 - \Gamma)e^{-2\gamma l} + \Gamma^3(1 + \Gamma)(1 - \Gamma)e^{-4\gamma l} - \Gamma^5(1 + \Gamma)(1 - \Gamma)e^{-6\gamma l} \\ + \Gamma^7(1 + \Gamma)(1 - \Gamma)e^{-8\gamma l} \dots$$

This reduces to:

$$S_{11} = -\Gamma \left( \frac{1 + e^{-2\gamma l}}{1 + \Gamma^2 e^{-2\gamma l}} \right)$$

Similarly, the  $S_{21}$  parameter of the gyrator in FIG. 19 can be represented as:

$$S_{21} = \left( \frac{(1 - \Gamma^2)e^{-\gamma l}}{1 + \Gamma^2 e^{-2\gamma l}} \right)$$

For a lossless case  $\gamma=j\beta$  when  $\beta l = \frac{(2N+1)\pi}{2}$ ,  $N=0, 1, 2, 3, \dots$  :

$$S_{11} = 0; S_{21} = (-1)^N$$

Similarly:

$$S_{12} = (-1)^{N+1}j; S_{22} = 0$$

Thus, changing  $Z_g$  does not affect the operation at center frequency and the structure acts as a gyrator for an  $Z_g$ .

**[0089]** However, as shown in FIGS. 20, 21, 22, and 24, the contrast between the impedances " $Z_g/Z_o$ " determines the bandwidth of this matching. For example, theoretically, the gyrator is matched over infinite bandwidth when  $Z_g = Z_o$  (as shown in the top row of the table of FIG. 22 where  $Z_g=Z_o=50\text{ohms}$ ). However, decreasing values of  $Z_g$  will result in decreasing bandwidths as shown for example in FIG. 22 (which is for a modulation frequency of 10GHz). That is, for each lower value of  $Z_g$  and each higher center frequency in the table of FIG. 22, the Q value (which equals the center frequency (in the column heading) divided by 3dB bandwidth) gets worse.

**[0090]** As shown in FIG. 20, the  $S_{11}$  parameter for the gyrator of FIG. 19 at a modulation frequency of 10GHz shows no reflections (or virtually no reflections) at odd multiples of the modulation frequency (i.e., 10GHz, 30GHz, 50GHz, 70GHz, and 90GHz), and strong reflections at other frequencies.

**[0091]** As shown in FIG. 21, the  $S_{21}$  parameter for the gyrator of FIG. 19 at a modulation frequency of 10GHz shows no attenuation (or virtually no attenuation) at  $Z_g$  equal to 49ohms (whose line is straight across at 0dB), and progressively larger attenuations at lower  $Z_g$  impedances of 25ohms, 5ohms, and 1ohm other than when at odd multiples of the modulation frequency (i.e., 10GHz, 30GHz, 50GHz, 70GHz, and 90GHz), where there is no attenuation (or virtually no attenuation). Similarly, as shown in FIG. 24, the  $S_{21}$  parameter for the gyrator of FIG. 23 at a modulation frequency of 200MHz shows no attenuation (or virtually no attenuation)

at  $Z_g$  equal to 100ohms (whose line is straight across at 0dB), and progressively larger attenuations at lower  $Z_g$  impedances of 80ohms, 60ohms, 40ohms, and 20ohms other than when at odd multiples of the modulation frequency (i.e., 20GHz, 30GHz, 50GHz, 70GHz, and 90GHz), where there is no attenuation (or virtually no attenuation).

**[0092]** In a circulator implementation in accordance with some embodiments, a 60ohm differential transmission line can be used. For these embodiments, the -1dB bandwidth of the gyrator can be 400MHz, while the -1dB bandwidth of the circulator is 200MHz. Since the bandwidth of the gyrator is greater than the bandwidth of the circulator, the usage of mismatched transmission line does not affect the bandwidth of the circulator in these embodiments.

**[0093]** In some embodiments, a 60ohm transmission line that is a quarter wave at 200MHz can be used. A comparable transmission line with the similar chip area could be 100ohm and a quarter wave at 333MHz. Hence by compromising the bandwidth of the gyrator, the modulation frequency can be reduced to 200MHz from 333MHz. As a result of this, the power consumption of the switches can be reduced by 40% when used in a circulator built at 1GHz. It is important to notice that, even if a gyrator is infinitely broadband, a circulator built using this gyrator is not infinitely broadband. So slightly relaxing the bandwidth of the gyrator should not compromise the bandwidth of the circulator built using the gyrator with a 60ohm transmission line.

**[0094]** If one chooses, a transmission line can be implemented with a much lower characteristic impedance, consequently the modulation frequency, and the lower limit will be determined by the minimum bandwidth required by the system and additional loss added in the gyrator due to multiple reflections as shown in FIGS. 20, 21, 22, and 24.

**[0095]** Although single transmission lines are illustrated herein as having certain delays, such transmission lines can be implemented as two or more transmission lines having the same total delay.

**[0096]** Although the disclosed subject matter has been described and illustrated in the foregoing illustrative implementations, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of implementation of the disclosed subject matter can be made without departing from the spirit and scope of the disclosed subject matter, which is limited only by the claims that follow. Features of the disclosed implementations can be combined and rearranged in various ways.

**What is claimed is:**

1. A circuit, comprising:
  - a first differential transmission line having: a first end having a first connection and a second connection; and a second end having a third connection and a fourth connection;
  - a first switch having a first side, a second side, and a control, wherein the first side of the first switch is connected to the first connection;
  - a second switch having a first side, a second side, and a control, wherein the first side of the second switch is connected to the first connection;
  - a third switch having a first side, a second side, and a control, wherein the first side of the third switch is connected to the second connection and the second side of the third switch is connected to the second side of the first switch and a first node;
  - a fourth switch having a first side, a second side, and a control, wherein the first side of the fourth switch is connected to the second connection and the second side of the fourth switch is connected to the second side of the second switch and a second node;
  - a fifth switch having a first side, a second side, and a control, wherein the first side of the fifth switch is connected to the third connection;
  - a sixth switch having a first side, a second side, and a control, wherein the first side of the sixth switch is connected to the third connection;
  - a seventh switch having a first side, a second side, and a control, wherein the first side of the seventh switch is connected to the fourth connection and the second side of the seventh switch is connected to the second side of the fifth switch and a third node;
  - an eighth switch having a first side, a second side, and a control, wherein the first side of the eighth switch is connected to the fourth connection and the second side of the eighth switch is connected to the second side of the sixth switch and a fourth node; and
  - at least one boosting circuit that, in response to a modulation signal drives the control of at least one of the control of the first switch, the control of the second switch, the control of the third switch, the control of the fourth switch, the control of the fifth switch, the control of the

sixth switch, the control of the seventh switch, and the control of the eighth switch with a drive signal.

2. The circuit of claim 1, further comprising:

a second differential transmission line having: a first end having a fifth connection and a sixth connection; and a second end having a seventh connection and an eighth connection;

a ninth switch having a first side, a second side, and a control, wherein the first side of the ninth switch is connected to the fifth connection;

a tenth switch having a first side, a second side, and a control, wherein the first side of the tenth switch is connected to the fifth connection;

an eleventh switch having a first side, a second side, and a control, wherein the first side of the eleventh switch is connected to the sixth connection and the second side of the eleventh switch is connected to the second side of the ninth switch and the first node;

a twelfth switch having a first side, a second side, and a control, wherein the first side of the twelfth switch is connected to the sixth connection and the second side of the twelfth switch is connected to the second side of the tenth switch and the second node;

a thirteenth switch having a first side, a second side, and a control, wherein the first side of the thirteenth switch is connected to the seventh connection;

a fourteenth switch having a first side, a second side, and a control, wherein the first side of the fourteenth switch is connected to the seventh connection;

a fifteenth switch having a first side, a second side, and a control, wherein the first side of the fifteenth switch is connected to the eighth connection and the second side of the fifteenth switch is connected to the second side of the thirteenth switch and the third node; and

a sixteenth switch having a first side, a second side, and a control, wherein the first side of the sixteenth switch is connected to the eighth connection and the second side of the sixteenth switch is connected to the second side of the fourteenth switch and the fourth node.

3. The circuit of claim 1, further comprising:

at least one other differential transmission line having a total delay of three quarters of a period of an operating frequency of the circuit, having a first side having a ninth connection and a tenth connection, and having a second side having an eleventh connection and a twelfth connection, wherein the ninth connection is connected to the second side of the first switch, the tenth connection is connected to the second side of the fourth switch, the eleventh connection is connected to the second side of the fifth switch, and the twelfth connection is connected to the second side of the eighth switch.

4. The circuit of claim 3, wherein the at least one other differential transmission line comprises:

a third differential transmission line having a delay of one quarter of the period of the operating frequency of the circuit;

a fourth differential transmission line having a delay of one quarter of the period of the operating frequency of the circuit; and

at least one fifth differential transmission line having a total delay of one quarter of the period of the operating frequency of the circuit,

wherein the third differential transmission line, the fourth differential transmission line, and the at least one fifth differential transmission line form a series connection between: the first node and the second node; and the third node and the fourth node.

5. The circuit of claim 4, further comprising a transmitter port, an antenna port, and a receiver port, wherein the third differential transmission line is connected between the transmitter port and the antenna port, and the fourth differential transmission line is connected between the antenna port and the receiver port.

6. The circuit of claim 4, wherein the at least one fifth differential transmission line comprises:

a sixth differential transmission line having a delay of one eighth of the period of the operating frequency of the circuit; and

a seventh differential transmission line having a delay of one eighth of the period of the operating frequency of the circuit,

wherein the sixth differential transmission line is connected between the third differential transmission line and the third node and the fourth node, and the seventh differential transmission line is connected between the fourth differential transmission line and the third node and the fourth node.

7. The circuit of claim 1, wherein the control of the first switch and the control of the fourth switch are connected to a first local oscillator signal, the control of the second switch and the control of the third switch are connected to a second local oscillator signal, the control of the fifth switch and the control of the eighth switch are connected to a third local oscillator signal, and the control of the sixth switch and the control of the seventh switch are connected to a fourth oscillator signal.

8. The circuit of claim 7, wherein the first oscillator signal and the first oscillator signal and the second oscillator signal are 180 degrees out of phase, the third oscillator signal and the fourth oscillator signal are 180 degrees out of phase, and the third oscillator signal is delay from the first oscillator signal by one quarter of a period of an operating frequency of the circuit.

9. The circuit of claim 8, wherein the first local oscillator, the second local oscillator, the third local oscillator, and the fourth local oscillator each have a 50% duty cycle.

10. The circuit of claim 1, wherein the first differential transmission line has a delay of one quarter of a period of an operating frequency of the circuit.

11. The circuit of claim 1, wherein the first differential transmission line is implemented as at least one C-L-C pi-type lumped section.

12. The circuit of claim 1, wherein the boosting circuit includes: a first plurality of switches and a first capacitor that are configured to charge the first capacitor when the boosting circuit is in a first state and to add a voltage across the first capacitor to the modulation signal to produce the drive signal when the boosting circuit is in a second state.

13. The circuit of claim 12, wherein the boosting circuit also includes: a second plurality of switches and a second capacitor that are configured to charge the second capacitor when the boosting circuit is in the second state and to add a voltage across the second capacitor to the modulation signal to produce the drive signal when the boosting circuit is in the first state.

14. The circuit of claim 13, wherein the second plurality of switches comprises:  
a seventeenth switch having a first side, a second side, and a control;  
an eighteenth switch having a first side, a second side, and a control, where the first side of the eighteenth switch is connected to the second side of the seventeenth switch and to a first side of the second capacitor, and wherein the second side of the eighteenth switch is connected to a positive voltage source;

a nineteenth switch having a first side, a second side, and a control, where the first side of the nineteenth switch is connected to the second side of the second capacitor, and wherein the second side of the nineteenth switch is connected to a negative voltage source; and

a twentieth switch having a first side, a second side, and a control, where the first side of the twentieth switch is connected to the second side of the second capacitor.

15. The circuit of claim 12, wherein the first plurality of switches comprises:

a twenty first switch having a first side, a second side, and a control;

an twenty second switch having a first side, a second side, and a control, where the first side of the twenty second switch is connected to the second side of the twenty first switch and to a first side of the first capacitor, and wherein the second side of the twenty second switch is connected to a negative voltage source;

a twenty third switch having a first side, a second side, and a control, where the first side of the twenty third switch is connected to the second side of the first capacitor, and wherein the second side of the twenty third switch is connected to a positive voltage source; and

a twenty fourth switch having a first side, a second side, and a control, where the first side of the twenty fourth switch is connected to the second side of the first capacitor.

16. The circuit of claim 1, wherein the boosting circuit includes: a second plurality of switches and a second capacitor that are configured to charge the second capacitor when the boosting circuit is in a second state and to add a voltage across the second capacitor to the modulation signal to produce the drive signal when the boosting circuit is in a first state.

17. The circuit of claim 16, wherein the second plurality of switches comprises:

a seventeenth switch having a first side, a second side, and a control;

an eighteenth switch having a first side, a second side, and a control, where the first side of the eighteenth switch is connected to the second side of the seventeenth switch and to a first side of the second capacitor, and wherein the second side of the eighteenth switch is connected to a positive voltage source;

a nineteenth switch having a first side, a second side, and a control, where the first side of the nineteenth switch is connected to the second side of the second capacitor, and wherein the second side of the nineteenth switch is connected to a negative voltage source; and

a twentieth switch having a first side, a second side, and a control, where the first side of the twentieth switch is connected to the second side of the second capacitor.

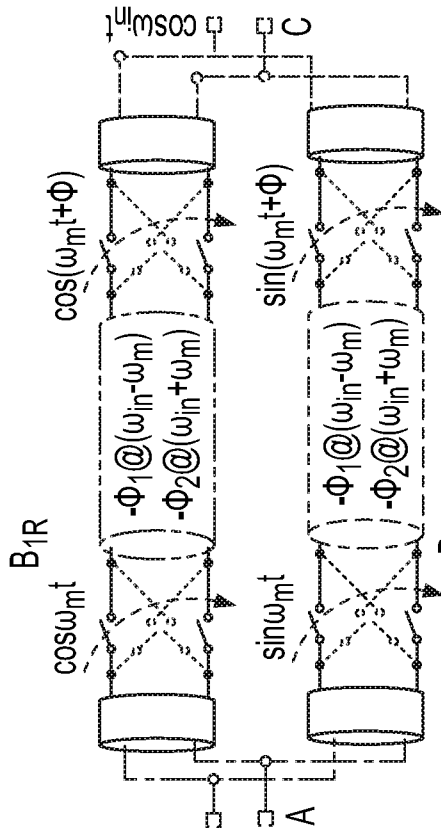


FIG. 1C

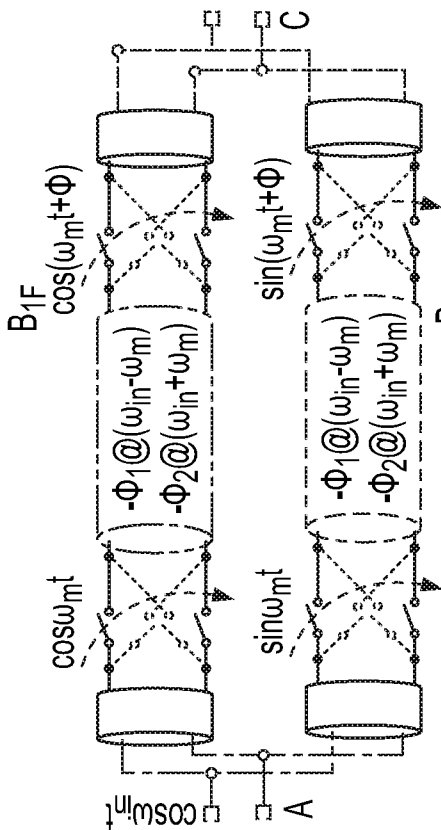


FIG. 1A

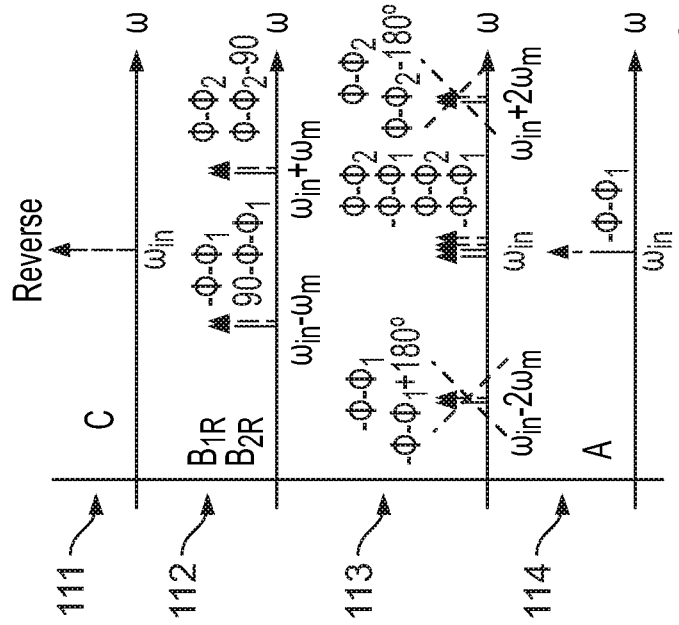


FIG. 1D

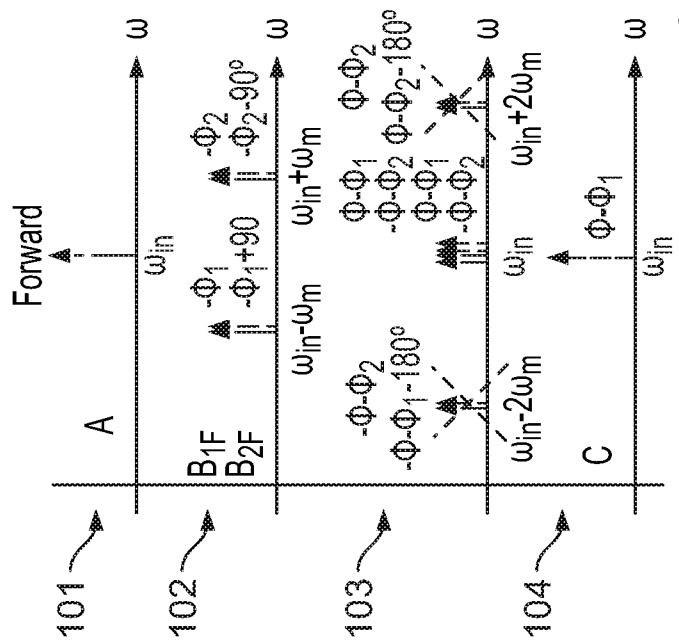


FIG. 1B

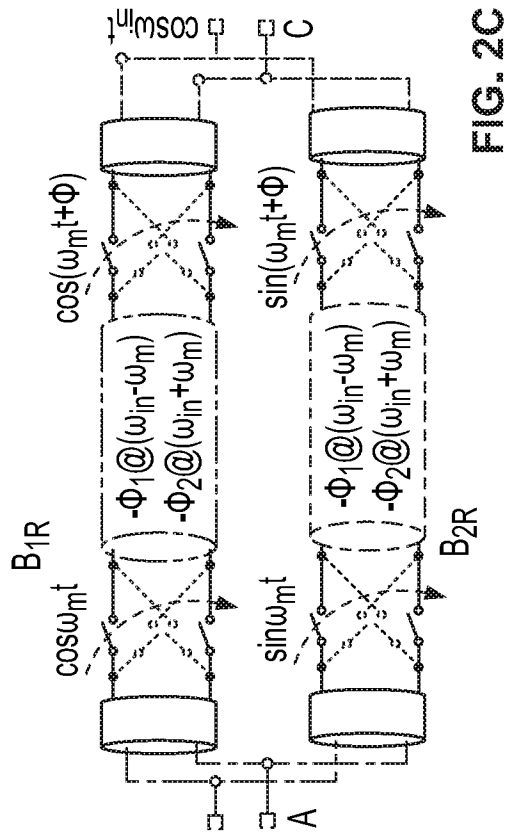


FIG. 2C

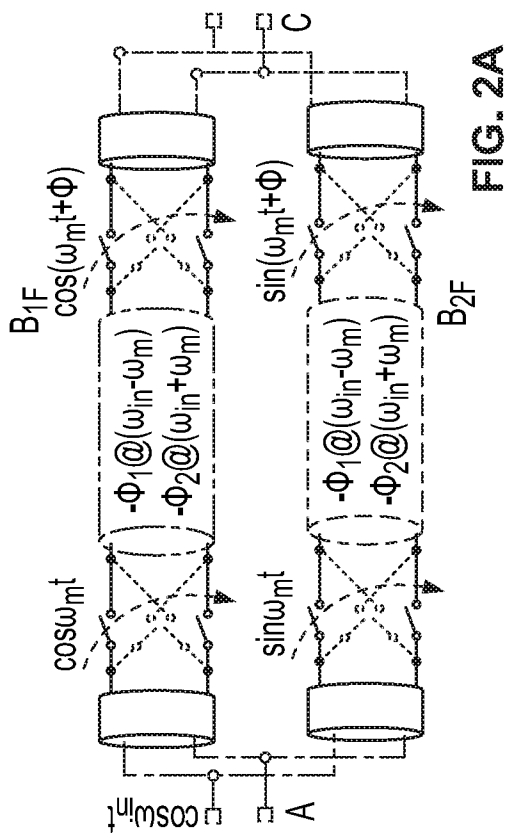


FIG. 2A

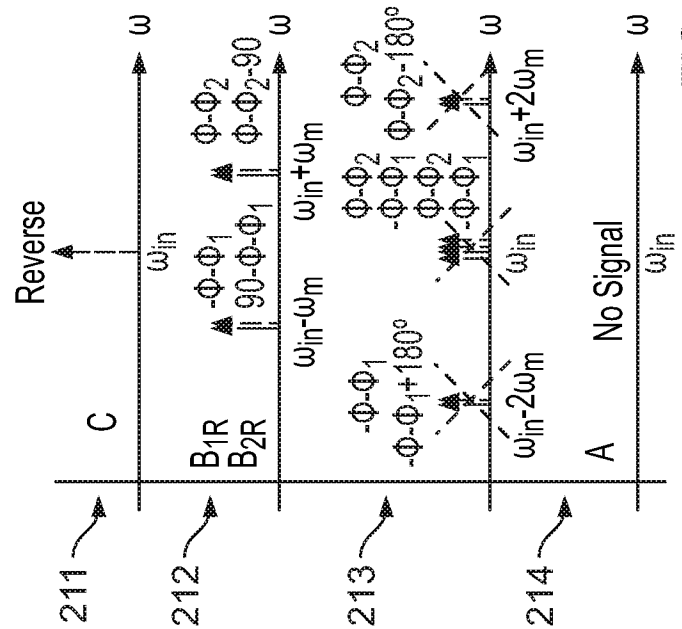


FIG. 2D

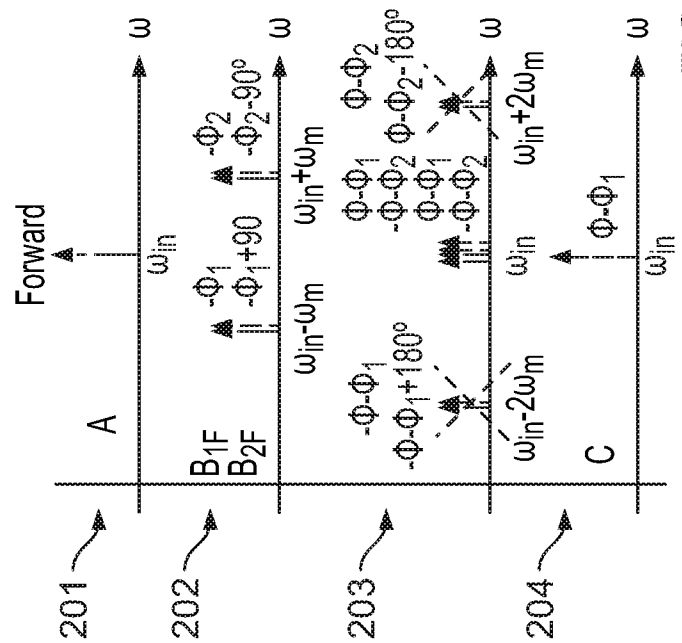


FIG. 2B

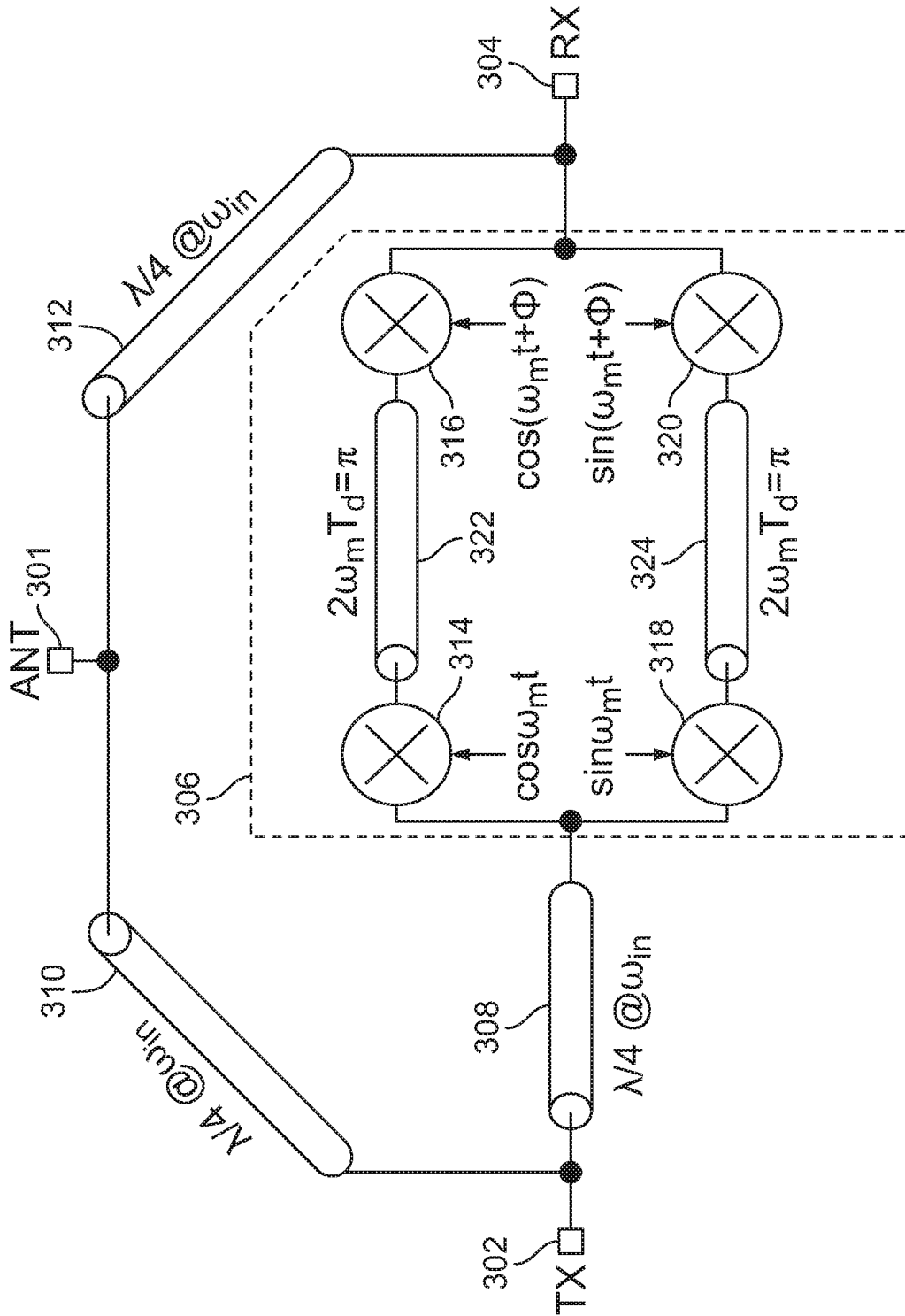
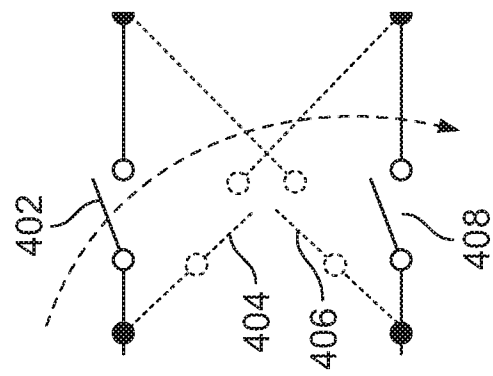
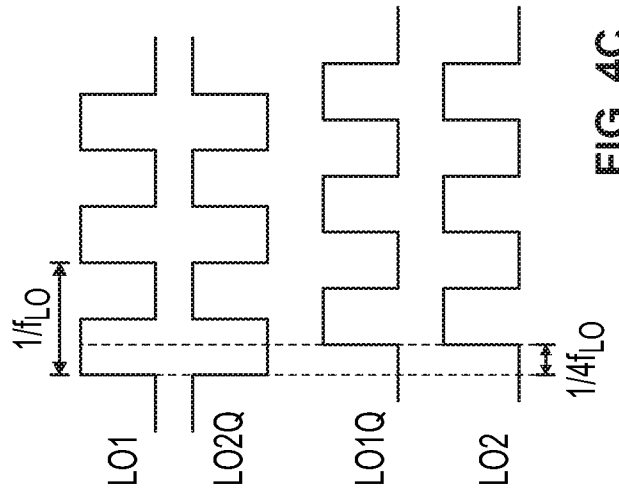
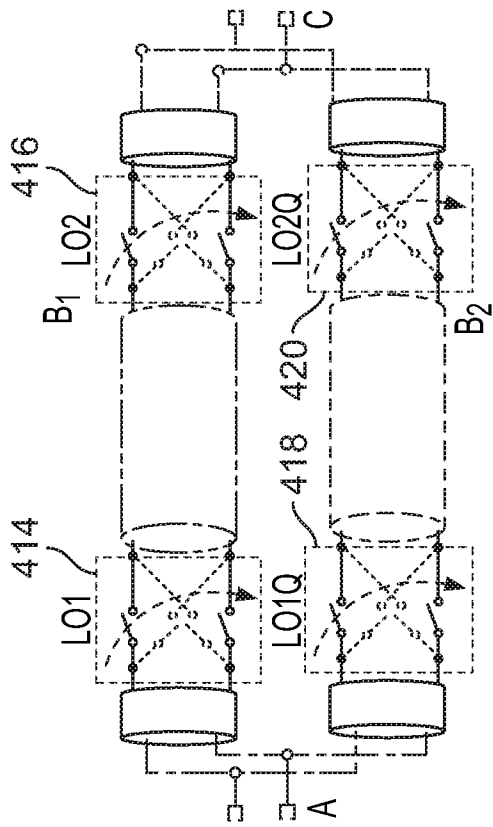


FIG. 3



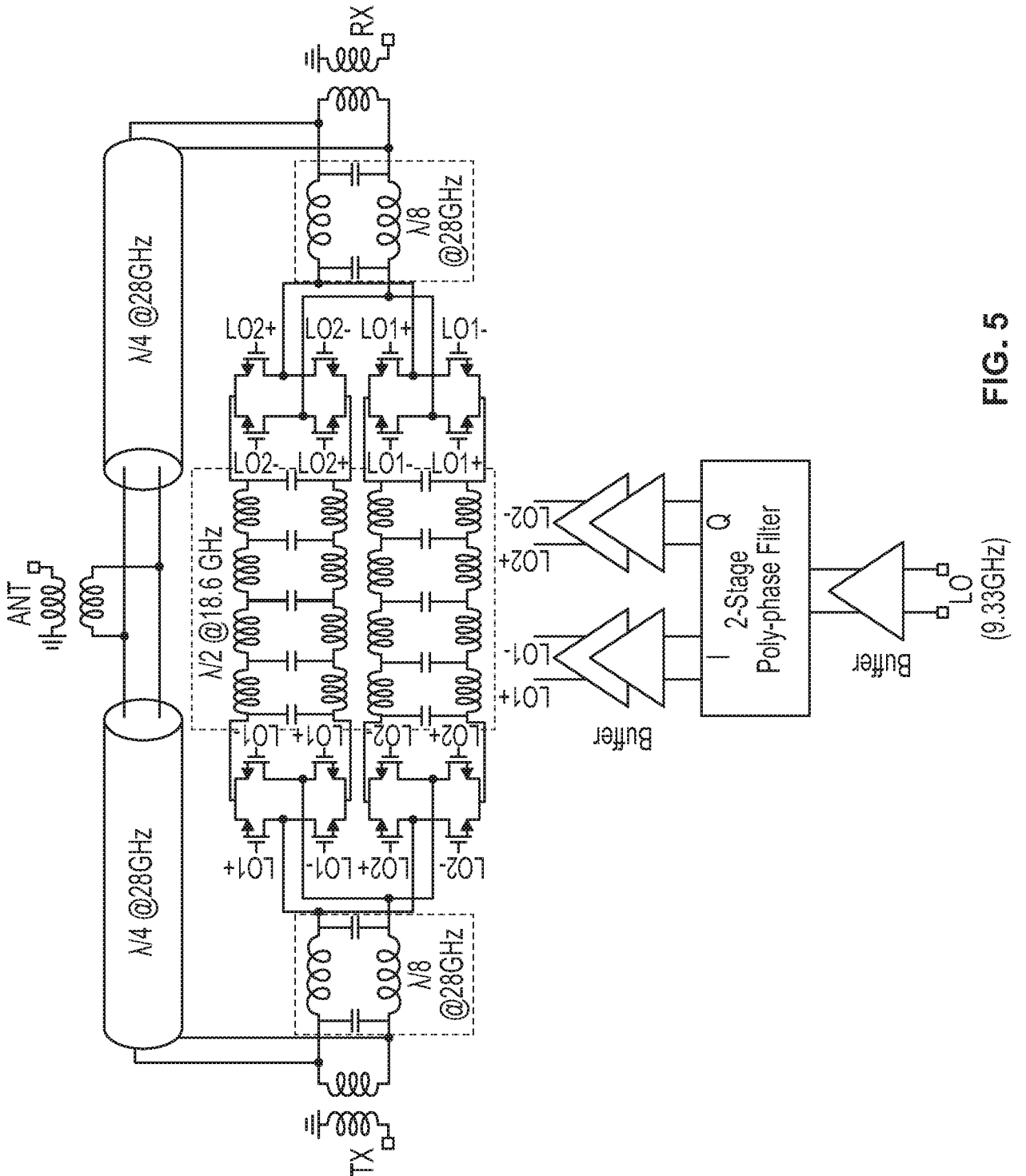


FIG. 5

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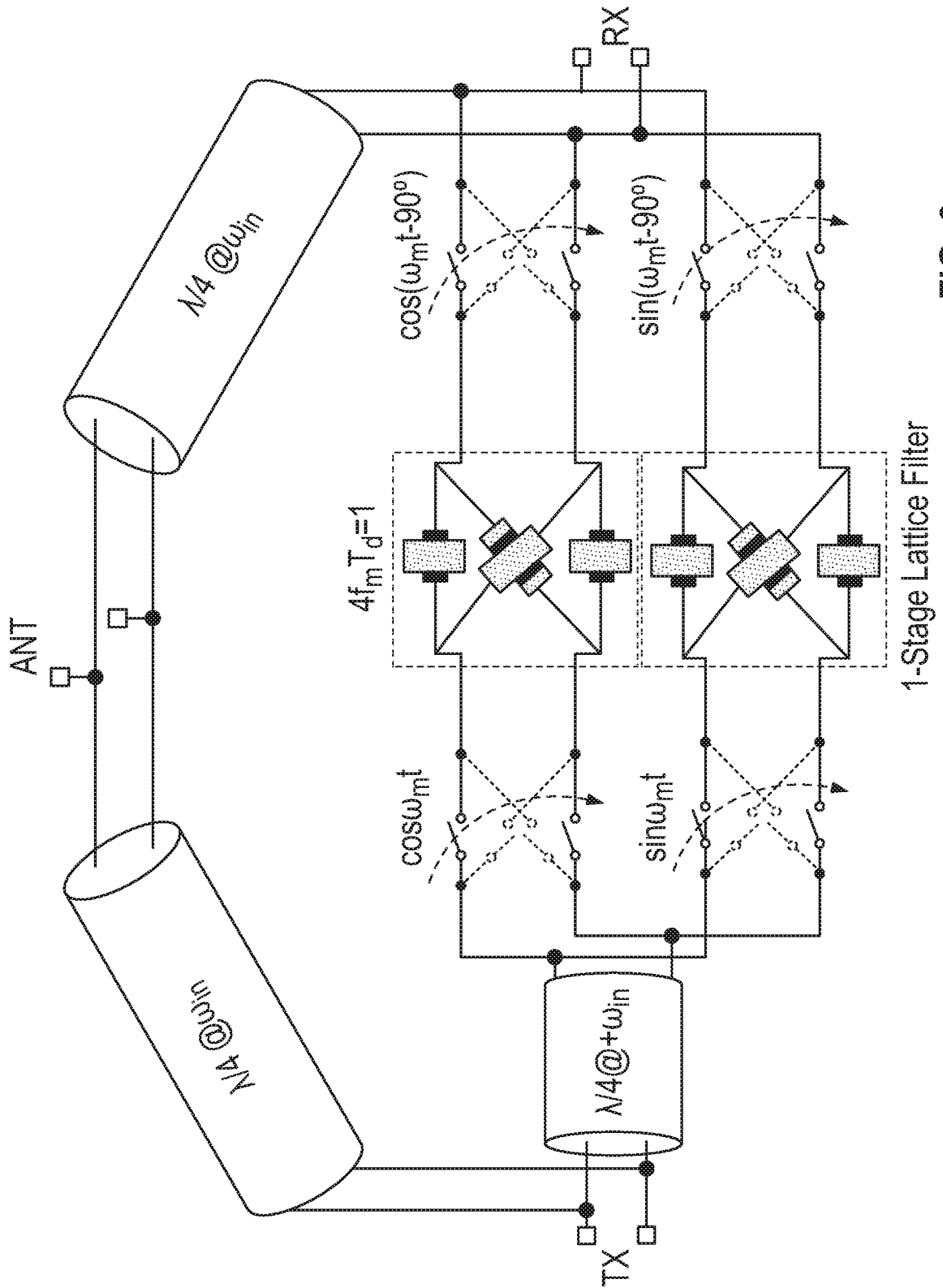


FIG. 6

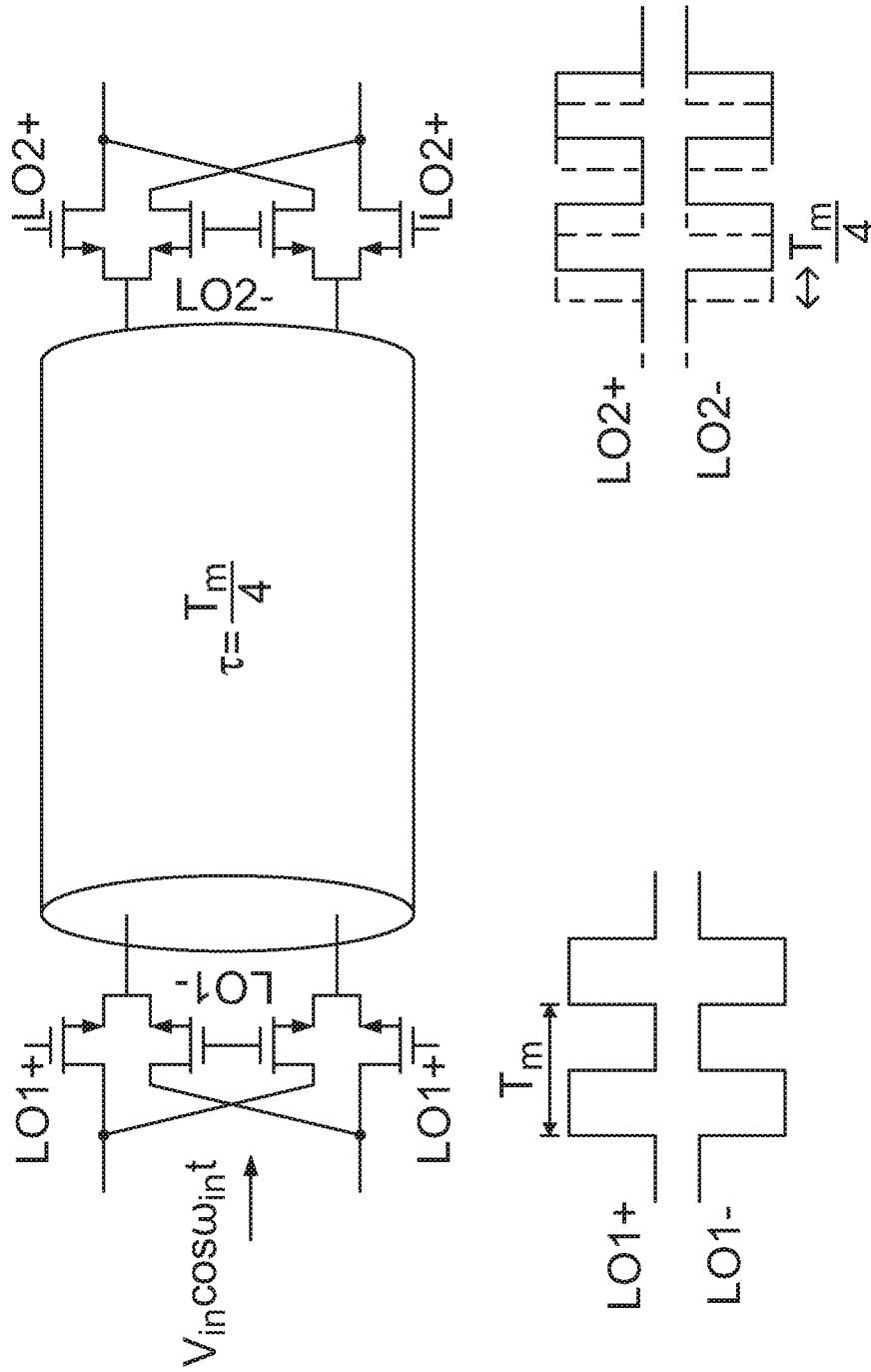
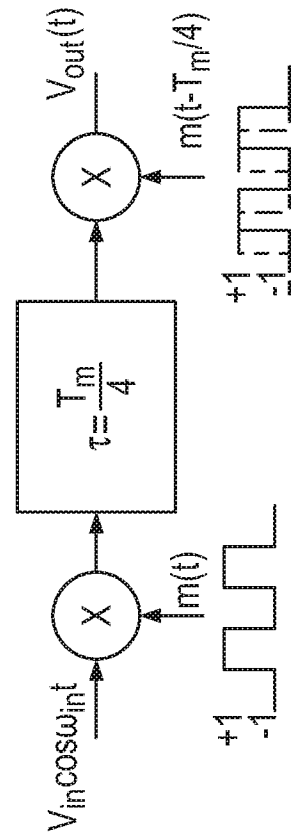
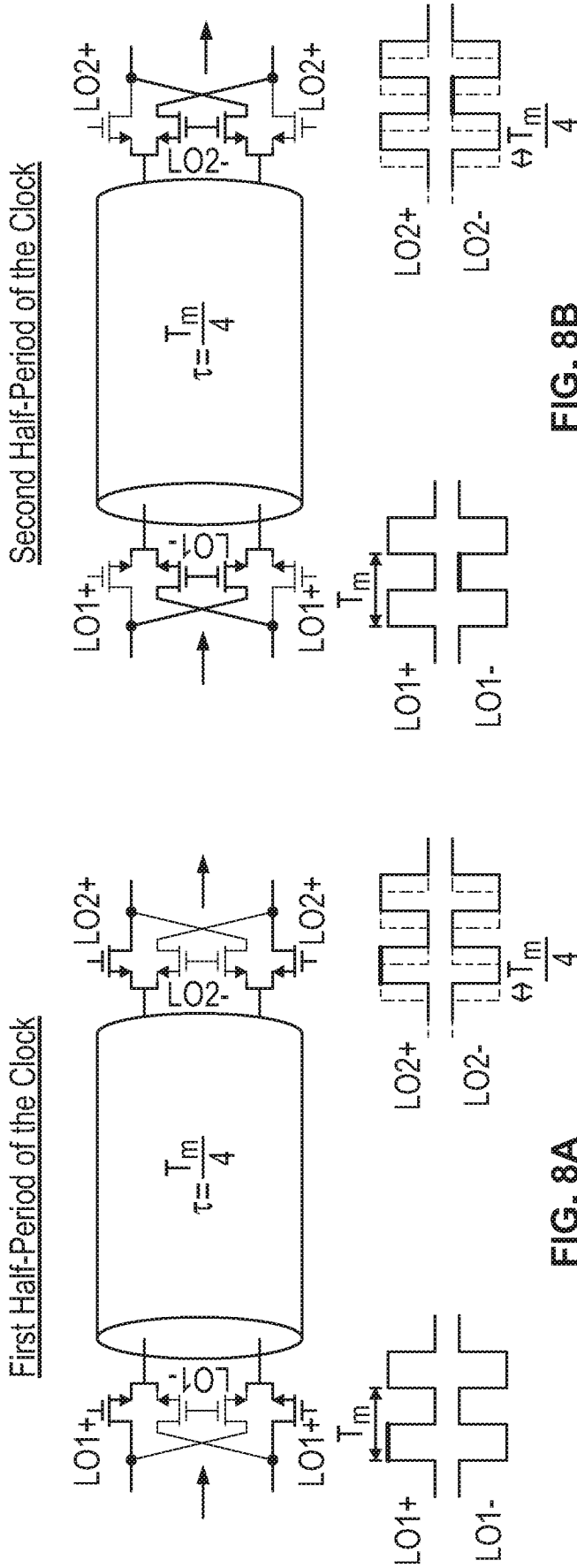


FIG. 7

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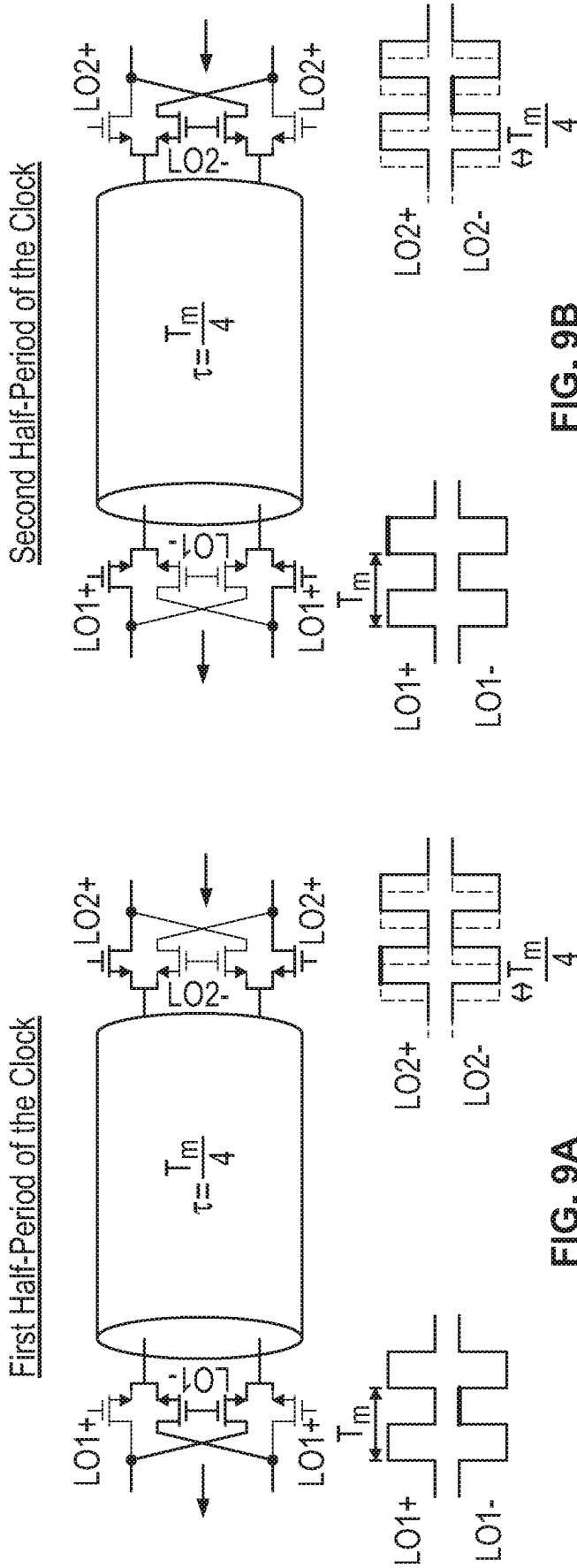


FIG. 9A

FIG. 9B

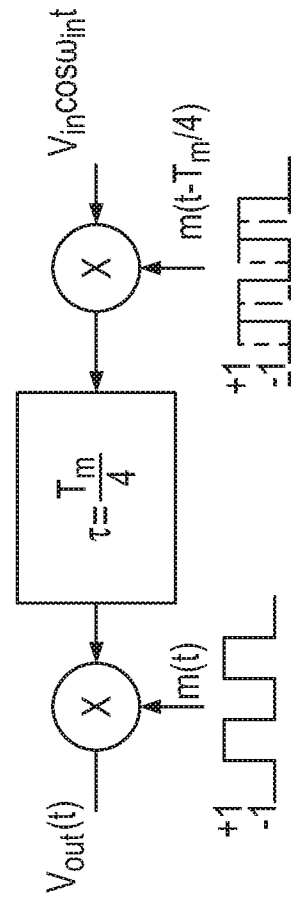


FIG. 9C

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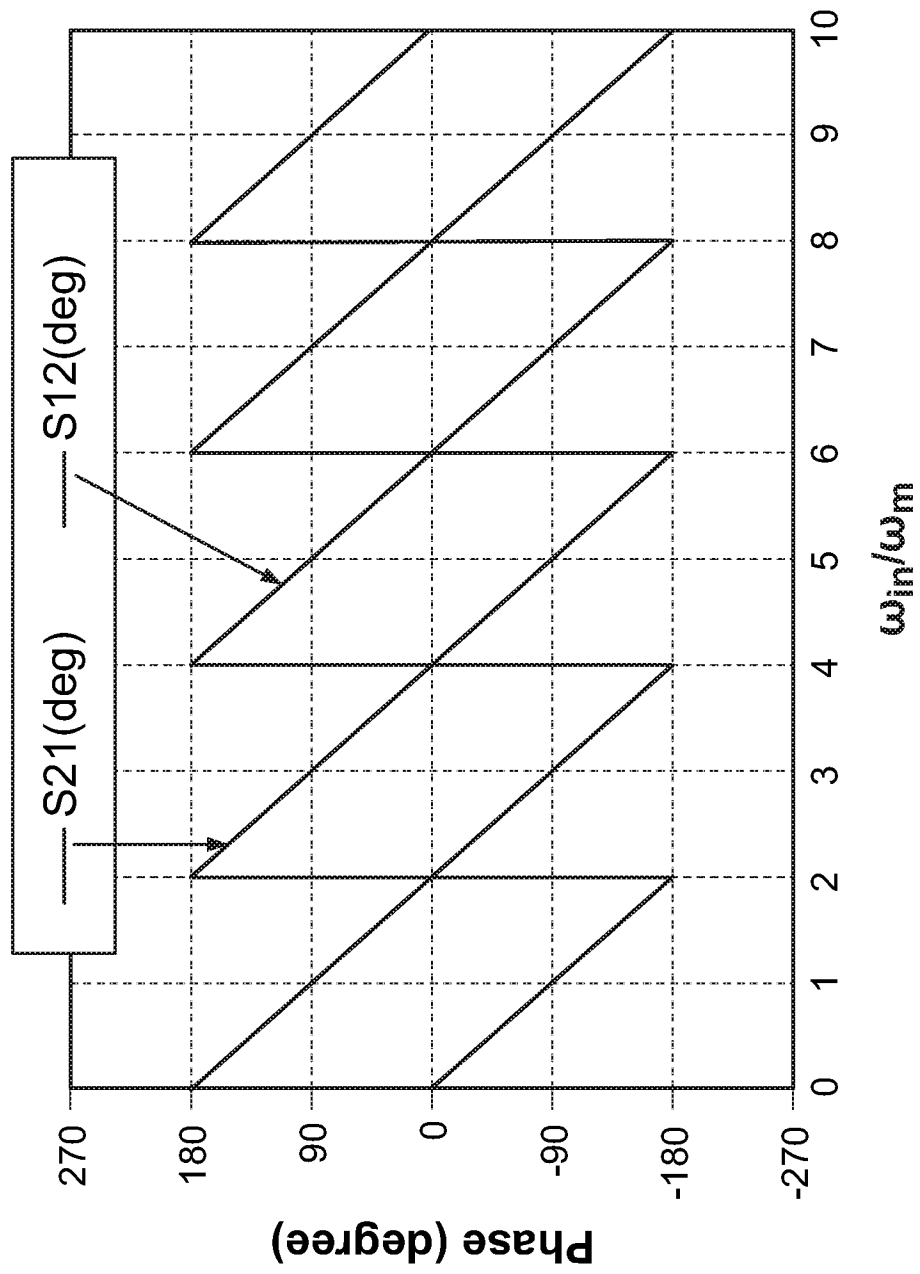


FIG. 10

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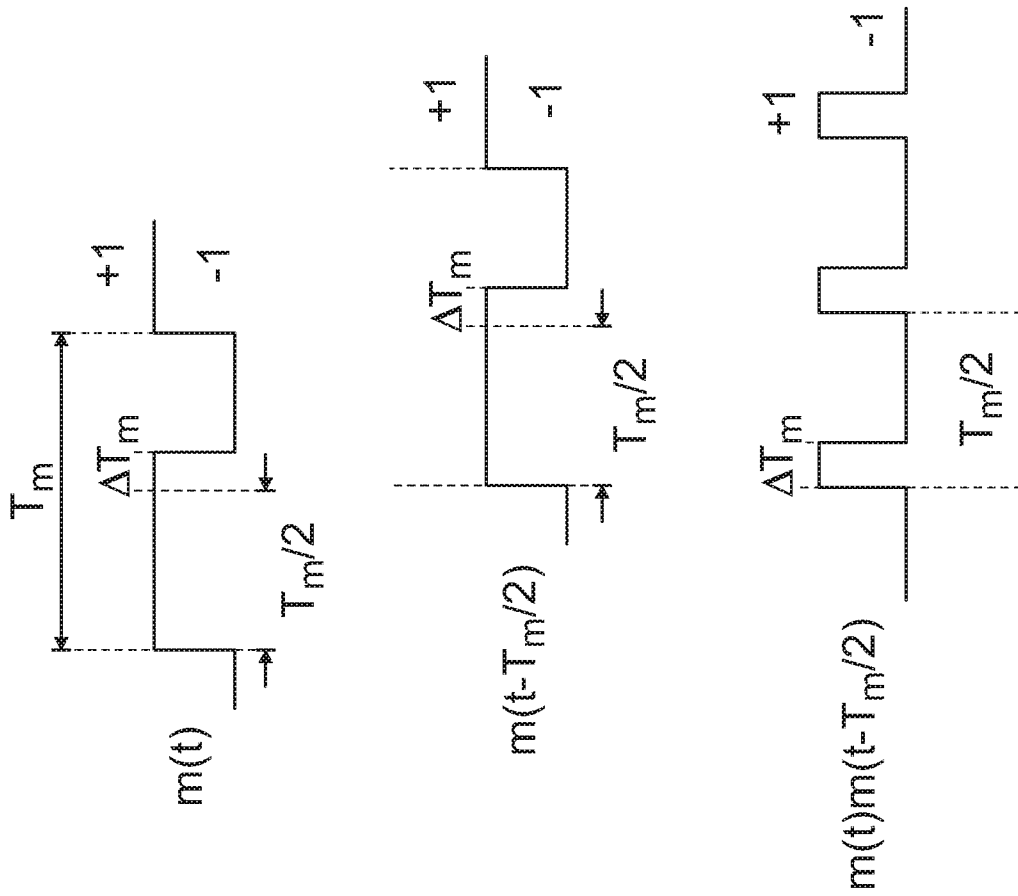


FIG. 11

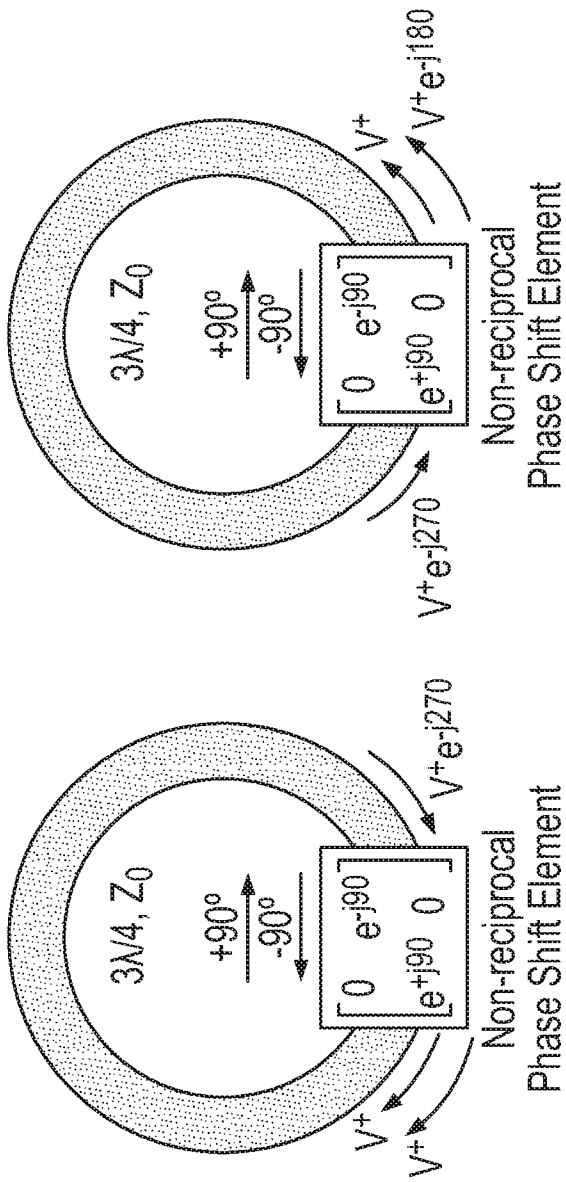


FIG. 12A

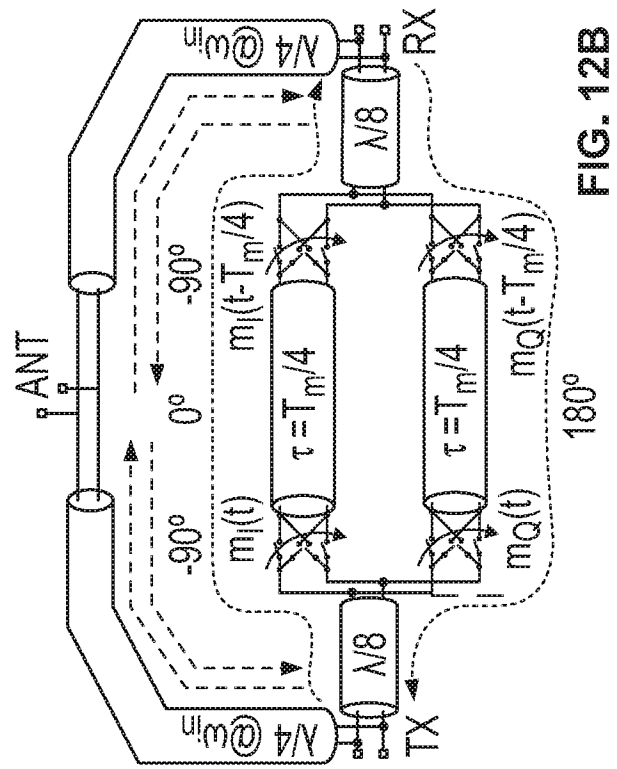


FIG. 12B



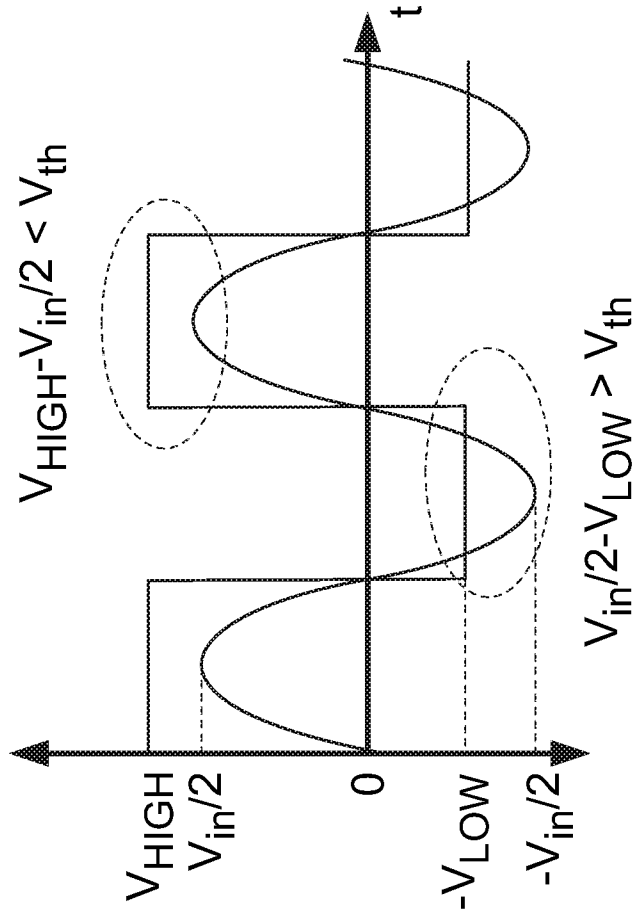


FIG. 14B

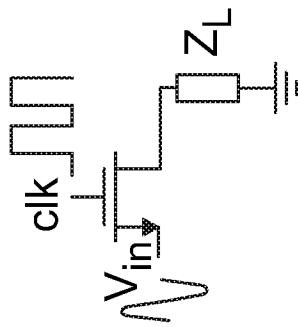


FIG. 14A



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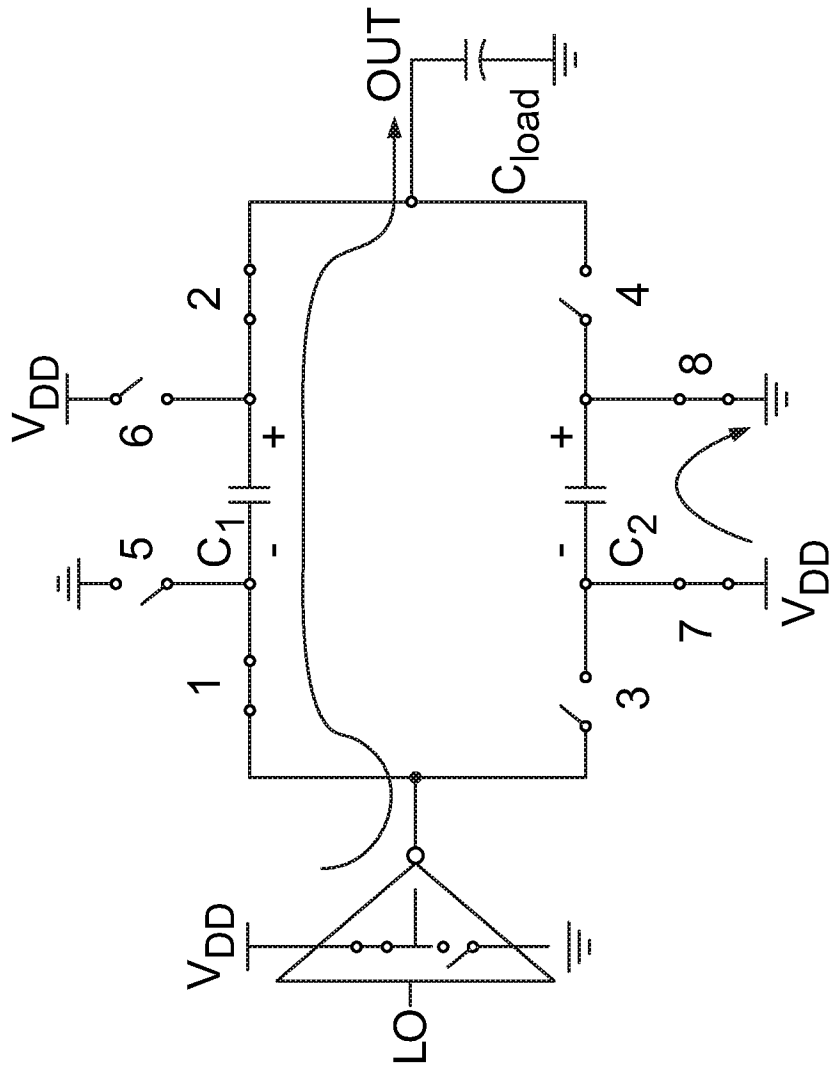
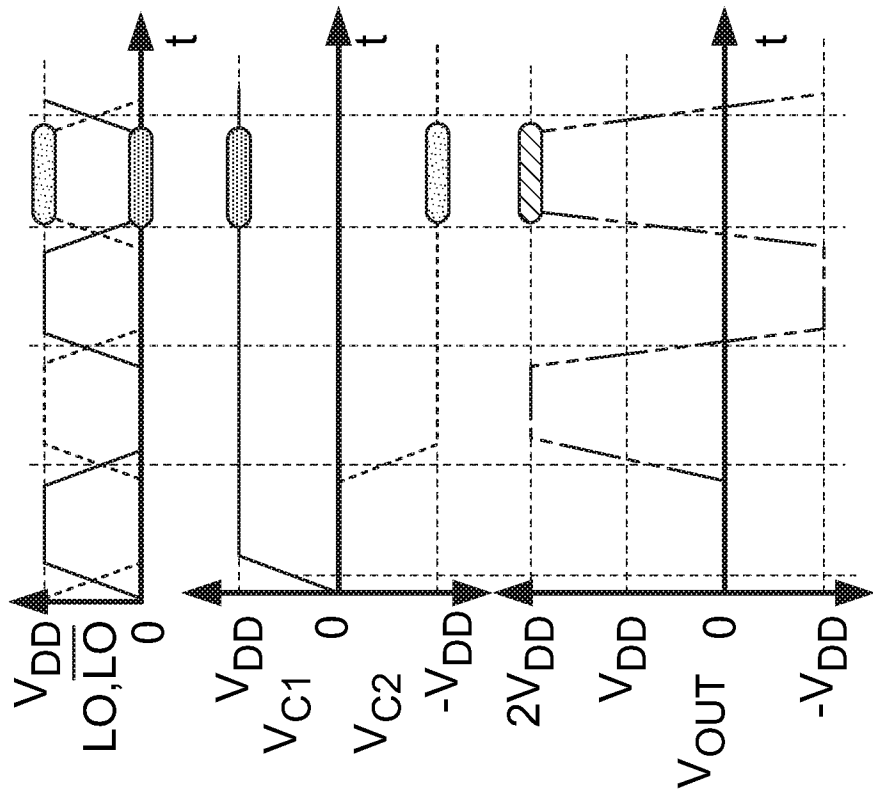


FIG. 16

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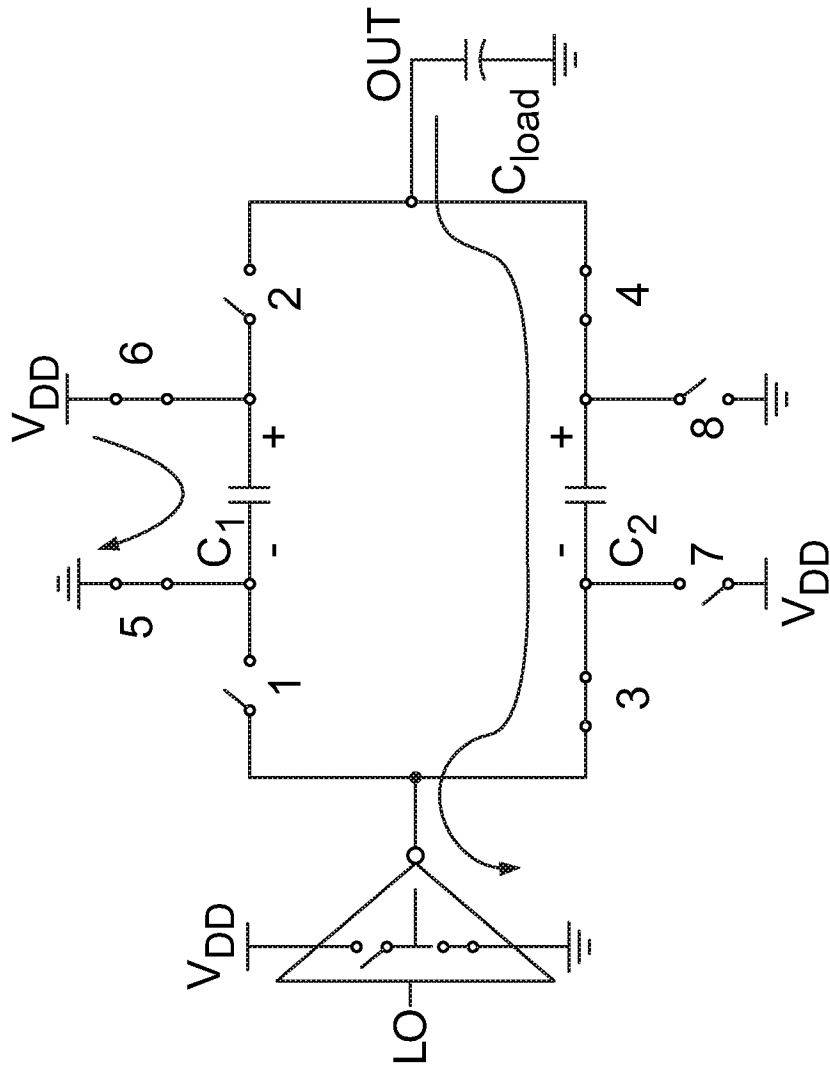
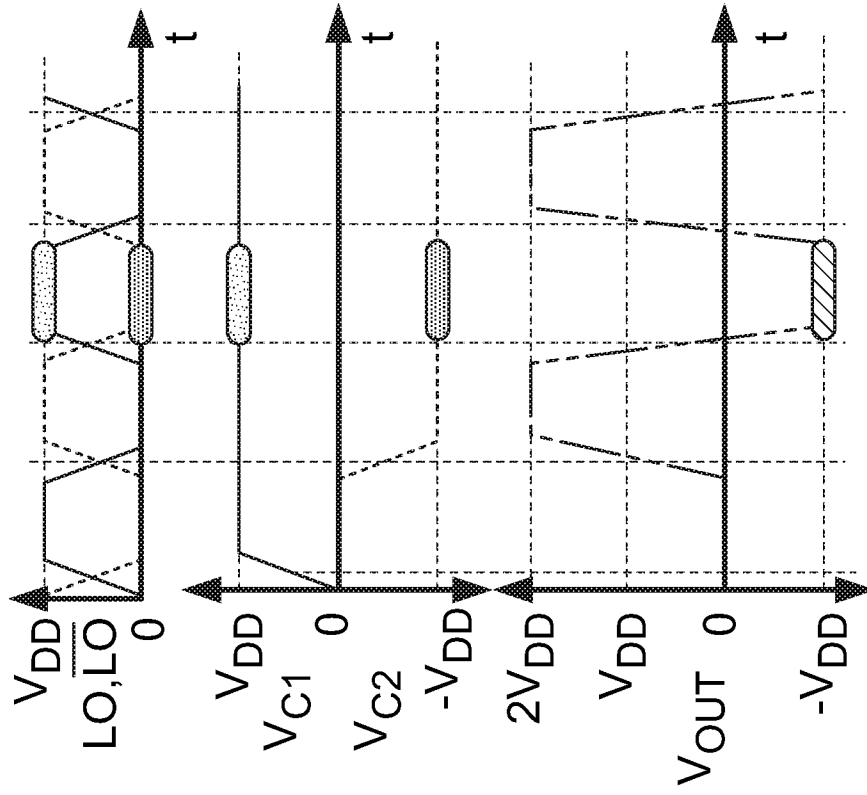


FIG. 17

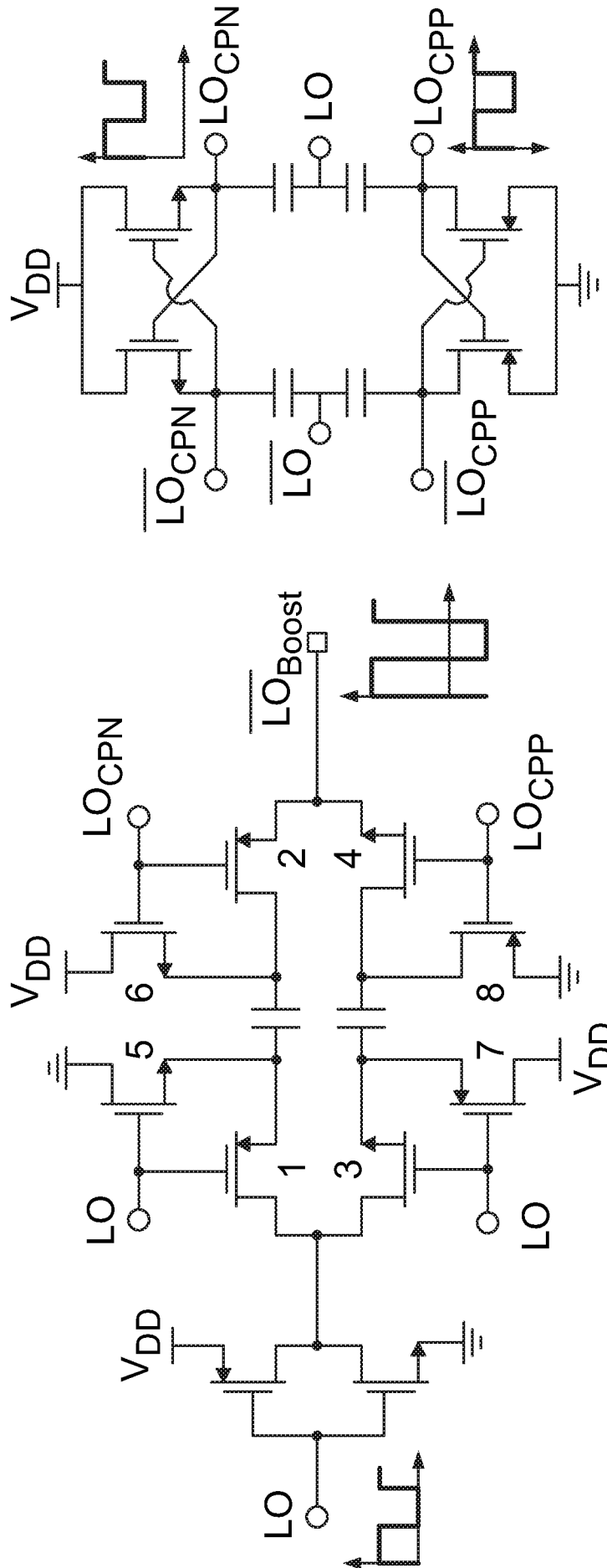


FIG. 18

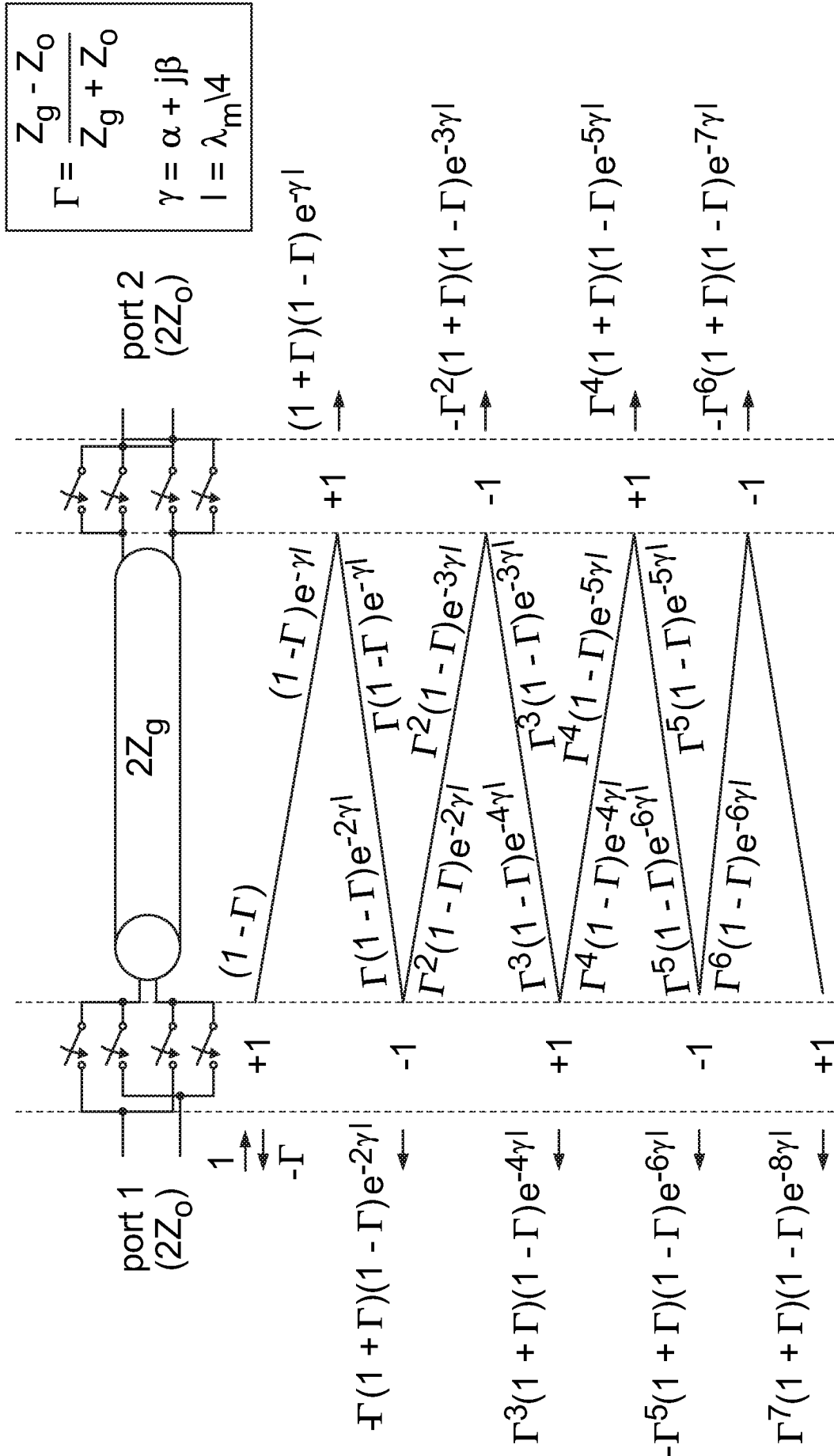


FIG. 19

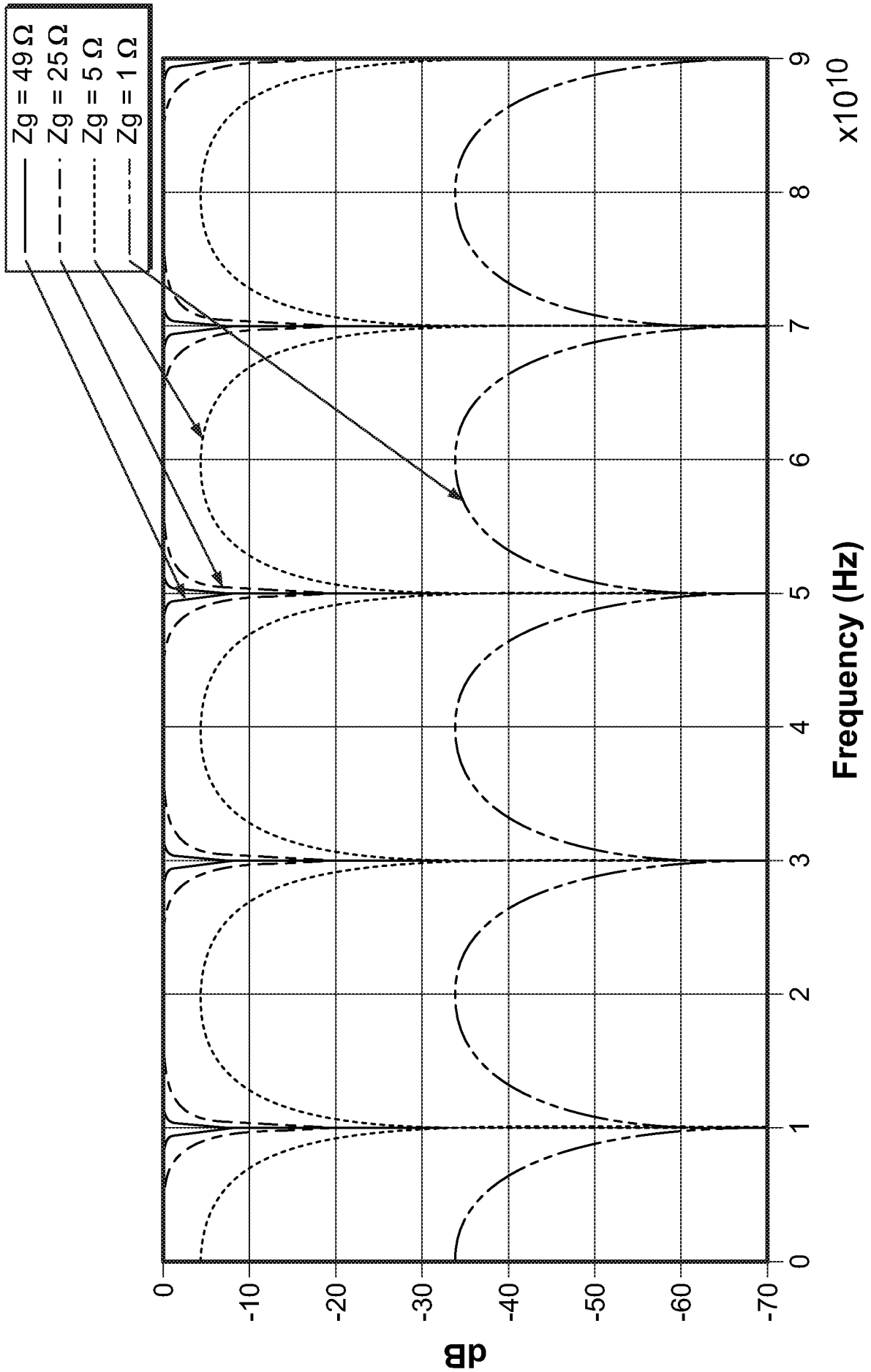


FIG. 20

S11

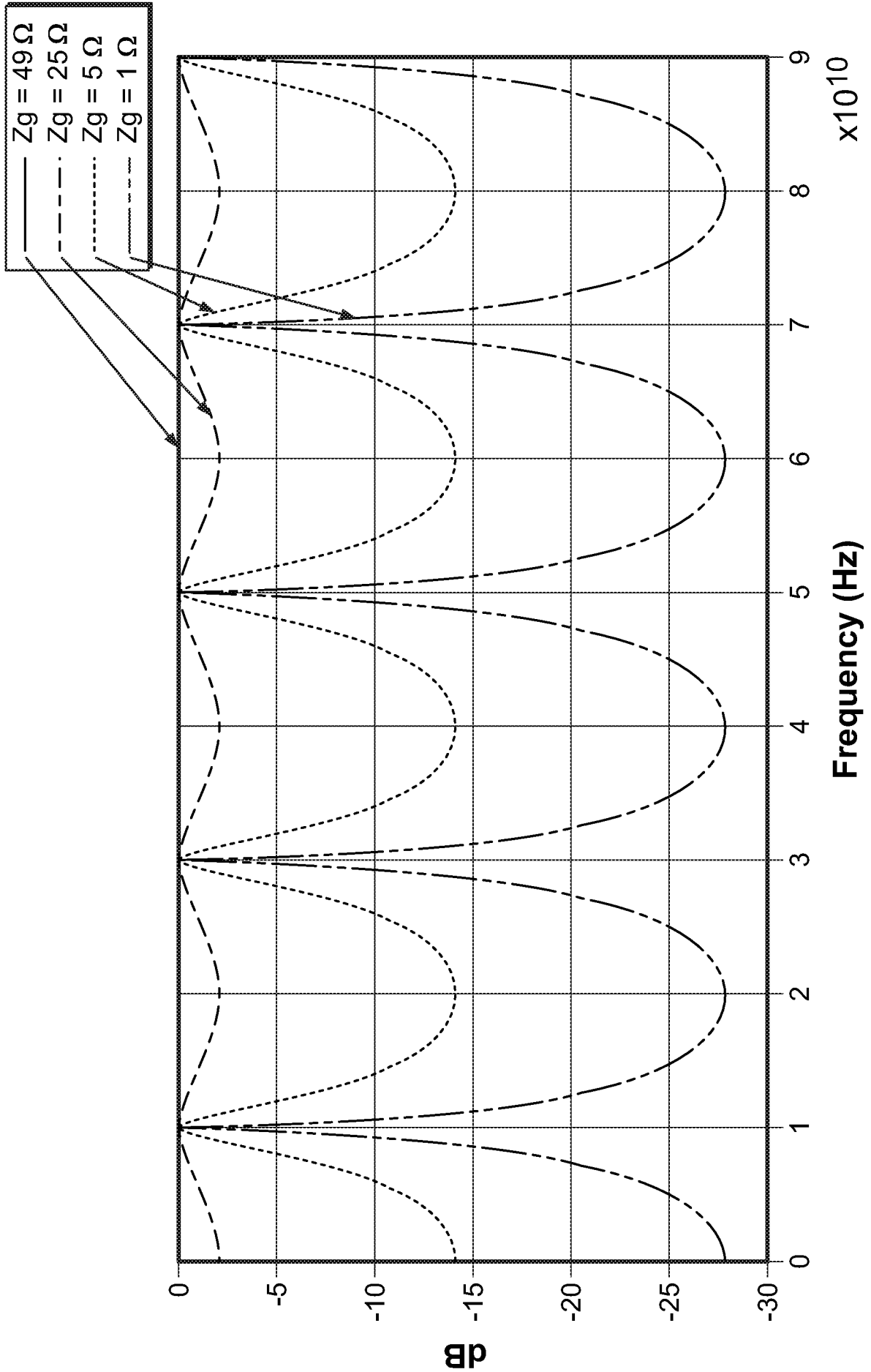


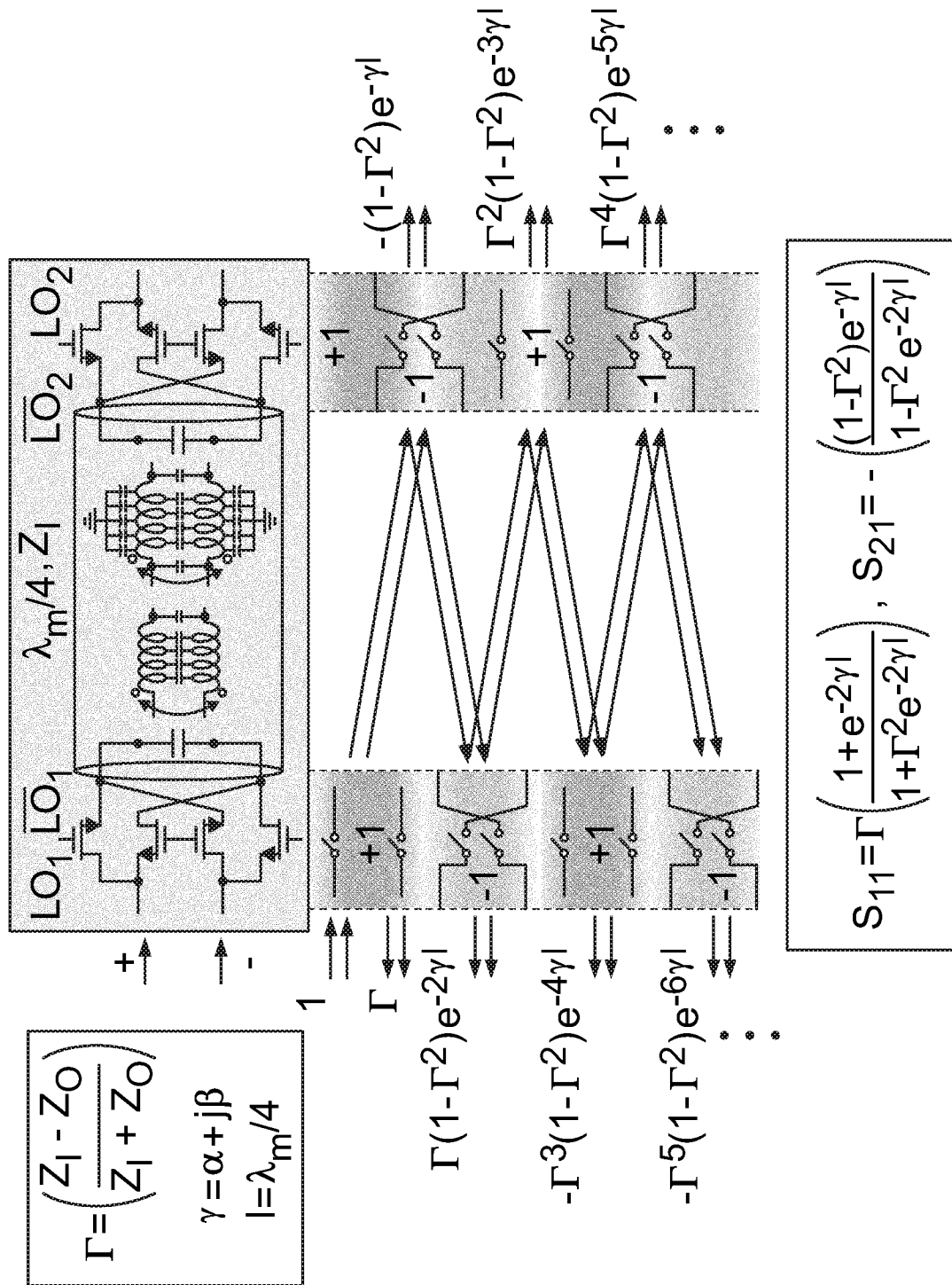
FIG. 21

S21

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Q of gyrator	Q @ 10 GHz	Q @ 30 GHz	Q @ 50 GHz	Q @ 70 GHz
Zg = 50	0	0	0	0
Zg = 10	1.83	5.5	9.15	12.8
Zg = 5	3.87	11.6	19.3	27
Zg = 2	9.8	28.4	48.9	68.3
Zg = 1	19.6	58.89	97.8	136.4

FIG. 22



For  $\beta = (2n+1)\pi/2 \rightarrow S_{11} = 0; S_{21} = +/-j$

FIG. 23

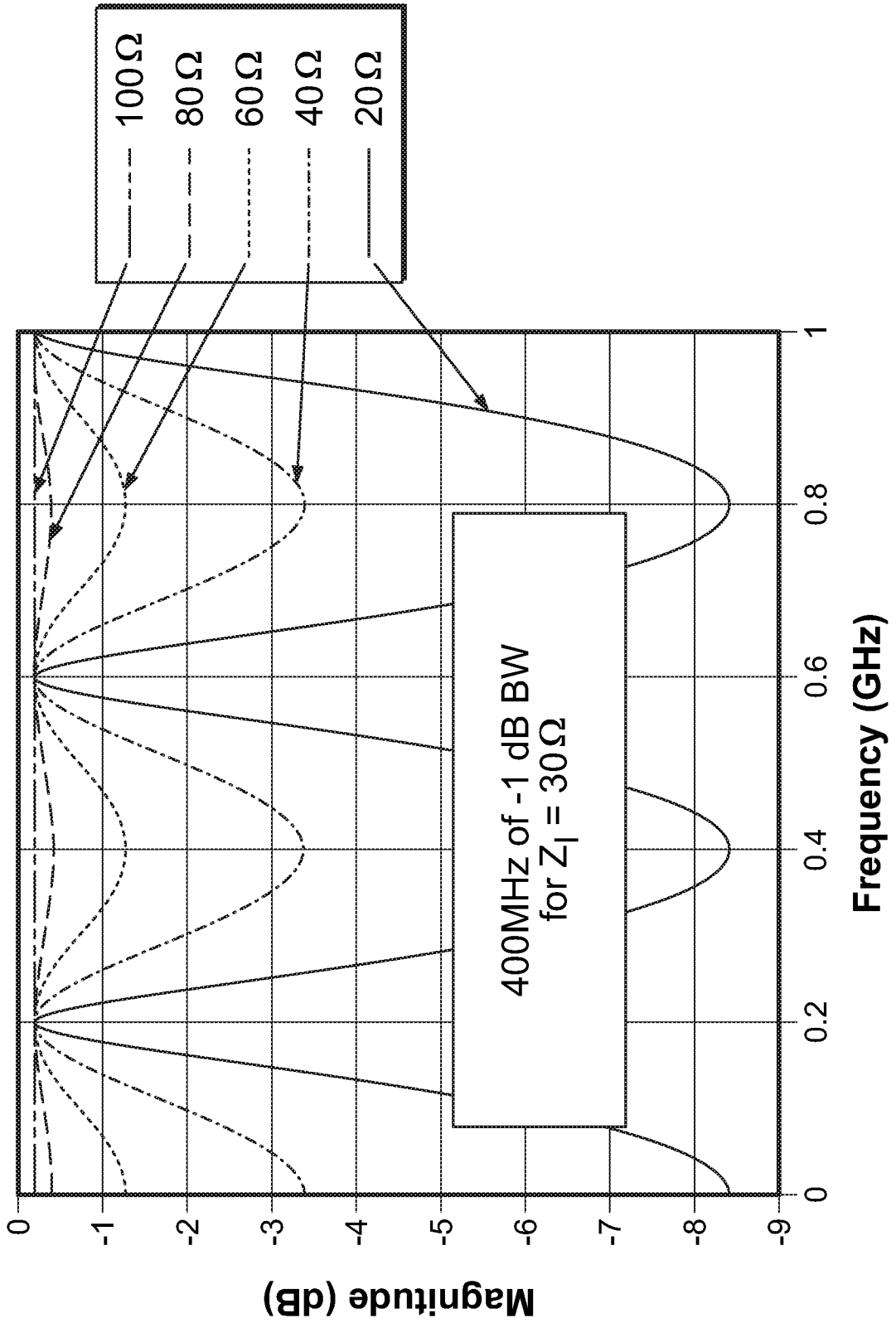


FIG. 24

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2020/014487

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H03D 7/16; H01P 1/38; H01P 1/383; H03D 7/14; H04L 5/14 (2020.01)

CPC - H03D 7/165; H01P 1/38; H01P 1/383; H03D 7/1441; H03D 7/1458; H03D 7/1466; H03D 7/161; H03D 2200/0003; H04L 5/14 (2020.02)

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 370/284; 370/276; 370/282 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2018/075113 A2 (DINC et al) 26 April 2018 (26.04.2018) entire document	1-13, 16
Y	US 6,559,689 B1 (CLARK) 06 May 2003 (06.05.2003) entire document	1-13, 16
A	US 9,253,875 B2 (LENT et al) 02 February 2016 (02.02.2016) entire document	1-17
A	US 9,521,023 B2 (MARTINEZ et al) 13 December 2016 (13.12.2016) entire document	1-17

 Further documents are listed in the continuation of Box C. See patent family annex.

\* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

20 March 2020

Date of mailing of the international search report

08 APR 2020

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