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(54) SEMICONDUCTOR DEVICE MANUFACTURE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London EC2V 8AH, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a method of manufacturing a semiconductor device in which a semiconductor layer is provided on a substrate region of a first conductivity type by epitaxial growth, after which a zone of electrically insulating material is provided locally in the layer, which zone extends from the surface of the layer throughout the thickness of the epitaxial layer and electrically insulates from each other two regions of the second conductivity type situated on either side of the insulating zone.

The invention furthermore relates to a semiconductor device manufactured by using the method.

Integrated semiconductor devices are known comprising a body of semiconductor material of a first conductivity type covered by an epitaxial layer, circuit elements of the said integrated circuit in said body being separated from each other by zones of insulating material, usually of a semiconductor oxide, for example, silicon oxide (SiO_2).

It is known that when such an insulating material is in contact with a semiconductor material an inversion layer (in the case of *p* - type material) or an enhancement layer (in the case of *n* - type material) is formed at the surface of the semiconductor material. Such a layer whose thickness is very small is caused by storage of charge in the dielectric material, the said charge being due to defects and to ions present in the material. This is the case, for example, with the *n*-type inversion layer which is formed in *p*-conductive silicon which is in contact with silicon oxide. When the zone of insulating material is used for insulating from each other two regions of which the conductivity type is opposite to that of the underlying body, the said inversion layer forms a channel which reduces the insulation qualities and which may even give rise to an actual short-circuit.

In order to avoid this drawback it is known to diffuse doping elements determining the conductivity type which is opposite to that of the inversion layer, but it is difficult to restrict the diffusion to the channel zone and to avoid, in the case of for example a substrate covered by an epitaxial layer, the said epitaxial layer experiencing the detrimental influence of the diffused doping elements.

It has also been suggested to locally introduce doping elements prior to the formation of an epitaxial layer, the said doping elements being diffused during the formation of the insulating zone which usually takes place by thermal oxidation. The drawback of this solution, however, is that a mask is indispensable for localizing the doping, while another drawback is that the said solution is restricted to the case in which the realization of the insulating zone comprises a thermal treatment at a high temperature and for a long period of time. The use of the said solution is difficult if the insulating zone is to be formed at low temperature, for example, by oxidation under pressure.

It is a particular object of the invention to avoid the drawbacks of the known method and the invention provides a method by which it is possible to eliminate the current channel which is caused by the inversion layer formed between a semiconductor material and an insulating layer, which channel may cause a short-circuit between regions which are to be insulated from each other.

According to the invention, a method as specified in the opening paragraph is characterized in that a surface layer of the first conductivity type having a higher doping concentration than the substrate region is provided over the entire surface of

the substrate region by ion implantation before growing the epitaxial layer, and in that the insulating zone is then provided over such a depth that it adjoins the said surface layer but does not traverse it completely.

It is to be noted that in the specification reference to ion implantation is to be understood to include also the usually-subsequent annealing treatment.

The inversion layer caused in the semiconductor and situated at the edge of the zone of insulating material is eliminated by the compensation obtained by the implanted doping ions. The implantation requires no thermal diffusion over a long period of time and/or at a very high temperature. The risk of disturbance of the epitaxial layer is no longer to be feared and the method is compatible with oxidation methods performed at low temperature.

The implantation is carried out throughout the entire surface of the substrate region and it is hence not necessary to use a localizing mask.

In certain cases the conductivity type of the epitaxial layer is opposite to the conductivity type of the substrate region, while the regions separated from each other by the insulating zone are formed by parts of the said epitaxial layer. In most of the cases the regions separated from each other by the said insulating layer are formed from strongly-doped surface regions which, prior to the provision of the epitaxial layer, adjoin the surface of the substrate region. Said surface regions of the second conductivity type can be clearly distinguished and afterwards form deep, usually coplanar, strongly-doped regions which partly penetrate into the substrate region and partly into the epitaxial layer. In all the cases the concentration of the implanted doping ions is much smaller than that of the said regions so as not to invert the conductivity type in the parts of the said regions which are situated at the interface between the substrate region and the epitaxial layer.

According to a preferred embodiment of the method according to the invention the implantation occurs *via* a thin layer which transmits the ions and which is previously provided on the said surface of the substrate region and is removed after the implantation and prior to the provision of the epitaxial layer. By implanting doping elements *via* a thin layer which transmits the ions and which is removed afterwards, it is possible to eliminate surface defects and to provide the implanted doping elements over a precise thickness and in a precise concentration; the subsequently performed epitaxial growth necessitates the use of the lowest possible doping concentration. When silicon is used, the thin ion-transmitting layer is preferably formed from silicon oxide.

Methods in accordance with the invention may be used for the manufacture of integrated circuits, in particular when the manufacture of the device includes no thermal treatment of a long duration and at high temperature after the formation of the epitaxial layer on the active surface of the device.

Embodiments of the invention will now be described in greater detail, by way of example, with reference to the accompanying drawing, in which:

Figure 1 is a diagrammatical sectional view of a part of a semiconductor device manufactured by means of a method in accordance with the invention,

Figure 2 is a diagrammatic sectional view of a part of a further semiconductor device manufactured by means of a method in accordance with the invention,

Figure 3 is a diagrammatic sectional view of a part of a third semiconductor device manufactured by means of a method in accordance with the invention,

Figures 4*a* to 4*j* are diagrammatic sectional views in various stages of manufacture of a semiconductor device obtained by using a method in accordance with the invention.

All the Figures are diagrammatic and the dimensions are not to scale, in particular with respect to the thickness dimension, so as to clarify the drawing.

The device shown in Figure 1 comprises a substrate region 1 in the form of a semiconductor body of a first conductivity type. This substrate 1 has thereon a layer 2 which is provided by epitaxial growth and the conductivity type of which is opposite to that of the substrate. The layer 2 has separate regions 3, 4 which are insulated from each other by a zone 5 of insulating material which extends down to the substrate 1. In the proximity of the surface 7 of the substrate 1 a thin layer 6 is provided by ion implantation over the entire surface 7 and the impurity concentration of which is greater than that of the substrate which at this stage is not yet covered by the layer 2, the ions used causing the first conductivity type. A part 8 of the implanted thin layer 6 situated below the insulating layer 5 eliminates the risk of an insulation defect which might be caused by an inversion layer in the substrate 1 along the junction with the insulating material of the zone 5.

The device shown in Figure 2 comprises a silicon substrate 11 in which two substantially coplanar, strongly doped regions 12 and 13 are formed the conductivity type of which is opposite to that of the substrate 11. The substrate has a

surface layer 16 which is of the same conductivity type as the substrate and is obtained *via* implantation. The said layer 16 is formed over the entire surface of the substrate *via* implantation, while after said operation an epitaxial layer 14 is grown, after which, in a direction at right angles to a part 18 of the layer 16 situated between the regions 12 and 13, the layer 14 is etched away and a localized oxidation is carried out until an insulating zone 15 thus formed extends down to the surface layer 16.

The inversion layer which could be caused in the substrate by the insulating zone 15 is eliminated by the ions implanted at 18, so that the short-circuit to which said inversion layer would give rise is prevented. Since the regions 12 and 13 are strongly doped, the doping concentration of the implanted layer is insufficient to invert the conductivity type in said regions, the doping concentration of the implanted zone being 10^3 to 10^5 times smaller than that of the said regions; however, the said concentration is larger than the doping concentration of the semiconductor body, for example 10 to 100 times larger.

The device shown in Figure 3 comprises a silicon substrate 21 in which a strongly doped region 22 is formed the conductivity type of which is opposite to that of the substrate. A layer 26 of the same conductivity type as the substrate is implanted in the said substrate over its entire surface 27, while after the said implantation an epitaxial layer 24 is formed and then, *via* a series of masking, diffusion and oxidation treatments, an insulating zone 25, a diffused zone 23 for contacting the region 22, and a zone 29 (which is provided simultaneously with the zone 23 *via* diffusion) are formed.

The inversion layer which would be caused in the said substrate by the insulating layer 25 is eliminated by the ions implanted in the part 28 of the layer 26. The region 22 and the zones 23, 29 are sufficiently strongly doped to prevent the implanted ions of the layer 26 from inverting the conductivity type of the said region 22 and the said zones 23, 29.

Another embodiment of the manufacture of a semiconductor device by means of a method in accordance with the invention will now be described.

The starting material is a body 31 of weakly doped silicon of *p* - conductivity type, in which the doping concentration is, for example, 10^{15} atoms/cm^3 (Figure 4*a*). On a major surface 32 of the said body 31 an oxide mask 33 is formed *via* oxidation and photoetching (Figure 4*b*), while doping material is deposited *via* the windows present in the said mask, and a prediffusion is carried out to form regions 34 and 35 of *n* - conductivity type which are to form strongly doped buried regions, the ultimate doping concentration in the said region being, for example 10^{21} arsenic atoms/cm^3 or 5.10^{19} antimony atoms/cm^3.

The oxide mask 33 is then removed by a suitable etching treatment (Figure 4*c*), while an oxide layer 37 is grown on the thus obtained free surface 36 (Figure 4*d*) to a thickness of approximately 0.02 micron, the said layer 37 being formed by a thermal oxidation treatment at 1000°C for 10 minutes in a dry oxygen atmosphere.

An implantation of boron ions through the oxide layer 37 is then carried out throughout the relevant surface of the body 31 with an energy of 120 to 180 KeV and a radiation dose of 10^{11} to 10^{13} ions per cm^2. In this manner an implanted layer 38 is obtained (Figure 4*e*) which, after an annealing treatment at 900°C for 15 minutes, has a thickness of 0.6 micron and a maximum concentration of 5.10^{16} to 10^{17} atoms per cm^3.

The next operation is the removal of the oxide layer 37 (Figure 4*f*), for example, by a suitable etching treatment in an etching bath containing hydrofluoric acid and ammonium fluoride. The surface 39 exposed in this manner is prepared for an epitaxial growth process, and a layer 40 of *n* or *p* - conductivity type is provided on that said surface 39 epitaxially from the gaseous phase (Figure 4*g*). The said layer 40 is doped, for example, with arsenic to obtain a concentration of 2.10^{15} to 10^{16} arsenic atoms per cm^3 so that the *n* - conductivity type and a resistivity of 0.5 ohm.cm to 2 ohm.cm are obtained. The thickness of the said layer 40 is 0.8 to 1.6 microns, and is, for example, equal to 1 micron.

A mask 42 is then provided on the surface of the layer 40, for example, a mask of thermal oxide with a thickness of 0.02 to 0.03 micron on which a silicon nitride layer is provided whose thickness is 0.07 to 0.10 micron (Figure 4*h*). Said mask comprises at least one window 41 which is situated directly above the part of the layer 38 between the buried regions 34 and 35 and which is destined to form an insulating zone between two parts of the epitaxial layer 40. *Via* the window 41 of the mask 42 the silicon of the layer 40 is then etched so as to form in this manner a cavity 43 (Figure 4*i*) whose depth is such that after the subsequent oxidation treatment the oxide surface is situated substantially in the same plane as the surface of the layer 40. The said etching treatment is carried out according to known methods, for example by means of a mixture comprising hydrofluoric acid, nitric acid, acetic acid and iodine, and this over a thickness which is approximately half the thickness of the layer 40.

The next treatment is an oxidation carried out according to one of the known methods in such manner that the formed oxide zone 44 (Figure 4*j*) extends down to the layer 38 without traversing it completely. In most of the cases, a heating at high temperature which is required for a thermal oxidation throughout the thickness of the epitaxial layer is detrimental for the device during its manufacture. For example, when it is necessary to prevent considerable diffusion of the dopant from one region into another region, for example, during the formation of very thin base zones of transistors, an insulating zone 44 is provided using a method in which only comparatively low temperatures are necessary, for example, by oxidation at high pressure. The method in accordance with the invention permits the obtaining of a layer 38 which eliminates the inversion layer below the zone 44 without a high-temperature thermal treatment being required, at least in this stage of the manufacture of the device.

The oxidation is carried out, for example, in an atmosphere of saturated water vapour at a pressure between 60 atmospheres (at 800°C) and 90 atmospheres (at 650°C) or in a dry water vapour atmosphere at a pressure between 100 atmospheres (at 800°C) and 250 atmospheres (at 650°C).

The operation lasts a few hours and may also be carried out in an oxygen atmosphere. In the case in which the thickness of the epitaxial layer is 1 micron, the duration of the oxidation is chosen to be so that an oxide thickness of 1.2 microns is achieved; the difference of 0.2 micron is sufficient to ensure the penetration of the insulating zone in the implanted layer, taking into account the required tolerances, for example, a thickness variation of 0.05 micron in the thickness of the epitaxial layer and an equally large variation in the oxide thickness.

WHAT WE CLAIM IS:—

1. A method of manufacturing a semiconductor device in which a semiconductor layer is provided on a substrate region of a first conductivity type by epitaxial growth, after which a zone of electrically insulating material is provided locally in the layer which zone extends from the surface of the layer throughout the thickness of the epitaxial layer and electrically insulates from each other two regions of the second conductivity type situated on either side of the insulating zone, characterized in that a surface layer of the first conductivity type having a higher doping concentration than the substrate region is provided over the entire surface of the substrate region by ion implantation before growing the epitaxial layer, and in that the insulating zone is provided over such a depth that it adjoins the said surface layer but does not traverse it completely.

2. A method as claimed in Claim 1, characterized in that the electrically insulating zone is provided by selective oxidation.

3. A method as claimed in Claim 1 or Claim 2, characterized in that the ion implantation occurs *via* a thin layer provided on the substrate region, which thin layer is removed prior to growing the epitaxial layer.

4. A method as claimed in any of the preceding Claims, characterized in that the said regions of the second conductivity type are formed by the parts of the epitaxial layer separated by the insulating zone.

5. A method as claimed in any of the Claims 1 to 3, characterized in that the said regions of the second conductivity type are buried layers and are provided prior to growing the epitaxial layer, the surface layer obtained by ion implantation having a doping concentration which is lower than that of the buried layers.

6. A method as claimed in Claim 5, characterized in that the surface layer obtained by ion implantantion has a doping concentration which is at least 10^3 and at most 10^5 times lower than that of the buried layers.

7. A method as claimed in any of the preceding Claims, characterized in that the doping concentration of the surface layer obtained by ion implantation is at least 10 times and at most 100 times higher than that of the underlying substrate region.

8. A semiconductor device manufactured by a method as claimed in any of the preceding Claims.

9. A semiconductor device substantially as described with reference to Figure 1 of the accompanying drawings.

10. A semiconductor device substantially as described with reference to Figure 2 of the accompanying drawings.

11. A semiconductor device substantially as described with reference to Figure 3 of the accompanying drawings.

12. A method of manufacturing a

semiconductor device, substantially as described with reference to Figures 4*a* to 4*j* of the accompanying drawings.

13. A semiconductor device manufactured by the method claimed in Claim 12.

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Sheet 1

FIG.1

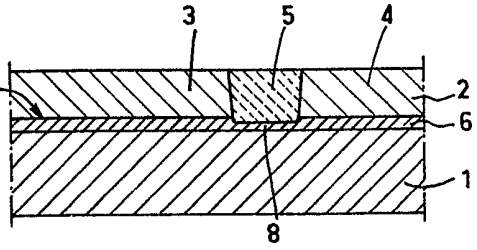


FIG.2

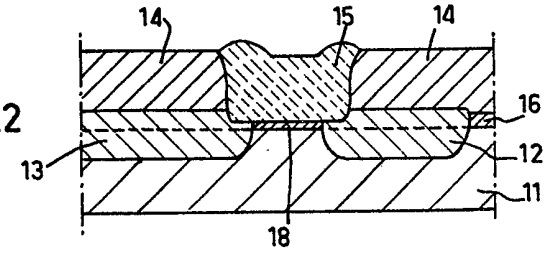
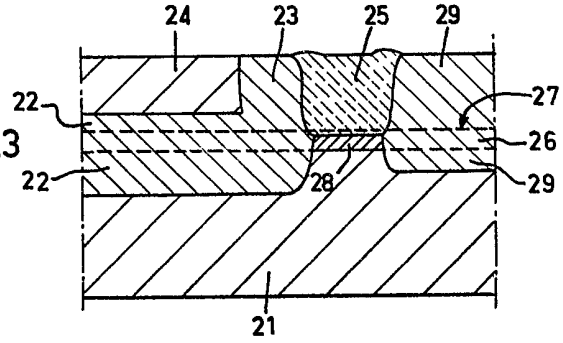


FIG.3



1572854 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

FIG.4a

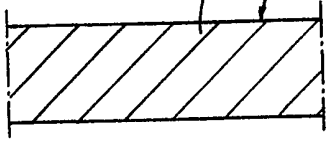


FIG.4b

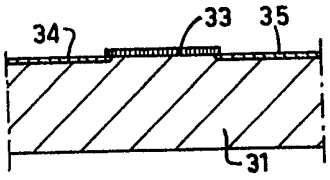


FIG.4c

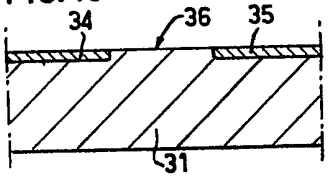


FIG.4d

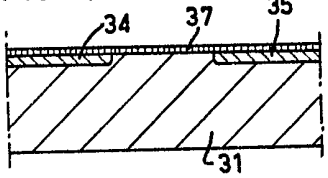


FIG.4e

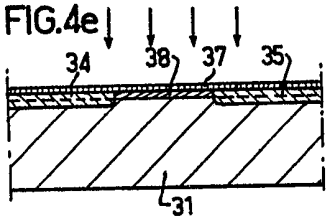


FIG.4f

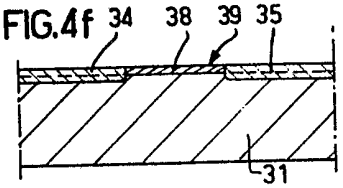


FIG.4g

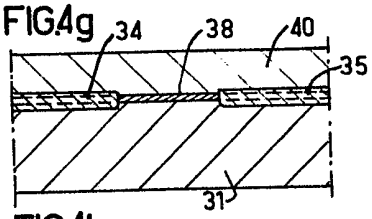


FIG.4h

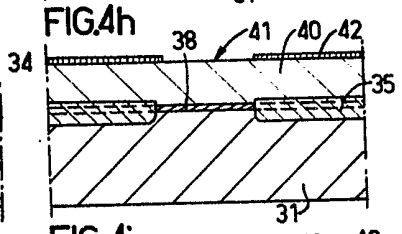


FIG.4i

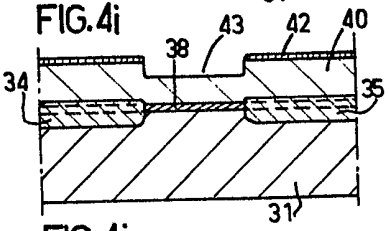


FIG.4j