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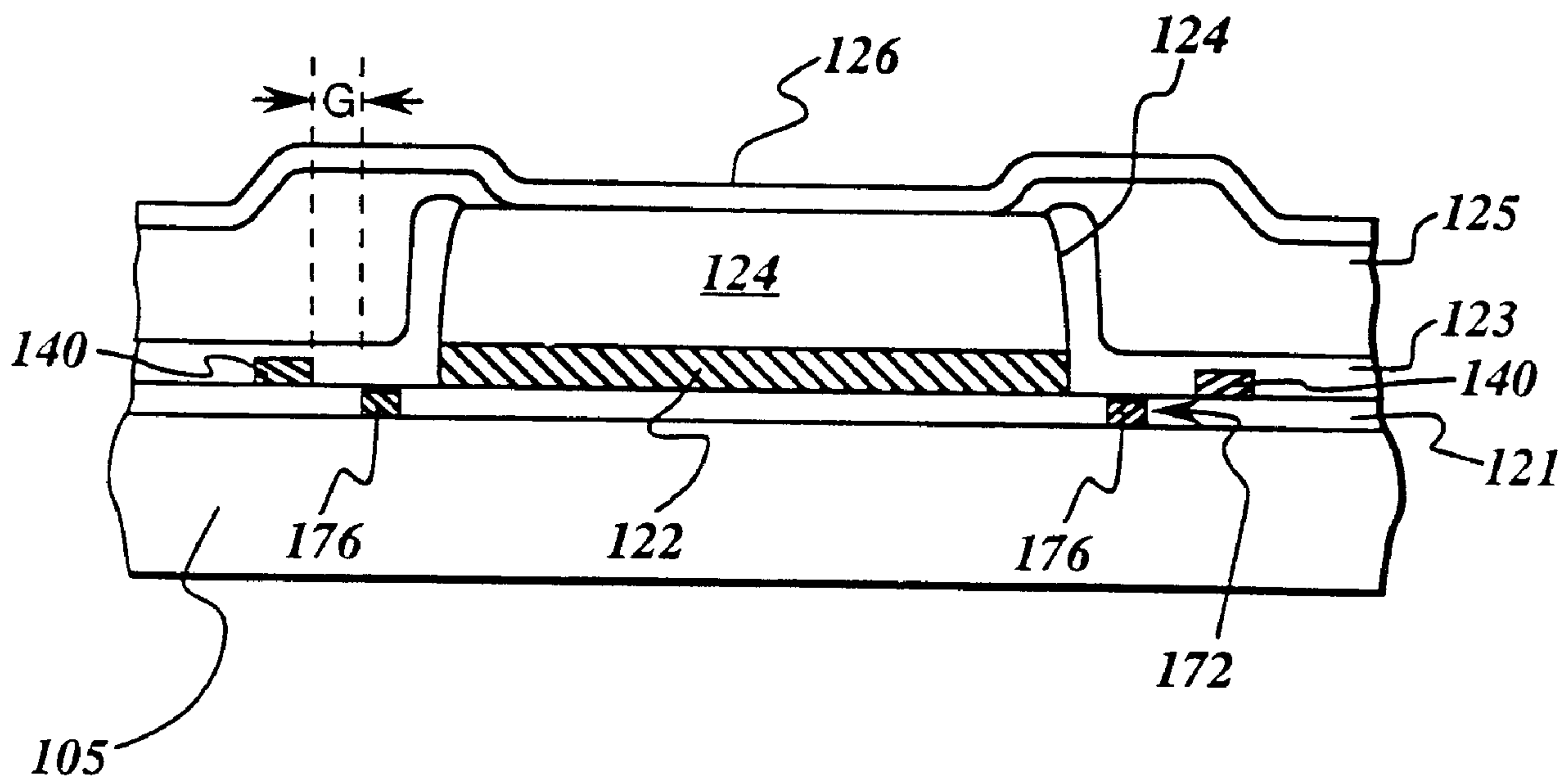
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(54) Titre : IMAGEUR TRANSISTORISE A CONDUCTEURS DE BLINDAGE DE PLAN D'ELECTRODES DE COMMANDE

(54) Title: SOLID STATE RADIATION IMAGER WITH GATE ELECTRODE PLANE SHIELD WIRES



(57) **Abrégé/Abstract:**

A solid state radiation imager that exhibits reduced capacitive coupling between pixel photodiodes and readout data lines, and thus further has reduced phantom images or image artifacts, includes a plurality of shield lines disposed at the same level of the device as the scan lines and associated gate electrodes for the switching transistors. The shield lines include respective pixel shielding spurs oriented along the same axis as the data lines and disposed between portions of the pixel photodiode and adjacent portions of the data lines. The shield lines are typically coupled to a shield voltage source such that the shield lines are maintained at a common potential.

SOLID STATE RADIATION IMAGER
WITH GATE ELECTRODE PLANE
SHIELD WIRES

ABSTRACT

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A solid state radiation imager that exhibits reduced capacitive coupling between pixel photodiodes and readout data lines, and thus further has reduced phantom images or image artifacts, includes a plurality of shield lines disposed at the same level
10 of the device as the scan lines and associated gate electrodes for the switching transistors. The shield lines include respective pixel shielding spurs oriented along the same axis as the data lines and disposed between portions of the pixel photodiode and adjacent portions of the data lines. The shield lines are typically coupled to a
15 shield voltage source such that the shield lines are maintained at a common potential.

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SOLID STATE RADIATION IMAGER
WITH GATE ELECTRODE PLANE
SHIELD WIRES

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Background of the Invention

This invention relates generally to solid state radiation imagers and in particular to structures in such imagers to reduce phantom noise and image artifacts.

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Solid state radiation imagers typically comprise a large flat panel imaging device having a plurality of pixels arranged in rows and columns. Each pixel includes a photosensor, such as a photodiode, that is coupled via a switching transistor to two separate address lines, a scan line and a data line. In each row of pixels, each
15 respective switching transistor (typically a thin film field effect transistor (FET)) is coupled to a common scan line through that transistor's gate electrode. In each column of pixels, the readout electrode of the transistor (e.g., the source electrode of the FET) is coupled to a data line. During nominal operation, radiation (such as
20 an x-ray flux) is pulsed on and the x-rays passing through the subject being examined are incident on the imaging array. The radiation is incident on a scintillator material and the pixel photosensors measure (by way of change in the charge across the diode) the amount of light generated by x-ray interaction with the scintillator. Alternatively, the x-
25 rays can directly generate electron-hole pairs in the photosensor (commonly called "direct detection"). The photosensor charge data are read out by sequentially enabling rows of pixels (by applying a signal to the scan line causing the switching transistors coupled to that scan line to become conductive), and reading the signal from the
30 respective pixels thus enabled via respective data lines (the

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photodiode charge signal being coupled to the data line through the conductive switching transistor and associated readout electrode coupled to a data line). In this way a given pixel can be addressed though a combination of enabling a scan line coupled to the pixel and
5 reading out at the data line coupled to the pixel.

The performance of flat panel imaging devices is degraded by capacitive coupling between data lines and the pixel photodiode electrodes. In particular, during some common imager operations the x-ray flux remains on during readout of the pixels. One
10 example of such operations is fluoroscopy in small or less sophisticated units as might be used in surgery or portable applications; such units use light weight and low cost x-ray generators which must be on continuously to produce an adequate output signal. Such units further typically are not adapted to rapidly cycle the x-ray
15 beam on and off during relevant periods to prevent radiating during the readout periods. Another example are imagers used in conjunction with radiation therapy in which the radiation source is on continuously (to maximize delivered dose) or is pulsed on periodically, which pulses can occur during the readout period. This
20 simultaneous excitation of the imager while reading out pixels results in image artifacts or "phantom" images. The phantom images occur as a result of capacitive coupling between the respective photodiode electrodes and adjacent data lines; during the readout of a given pixel attached to a given data line, the potential of the other pixel
25 electrodes (e.g., the non-read pixels) continue to change as the radiation flux strikes the imager. The change in potential of the pixels not being read out is capacitively coupled into the data line, thereby inducing an additional charge which is read out by the amplifier and presented as part of the signal from the addressed pixel. This effect
30 produces cross-talk or contrast degradation in the image, and is commonly evidenced as bright lines in the display readout.

It is desirable that a solid state imager array exhibit minimal cross-talk and be capable of generating a stable and

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accurate image in multiple modes of operation, including modes in which pixels are being read out while the x-ray flux is being applied.

Summary of the Invention

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A solid state radiation imager that exhibits reduced capacitive coupling between pixel photodiodes and readout data lines, and thus further has reduced phantom images or image artifacts, includes a plurality of shield lines disposed at the same level of the device as the scan lines and associated gate electrodes for the switching transistors. The shield lines include respective pixel shielding spurs oriented along the same axis as the data lines and disposed between portions of the pixel photodiode and adjacent portions of the data lines. The shield lines are separated from adjacent portions of scan lines by a shield line gap distance. The shield line typically includes a bus portion that is oriented along the same axis as the scan lines, or alternatively, along the axis of the data lines, with the shield line spurs extending from the bus portion. The shield lines are typically coupled to a shield voltage source such that the shield lines are maintained at a common potential. The shield lines typically comprise the same conductive material as the scan lines and are fabricated during the imager array fabricating process coincidentally with the deposition and patterning of the scan line conductive material.

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Brief Description of the Drawings

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself,

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however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description in conjunction with the accompanying drawings in which like characters represent like parts
5 throughout the drawings, and in which:

Figure 1(A) is a plan view of a portion of an imager array in accordance with the prior art.

Figure 1(B) is a partial cross-sectional view of a representative pixel taken along line I-I of Figure 1(A).

10 Figure 2(A) is plan view of an imager array having shield lines in accordance with one embodiment of the present invention.

Figure 2(B) is a partial cross-sectional view of a representative pixel taken along line II-II of Figure 2(A) in accordance with the present invention.

15 Figure 3 is a partial cross-section view of a representative pixel in accordance with another embodiment of the present invention.

Detailed Description of the Invention

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A solid state radiation imager 100 comprises a plurality of pixels 110 (a representative one of which is illustrated in Figure 1(A)) that are arranged in a matrix-like imager array pattern comprising rows and columns of pixels 110. For purposes of
25 illustration and not limitation, imager 100 has a first axis 101 that is the axis along which the rows of pixels are aligned, and a second axis 102 that is the axis along which the columns of pixels are aligned. Each pixel 110 comprises a photosensor 120 and a thin film switching

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transistor 130. Photosensor 120 typically comprises a photodiode having a pixel electrode 122 that corresponds with the active (that is, photosensitive) area of the device. Switching transistor 130 typically comprises a thin film field effect transistor (FET) having a gate
5 electrode 132, a drain electrode 134 and a source electrode (or readout electrode) 136. Imager 100 further comprises a plurality of data lines 140 and scan lines 150. At least one scan line 150 is disposed along first axis 101 for each row of pixels in the imager array pattern. Each scan line is coupled to the respective gate electrodes
10 132 of pixels in that row of pixels. At least one data line is disposed along second axis 102 for each column of pixels in the imager array pattern, and is coupled to the respective readout electrodes 136 of pixels in that column of pixels.

A partial cross-sectional view of one pixel 110 is
15 presented in Figure 1(B). Photodiode 120 is disposed over a substrate 105. For ease of illustration, dielectric material layers that may be disposed between pixel electrode 122 and substrate 105 are illustrated with a generic first material layer 121. Photodiode further comprises a photosensitive material body 124 (typically comprising
20 amorphous silicon) that is electrically coupled to a common electrode 126 (typically comprising indium tin oxide) that is disposed over the imager array. A second dielectric material layer 123, typically comprising silicon nitride or the like, extends over a portion of the sidewalls of the photosensitive material body 124, and a third
25 dielectric layer 125, comprising polyimide or the like, is disposed between common electrode 126 and other components in the imager array (except for the contact point to photosensitive material body 124 through a via in second dielectric material layer 123 and third dielectric layer 125).

30 In an imager array as illustrated in Figure 1(B), there are several sources of capacitive coupling between conductive components in the array. For example, there is capacitive coupling between each data line 140 and adjacent pixel electrodes 122. As

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used herein, "adjacent" conductive components refers to components that are spatially near one another but not in direct physical contact so that no direct conductive path (or short circuit) exists between the two components. For analysis purposes, the coupling between a data
5 line and an adjacent photodiode base electrode is broken down into a first capacitance C_{10} (the representation in phantom in Figure 1(B) is for illustrative purposes and does not represent a separate capacitor component in the array) that predominantly represents coupling through the substrate and materials disposed under the pixel
10 electrode 122 (as used herein, "under", "over", "above" and the like are used to refer to the relative position of a component with respect to the substrate, and does not in any way connote any limitation on the orientation, use, or operation of the imager array). A second capacitance C_{20} denotes capacitive coupling through array elements
15 above base electrode 122. It has been observed that the "lower" path capacitance, C_{10} , frequently is a larger contributor to induced capacitance than the "upper" path capacitance, C_{20} . Other sources of capacitive coupling are between pixel electrode 122 and common
20 electrode 126 (denoted as C_{21} in Figure 1(B)) and between data line 140 and common electrode 126 (denoted as C_{22} in Figure 1(B)). The total pixel capacitance (exclusive of typically small parasitic capacitance to scan lines) is expressed as:

$$C_{\text{pixel}} = 2 (C_{10} + C_{20}) + C_{21}$$

C_{pixel} is dominated by C_{21} (base electrode to common electrode)
25 because the pixel electrode area is much larger than the data line area. The total pixel capacitance is a function of the induced capacitance to data lines on either side of the pixel, hence factor of two with respect to the sum of C_{10} and C_{20} .

The capacitive coupling effect is most often of concern in
30 operations in which the imager is excited (that is, the radiation of interest (e.g., x-rays) are incident on the imager) during all or a portion of the time the pixels are being read out. The signal read out during the period of time that the imager is excited will be larger than when

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the imager is not being excited. One approximation of the increase normalized to average signal can be expressed as:

$$2 \left[\left(\frac{C_{10} + C_{20}}{C_{\text{pixel}}} \right) \right] \times \left[\frac{\text{\# pixels per readout channel}}{\text{\# of scan lines with pixels exposed to radiation beam}} \right] \times \left[\frac{\text{integration time}}{\text{line scan time}} \right]$$

The expression $(C_{10} + C_{20})$ represents the coupling capacitance between a single pixel electrode and one adjacent data line; in the array layout, each data line 140 is typically adjacent to two pixel electrodes 140. The ratio of the amplifier integration time to line scan time is relatively small, about 0.85. In continuous fluoroscopy, or in pulsed fluoroscopy if the beam on time is a significant fraction of interframe time, the size of the coupling effect is $2 [(C_{10} + C_{20}) / C_{\text{pixel}}]$, which ratio provide a useful way to characterize the magnitude of the capacitive coupling effect. For imagers having the construction described above with respect to Figures 1(A) and 1(B), the value of $2 [(C_{10} + C_{20}) / C_{\text{pixel}}]$ calculated from the structure or inferred from imager data is in the range of about 0.5%. This value is significant because typical contrast modulation in x-ray imagers is in the range between about 0.1% to about 10%.

In accordance with this invention, radiation imager 100 further comprises a plurality of shield lines 170 (Figures 2(A) and 2(B)) that are disposed so as to reduce the capacitive coupling between a pixel electrode 122 and adjacent data lines 140. Shield lines 170 are disposed at a first level 172 over substrate 105 that is the same level at which scan lines 150 are disposed over substrate 105, and typically shield lines 170 comprise the same conductive material as scan lines (e.g., molybdenum, chromium, titanium, and the like) and are formed coincidentally with the scan lines in the same metal deposition and patterning steps (thus not adding steps to the fabrication process). The structure of the present invention with shield lines 170 provides a shielding effect between the respective pixel

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electrodes 122 and the data lines 140 so that the induced capacitance between these components is reduced, and in particular, induced capacitance value C_{10} (the "lower" path capacitance as illustrated in Figure 1(B)) is reduced by the positioning of the shield lines at a level beneath the pixel electrode. Another approach to reduction of induced capacitance with the use of a ground plane electrode is presented in copending Canadian application Serial No. 2,184,428 entitled "Flat Panel Imaging Device with Ground Plane Electrode" which is assigned to the assignee of the present invention.

Each shield line 170 comprises a bus portion 174 from which respective pixel shielding spurs 176 extend so as to be disposed between a pixel electrode 122 and adjacent data line portions 140. In one embodiment of the present invention that is illustrated in Figure 2(A), shield line bus portion 174 is aligned along first axis 101 parallel to rows of pixels 110; alternatively, shield line bus portion 174 is oriented along second axis 102 parallel to columns of pixels 110.

Shielding spurs 176 are disposed so as to be separated from adjacent portions of data line 140 by a shield line gap distance "G", which distance is in the range of between about 2 μm and about 20 μm , and commonly is about 5 μm (as illustrated in Figure 2(A), gap distance G is shortest lateral distance portions of separating shield line 170 from portions of data line 140). The minimum value of the shield line gap distance is generally limited by processing techniques (e.g., photolithographic processes) and the resolution with which conductive structures can be reliably fabricated in the imager and the maximum distance determined by considerations relating to fill factor and optimizing the portion of the array area that comprises the active area of the photodiodes.

In one embodiment of the present invention, as illustrated in Figure 2(A) and 2(B), shield line 170 is disposed such

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that it does not underlie any portion of pixel electrode 122. In an alternative embodiment of the present invention as illustrated in Figure 3, shield line 170 underlies pixel electrode 122 by an overlap distance "D", which is typically in the range between about 1 μm and about 20 μm . The width of the shield spur lines can thus vary between about 2 μm and about 50 μm dependent upon the amount, if any, of overlap distance D.

In modeling analyses, the shield line structure illustrated in Figures 2(A) and 2(B) exhibits greatest effectiveness in reducing capacitance at relatively small shield line gap distances, e.g., less than about 5 μm . Such analyses (based on a device with a structure similar to that illustrated in Figure 2(A) and 2(B)) suggest a reduction of capacitance between data line 140 and pixel electrode 122 from a value of about 0.1 pf/cm to a value of about 0.06 pf/cm for a gap distance of about 2 μm ; and a reduction of capacitance from a value of about 0.09 pf/cm to a value of about 0.05 pf/cm for a gap distance of about 5 μm .

Disposition of portions of shield line 170 under pixel electrode 122 serves to enhance the effectiveness of shield line 170 in reducing capacitance between data line 140 and pixel electrode 122; typically a reduction of capacitance from a value of about 0.1 pf/cm to a value of about 0.001 pf/cm for a gap distance of about 5 μm .

Shield lines 170 are further coupled to a shield common voltage source 190 (Figure 2(A)). Shield common voltage source 190 maintains the shield line (and the shield line spurs attached thereto) disposed around a pixel that is being addressed at a fixed potential. In the arrangement illustrated in Figure 2(A), each shield line is coupled to voltage source 190 such that all shield lines are maintained at the same constant potential during array operation. The presence of the shield lines tends to disrupt electric field lines between pixel electrode 122 and data line 140, thus reducing the capacitance between those two components of the imager array.

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Alternatively, shield common voltage source 190 comprises the same voltage source used for array common electrode 126, and shield lines are coupled to common electrode 126 through vias 177 (a representative one of which is illustrated in Figure 2(A); for ease of
5 illustration alternative embodiments are shown in one figure, although typically only one type of connecting structure would be used in a give imaging array) opened in the array to provide a conductive path between shield line 170 at the first level of the array and the common electrode material (typically indium tin oxide) disposed over the
10 photodiode structures. Alternatively, shield lines 170 can be coupled to an adjoining pixel's scan line 150 (not illustrated) such that the shield lines for a given row of pixels is maintained at the same potential as a scan line for another row of pixels, typically the next adjoining row of pixels. In this way, the shield line is held at a
15 constant potential while a particular row of pixels is being addressed; the shield line will undergo a change in potential when the scan line to which it is coupled is addressed, but at that time the particular row of pixels that is shielded by that shield line is not being addressed.

The shield line structure of the present invention thus
20 enhances imager performance by reducing induced capacitance between data lines and pixel electrodes, thereby reducing phantom images or image artifacts in images.

It will be apparent to those skilled in the art that, while the invention has been illustrated and described herein in
25 accordance with the patent statutes, modifications and changes may be made in the disclosed embodiments without departing from the true spirit and scope of the invention. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

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What is claimed is:

1. A solid state radiation imager for generating images with reduced image artifacts during read-out of the imager and having components disposed in levels above a substrate, comprising:

a plurality of pixels disposed in an imaging array pattern comprising rows and columns, each of said pixels comprising a photosensor coupled to a thin film switching transistor;

a plurality of scan lines disposed at a first level with respect to said substrate along a first axis of said imaging array pattern, each row of pixels in said imaging array pattern having a respective scan line, each of said respective scan lines being coupled to a respective gate electrode in said thin film switching transistors for each pixel disposed along the respective row of pixels in said imaging array pattern;

a plurality of data lines disposed at a second level with respect to said substrate along a second axis of said imaging array pattern, each column of pixels in said imaging array pattern having a corresponding data line, each of said respective data lines being coupled to a respective readout electrode in said thin film switching transistors for each pixel disposed along the respective column of pixels in said imaging array pattern;

a plurality of shield lines disposed at said first level with respect to said substrate and separated from adjacent portions of said data lines by a shield line gap distance, each of said shield lines further comprising respective pixel shielding spurs disposed along said second axis between portions of said pixels and adjacent portions of said data lines.

2. The imager of claim 1 wherein said pixel shielding spurs are disposed along said second axis on opposite sides of each of said pixels.

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- 3. The imager of claim 2 wherein said shield lines comprise the same conductive material as said scan lines.**
- 4. The imager of claim 3 wherein the width of said respective pixel shielding spurs is in the range between about 2 μm to about 50 μm .**
- 5. The imager of claim 3 wherein said shield line gap distance is in the range between about 2 μm and 20 μm .**
- 6. The imager of claim 3 wherein each of said pixels comprises a photosensitive active area and portions of said respective pixel shielding spurs oriented along said second axis underlie the active region of the respective pixel by a pixel overlap distance between about 1 μm and about 20 μm .**
- 7. The imager of claim 1 wherein the shield line disposed to shield a respective row of pixels is electrically coupled to the scan line for a row of pixels other than the row said shield line is disposed to shield.**
- 8. The imager of claim 1 wherein each of said shield lines comprises a bus portion, said respective pixel shielding spurs extending from said bus portion of said shield line.**
- 9. The imager of claim 8 wherein said shield line bus portion is aligned along said first axis.**
- 10. The imager of claim 8 wherein each of said shield lines disposed within said imaging array pattern is coupled to a shield voltage source such that said shielding lines are maintained at a fixed potential.**

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11. The imager of claim 10 wherein said radiation imager comprises a common electrode and said shield lines are coupled to said common electrode through at least one via connection.

12. The imager of claim 10 wherein said shield voltage source is disposed outside said imaging array pattern.

13. The imager of claim 8 wherein said shield line bus portion is aligned along said second axis.

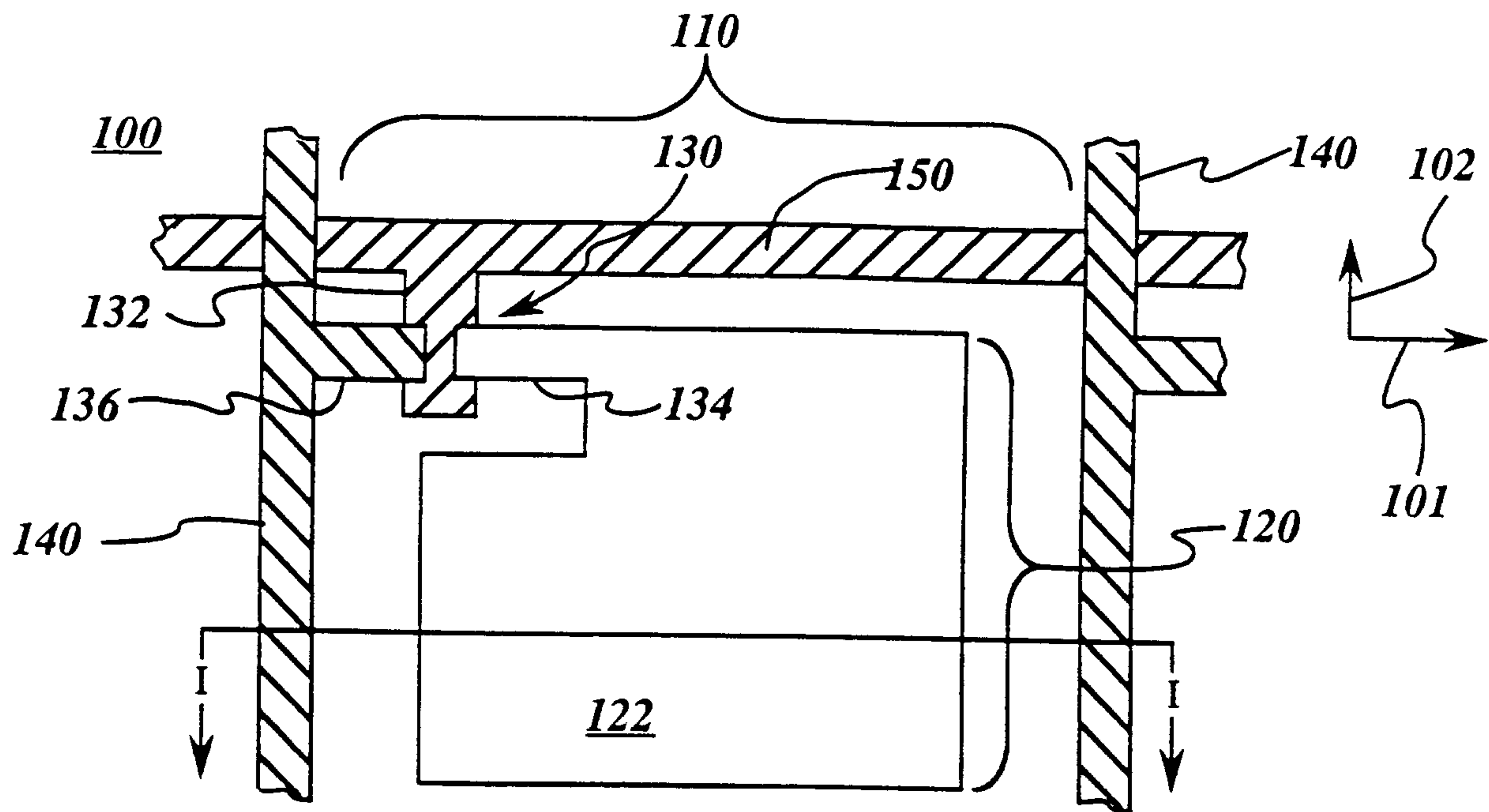


fig. 1A
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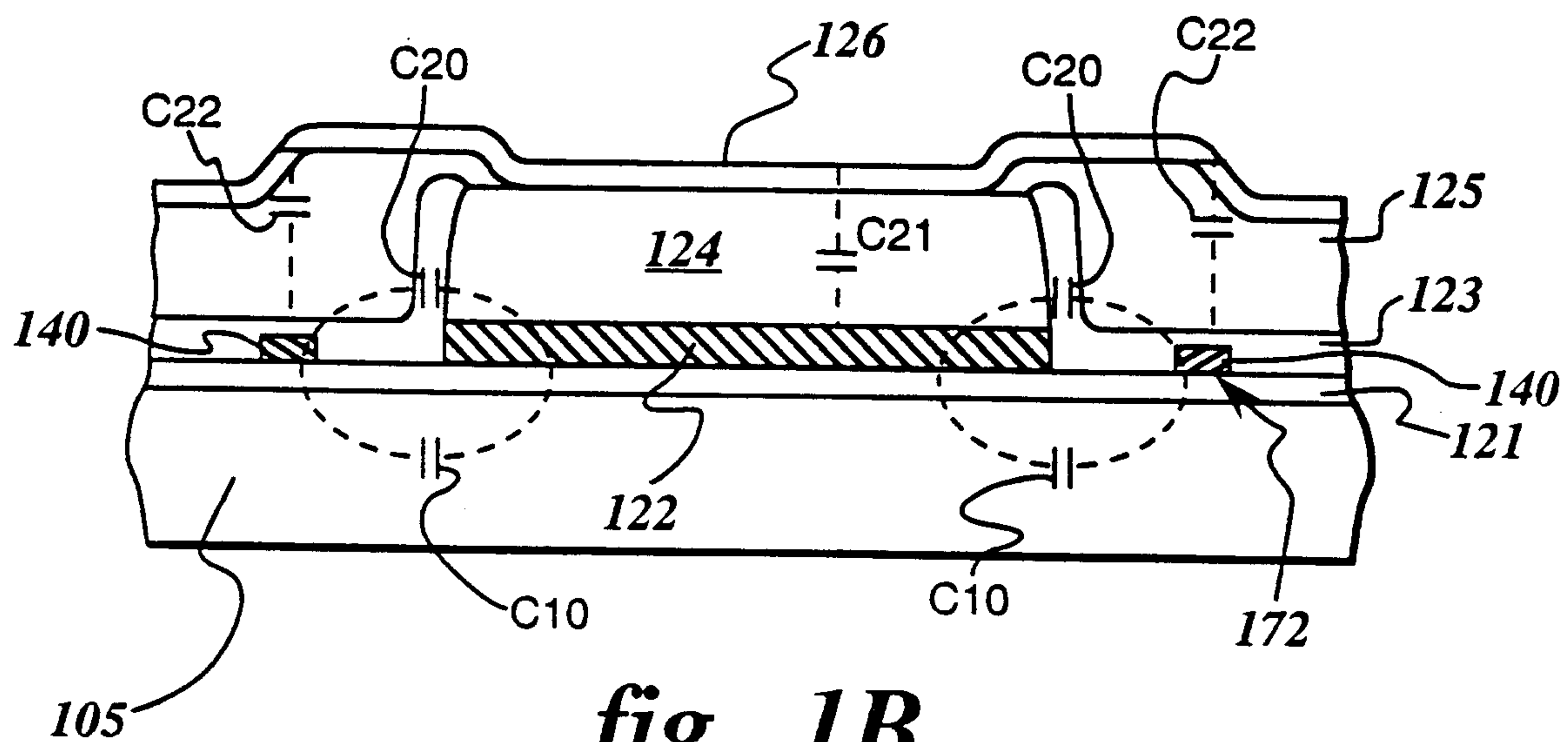


fig. 1B
PRIOR ART

