



**(43) International Publication Date**  
**21 December 2007 (21.12.2007)**

**(10) International Publication Number**  
**WO 2007/145727 A2**

**(51) International Patent Classification:**  
**G01R 1/06 (2006.01)**

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**(21) International Application Number:**  
PCT/US2007/010800

**(81) Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

**(22) International Filing Date:** 3 May 2007 (03.05.2007)

(25) **Filing Language:** English

(26) **Publication Language:** English

**(30) Priority Data:**

60/813,119	12 June 2006 (12.06.2006)	US
60/831,477	17 July 2006 (17.07.2006)	US
11/710,225	22 February 2007 (22.02.2007)	US

**(84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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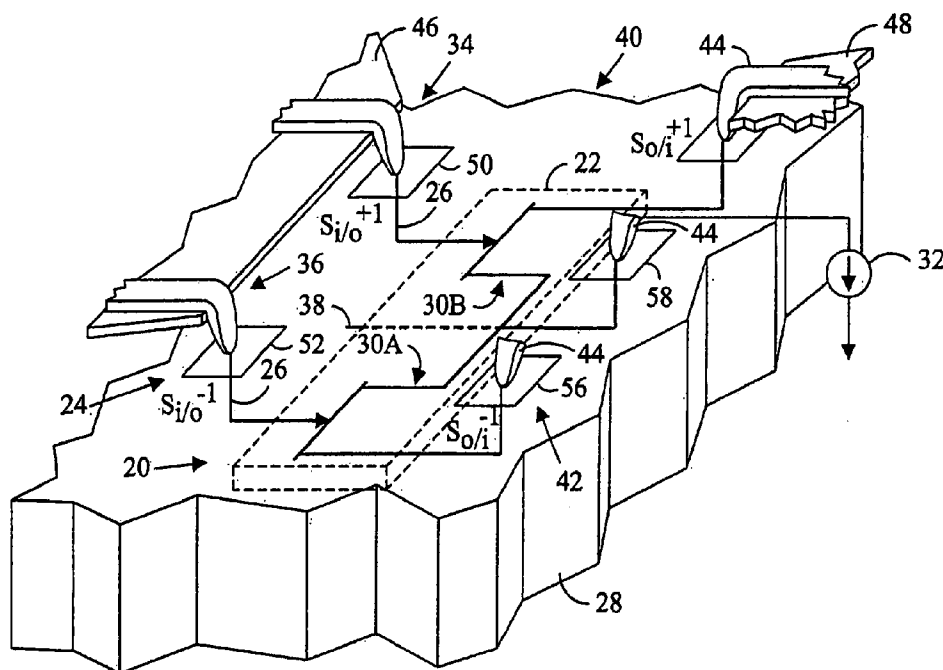
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**Published:**

— *without international search report and to be republished upon receipt of that report*

*[Continued on next page]*

**(54) Title:** DIFFERENTIAL SIGNAL PROBING SYSTEM



**(57) Abstract:** A probe measurement system comprises a probe with a linear array of probe tips enabling a single probe to be used when probing a test structure with a differential signal.



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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

## DIFFERENTIAL SIGNAL PROBING SYSTEM

### CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims the benefit of U.S. Provisional Application No. 60/ 813,119, filed June 12, 2006 and U.S. Provisional Application No. 60/ 813,477, filed July 17, 2006.

### BACKGROUND OF THE INVENTION

**[0002]** The present invention relates to probe measurement systems for testing integrated circuits and other microelectronic devices and, more particularly, probe measurement systems utilizing differential signaling for testing microelectronic devices.

**[0003]** Integrated circuits (ICs) are economically attractive because large numbers of often complex circuits, for example microprocessors, can be inexpensively fabricated on the surface of a wafer or substrate. Following fabrication, individual dies, including one or more circuits, are separated or singulated and encased in a package that provides for electrical connections between the exterior of the package and the circuit on the enclosed die. The separation and packaging of a die comprises a significant portion of the cost of manufacturing an integrated circuit device and to monitor and control the IC fabrication process and avoid the cost of packaging defective dies, manufacturers commonly add electrical circuits or test structures to the wafer to enable on-wafer testing or "probing" to verify characteristics of the integrated circuits before the dies are singulated.

**[0004]** Referring to FIG. 1, a test structure 20 typically includes a device-under-test (DUT) 22, a plurality of metallic probe or bond pads 24 that are deposited at the wafer's surface and a plurality of conductive vias 26 that connect the probe pads to the DUT which is typically fabricated beneath the surface of the wafer 28. The DUT typically comprises a simple circuit that includes a copy of one or more of the basic elements of the integrated circuit, such as a single line of conducting material, a chain of vias or a single transistor. The circuit elements of the DUT are typically produced with the same process and in the same layers of the fabrication as the corresponding elements of the integrated circuit. The marketable ICs are typically evaluated or characterized "on-wafer" by applying a test instrument generated signal to the test structure and measuring the response of the test structure to the signal. Since the circuit elements of the DUT are fabricated with the same process as the corresponding elements of the marketable integrated circuit, the electrical properties of the DUT are expected to be representative of the electrical properties of the corresponding components of the ICs.

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**[0005]** Integrated circuits commonly utilize single ended or ground referenced signaling with a ground plane at the lower surface of the substrate on which the active and passive devices of the circuit are fabricated. As a result of the physical make up of the devices of an integrated circuit, parasitic interconnections exist between many of the parts of the individual devices and between parts of the devices and the wafer on which the devices are fabricated. These interconnections are commonly capacitive and/or inductive in nature and have frequency dependent impedances. For example, the terminals of transistors fabricated on semi-conductive substrates or wafers are typically capacitively interconnected, through the substrate, to the ground plane. The impedance of this parasitic capacitive interconnection is frequency dependent and at higher frequencies the ground potential and the true nature of ground referenced signals becomes uncertain.

**[0006]** Balanced devices utilizing differential signals are more tolerant to poor radio frequency (RF) grounding than single ended devices making them attractive for high performance ICs. A differential gain cell 30 is a balanced device comprising two nominally identical circuit halves 30A, 30B. When biased, with a DC current source 32, and stimulated with a differential mode signal, comprising even and odd mode components of equal amplitude and opposite phase ( $S_i^{+1}$  and  $S_i^{-1}$ ) 34, 36, a virtual ground is established at the symmetrical axis 38 of the two circuit halves. At the virtual ground, the potential at the operating frequency does not change with time regardless of the amplitude of the stimulating signal. The quality of the virtual ground of a balanced device is independent of the physical ground path and, therefore, balanced or differential circuits can tolerate poor RF grounding better than circuits operated with single ended signals.

**[0007]** In addition, the two waveforms of the differential output signal ( $S_o^{+1}$  and  $S_o^{-1}$ ) 40, 42 are mutual references providing faster and more certain transition from one binary value to the other for digital devices and enabling operation with a reduced voltage swing for the signal. Typically, differential devices can operate at lower signal power and higher data rates than single ended devices. Moreover, noise from external sources, such as adjacent conductors, tends to couple, electrically and electromagnetically, in the common mode and cancel in the differential mode. As a result, balanced or differential circuits have good immunity to noise, including noise at even-harmonic frequencies since signals that are of opposite phase at the fundamental frequency are in phase at the even harmonics. Improved tolerance to poor RF grounding, increased resistance to noise and reduced power consumption make differential devices attractive for ICs that operate at higher frequencies. A test structure comprising a differential gain cell enables on wafer testing and characterization of differential devices included in the marketable ICs fabricated on the wafer.

**[0008]** At higher frequencies, on-wafer characterization is commonly performed with a network analyzer. The network analyzer comprises a source of an AC signal, commonly, a

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radio frequency (RF) signal, that is used to stimulate the DUT of a test structure. A forward-reverse switch directs the stimulating signals to one or more of the probe pads of the test structure. Directional couplers or bridges pick off the forward or reverse waves traveling to or from the test structure which are down-converted by intermediate frequency (IF) sections of the network analyzer where the signals are filtered, amplified and digitized for further processing and display. The result is a plurality of s-parameters (scattering parameters), the ratio of a normalized power wave comprising the response of the DUT to the normalized power wave comprising the stimulus supplied by the signal source.

**[0009]** At higher frequencies, the preferred interconnection for communicating signals between the test structure, the source of the stimulating test signal and the sink for the output signals of the test structure is coaxial cable. The transition between the coaxial cable and the probe pads of the test structure is preferably provided by movable probes having one or more conductive probe tips 44 that are arranged to be co-locatable with respective probe pads of the test structure. The test instrumentation and the test structure can be temporarily interconnected for probing by bringing the probe tips of the probe(s) into contact with the probe pads of the test structure. Typically, two probes 46, 48 are utilized when probing a differential or balanced test structure. A differential gain cell requires two input probe pads 50, 52 and two output probe pads 54, 56 for the even and odd mode components of the differential input and output signals and a bias probe pad 58 through which the transistors of the cell are biased. The probe pads of differential test structures are arranged to avoid physical contact and crosstalk between the two probes during simultaneous engagement with the test structure. As a result, the probe pads of a differential test structure occupy a significant portion of the useable surface of a wafer and, typically, must be fabricated in an area of the wafer in which one or more dies containing marketable ICs could otherwise be fabricated. However, test structures serve no purpose after the dies containing the marketable ICs are singulated and manufacturers of ICs are under continuous cost pressure to maximize the number of marketable ICs that are manufactured on each wafer.

**[0010]** What is desired, therefore, is a compact, simplified probe measurement system for communicating differential signals between a test instrument and a test structure.

#### BRIEF DESCRIPTION OF THE DRAWINGS

- [0011]** FIG. 1 is a perspective illustration of a portion of a wafer including a differential test structure having probe pads arranged for engagement by a two probes.
- [0012]** FIG. 2 is a perspective illustration of a portion of a wafer including a differential test structure engageable by a single probe having a linear array of probe tips.
- [0013]** FIG. 3 is a schematic diagram of a probe system utilizing a two-port network analyzer for testing a differential test structure.

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- [0014]** FIG. 4 is a schematic diagram of a probe system utilizing a four-port network analyzer for testing a differential test structure.
- [0015]** FIG. 5 is a schematic diagram of a probe system utilizing a differential test structure as a frequency converter.
- [0016]** FIG. 6 is a perspective view of a probe for testing a differential test structure.
- [0017]** FIG. 7 is a section view of the probe of FIG. 6 along line A-A.
- [0018]** FIG. 8 is a top view of a probe head of a probe for engaging a differential test structure.
- [0019]** FIG. 9 is an elevation view of the probe head of FIG. 8.
- [0020]** FIG. 10 is a bottom view of the probe head of FIG. 8.
- [0021]** FIG. 11 is a perspective view of a probe including a linear array of four probe tips and a fifth probe tip.
- [0022]** FIG. 12 is a bottom view of a probe head of the probe of FIG. 11.
- [0023]** FIG. 13 is a perspective view of an embodiment of a differential signal probe comprising cables including having a plurality of conductors.
- [0024]** FIG. 14 is a top view of a probe head of the probe of FIG. 13.
- [0025]** FIG. 15 is a top view and an elevation view of a probe head comprising a dielectric membrane plate.
- [0026]** FIG. 16 is a top view of an additional embodiment of a probe head.
- [0027]** FIG. 17 is an elevation view of the probe head of FIG. 16.
- [0028]** FIG. 18 is a bottom view of the probe head of FIG. 16.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0029]** Circuits utilizing differential signaling are becoming increasingly common for a wide range of higher frequency applications. The benefits of differential signaling or balanced devices include lower power levels, faster state transition for binary devices, good immunity from noise, minimal susceptibility to electromagnetic coupling at higher frequencies, and greater tolerance of poor grounding conditions which are commonly encountered when integrated circuits are operated at high frequencies. The integrity of the process used to manufacture marketable integrated circuits (ICs) is tested by fabricating a plurality of test structures on the wafer using the same process that is used to fabricate the ICs. Characteristics of the marketable ICs are inferred by stimulating the test structure with a test instrument generated signal and capturing the response of the test structure. While test structures are typically simple circuits, the response of similar devices included in the more complex marketable ICs is expected to be similar to the response of the test structure because the devices in the marketable ICs and similar devices in the test structures are fabricated with the same process.

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**[0030]** While differential signaling provides a number of advantages, particularly at higher frequencies and in noisier environments, the use of balanced or differential devices in the DUTs of test structures is limited. The probe pads of differential test structures are arranged so that two probes can simultaneously engage the probe pads while avoiding physical contact and crosstalk between the probe tips. The probe pads are spread over a significant area of the surface of the wafer and, typically, must be fabricated in an area of the wafer that could otherwise accommodate one or more dies containing marketable ICs. However, test structures serve no purpose after the dies containing the marketable ICs are singulated and manufacturers of ICs are under continuous cost pressure to maximize the number of marketable ICs manufactured on each wafer. The inventors concluded that the number of dies comprising marketable ICs fabricated on a wafer could be increased if the differential test structure could be connected to the test instrumentation with a single probe enabling rearrangement of the probe pads and fabrication of the test structure in a saw street between dies.

**[0031]** Referring in detail to the drawings where similar parts are identified by like reference numerals, and, more particularly to FIG. 2, the test structure 120 comprises a DUT 122 that includes a differential gain cell 124 that is responsive to a differential mode input signal. The differential mode input signal comprises an even mode component ( $S_i^{+1}$ ) and an odd mode component ( $S_i^{-1}$ ) that has substantially the same amplitude as the even mode component but which is opposite in phase of the even mode component. The differential gain cell 124 comprises two substantially identical field effect (JFET) transistors 126A and 126B. However, a DUT typically comprises components corresponding to the components utilized in the marketable integrated circuits fabricated on the wafer and other types of transistors, such as bipolar junction (BJT) transistors or MOSFET transistors can be used in the construction of the differential gain cell of a test structure.

**[0032]** The five probe pads 130, 132, 134, 136 and 138 through which the DUT is biased and through which the components of the differential signals are communicated to and from the test structure are arranged in a substantially linear array reducing the breadth of the probe pad arrangement and enabling placement of the test structure between dies 144 in a saw street 146 (indicated by a bracket) that is only slightly wider than the width of a probe pad. The source terminals of the transistors of the differential gain cell are interconnected as a transistor bias terminal 148. The bias terminal is interconnected to the bias bond or probe pad 130 located in the center of the linear array of probe pads. The gates of the transistors comprise input terminals of the DUT and are connected to respective signal input probe pads 136, 138. The drains of the transistors of the differential gain cell comprise the output signal terminals of the DUT and are interconnected to the output signal probe pads 132, 134. Typically, the DUT 122 is relatively small and comprises circuit elements that are fabricated beneath the

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surface of the wafer. The probe pads are conductively connected to the terminals of the DUT by vias 26 that extend from the probe pads on the surface of the wafer to the subsurface strata in which the circuit elements of the DUT and the corresponding circuit elements of the integrated circuit have been fabricated.

**[0033]** Referring to FIG. 3, at higher frequencies the DUT, for example the DUT 122, of a differential test structure is typically stimulated with a signal generated by a network analyzer. A typical two-port network analyzer 202 outputs a single ended (ground referenced) modulated signal, which may include a DC offset, at the port of an RF signal source 204. In the probe measurement system 200, the single ended input signal is conducted to a balun 206 which converts the single ended signal to a balanced or differential signal comprising differential components having substantially the same amplitude but opposite phase. The two components of the differential input signal are transmitted to respective bias tees 208, 210 which separate the modulated portion of the input signal from the DC portion. A bias tee comprises a capacitor 212 in series with an RF port 214 that blocks transmission of the DC component of the input signal from the RF port. An inductor 216, in series with a DC port 210 of the bias tee blocks, the modulated signal but permits transmission of the DC portion of the input signal to the DC port. The modulated components of differential input signal,  $S_i^{+1}$  and  $S_i^{-1}$ , are communicated to respective probe tips 156, 158 via interconnections to the RF ports of the respective input signal bias tees. The probe tips 156, 158 are arranged on a probe 160 which is movable relative to the test structure so that the probe tips may be co-located with the respective input signal probe pads 136, 138 connected to the DUT 122 of a test structure.

**[0034]** Similarly, the differential output signal components ( $S_o^{+1}$  and  $S_o^{-1}$ ) which are controlled by the input signals at the respective input terminals of the differential gain cell are communicated from the respective probe pads 132, 134 to respective output signal probe tips 152, 154 that are interconnected to respective bias tees 220, 222. The modulated portions of the differential output signal components are transmitted to a balun 224 while DC portions of the differential output signal components are blocked from the network analyzer by the capacitors 214 in series with the RF ports of the bias tees. The balun converts the differential signal components to a single ended signal which is transmitted to a signal sink 226 of the network analyzer. The signal sink typically comprises one or more intermediate frequency (IF) sections where, typically, the signals are filtered, amplified and digitized for further processing and display.

**[0035]** The transistors of the differential gain cell of the DUT are biased by a DC current that is communicated between the DC ports of the bias tees and bias probe pad 130 by a bias probe tip 150 of the probe. An alternative embodiment of the test structure 122 includes additional probe pads 140, 142 located distal of the respective ends of the linear array of five probe pads and which are interconnected with the bias probe pad 130. Spatially



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corresponding additional probe tips 162, 164, interconnected with the centrally located bias probe tip 150, are included in an alternative embodiment of the probe 160 to engage the additional probe pads of the alternative test structure probe pad arrangement.

**[0036]** While many network analyzers output only single ended signals, the accuracy of a probe system utilizing single ended signals to probe a differential test structure is limited because the reference plane for de-embedding the test structure is located at the ports of the baluns nearest the DUT. Referring to FIG. 4, a four port network analyzer 302 can output differential signals directly permitting mixed mode analysis and de-embedding of the DUT at its terminals. In the probe measurement system 300, the differential input signal components, including a DC offset, are output at the ports 306, 308 of the signal source 304 and transmitted to respective bias tees 316, 318. The capacitor 320 in series with the RF port of a bias tee blocks the transmission of the DC component of the input signal from the RF port. The modulated portion of the differential input signal components ( $S_i^{+1}$  and  $S_i^{-1}$ ) are communicated from the RF port of the respective bias tee 316, 318 to a respective probe tip 156, 158 of the probe 360. Each of the probe tips is co-locatable with a respective one of the probe pads 136, 138 that is interconnected to conduct an input signal component to the DUT. Similarly, the differential output signal components ( $S_o^{+1}$  and  $S_o^{-1}$ ) are transmitted from respective probe pads 132, 134 to respective probe tips 152, 154 and then to respective bias tees 332, 334. The capacitors of the bias tees in series with the RF port, block the transmission of DC from the bias tees to the two signal input ports 312, 310 of the signal sink 302. The outputs at the DC ports of the bias tees are transmitted to the bias probe tip 150 which is arranged for contact with the bias probe pad 130 of the DUT. FIG. 4 illustrates another alternative arrangement of probe pads and probe tips where the output signals are sourced from the probe pads at the ends of the linear array of five probe pads and the input signals are transmitted to the probe pads immediately adjacent to the central probe pad of the linear array of five probe pads.

**[0037]** A network analyzer is expensive and the cost of a probe measurement system that includes a network analyzer substantially impacts the cost of producing high frequency ICs. The inventors realized that the differential gain cell could be utilized as a passive frequency converter enabling parametric RF testing with a less costly probe measurement system that utilizes a low frequency spectrum analyzer rather than a more costly network analyzer. Referring to FIG. 5, in the probe measurement system 600 a first signal generator 602 transmits a single ended, modulated signal having a frequency ( $f_1$ ) to a first balun 604. The balun converts the single ended signal to a differential signal comprising even and odd mode components of substantially equal amplitude and opposite phase angle. The differential signal components are conducted to a probe 360 including a plurality of probe tips arranged to be co-locatable with the probe pads of a test structure including a DUT 322 comprising a differential

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gain cell 325. The components of the differential signals from the first signal generator are conducted by probe tips 152 and 154 to respective probe pads 132 and 134 which are connected to the gates of the transistors of the differential gain cell. The transistors of the differential gain cell are biased by the connection of their source terminals to ground 620 through the probe pad 130 and the contacting probe tip 150.

**[0038]** A second signal generator 606 outputs a second single ended, modulated signal having a second frequency ( $f_2$ ) to a second balun 608 which converts the single ended signal to a differential signal comprising components of substantially equal amplitude and opposite phase. The signal is transmitted to the drains of the transistors of the differential gain cell through high pass filter capacitors 616 which block the transmission of low frequency signals. The outputs of the DUT which are controlled by the input signals at the respective gates of the transistors are conducted to the output signal probe pads 136 and 138 and respective contacting probe tips 156, 158. The respective components of the signals from the second signal generator and the output terminals of the DUT, having respective second and first frequencies, are combined producing respective components of a differential combined output signal. The components of the combined output signal comprise an upper frequency ( $f_1 + f_2$ ) combined output signal band and a lower frequency ( $f_1 - f_2$ ) combined output signal band. The differential components of the lower frequency combined output signal band are separated from the upper frequency combined output signal band by the low pass filters 614 and converted to a single ended signal by a balun 612. The lower frequency ( $f_1 - f_2$ ), single ended signal is conducted to a signal sink 610 for analysis, such as comparison with the results obtained by testing other differential gain cells having known characteristics, and display. Utilizing the differential test structure as a frequency converter enables stimulation of the test structure with a high frequency signal but permits analyzing the result with a relatively less expensive, lower frequency capable, signal sink, such as a spectrum analyzer.

**[0039]** Typically, coaxial cable interconnects the network analyzer, other test instrumentation and the probe which provides the transition from the signal paths provided by the coaxial cable to the signal paths comprising the probe pads fabricated on the surface of a wafer. Referring FIGS. 6, 7 and 8, the probe 500 comprises a support block 502 which is suitably constructed for connection to a movable probe supporting member 504 of a probe station. For example, the support block 502 includes an aperture 506 for engagement by a snugly fitting alignment pin 508 that projects vertically from the probe supporting member. In addition, the support block includes a pair of countersunk apertures 510 to accept a pair of fastening screws 512 arranged to engage threaded holes in the probe supporting member and secure the probe to the probe supporting member.

**[0040]** The probe includes a plurality of input ports 530, 532, 534, 536, 538 which, in the embodiment depicted, comprise spark-plug type, K connectors. This connector enables the

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external connection of an ordinary coaxial cable to an input port permitting a well shielded high frequency transmission channel to be established between the probe and the test instrument. If desired, other types of connectors can be used, such as a 2.4 mm. connector, a 1.85 mm. connector or a 1 mm. connector.

**[0041]** In the depicted embodiment, a semi-rigid coaxial cable 514 is connected at its rearward end to each K connector comprising one of the ports of the probe. These coaxial cables preferably include an inner conductor 516, an inner dielectric 518 and an outer conductor 520 and are preferably of phase-stable low-loss type. The coaxial cable may likewise include other layers of materials, as desired. To prepare the rearward ends of the cables for connection to an appropriate K-connector, the rearward end is stripped to expose the inner conductor, and this inner conductor is temporarily held inside a dummy connector while the adjacent outer conductor is soldered within a bore 522 formed in the primary support block. A recess 524 in the support block below this bore provides access to facilitate the soldering process. The dummy connector is then removed and a K-connector is screwed into each of the threaded openings formed in the block above the bore so as to effect electrical connection between the connectors and the coaxial cables. A thread locking compound may be applied to the threads of the K-connectors prior to their installation to ensure a secure physical connection.

**[0042]** The forward ends of the cables remain freely suspended and, in this condition, serve as a movable support for a probe head 540 of the probe. Before being connected to the K-connector, the cables are bent along first and second intermediate portions in the manner shown so that a generally upwardly curving 90° bend and a downwardly curving bend, respectively, are formed in the cable. The protruding ends of the coaxial cables may be slidably inserted into a tube 526 comprising semi-flexible microwave-absorbing material. One material used for forming the tube comprises iron and urethane. The semi-flexible tube of microwave absorbing material serves to substantially reduce the levels of microwave energy that travel along the outer conductor of the semi-rigid cable.

**[0043]** Referring also to FIGS. 9 and 10, the probe includes a microstrip style probe head 540 that includes a dielectric plate 560 having generally planar upper and lower surfaces that is affixed to the forward ends of the coaxial cables 550, 552, 554, 556, 558. The underside of each cable is cut away to form a shelf 562, and the dielectric plate is affixed to the shelf. Alternatively, the dielectric plate may be supported by an upwardly facing shelf cut away from the cable or the end of the cable without a shelf. A conductive bias layer 564 comprising a thin, generally planar conductive material is affixed to the bottom of the dielectric plate. A thin, generally planar, bias layer has a low profile that is less likely to interfere with the ability to effectively probe a DUT by accidentally contacting the device. A via 566, electrically couples the bias layer to the center conductor of the coaxial cable 550 connected to the bias input

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port 530 of the probe. The bias layer may be provided with any DC voltage potential suitable for biasing the transistors of the differential gain cell of the DUT. The bias layer preferably covers substantially all of the lower surface of the dielectric plate. Alternatively, the bias layer may cover a portion greater than 50%, 60%, 70%, 80%, 90% of the surface of the dielectric plate and/or the region directly under a majority (or more) of the length of a conductive signal trace secured to the opposing side of the plate.

**[0044]** One or more conductive signal traces are supported by the upper surface of the dielectric plate. The conductive traces may be deposited, using any technique, or otherwise secured on the upper surface of the dielectric plate. A conductive signal trace is electrically interconnected to the inner conductor of each of the coaxial cables 552, 554, 556, 558. The respective interconnected conductive traces 572, 574, 576, 578 normally conduct the components of the differential signals to and from the DUT. Separated by dielectric material, each conductive trace, together with the bias layer, forms one type of a microstrip transmission structure. Other layers above, below, and/or between the bias layer and the conductive trace(s) may be included, if desired.

**[0045]** Conductive vias 568 passing through the dielectric plate enables transference of the signal path from the conductive traces on the upper surface of the plate to the lower surface of the plate. The conductive via substantially reduces the capacitance of the signal path compared to a conductive finger extending over the end of the dielectric plate. The conductive via provides a path from one side of the plate to the other that is free from an air gap between the via and the dielectric for at least a majority of the thickness of the plate.

**[0046]** The lower surface of the dielectric plate includes a plurality of contact bumps or probe tips 580, 582, 584, 586, 588 that are respectively electrically connected to the bias layer or to the vias extending from respective conductive traces on the upper surface of the dielectric plate. The probe tips are arranged in a linear array with the centroids of the lower ends of the probe tips being substantially aligned and arranged generally parallel to forward edge of the probe head. The probe tips are spatially arranged proximate the adjacent tip(s) in the linear array so as to be co-locatable with the respective probe pads that conduct the signals for the test structure that is to be probed. It is to be understood that the probe tips may take any suitable form, such as a bump, a patterned structure, or an elongate conductor. The bias layer may laterally encircle one or more of the probe tips or may extend beyond one or more of the probe tips to reduce crosstalk with other probes.

**[0047]** Referring to FIGS. 16, 17 and 18, in an additional embodiment of a probe head 900 for testing a differential test structure, a conductive shield 902, which is preferably planar in nature, is affixed to the bottom of a lower dielectric plate 904. The conductive shield, may be for example, a thin conductive material (or otherwise) that is affixed to the lower plate 904. A shield of thin generally planar conductive material is less likely to accidentally contact

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the test structure when the probe tips are contact with the probe pads. The conductive shield is electrically coupled to an outer conductor 520 of at least one of the coaxial cables 550, 552, 554, 556, 558 by a via 910 to form a ground plane. The outer conductor is typically connected to ground, though the outer conductor may be provided with any suitable voltage potential (either DC or AC). The conductive shield 902 preferably covers substantially all of the lower surface of the lower dielectric plate 904. Alternatively, the conductive shield 902 may cover greater than 50%, 60%, 70%, 80%, 90%, and/or the region directly under a majority (or more) of the length of a conductive signal trace on the opposing side of the probe head. The bias voltage for the transistors of the DUT is conducted to the bias probe tip 580 through a middle conductive layer 906 which is conductively connected to the bias probe tip and to the center conductor of the coaxial cable 550 by vias. Overlaying the middle conductive layer, an upper dielectric plate 908 includes an upper surface to which are secured the traces 572, 574, 576, 578 that conduct the components of the differential input and output signals. The traces are in contact with the center conductors of the respective coaxial cables and are connected to the respective probe tips by vias extending from the upper surface of the upper dielectric plate to the probe tips.

**[0048]** Referring to FIGS. 11 and 12, in another embodiment of a probe for a testing a differential test structure, the probe 600 comprises support block 602 securable to the probe supporting member 504. A plurality of ports 532, 534, 536, 538 are attached to the support block and electrically connected to a plurality of coaxial cables that extend to a probe head 604. The connector of the centrally located port 530 is electrically connected to a coaxial cable 606 which extends to a probe tip 608 supported by an arm 610 attached to the support block 602. The probe head 604 comprises a dielectric plate 612 which supports four probe tips 582, 584, 586, 588 arranged in a linear array and which conduct the components of the differential input and output signals to and from the test structure. The bias for the transistors of the test structure is conducted from the port 530 to a probe pad of a test structure by a probe tip 608 which is proximate the third and fourth probe tips of the linear array of probe tips 582, 584, 586, 588 but not in linear alignment with the probe tips included in the linear array through which the components of the differential signals are conducted.

**[0049]** Referring to FIGS. 13 and 14, the ports 702, 704 of the probe 700 of alternative embodiment are arranged to provide electrical interconnections to a coaxial cable having more than two conductors. For example, the conductors may be triaxial cables having three conductors separated by intervening dielectric layers. The triaxial cables 706, 708 are electrically interconnected to the respective ports, at least one of which is insulated from the support block, at their rearward ends. The freely suspended forward support ends of the triaxial cables support a probe head 710 comprising a dielectric plate 712 secured to a shelf formed in each of the ends of the two triaxial cables. The removal of a portion of the triaxial cable to form

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the shelf exposes the inner conductor 714, the inner dielectric layer 716, the intermediate conductor 718, the outer dielectric layer 720 and the outer conductor 722 that comprise the cable. The conductors of the triaxial cables are interconnected to respective probe tips formed on the lower surface of the dielectric plate. For example, if the DC bias is conducted to the probe head through the outer conductors of the triaxial cables, the central probe tip 150 can be interconnected to the outer conductors by a bias layer 724 supported on the lower surface of the dielectric plate that is electrically interconnected to the central probe tip 150 and electrically interconnected to the outer conductors by vias 726, 728, 730 extending through the dielectric plate. In addition, the linear array of probe tips includes probe tips 162 and 164 for engaging probe pads 142 and 140 of an alternative embodiment comprising seven probe pads and are also interconnected to the bias layer. The components of the differential input and output signals are conducted from the respective inner conductors and respective intermediate conductors to the probe tips 152, 154, 156 and 158 by traces 736, 738, 740, 742 on the upper surface of the dielectric plate that are electrically interconnected to the respective conductor exposed at the shelf in the triaxial cable and vias 744, 746, 748, 750 extending between the upper and lower surfaces of the dielectric plate.

**[0050]** Referring to FIG. 15, in an additional embodiment a flexible dielectric membrane plate 802 may be substituted for a more rigid dielectric plate. An example of membrane material is described in U.S. Pat. No. 5,914,613. In general, membrane based probes are characterized by a flexible (or semi-flexible) plate or substrate with traces supported thereon together with contacting portions or probe tips being supported thereon. The linear array of probe tips 850, 852, 854, 856, 858 are arranged to be co-locatable with the probe pads of the DUT. The traces are normally on the opposing side of the membrane and connected to the probe tips with vias. In many cases, the membrane technology may be significantly thinner than ceramic based substrates or plates, such as 40, 30, 20, 10, 5, or 3 microns or less. Normally the dielectric constant of the membrane material is 7 or less, sometimes less than 6, 5, or 4 depending on the particular material used. While normally using a membrane substrate with a lower dielectric constant is unsuitable, using a significantly thinner substrate together with a material having a lower dielectric constant raises the theoretical frequency range of effective signal transmission to hundreds of GHz. The significantly thinner substrate material permits positioning the lower bias layer significantly closer to the signal traces than the relatively thick ceramic substrate, and therefore tends to more tightly confine the electromagnetic fields.

**[0051]** When a probe tip of a membrane based probe head comes into contact with a probe pad, as in most probes, it tends to skate across the pad as additional pressure is exerted. This skating is the result of the angled probe and/or co-axial cable flexing while under increasing pressure against the probe pad. A limited amount of skating is useful to "scrub" away oxide layers, or otherwise, that may build up on the probe pad. In many cases the probe

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pad is typically relatively small and excessive skating from the application of slightly too much pressure results in the probe simply skating off the probe pad. In addition, if excessive pressure is exerted damage to the probe and/or probe pad may result. Accordingly, there is an acceptable range of pressure and skating that should be maintained.

**[0052]** A probe measurement system including a probe comprising a linear array of probe tips enables testing of a differential or balanced test structure with a single probe facilitating fabrication of the test structure in a saw street between dies on a wafer.

**[0053]** The detailed description, above, sets forth numerous specific details to provide a thorough understanding of the present invention. However, those skilled in the art will appreciate that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuitry have not been described in detail to avoid obscuring the present invention.

**[0054]** All the references cited herein are incorporated by reference.

**[0055]** The terms and expressions that have been employed in the foregoing specification are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims that follow.

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## Claims:

I (we) claim:

1. A probe for testing a differential test structure having a plurality of probe pads, said probe comprising:
  - (a) a first probe tip connectable to conduct a first mode component of a first differential signal;
  - (b) a second probe tip proximate said first probe tip and connectable to conduct a first mode component of a second differential signal ;
  - (c) a third probe tip proximate said second probe tip;
  - (d) a fourth probe tip proximate said third probe tip and connectable to conduct a second mode component of said second differential signal ; and
  - (e) a fifth probe tip proximate said fourth probe tip and connectable to conduct a second mode component of first differential signal; said first, said second, said fourth and said fifth probe tips being arranged in a substantially linear array and, with said third probe tip, contemporaneously co-locatable with respective probe pads of said test structure.
2. The probe of claim 1 wherein a source of said first differential signal comprises said respective probe pads of said test structure co-locatable with said first and said fifth probe tips.
3. The probe of claim 1 wherein a source of said second differential signal comprises said respective probe pads of said test structure co-locatable with said second and said fourth probe tips.
4. The probe of claim 1 wherein said third probe tip is interconnected to a source of a direct current.
5. The probe of claim 1 wherein said third probe tip is aligned substantially linearly with said linear array of said first, said second, said fourth and said fifth probe tips.
6. The probe of claim 5 further comprising:
  - (a) a sixth probe tip proximate said first probe tip; and
  - (b) a seventh probe tip proximate said fifth probe tip; said sixth and said seventh probe tips being arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips; interconnected to said third probe tip and co-locatable with respective probe pads of said test structure.



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7. The probe of claim 6 wherein said third probe tip is interconnected to a source of a direct current.
8. A probe for testing a differential test structure having a plurality of probe pads, said probe comprising:
  - (a) a dielectric plate having a substantially planar first surface and a second surface;
  - (b) a first probe tip projecting from said first surface and connectable to conduct a first mode component of a first differential signal ;
  - (c) a second probe tip projecting from said first surface proximate said first probe tip and connectable to conduct a second mode component of a first differential signal;
  - (d) a third probe tip projecting from said first surface proximate said second probe tip;
  - (e) a fourth probe tip projecting from said first surface proximate said third probe tip and connectable to conduct a second mode component of said second differential signal; and
  - (f) a fifth probe tip projecting from said first surface proximate said fourth probe tip and connectable to conduct a second mode component of said first differential signal; said first, said second, said fourth and said fifth probe tips being arranged in a substantially linear array and contemporaneously co-locatable with respective probe pads of said test structure.
9. The probe of claim 8 wherein a source of said first differential signal comprises said respective probe pads of said test structure co-locatable with said first and said fifth probe tips.
10. The probe of claim 8 wherein a source of said second differential signal comprises said respective probe pads of said test structure co-locatable with said second and said fourth probe tips.
11. The probe of claim 8 wherein said third probe tip is interconnected to a source of a direct current.
12. The probe of claim 8 wherein said third probe tip is aligned substantially linearly with said linear array of said first, said second, said fourth and said fifth probe tips.

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13. The probe of claim 12 further comprising:
  - (a) a sixth probe tip proximate said first probe tip; and
  - (b) a seventh probe tip proximate said fifth probe tip; said sixth and said seventh probe tips being arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips; interconnected to said third probe tip and co-locatable with respective probe pads of said test structure.
14. The probe of claim 8 further comprising:
  - (a) a first conductor overlaying an area of said first surface and electrically interconnected with said third probe tip;
  - (b) a second conductor extending from said first surface to said second surface of said dielectric plate and electrically interconnected with said first conductor; and
  - (c) a conductor of direct current electrically interconnected with said second conductor.
15. The probe of claim 14 further comprising:
  - (a) a sixth probe tip projecting from said first surface proximate said first probe tip; and
  - (b) a seventh probe tip projecting from said first surface proximate said fifth probe tip, said sixth and said seventh probe tips being electrically interconnected with said first conductor and arrayed substantially linearly with said first, said second, said third, said fourth and said fifth probe tips and respectively co-locatable with probe pads of said test structure.
16. The probe of claim 8 further comprising:
  - (a) a first conductor overlaying an area of said second surface; and
  - (b) a second conductor extending from said second surface of said dielectric plate and electrically interconnecting said first conductor with a ground potential.
17. The probe of claim 8 wherein said dielectric plate is rigid.
18. The probe of claim 8 wherein said dielectric plate is flexible.
19. A system for measuring a performance of a differential test structure having a plurality of probe pads, said system comprising:

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- (a) a source of a modulated differential signal comprising an even mode component and an odd mode component of approximately equal amplitude and opposite phase angle, said differential signal including a direct current component;
  - (b) a first bias tee interconnected with said source, said first bias tee separating said direct current component from one of said even mode component and said odd mode component of said modulated differential signal;
  - (c) a second bias tee interconnected with said source, said second bias tee separating said direct current component from the other of said even mode component and said odd mode component of said modulated differential signal;
  - (d) a probe comprising:
    - (i) a first probe tip interconnected to communicate one of said even mode component and said odd mode component of said modulated differential signal from one of said first bias tee and said second bias tee to a first probe pad of said test structure;
    - (ii) a second probe tip co-locatable with a second probe pad of said test structure;
    - (iii) a third probe tip interconnected with at least one of said first bias tee and said second bias tee to conduct said direct current component to a third probe pad of said test structure;
    - (iv) a fourth probe tip co-locatable with a fourth probe pad of said test structure;
    - (v) a fifth probe tip interconnected to communicate the other of said even mode component and said odd mode component of said modulated differential signal from the other of said first bias tee and said second bias tee to a fifth probe pad of said test structure, said first, said second, said third, said fourth and said fifth probe tips arranged to be contemporaneously co-locatable with said respective probe pads of said test structure and at least said first, said second, said fourth and said fifth probe tips being arranged in a substantially linear array; and
  - (e) a signal sink interconnected with said second probe tip and said fourth probe tip, said sink receiving a signal conducted from said second probe pad and said fourth probe pad of said test structure.
20. The system for measuring a performance of a differential test structure of claim 19 wherein said source of said modulated differential signal comprising an even mode component and an odd mode component of approximately equal amplitude and opposite phase angle comprises:

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- (a) a source of a single ended signal including a modulated signal component and a direct current component; and
  - (b) a first balun interconnecting said source and said first and said second bias tees, said first balun converting said single ended signal to a differential signal comprising an even mode component and an odd mode component of approximately equal amplitude and opposite phase angle.
- 21. The system for measuring a performance of a differential test structure of claim 20 further comprising a second balun interconnecting said second and said fourth probe tips and said sink, said second balun converting a differential signal transmitted from said second probe pad and said fourth probe pad to a single ended signal.
- 22. The system for measuring a performance of a differential test structure of claim 19 wherein:
  - (a) said second probe tip is proximate said first probe tip;
  - (b) said third probe tip is proximate said second probe tip;
  - (c) said fourth probe tip is proximate said third probe tip; and
  - (d) said fifth probe tip is proximate said fourth probe tip.
- 23. The system for measuring a performance of a differential test structure of claim 19 wherein:
  - (a) said second probe tip is proximate said first probe tip;
  - (b) said third probe tip is proximate said first probe tip;
  - (c) said fourth probe tip is proximate said fifth probe tip; and
  - (d) said fifth probe tip is proximate said third probe tip.
- 24. A system for measuring a characteristic of a differential gain cell having a first input terminal, a second input terminal, a first output terminal for transmitting a first output signal controllable by a signal at said first input terminal and a second output terminal for transmitting a second output signal controllable by a signal at said second input terminal, said system comprising:
  - (a) a source of a first differential signal having a first frequency of modulation, said first differential signal comprising a first mode component and a second mode component of approximately equal magnitude and opposite phase angle;
  - (b) an interconnection of said source and said first input terminal of said differential gain cell enabling communication of said first mode component of said first differential signal to said first input terminal;

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- (c) an interconnection of said source and said second input terminal of said differential gain cell enabling communication of said second mode component of said first differential signal to said second input terminal;
  - (d) a source of a second differential signal having a second frequency of modulation, said second differential signal comprising a first mode component and a second mode component of approximately equal magnitude and opposite phase angle;
  - (e) an interconnection of said first output terminal of said differential gain cell and said second source enabling conducting of a first combined signal comprising a combination of said first mode component of said second differential signal and a first mode component of an output signal of said differential gain cell;
  - (f) an interconnection of said second output terminal of said differential gain cell and said second source enabling conducting of a second combined signal comprising a combination of said second mode component of said second differential signal and a second mode component of an output signal of said differential gain cell;
  - (g) a first filter selectively permitting transmission of a portion of said first combined signal having a frequency approximately equal to a difference between said first frequency and said second frequency;
  - (h) a second filter selectively permitting transmission of a portion of said second combined signal having a frequency approximately equal to a difference between said first frequency and said second frequency; and
  - (i) a signal sink interconnected to said first filter and said second filter, said signal sink enabling analysis of said first and said second combined signals.
25. The system for measuring a characteristic of a differential test structure of claim 24 wherein said source of said first differential signal comprises:
- (a) a source of a single ended signal; and
  - (b) a first balun interconnecting said source and said first and said input terminals of said differential gain cell.
26. The system for measuring a characteristic of a differential test structure of claim 24 wherein said source of said second differential signal comprises:
- (a) a source of a single ended signal; and
  - (b) a balun interconnecting said source and said first and said output terminals of said differential gain cell.

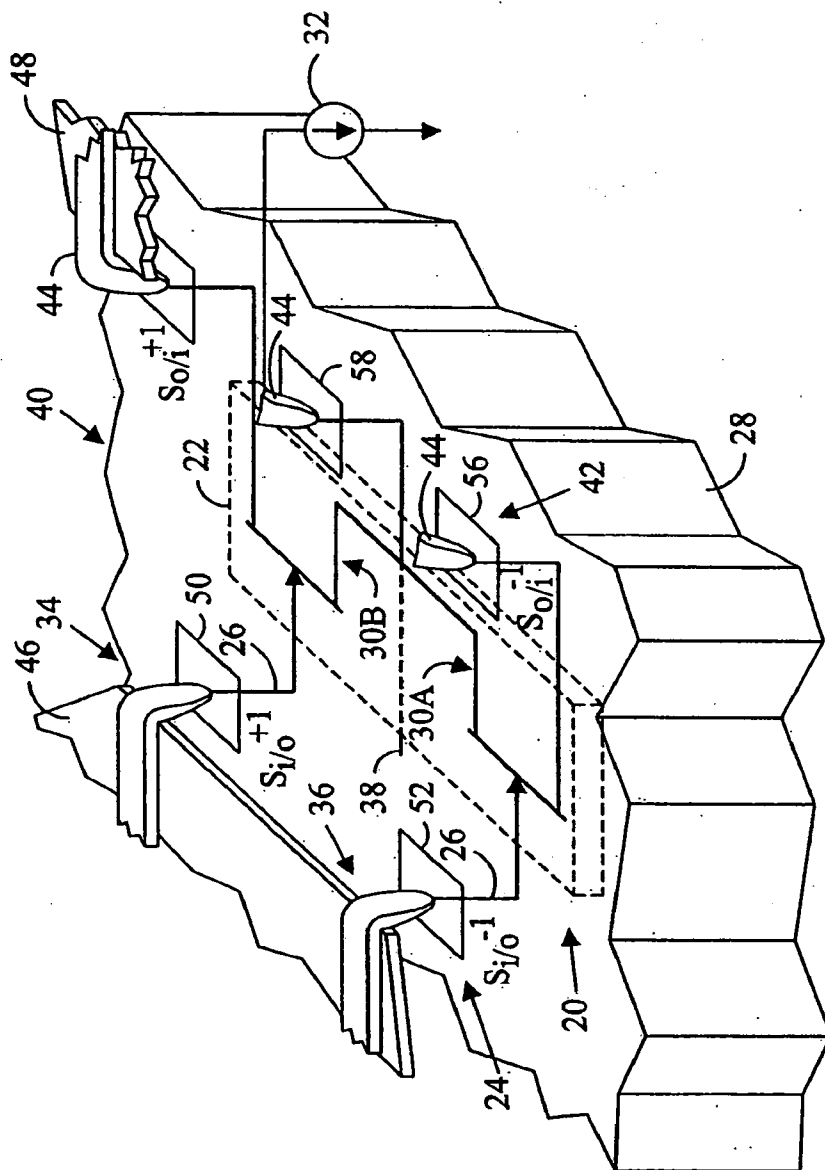


FIG. 1

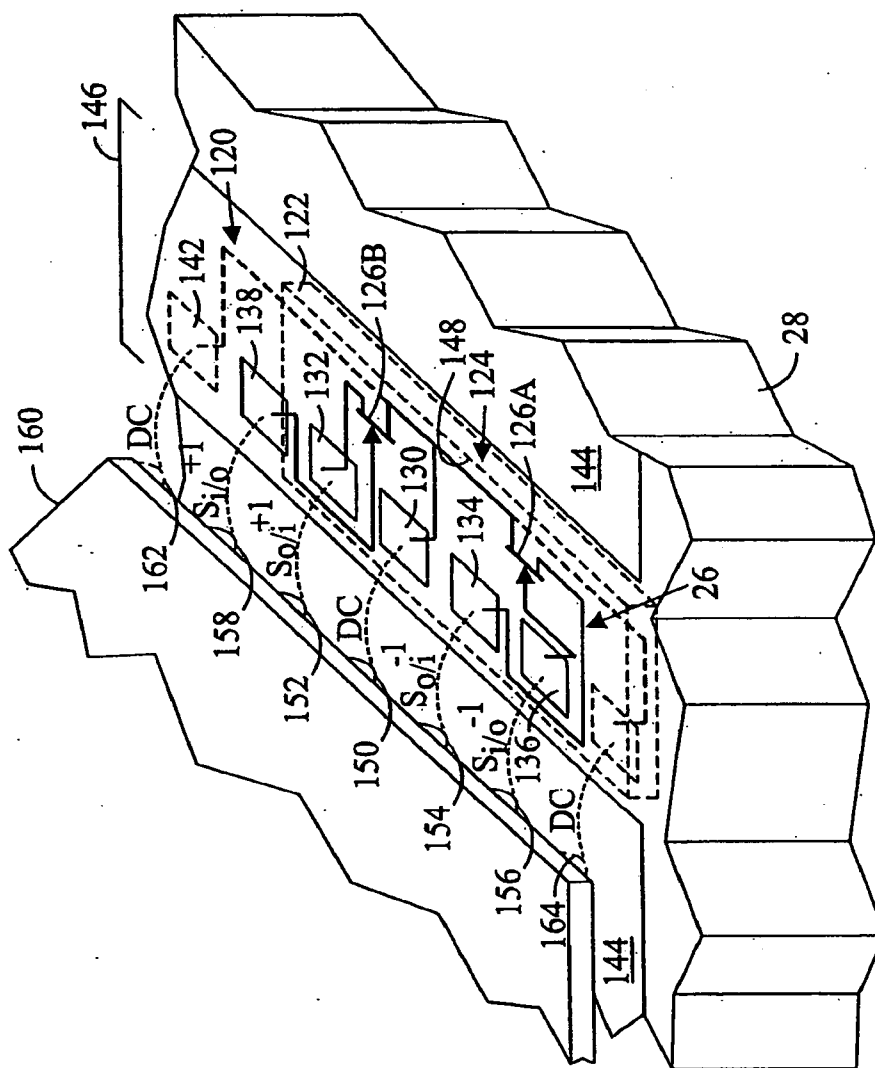


FIG. 2

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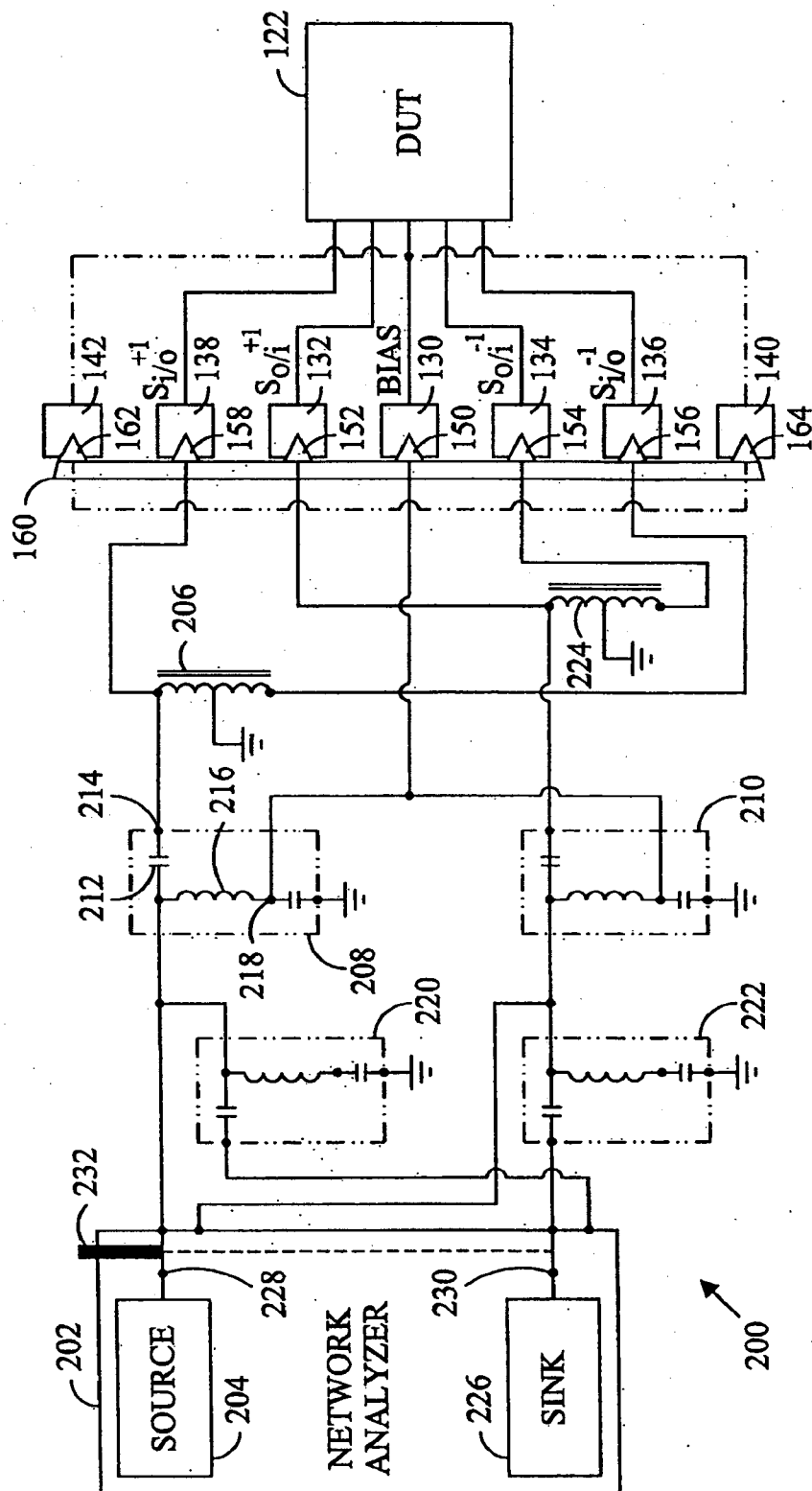


FIG. 3



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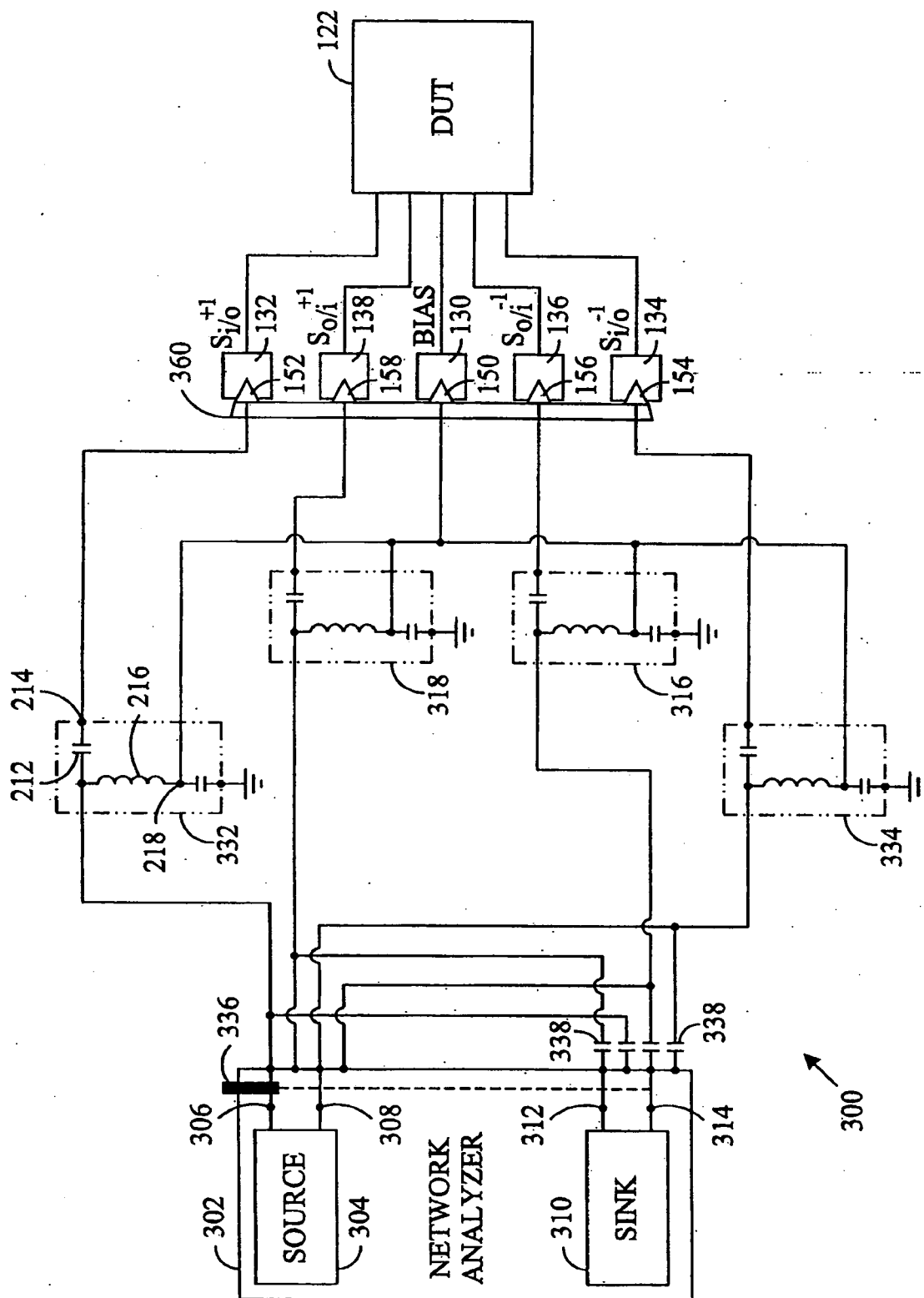


FIG. 4

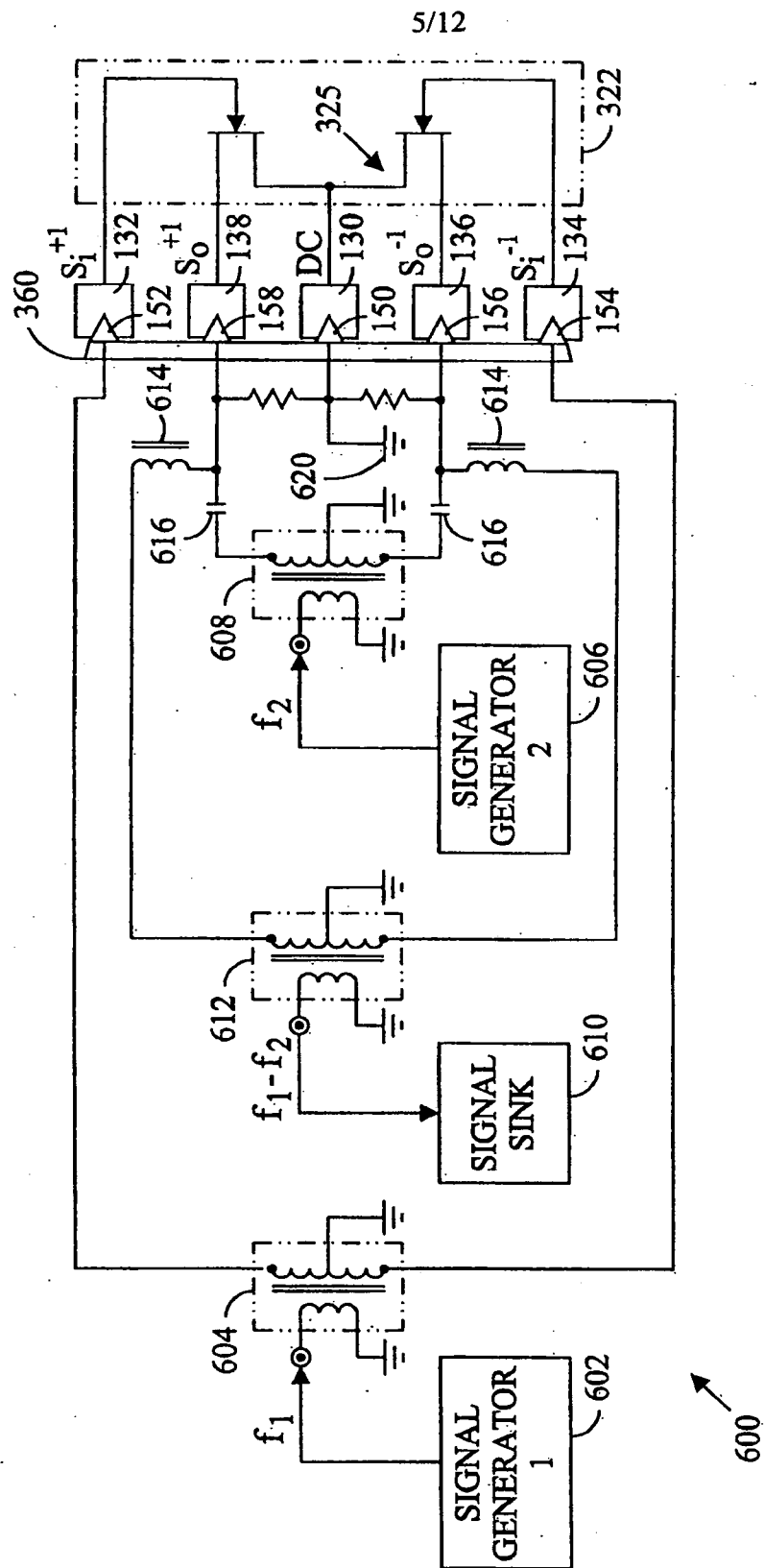


FIG. 5

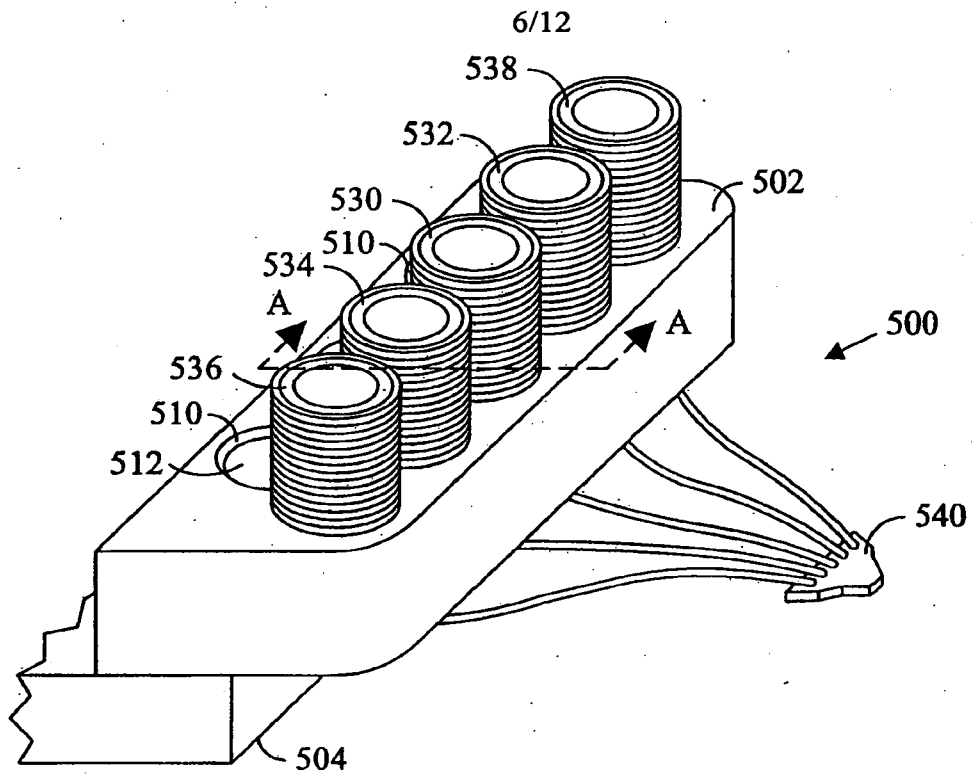


FIG. 6

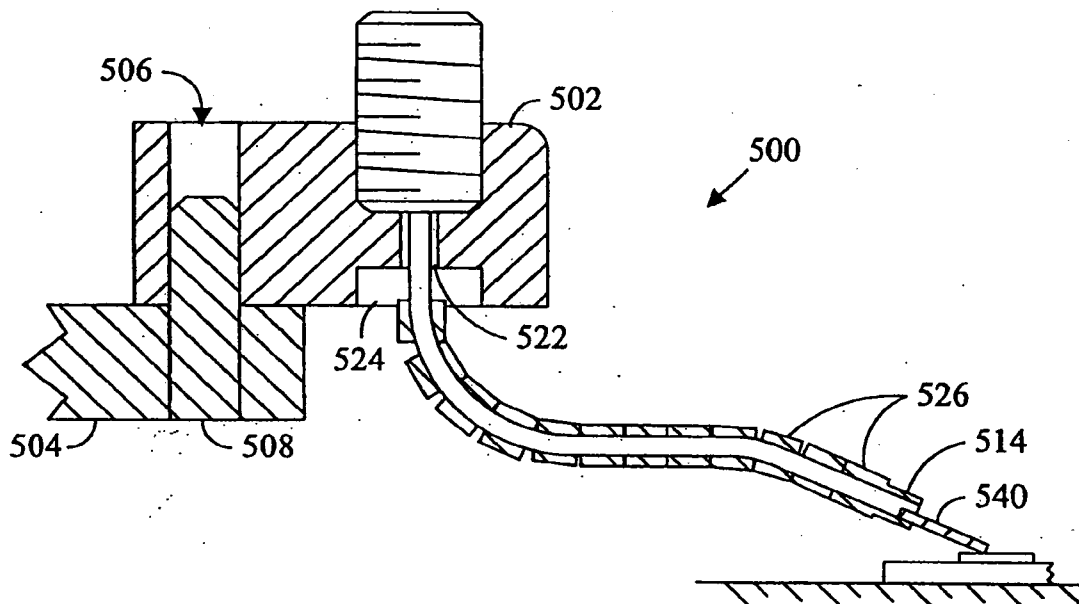


FIG. 7

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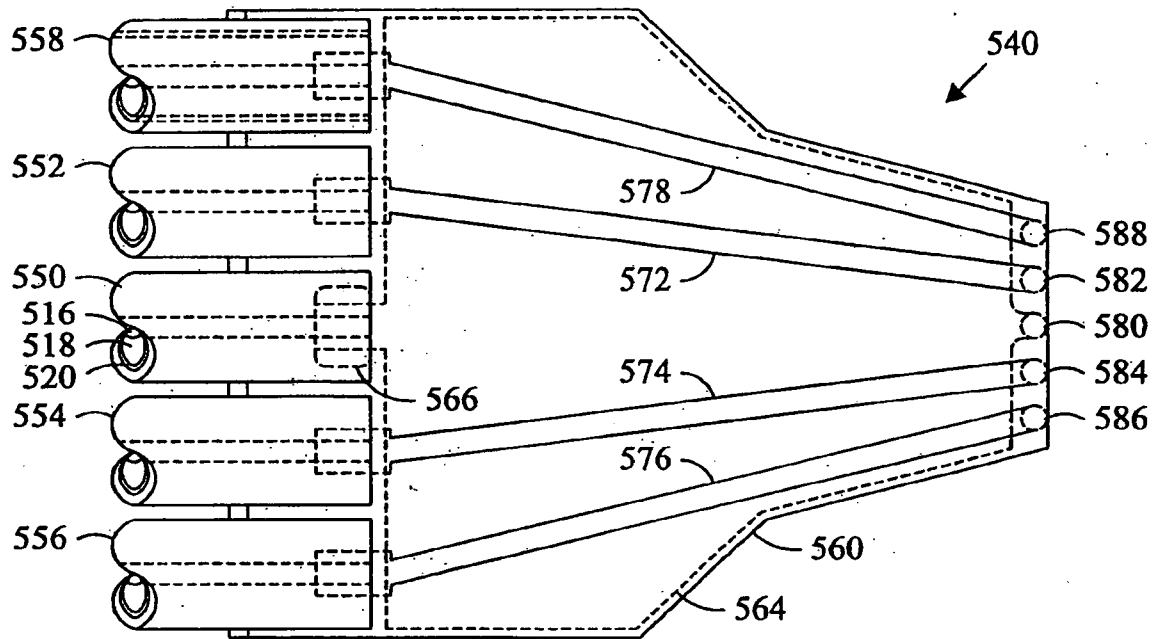


FIG. 8

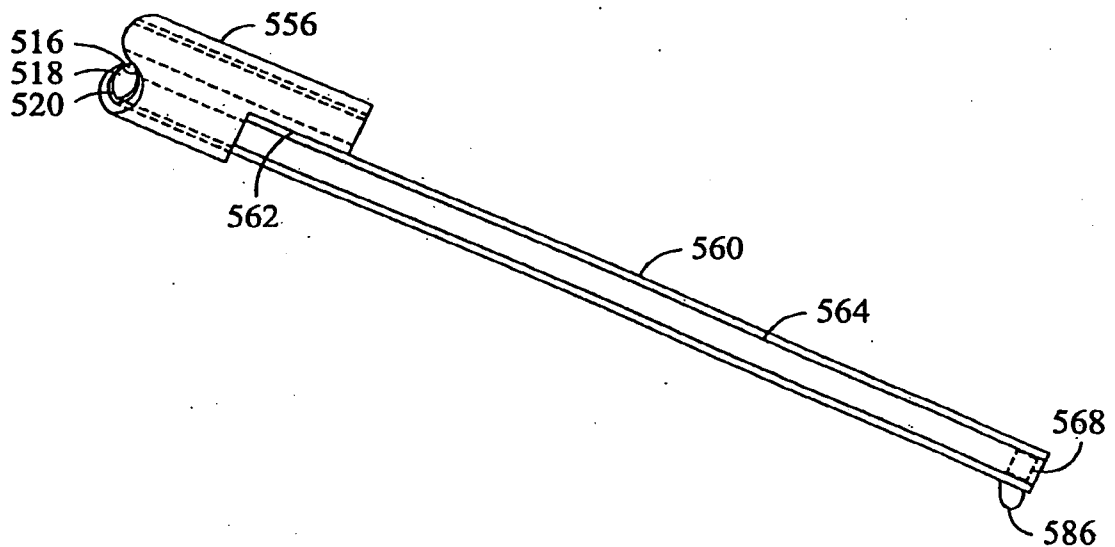


FIG. 9

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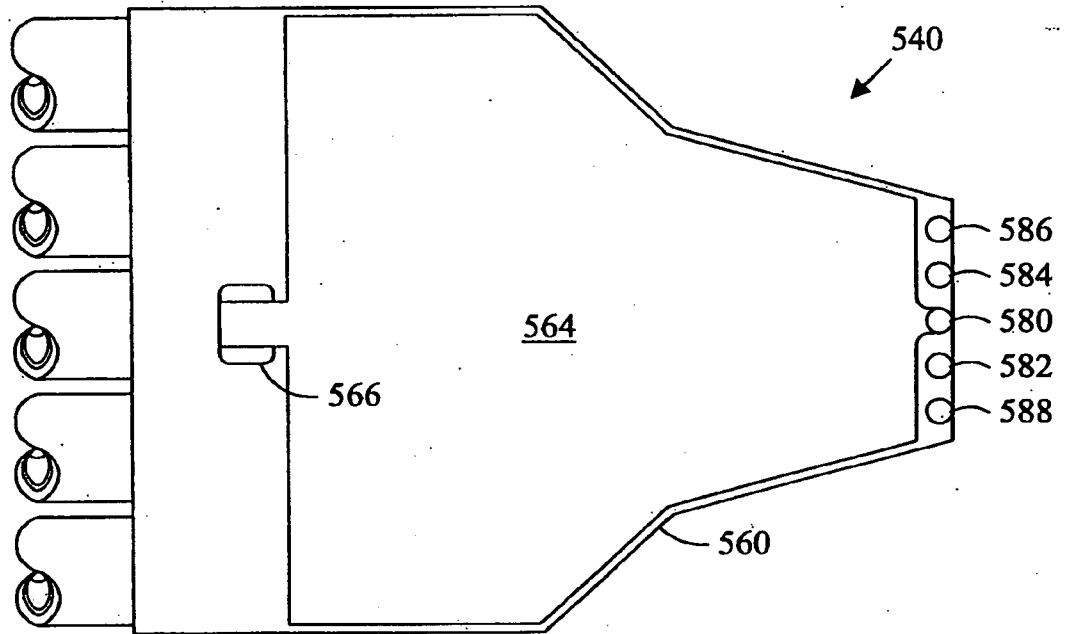


FIG. 10

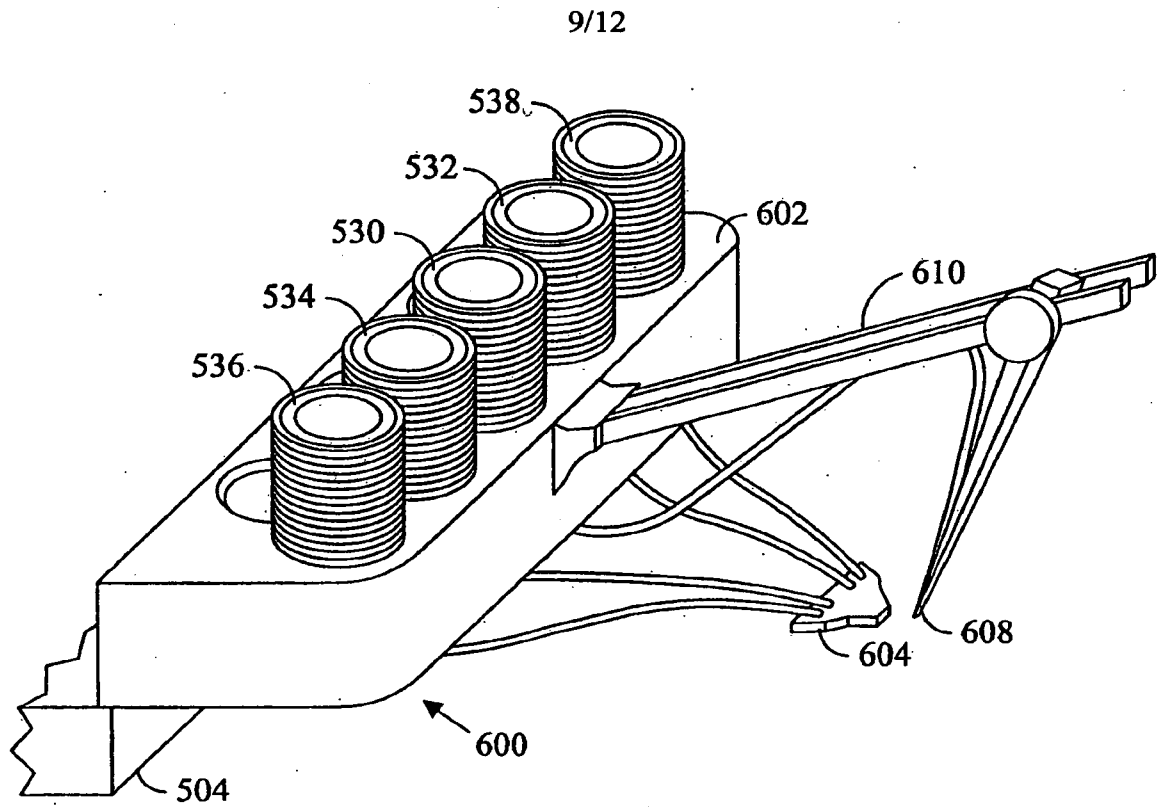


FIG. 11

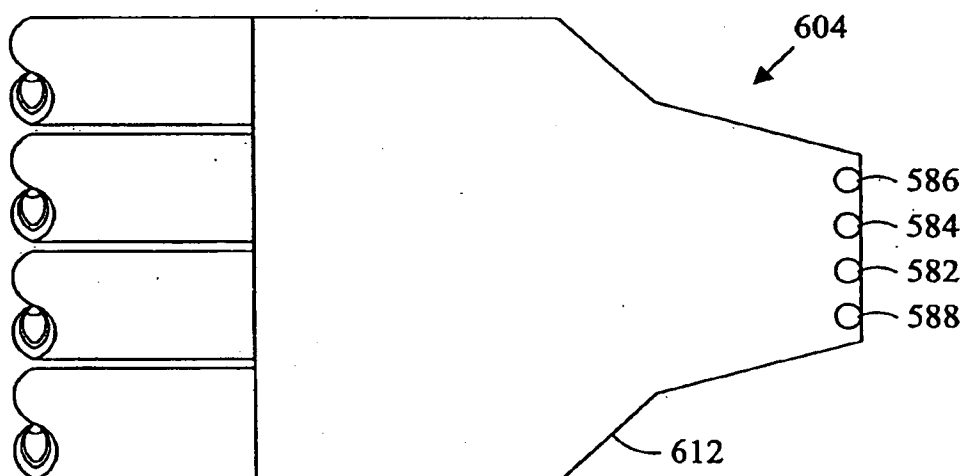


FIG. 12

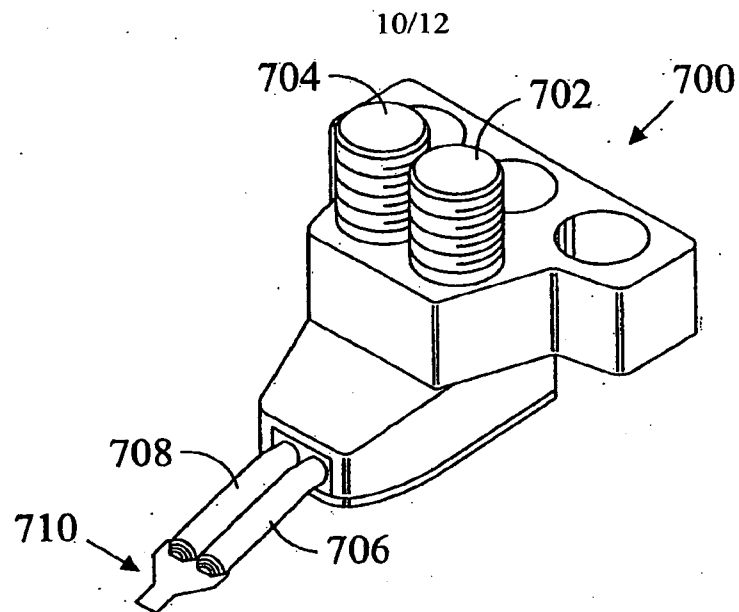


FIG. 13

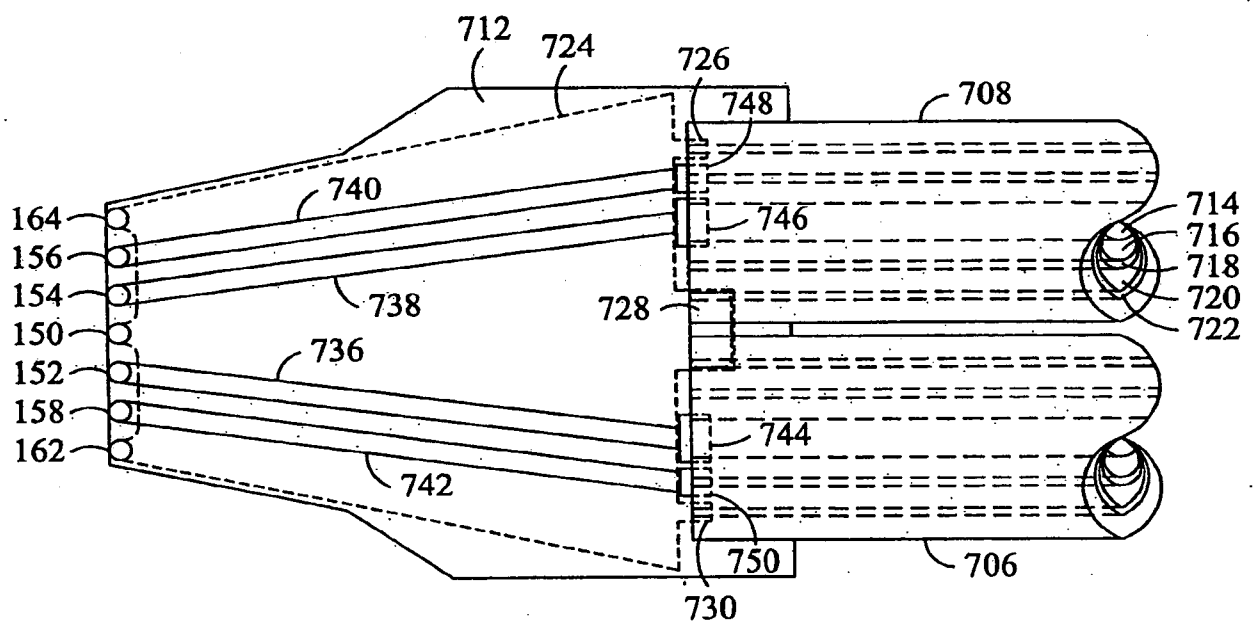


FIG. 14

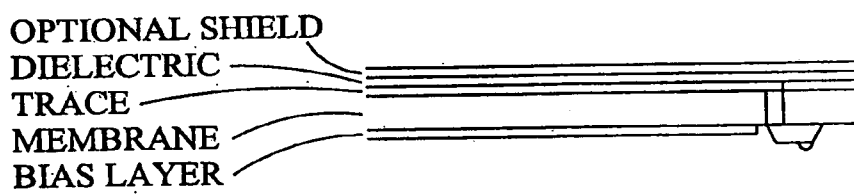
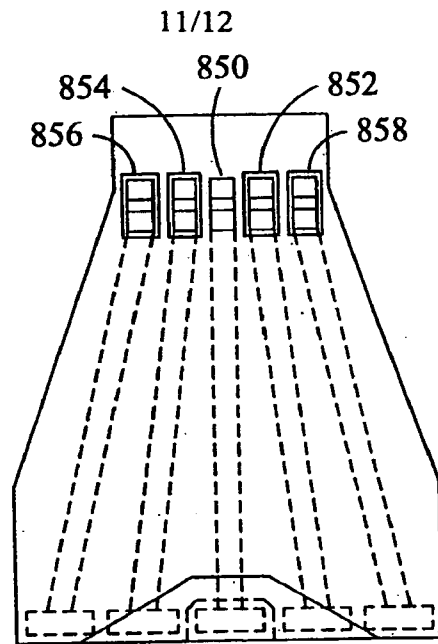


FIG. 15

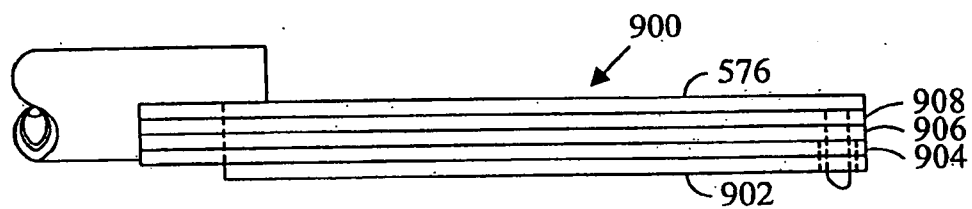


FIG. 17



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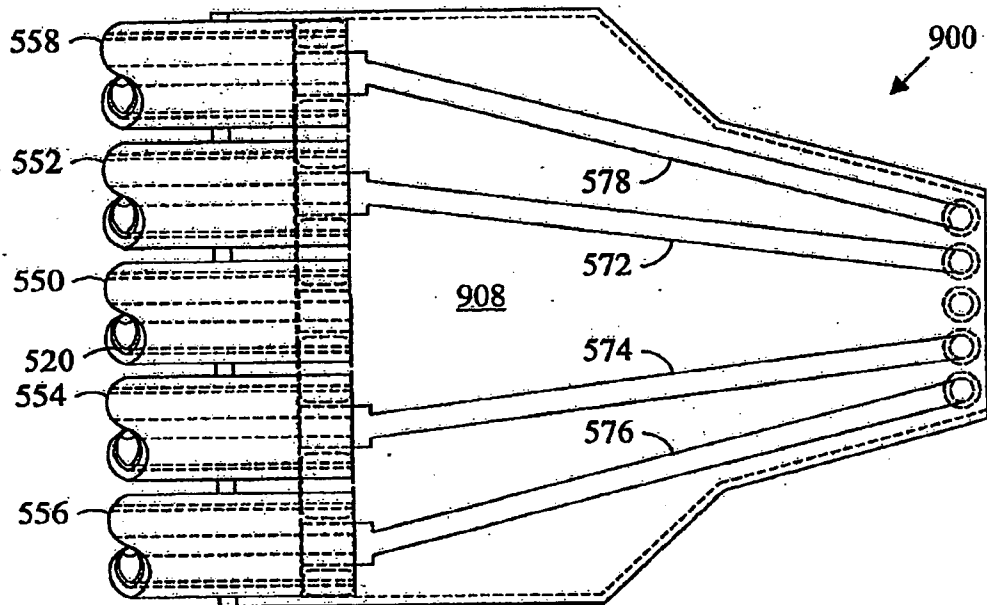


FIG. 16

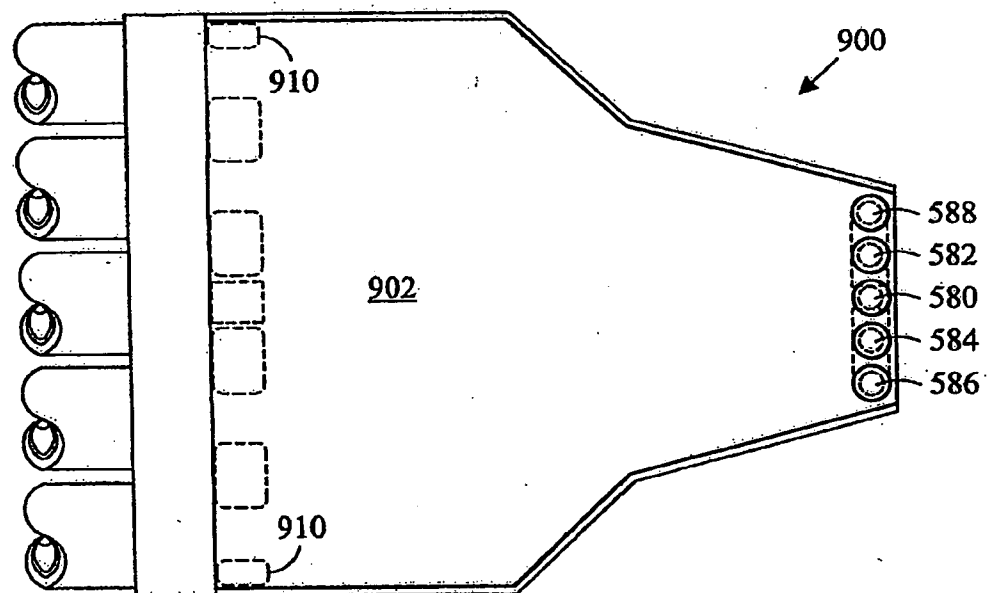


FIG. 18