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Hsu

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(54) **MANUFACTURING METHOD OF SOLDER BALL DISPOSING SURFACE STRUCTURE OF PACKAGE SUBSTRATE**

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(21) Appl. No.: **11/873,616**

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(65) **Prior Publication Data**

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(51) **Int. Cl.**
H01L 21/00 (2006.01)

(52) **U.S. Cl.** **438/613**; 438/612; 438/615

(58) **Field of Classification Search** 438/613, 438/612, 615

See application file for complete search history.

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(57) **ABSTRACT**

A manufacturing method of a solder ball disposing surface structure on a core board including: providing a core board with a first metal layer and an opposing metal bump-equipped second metal layer; forming resists on the first and second metal layers respectively; forming third, fourth and fifth openings in the resists; removing the first and second metal layers in the third and fourth openings to form first and second circuit layers and metal pads respectively; removing the metal bumps in the fifth openings to form metal flanges; removing the resists; forming first and second insulative protection layers on the first and second circuit layers and metal pads respectively; forming first and second openings in the first and second insulative protection layers to expose the first circuit layer as electrical connecting pads and expose the metal flanges respectively. Accordingly, increased contact surface area for mounting conductive elements prevents detachment thereof.

20 Claims, 12 Drawing Sheets

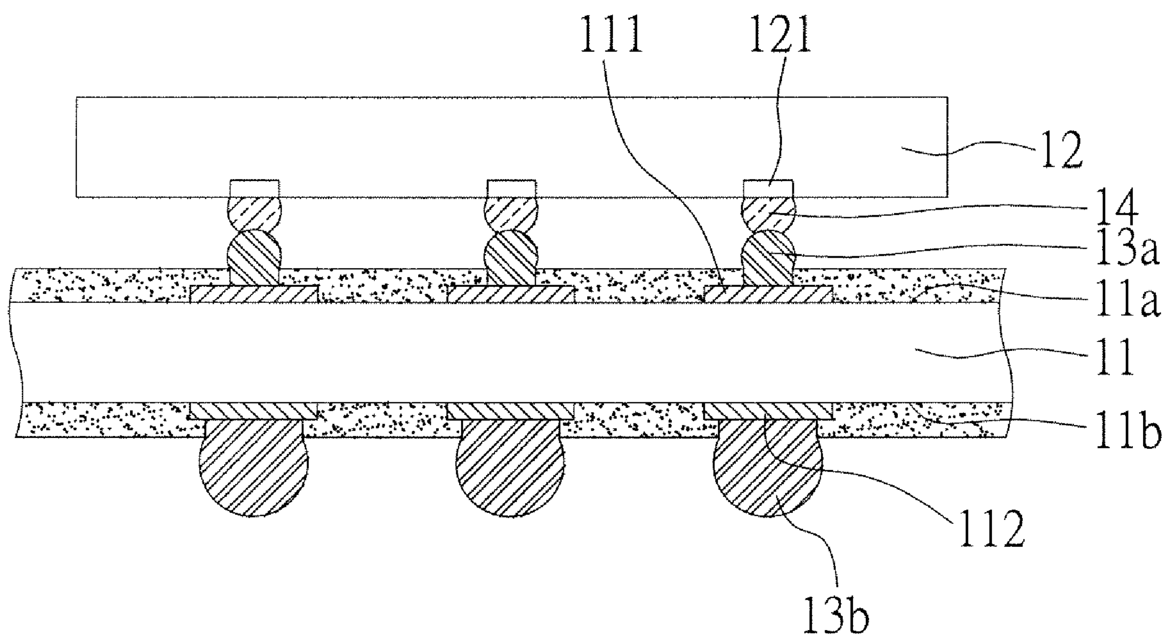

FIG. 1 (PRIOR ART)

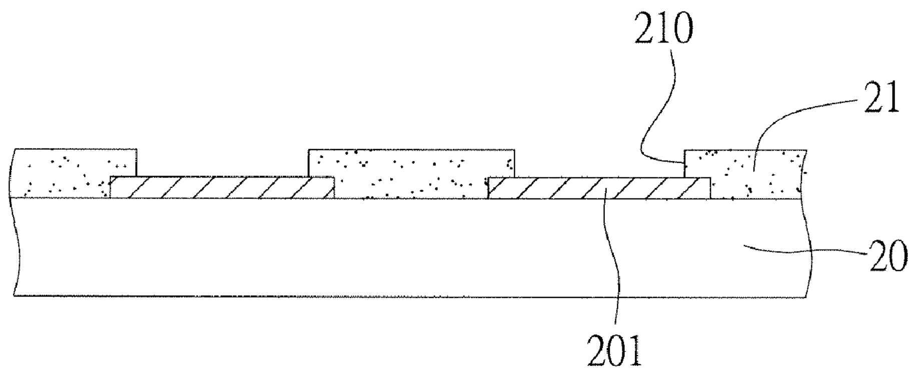

FIG. 2A (PRIOR ART)

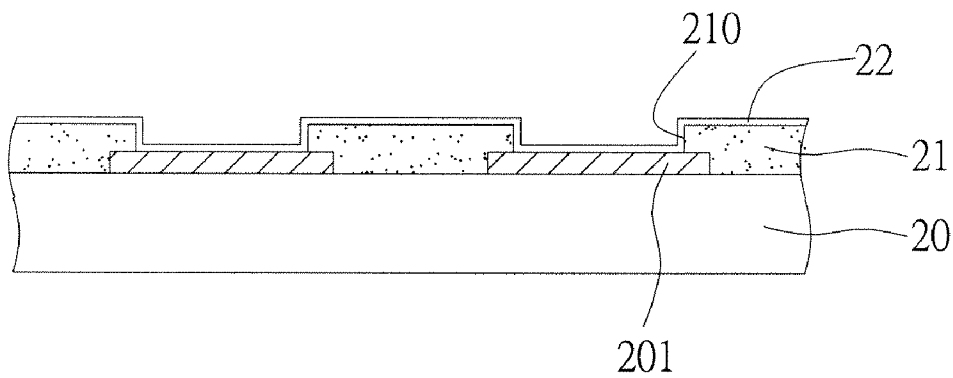

FIG. 2B (PRIOR ART)

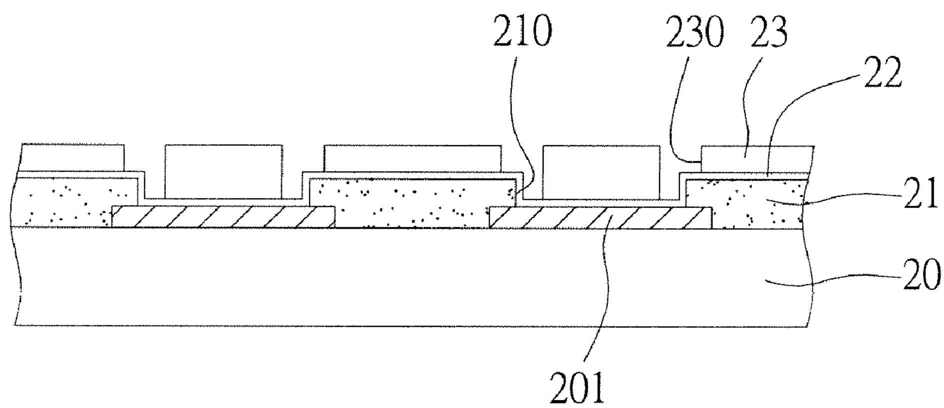

FIG. 2C (PRIOR ART)

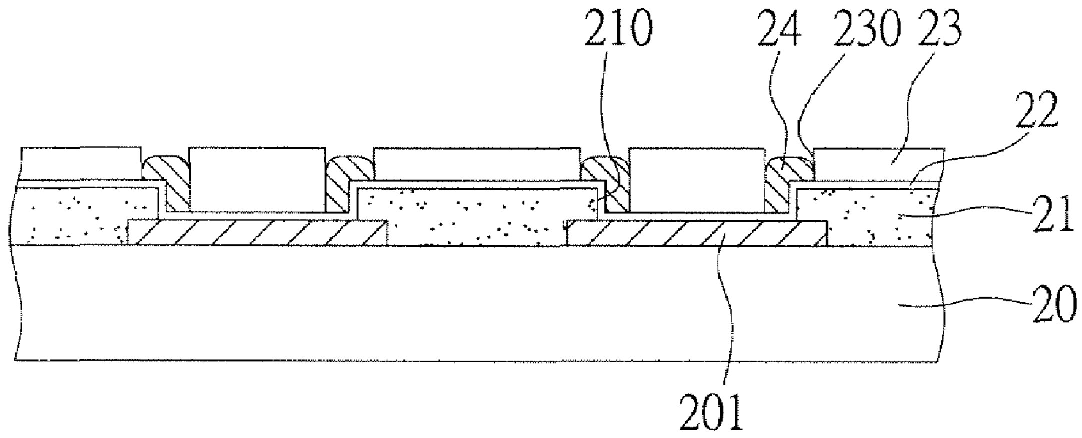

FIG. 2D (PRIOR ART)

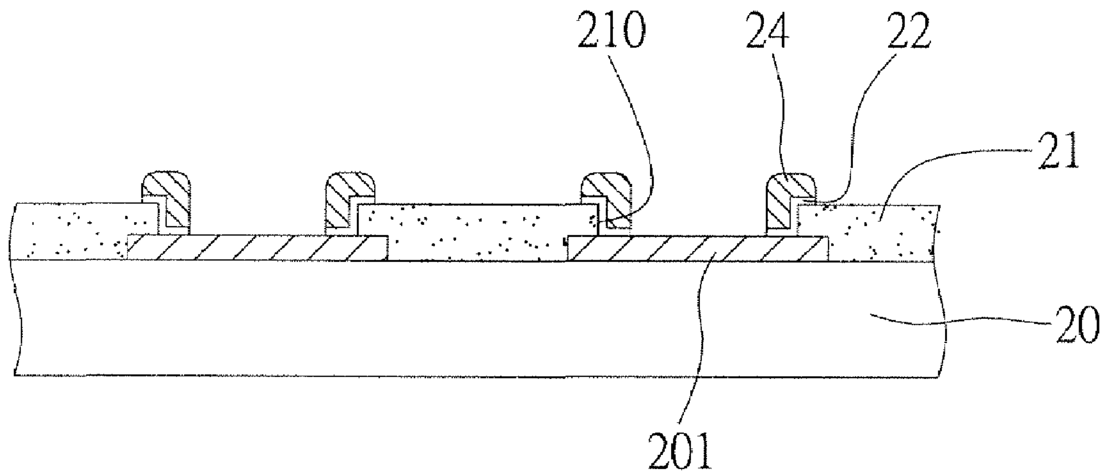

FIG. 2E (PRIOR ART)

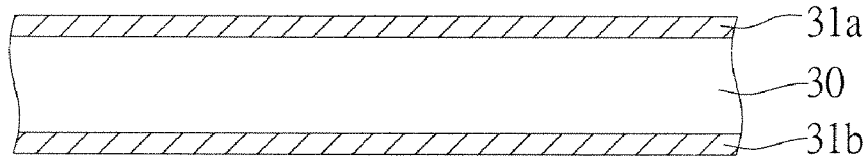

FIG. 3A

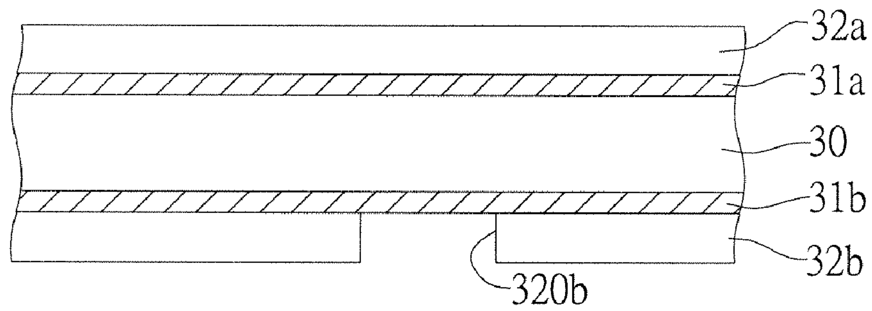

FIG. 3B

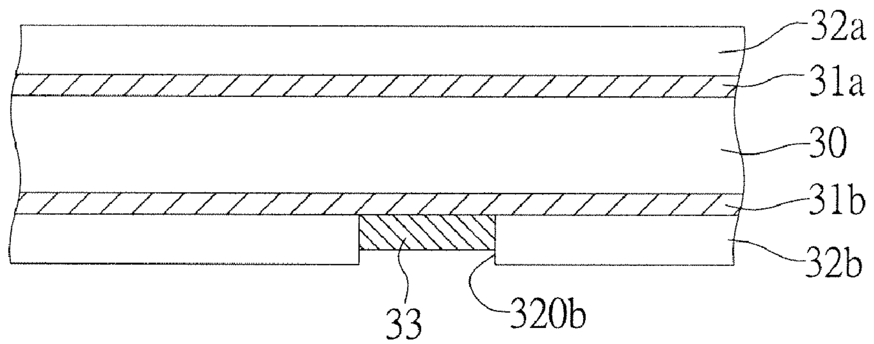

FIG. 3C

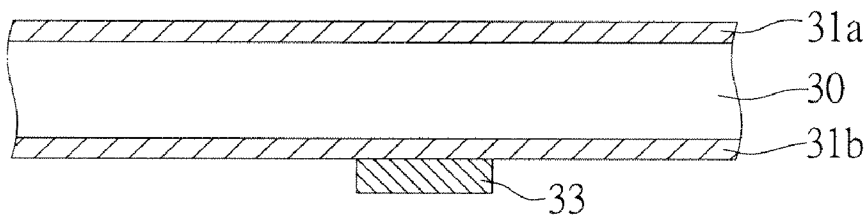

FIG. 3D

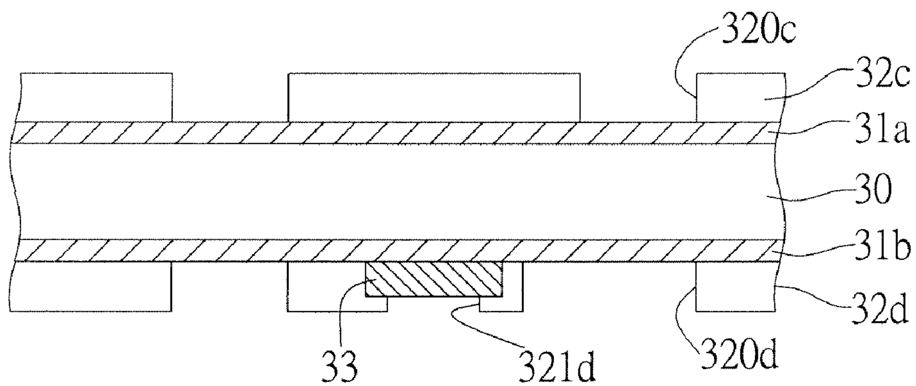

FIG. 3E

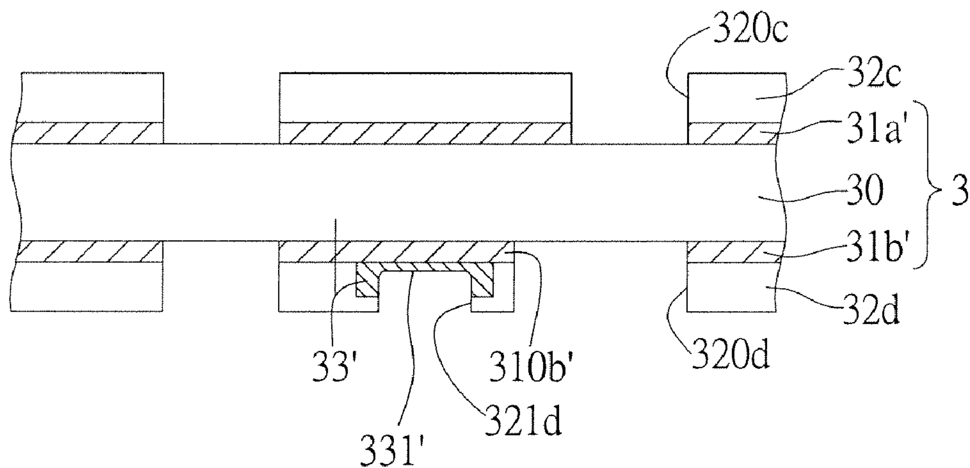

FIG. 3F

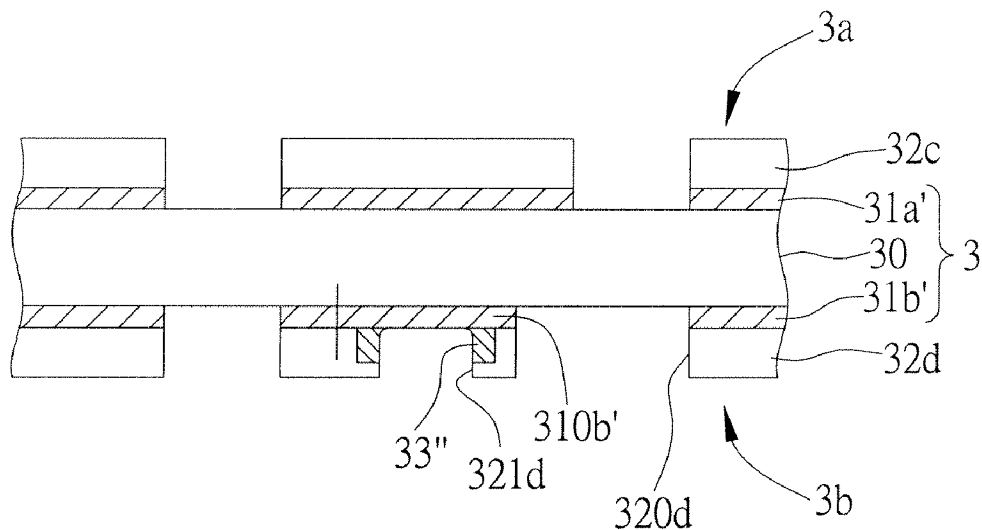

FIG. 3F'

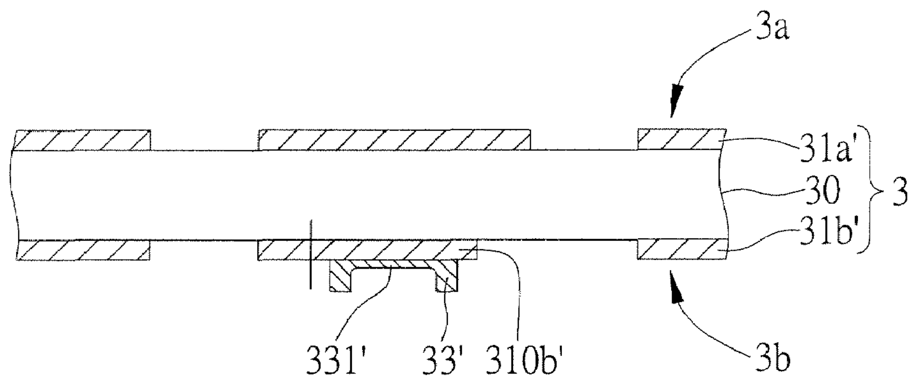

FIG. 3G

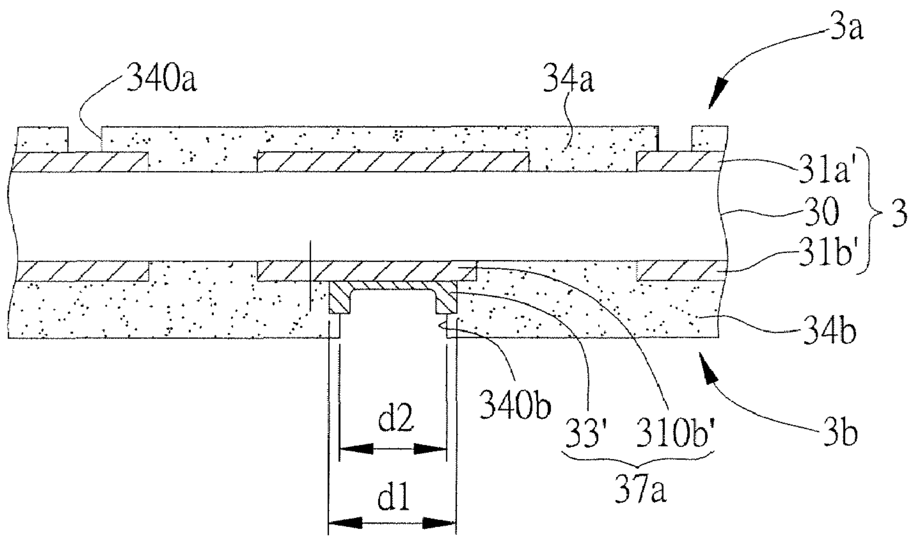

FIG. 3H

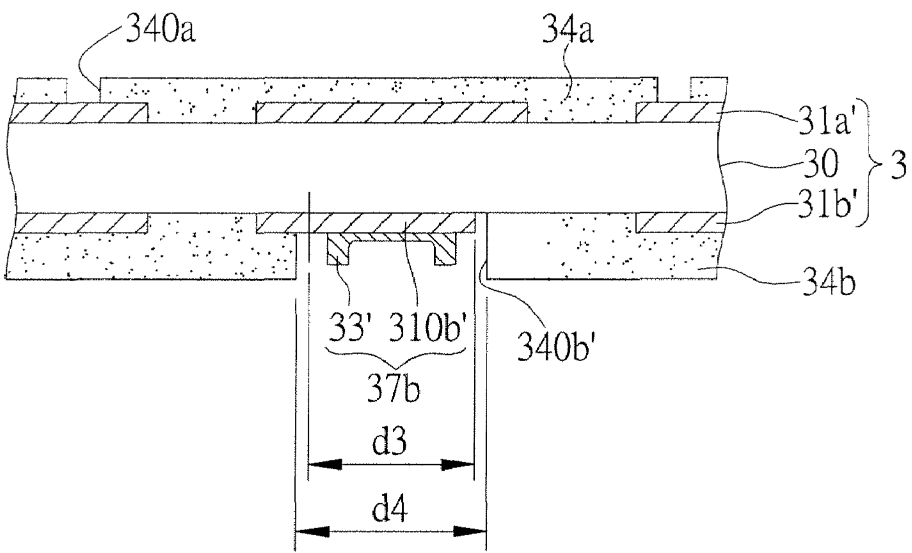

FIG. 3H'

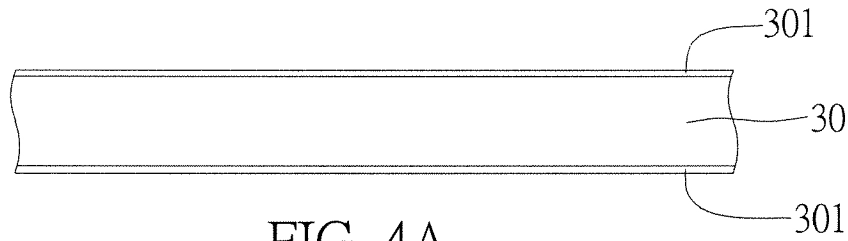

FIG. 4A

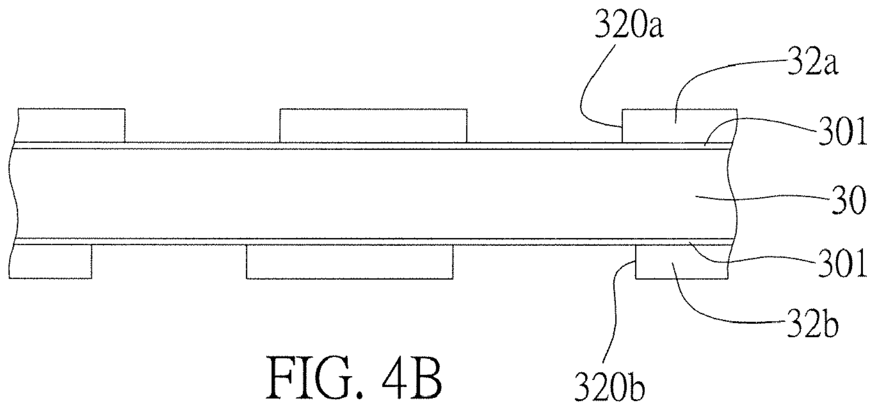

FIG. 4B

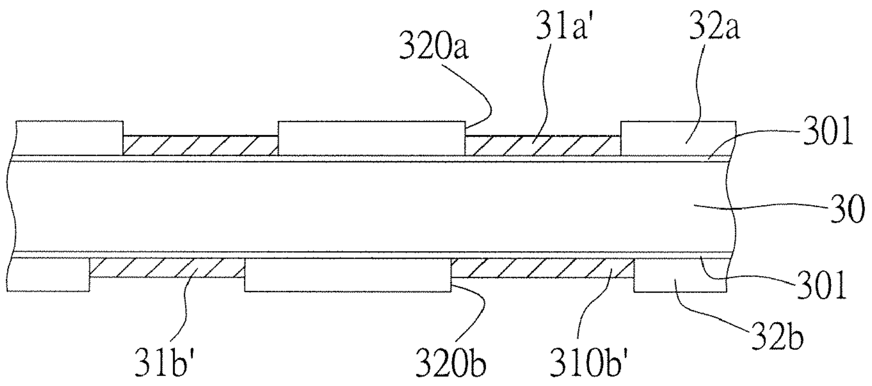

FIG. 4C

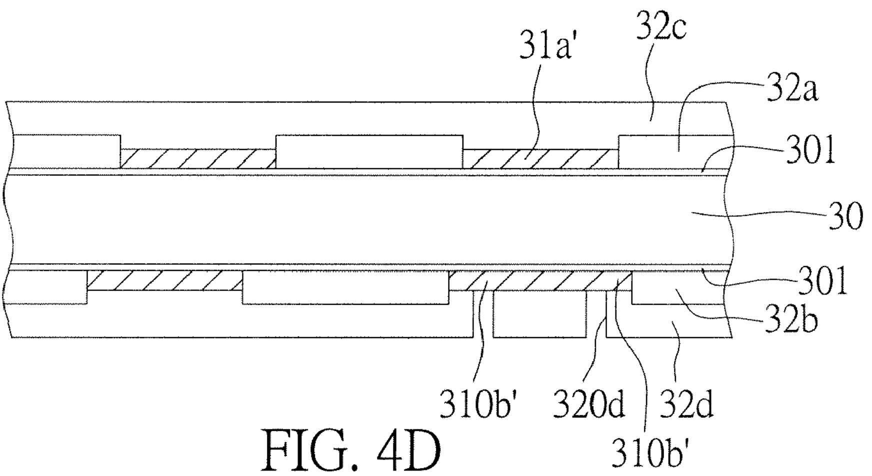

FIG. 4D

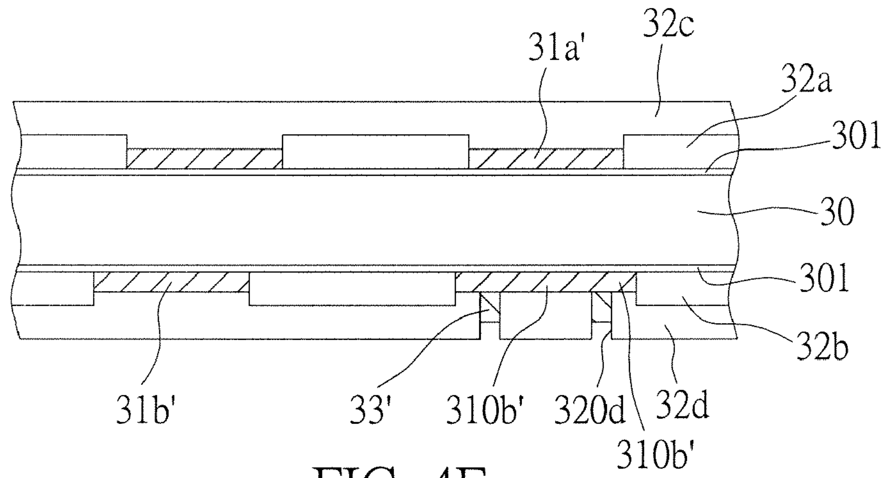

FIG. 4E

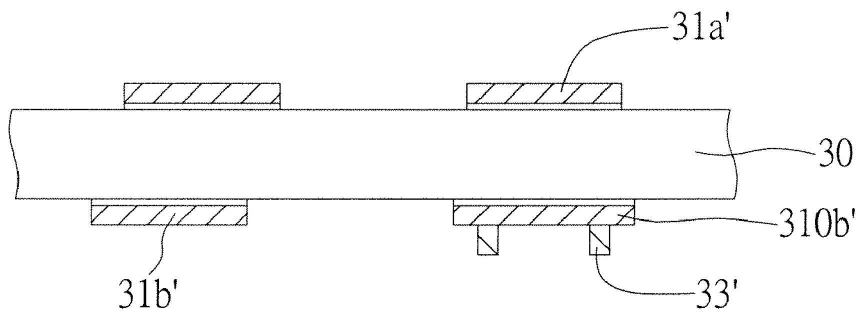

FIG. 4F

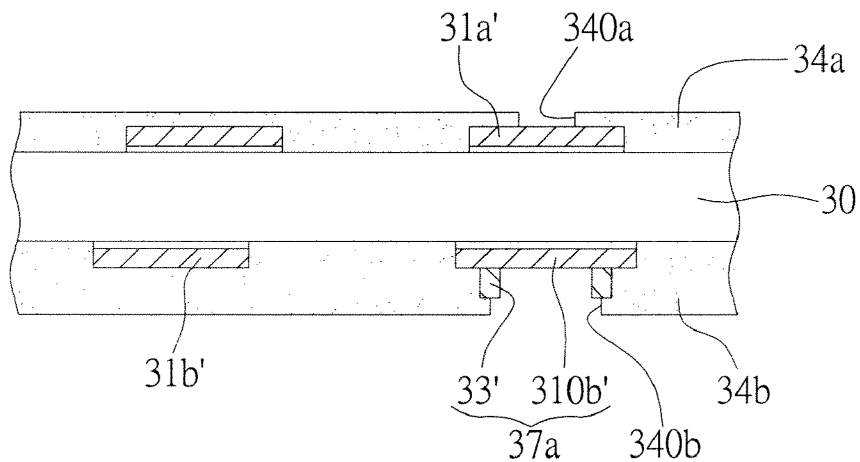

FIG. 4G

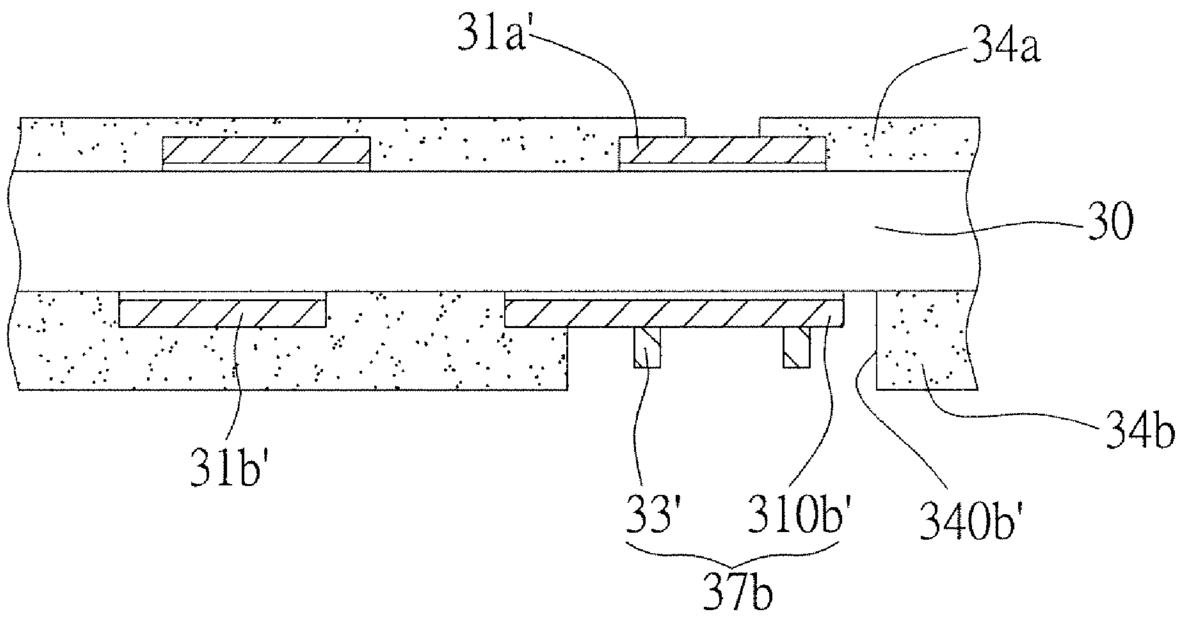

FIG. 4G'

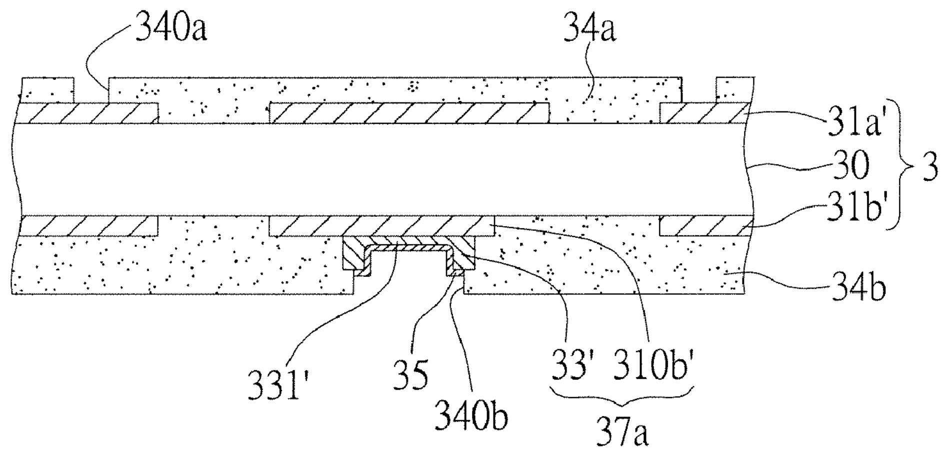

FIG. 5A

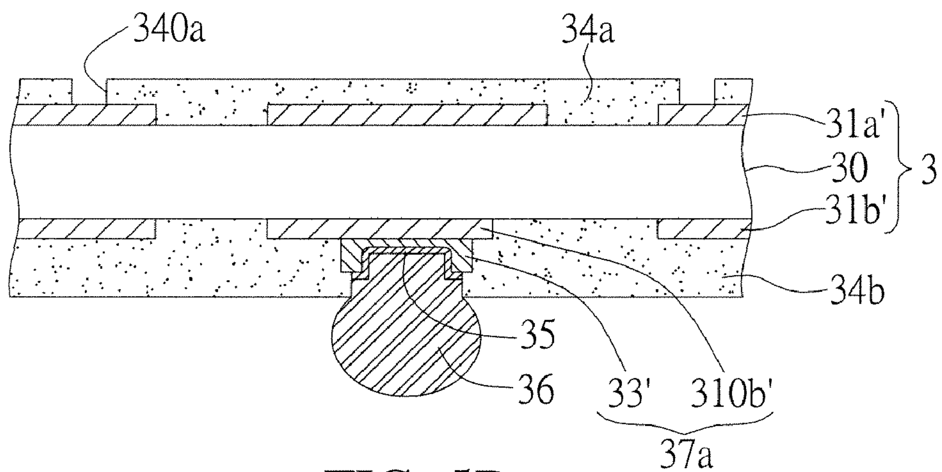

FIG. 5B

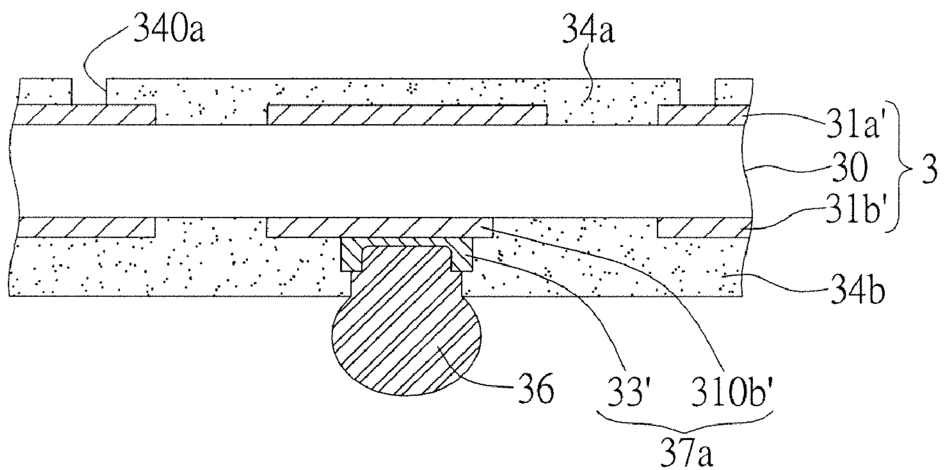

FIG. 5C

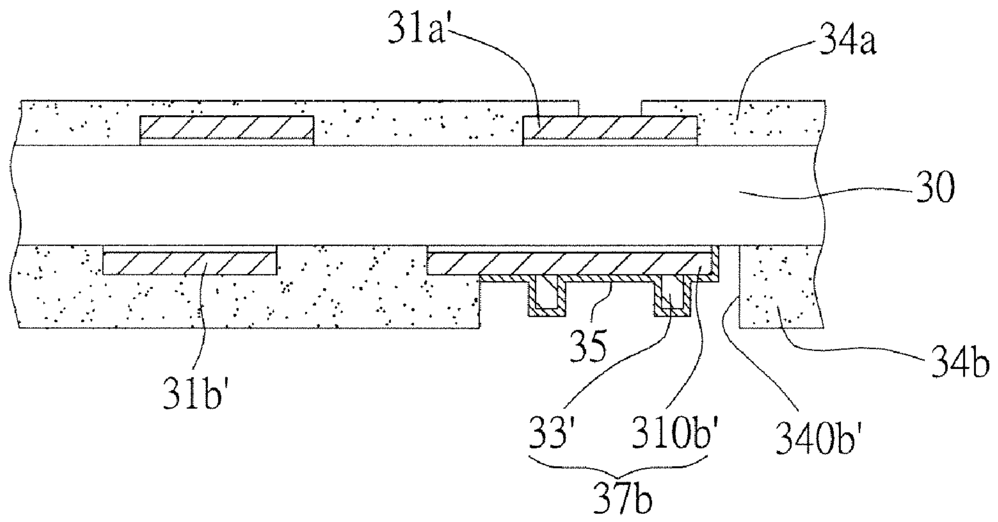

FIG. 6A

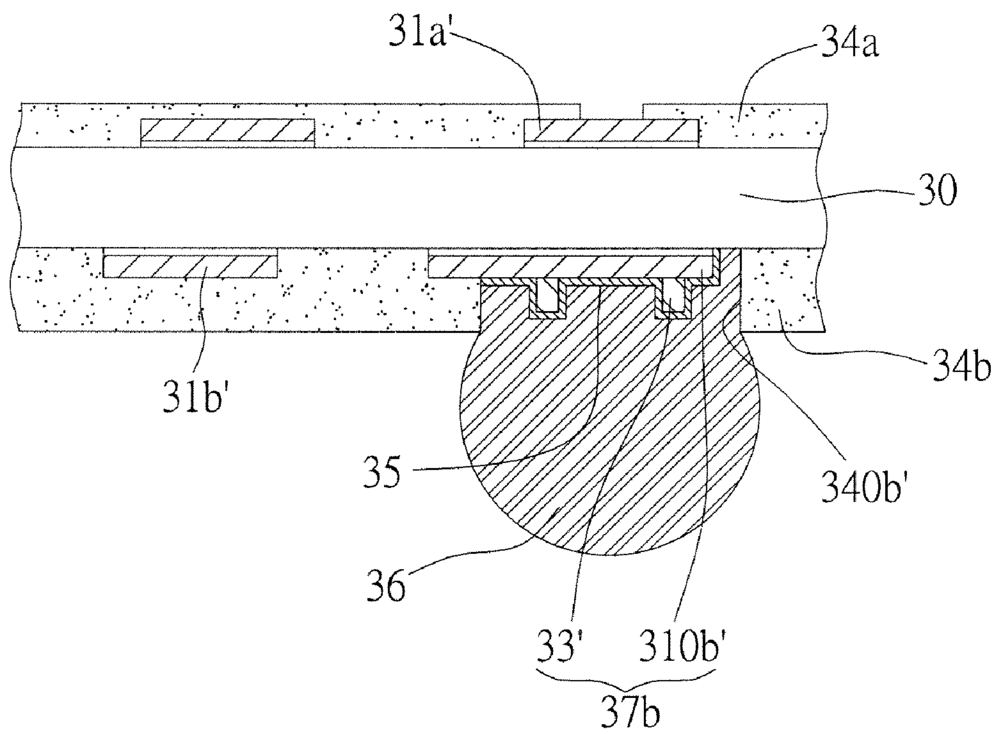

FIG. 6B

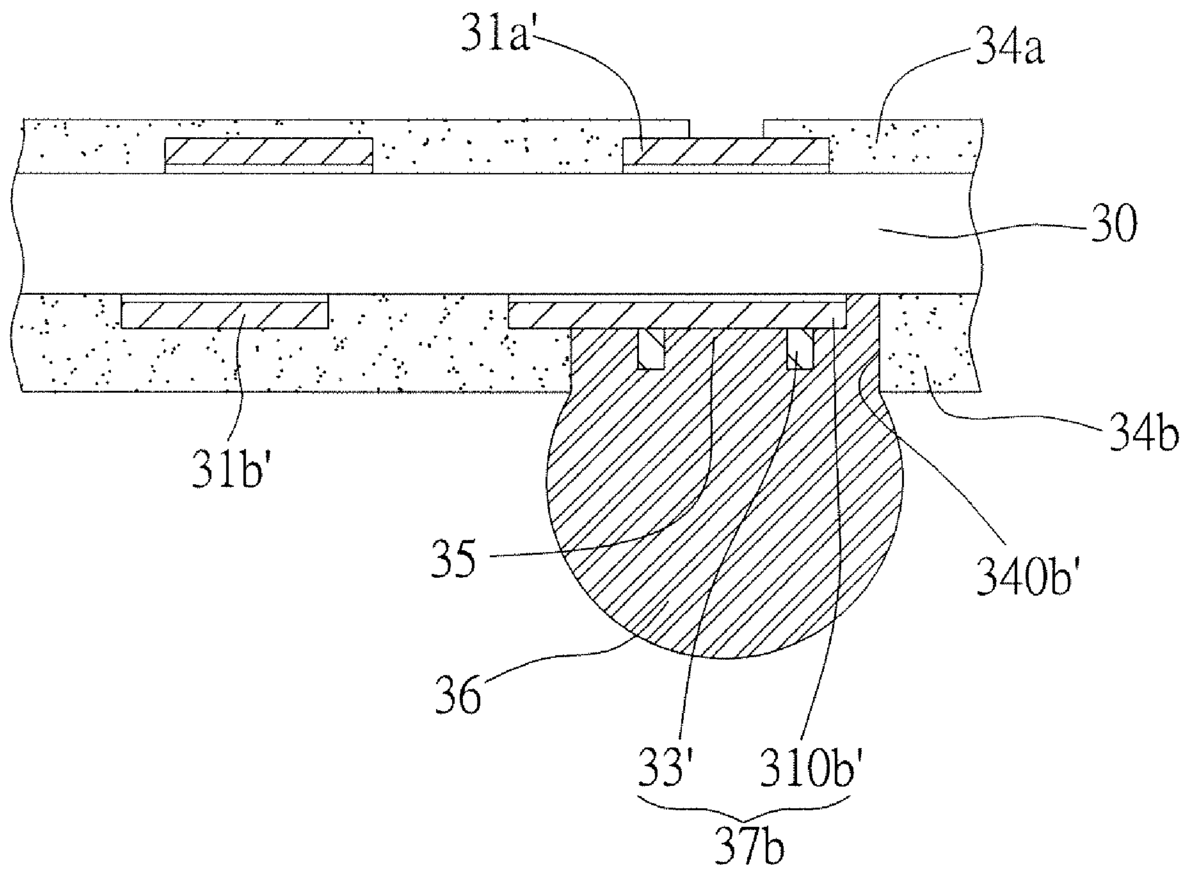

FIG. 6C

MANUFACTURING METHOD OF SOLDER BALL DISPOSING SURFACE STRUCTURE OF PACKAGE SUBSTRATE

CROSS REFERENCE TO RELATED APPLICATION

This application is related to the disclosure of Taiwanese Patent Application Number 096135299 filed on Sep. 21, 2007, the disclosure of which is expressly incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates generally to manufacturing methods of solder ball disposing surface structures, and more particularly to a manufacturing method of solder ball disposing surface structures of a package substrate.

BACKGROUND

Along with the rapid development of the electronic industries, the present electronic products are developed towards multi-function and high performance. To meet requirements of semiconductor packages for high integration and miniaturization, package substrates for carrying semiconductor chips have been developed from single layer boards to multi-layer boards. Meanwhile, interlayer connection techniques have been used to increase available circuit layout area in a limited space, thereby meeting requirements of high-density integrated circuits.

The present package substrates for carrying semiconductor chips comprise wire bonding package substrates, chip scale package (CSP) substrates, flip chip ball grid array (FCBGA) package substrates and so on. FIG. **1** exemplifies a conventional flip-chip package substrate. As shown in FIG. **1**, a package substrate **11** is provided, which comprises a first surface **11***a* for chip mounting and a second surface **11***b* for solder ball attachment. A plurality of first electrical connecting pads **111** to be electrically connected with a semiconductor chip **12** are formed on the first surface **11***a*, and a plurality of first conductive elements **13***a* made of solder material are formed on surface of the first electrical connecting pads **111**. Further, a plurality of second electrical connecting pads **112** to be electrically connected with other electronic device such as a printed circuit board are formed on the second surface **11***b*, and a plurality of second conductive elements **13***b* made of solder material are formed on surface of the second electrical connecting pads **112**. The semiconductor chip **12** has a plurality of electrode pads **121**. Metal bumps **14** are formed on the surface of each of the electrode pads **121** in a flip-chip manner and corresponding in position to the first conductive elements **13***a* of the package substrate **11**. Then at a reflow temperature capable of melting the first conductive elements **13***a*, the first conductive elements **13***a* are reflowed to the corresponding metal bumps **14**, thereby electrically connecting the semiconductor chip **12** to the package substrate **11**.

However, as the contact area between the second electrical connecting pads **112** on the second surface **11***b* of the package substrate **11** and the corresponding second conductive elements **13***b* is only limited to the exposed area of the second electrical connecting pads **112**, the bonding force between the second conductive elements **13***b* and the second electrical connecting pads **112** can be poor due to insufficient contact area therebetween, and accordingly the second conductive elements **13***b* can easily detach from the second electrical connecting pads **112**. For example, if the pitch between the second electrical connecting pads **112** is decreased from 800 μm to 400 μm, and the diameter of each of the openings for the second electrical connecting pads **112** is decreased from 500 μm to 250 μm, the contact area will be decreased to one-fourth of the initial contact area, which thus seriously reduces the bonding force between the conductive elements and the electrical connecting pads.

FIGS. **2**A to **2**E are diagrams showing a conventional method for increasing the contact area between the conductive elements and the electrical connecting pads on the solder ball disposing surface of a package substrate. As shown in FIG. **2**A, the solder ball disposing surface of the package substrate **20** is formed with electrical connecting pads **201**. An insulative protection layer **21** is formed on the solder ball disposing surface and the electrical connecting pads **201**, and a plurality of openings **210** is formed in the insulative protection layer **21** for exposing a part of the surface of the electrical connecting pads **201**. As shown in FIG. **2**B, a conductive layer **22** is formed on the insulative protection layer **21** and the exposed surface of the electrical connecting pads **201**. As shown in FIG. **2**C, a resist layer **23** is formed on the conductive layer **22**, and a plurality of ring-shaped openings **230** is formed in the resist layer **23** by exposure and development so as to expose the conductive layer **22** on the electrical connecting pads **201** around the openings **210** of the insulative protection layer **21**. As shown in FIG. **2**D, by using the conductive layer **22** as a current conductive path for electroplating, flanges **24** are formed in the ring-shaped openings **230**, the flanges **24** being attached to periphery of the openings **210** of the insulative protection layer **21**. Finally, the resist layer **23** and the conductive layer **22** covered by the resist layer **23** are removed so as to expose the flanges **24** and a part of the surface of the electrical connecting pads **201**.

However, since the conductive layer **22** is left between the flanges **24** and the electrical connecting pads **201**, the bonding strength between the flanges **24** and the electrical connecting pads **201** is reduced. In addition, as the formed flanges **24** are attached to the periphery of the openings **210** of the insulative protection layer **21**, the present method provides only a limited increase of the contact area for the conductive elements such as solder balls subsequently formed on the electrical connecting pads **201** and the flanges **24**. As a result, detaching of the solder balls still can easily occur. Therefore, how to provide a structure capable of increasing the bonding force between solder balls and electrical connecting pads on the solder ball disposing surface of a package substrate so as to avoid detaching of the solder balls from the electrical connecting pads caused by reduced bonding area has become urgent.

SUMMARY

According to the above drawbacks, an objective of the present invention is to provide a manufacturing method of a solder ball disposing surface structure of a package substrate through which contact area of the surface structure for mounting conductive elements can be increased.

Another objective of the present invention is to provide a manufacturing method of a solder ball disposing surface structure of a package substrate through which the bonding force between the solder ball disposing surface structure and the conductive elements can be increased.

In order to attain the above and other objectives, the present invention discloses a manufacturing method of a solder ball disposing surface structure of a package substrate, which comprises: providing a core board with a first metal layer and a second metal layer respectively formed on two opposite

surfaces thereof; forming metal bumps on the second metal layer by electroplating; forming a third resist layer on the first metal layer and forming third openings in the third resist layer for exposing a part of the surface of the first metal layer, and forming a fourth resist layer on the second metal layer and the metal bumps and forming fourth openings in the fourth resist layer for exposing a part of the surface of the second metal layer and forming fifth openings in the fourth resist layer for exposing a part of the surface of the metal bumps; removing the first and second metal layers in the third and fourth openings of the third and fourth resist layers so as to respectively form a first circuit layer, a second circuit layer and metal pads on the two opposite surfaces of the core board, and removing the metal bumps in the fifth openings so as to form metal flanges disposed around the metal pads; removing the third and fourth resist layers; forming a first insulative protection layer on the core board and the first circuit layer and forming first openings in the first insulative protection layer for exposing a part of the surface of the first circuit layer as electrical connecting pads; and forming a second insulative protection layer on the core board, the second circuit layer and the metal pads, and forming second openings in the second insulative protection layer so as to expose a part of the surface of the metal flanges.

Therein, size of the second openings can be not bigger than outer diameter of the metal flanges. Alternatively, size of the second openings can be bigger than outer diameter of the metal pads.

The core board can be a two-layer or multi-layer circuit board with a dielectric layer on surface thereof or an insulating board. The metal flanges can have a shape of circle, ellipse, rectangle or irregular shape. The metal pads can have a shape of circle, ellipse, rectangle or irregular shape. Outer diameter of the metal flanges is not bigger than that of the metal pads.

The manufacturing method of forming the metal bumps on the second metal layer by electroplating comprises: forming a first resist layer and a second resist layer on the first metal layer and the second metal layer respectively, the second resist layer having openings for exposing a part of the surface of the second metal layer; forming metal bumps on the second metal layer in the second openings of the second resist layer by electroplating; and removing the first and second resist layers so as to expose the first metal layer, the second metal layer and the metal bumps.

In the above-described manufacturing method, the metal bumps in the fifth openings are partly removed so as to form a metal layer on the metal pads. A surface treatment layer is formed on the metal flanges and the metal layer. The surface treatment layer may be one of an OSP (Organic solderability preservatives) layer, a Ni/Au layer, a Ni/Pd/Au layer and a Sn/Pb layer. Alternatively, the surface treatment layer may be made of one of the group consisting of Au, Ag, Sn and Cu. Conductive elements of solder balls are further formed on the surface treatment layer or formed on the metal flanges and the metal layer.

According to another embodiment of the present invention, the metal bumps in the fifth openings are thoroughly removed so as to expose a part of the surface of the metal pads. A surface treatment layer is formed on the metal flanges and the metal pads. The surface treatment layer may be one of an OSP layer, a Ni/Au layer, a Ni/Pd/Au layer and a Sn/Pb layer. Alternatively, the surface treatment layer may be made of one of the group consisting of Au, Ag, Sn and Cu. Conductive elements of solder balls are further formed on the surface treatment layer or formed on the metal flanges and the metal pads.

The present invention provides another manufacturing method of a solder ball disposing surface structure of a package substrate, which comprises: providing a core board; forming a conductive layer on two opposite surfaces of the core board; respectively forming a first resist layer and a second resist layer on the conductive layer on the two opposite surfaces of the core board, the first and second resist layers respectively having first openings and second openings for exposing a part of the surface of the conductive layer; respectively forming a first circuit layer and a second circuit layer in the first and second openings of the first and second resist layers by electroplating, wherein the second circuit layer has metal pads; forming a third resist layer on the first resist layer and the first circuit layer, and forming a fourth resist layer on the second resist layer and the second circuit layer, the fourth resist layer having ring-shaped openings for exposing a part of the surface of the metal pads; forming metal flanges on the metal pads by using the conductive layer as a current conductive path for electroplating; removing the third resist layer, the first resist layer and the conductive layer covered by the first resist layer, the fourth resist layer, the second resist layer, and the conductive layer covered by the second resist layer, thereby exposing the first circuit layer, the second circuit layer and the metal flanges on the metal pads; forming a first insulative protection layer on the core board and the first circuit layer and forming first openings in the first insulative protection layer for exposing a part of the surface of the first circuit layer as electrical connecting pads; and forming a second insulative protection layer on the core board, the second circuit layer and the metal pads, and forming second openings in the second insulative protection layer so as to expose a part of the surface of the metal flanges.

Therein, size of the second openings can be not bigger than outer diameter of the metal flanges. Alternatively, size of the second openings can be bigger than outer diameter of the metal pads.

The core board can be a two-layer or multi-layer circuit board with a dielectric layer on surface thereof, a copper clad laminate board, or an insulating board. The metal flanges can have a shape of circle, ellipse, rectangle or irregular shape. The metal pads can have a shape of circle, ellipse, rectangle or irregular shape. Outer diameter of the metal flanges is not bigger than that of the metal pads.

A surface treatment layer can further be formed on the metal flanges and the metal pads. The surface treatment layer may be one of an OSP layer, a Ni/Au layer, a Ni/Pd/Au layer and a Sn/Pb layer. Alternatively, the surface treatment layer may be made of one of the group consisting of Au, Ag, Sn and Cu. Conductive elements of solder balls are further formed on the surface treatment layer or formed on the metal flanges and the metal pads.

According to the present invention, as metal flanges are formed on the metal pads of the solder ball disposing surface of a package substrate, contact area of the metal pads is increased. In addition, the bonding area for conductive elements on electrical connecting pads can further be increased by adjusting type of openings in the insulative protection layer. Moreover, since no conductive layer is formed between the metal pads and the metal flanges as in the prior art, the bonding strength between the metal pads and the metal

flanges is improved, thereby preventing detaching of the conductive elements subsequently formed on the metal pads and the metal flanges.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a diagram of a conventional package substrate with a semiconductor chip disposed thereon;

FIGS. **2**A to **2**E are sectional diagrams showing a conventional method for forming flanges on electrical connecting pads of a package substrate;

FIGS. **3**A to **3**H are sectional diagrams showing a manufacturing method of a solder ball disposing surface structure of a package substrate according to a first embodiment of the present invention, wherein FIG. **3**F' is another embodiment of FIG. **3**F and FIG. **3**H' is another embodiment of FIG. **3**H;

FIGS. **4**A to **4**G are sectional diagrams showing a manufacturing method of a solder ball disposing surface structure of a package substrate according to a second embodiment of the present invention;

FIG. **4**G' is another embodiment of FIG. **4**G;

FIG. **5**A is a diagram showing a solder ball disposing surface structure with a surface treatment layer disposed on the metal pads and the metal flanges of SMD pads;

FIG. **5**B is a diagram showing a solder ball disposing surface structure with conductive elements disposed on the surface treatment layer of FIG. **5**A;

FIG. **5**C is a diagram showing a solder ball disposing surface structure with conductive elements disposed on the metal pads and the metal flanges of SMD pads;

FIG. **6**A is a diagram showing a solder ball disposing surface structure with a surface treatment layer disposed on the metal pads and the metal flanges of NSMD pads;

FIG. **6**B is a diagram showing a solder ball disposing surface structure with conductive elements disposed on the surface treatment layer of FIG. **6**A; and

FIG. **6**C is a diagram showing a solder ball disposing surface structure with conductive elements disposed on the metal pads and the metal flanges of NSMD pads.

DETAILED DESCRIPTION

The following illustrative embodiments are provided to illustrate the disclosure of the present invention, these and other advantages and effects can be apparent to those skilled in the art after reading the disclosure of this specification.

First Embodiment

FIGS. **3**A to **3**H are sectional diagrams showing a manufacturing method of a solder ball disposing surface structure of a package substrate according to a first embodiment of the present invention.

As shown in FIG. **3**A, a core board **30** with a first metal layer **31***a* and a second metal layer **31***b* respectively formed on two opposite surfaces thereof is provided. The core board **30** can be a two-layer or multi-layer circuit board with a dielectric layer on surface thereof or an insulating board. Since the manufacturing technique of circuit boards is well known in the art and not characteristic of the present invention, detailed description thereof is omitted.

As shown in FIG. **3**B, a first resist layer **32***a* and a second resist layer **32***b* are formed on the first metal layer **31***a* and the second metal layer **31***b*, respectively. The first and second resist layers **32***a*, **32***b* can be such as a dry film or liquid photoresist, which is formed on the first and second metal layers **31***a*, **31***b* by printing, spin coating or attaching and then patterned by exposure and development so as to form second openings **320***b* in the second resist layer **32***b* for exposing a part of the surface of the second metal layer **31***b*.

As shown in FIG. **3**C, by using the second metal layer **31***b* as a current conductive path for electroplating, metal bumps **33** are formed on the second metal layer **31***b* exposed from the second openings **320***b* of the second resist layer **32***b*.

As shown in FIG. **3**D, the first and second resist layers **32***a*, **32***b* are removed so as to expose the first and second metal layers **31***a*, **31***b* and the metal bumps **33**.

As shown in FIG. **3**E, a third resist layer **32***c* is formed on the first metal layer **31***a*, and a plurality of third openings **320***c* is formed in the third resist layer **32***c* for exposing a part of the surface of the first metal layer **31***a*; and a fourth resist layer **32***d* is formed on the second metal layer **31***b* and the metal bumps **33**, and fourth openings **320***d* are formed in the fourth resist layer **32***d* for exposing a part of the surface of the second metal layer **31***b* and fifth openings **321***d* are formed in the fourth resist layer **32***d* for exposing a part of the surface of the metal bumps **33**.

As shown in FIGS. **3**F and **3**F', the first metal layer **31***a* in the third openings **320***c* of the third resist layer **32***c*, the second metal layer **31***b* in the fourth openings **320***d* of the fourth resist layer **32***d*, as well as the metal bumps **33** in the fifth opening **321***d* are removed by etching, thereby forming a first circuit layer **31***a*', a second circuit layer **31***b*' and metal pads **310***b*' on the two opposite surfaces of the core board **30**, respectively. Therein, each metal bump **33** is partly removed so as to form a metal flange **33'** that is disposed around the metal pad **310***b*' and meanwhile form a metal layer **331'** on the metal pad **310***b*' inside the metal flange **33'**, as shown in FIG. **3**F. Alternatively, each metal bump **33** in the fifth opening **321***d* can be thoroughly removed, thereby only forming a metal flange **33"** that is disposed around the metal pad **310***b*', as shown in FIG. **3**F'. Thus, the core board **30**, the first circuit layer **31***a*' and the second circuit layer **31***b*' constitute a package substrate **3**, which has a chip disposing surface **3***a* with the first circuit layer **31***a*' and an opposed solder ball disposing surface **3***b* with the second circuit layer **31***b*'.

As shown in FIG. **3**G, the third and fourth resist layers **32***c*, **32***d* are removed so as to expose the first circuit layer **31***a*', the second circuit layer **31***b*', the metal pads **310***b*' and the metal flanges **33'** disposed around the metal pads **310***b*'.

As shown in FIGS. **3**H and **3**H', a first insulative protection layer **34***a* is formed on the core board **30** and the first circuit layer **31***a*', and first openings **340***a* is formed in the first insulative protection layer **34***a* so as to expose a part of the surface of the first circuit layer **31***a*' as electrical connecting pads for electrically connecting a semiconductor chip. A second insulative protection layer **34***b* is formed on the core board **30**, the second circuit layer **31***b*' and the metal pads **310***b*', and the second insulative protection layer **34***b* has second openings **340***b* formed for exposing a part of the surface of the metal flanges **33'**, wherein size d**2** of the second openings **340***b* is smaller than outer diameter d**1** of the metal flanges **33'** such that solder mask defined (SMD) pads **37***a* can be formed, as shown in FIG. **3**H. Alternatively, as shown in FIG. **3**H', size d**4** of the second openings **340***b*' is bigger than size d**3** of the metal pads **310***b*' such that the metal pads **310***b*' and the metal flanges **33'** can be exposed to form non solder mask defined (NSMD) pads **37***b*.

Thus, the present invention provides a solder ball disposing surface structure of a package substrate. As shown in FIG. **3**H, the package substrate **3** has a chip disposing surface **3***a* with a first circuit layer **31***a*' and a solder ball disposing surface **3***b* with a second circuit layer **31***b*', a first insulative protection layer **34***a* being formed on the chip disposing surface **3***a* and

the first circuit layer **31**a'. The solder ball disposing surface structure comprises: metal pads **310**b', which are a part of the second circuit layer **31**b'; metal flanges **33'** disposed around the metal pads **310**b'; and a second insulative protection layer **34**b formed on the solder ball disposing surface **3**b and having second openings **340**b.

According to the above structure, size of the second openings **340**b can be smaller than outer diameter of the metal flanges **33'** so as to expose a part of the surface of the metal flanges **33'**, thereby forming SMD pads **37**a; or size of the second openings **340**b' can be bigger than that of the metal pads **310**b' so as to expose the metal pads **310**b' and the metal flanges **33'**, thereby forming NSMD pads **37**b. The metal flanges **33'** can have a shape of circle, ellipse, rectangle or irregular shape. The metal pads **310**b' can have a shape of circle, ellipse, rectangle or irregular shape. Outer diameter of the metal flanges **33'** is not bigger than that of the metal pads **310**b'.

Second Embodiment

FIGS. **4**A to **4**G are sectional diagrams showing a manufacturing method of a solder ball disposing surface structure of a package substrate according to a second embodiment of the present invention.

As shown in FIG. **4**A, a core board **30** with a conductive layer **301** formed on two opposite surfaces thereof is provided. The core board **30** can be an insulating board, a copper clad laminate board or a two-layer or multi-layer circuit board having dielectric layer on surface thereof. Since the manufacturing technique of circuit boards is well known in the art and not characteristic of the present invention, detailed description thereof is omitted.

As shown in FIG. **4**B, a first resist layer **32**a and a second resist layer **32**b are formed on the conductive layer **301** of the two opposite surfaces of the core board **30**, respectively. The first and second resist layers **32**a, **32**b respectively have first openings **320**a and second openings **320**b for exposing a part of the surface of the conductive layer **301**.

As shown in FIG. **4**C, by using the conductive layer **301** as a current conductive path for electroplating, a first circuit layer **31**a' is formed in the first openings **320**a of the first resist layer **32**a and a second circuit layer **31**b' is formed in the second openings **320**b of the second resist layer **32**b, wherein the second circuit layer **31**b' has metal pads **310**b'.

As shown in FIG. **4**D, a third resist layers **32**c is formed on surfaces of the first resist layer **32**a and the first circuit layer **31**a', and a fourth resist layer **32**d is formed on surfaces of the second resist layer **32**b and the second circuit layer **31**b', wherein the fourth resist layer **32**d has ring-shaped openings **320**d for exposing a part of the surface of the metal pads **310**b'.

As shown in FIG. **4**E, by using the conductive layer **301** as a current conductive path for electroplating, metal flanges **33'** are formed on the surface of the metal pads **310**b'.

As shown in FIG. **4**F, the third resist layer **32**c, the first resist layer **32**a and the conductive layer **301** covered by the first resist layer **32**a, the fourth resist layer **32**d, the second resist layer **32**b and the conductive layer **301** covered by the second resist layer **32**b are removed so as to expose the first circuit layer **31**a', the second circuit layer **31**b' and the metal flanges **33'** on the metal pads **310**b'.

As shown in FIGS. **4**G and **4**G', a first insulative protection layer **34**a is formed on the core board **30** and the first circuit layer **31**a', and the first insulative protection layer **34**a has first openings **340**a formed so as to expose a part of the surface of the first circuit layer **31**a' as electrical connecting pads for electrically connecting a semiconductor chip. A second insulative protection layer **34**b is formed on the core board **30**, the second circuit layer **31**b' and the metal pads **310**b', and the second insulative protection layer **34**b has second openings **340**b formed for exposing a part of the surface of the metal flanges **33'**, wherein size of the second openings **340**b is smaller than outer diameter of the metal flanges **33'** such that solder mask defined (SMD) pads **37**a can be formed, as shown in FIG. **4**G. Alternatively, as shown in FIG. **4**G', size of the second openings **340**b' is bigger than that of the metal pads **310**b' such that the metal pads **310**b' and the metal flanges **33'** can be exposed to form non solder mask defined (NSMD) pads **37**b. The metal flanges **33'** can have a shape of circle, ellipse, rectangle or irregular shape. The metal pads **310**b' can have a shape of circle, ellipse, rectangle or irregular shape. Outer diameter of the metal flanges **33'** is not bigger than that of the metal pads **310**b'.

Referring to FIGS. **5**A to **5**C, a surface treatment layer **35** is further formed on the SMD pads **37**a. The surface treatment layer **35** may be one of an OSP layer, a Ni/Au layer, a Ni/Pd/Au layer and a Sn/Pb layer. Alternatively, the surface treatment layer **35** may be made of one of the group of consisting of Au, Ag, Sn and Cu. As shown in FIG. **5**B, conductive elements **36** of solder balls are further formed on the surface treatment layer **35**. Alternatively, as shown in FIG. **5**C, conductive elements **36** of solder balls are formed on the SMD pads **37**a.

Referring to FIGS. **6**A to **6**C, a surface treatment layer **35** is formed on the NSMD pads **37**b. The surface treatment layer **35** may be one of an OSP layer, a Ni/Au layer, a Ni/Pd/Au layer and a Sn/Pb layer. Alternatively, the surface treatment layer **35** may be made of one of the group of consisting of Au, Ag, Sn and Cu. As shown in FIG. **6**B, conductive elements **36** of solder balls are further formed on the surface treatment layer **35**. Alternatively, as shown in FIG. **6**C, conductive elements **36** of solder balls are formed on the NSMD pads **37**b.

According to the present invention, metal flanges are formed on the metal pads of the solder ball disposing surface of a package substrate, thereby increasing the contact area of the metal pads. In addition, the bonding area for conductive elements on electrical connecting pads can further be increased by adjusting type of openings in the insulative protection layer. Moreover, since no conductive layer is formed between the metal pads and the metal flanges as in the prior art, the bonding strength between the metal pads and the metal flanges is improved, thereby preventing detaching of the conductive elements subsequently formed on the metal pads and the metal flanges.

The above-described descriptions of the detailed embodiments are only to illustrate the preferred implementation according to the present invention, and it is not to limit the scope of the present invention, Accordingly, all modifications and variations completed by those with ordinary skill in the art should fall within the scope of present invention defined by the appended claims.

What is claimed is:

1. A manufacturing method of a solder ball disposing surface structure of a package substrate comprising:

providing a core board with a first metal layer and a second metal layer respectively formed on two opposite surfaces thereof;

forming metal bumps on the second metal layer by electroplating;

forming a third resist layer on the first metal layer and forming third openings in the third resist layer for exposing a part of the surface of a first metal layer, and forming

a fourth resist layer on the second metal layer and the metal bumps and forming fourth openings in the fourth resist layer for exposing a part of a surface of the second metal layer and forming fifth openings in the fourth resist layer for exposing a part of surfaces of the metal bumps;

removing the first and second metal layers in the third and fourth openings of the third and fourth resist layers so as to respectively form a first circuit layer, a second circuit layer and metal pads on the surfaces of the first and second metal layers of the core board, and removing the metal bumps in the fifth openings so as to form metal flanges disposed around the metal pads;

removing the third and fourth resist layers;

forming a first insulative protection layer on the core board and the first circuit layer and forming first openings in the first insulative protection layer for exposing a part of a surface of the first circuit layer as electrical connecting pads; and

forming a second insulative protection layer on the core board, the second circuit layer and the metal pads, and forming second openings in the second insulative protection layer so as to expose a part of surfaces of the metal flanges.

2. The manufacturing method of claim **1**, wherein size of the second openings is not bigger than outer diameter of the metal flanges.

3. The manufacturing method of claim **1**, wherein size of the second openings is bigger than outer diameter of the metal pads.

4. The manufacturing method of claim **1**, wherein the core board is one of a two-layer or multi-layer circuit board with a dielectric layer on surface thereof and an insulating board.

5. The manufacturing method of claim **1**, wherein outer diameter of the metal flanges is not bigger than that of the metal pads.

6. The manufacturing method of claim **1**, wherein the manufacturing method of forming the metal bumps on the second metal layer by electroplating comprises:

forming a first resist layer and a second resist layer on the first metal layer and the second metal layer respectively, the second resist layer having openings for exposing a part of the surface of the second metal layer;

forming metal bumps on the second metal layer in the second openings of the second resist layer by electroplating; and

removing the first and second resist layers so as to expose the first metal layer, the second metal layer and the metal bumps.

7. The manufacturing method of claim **1**, wherein the metal bumps in the fifth openings are partly removed so as to form a metal layer on the metal pads.

8. The manufacturing method of claim **7**, further comprising forming a surface treatment layer on the metal flanges and the metal layer.

9. The manufacturing method of claim **8**, further comprising forming conductive elements of solder balls on the surface treatment layer.

10. The manufacturing method of claim **7**, further comprising forming conductive elements of solder balls on the metal flanges and the metal layer.

11. The manufacturing method of claim **1**, wherein the metal bumps in the fifth openings are thoroughly removed so as to expose a part of the surface of the metal pads.

12. The manufacturing method of claim **11**, further comprising forming a surface treatment layer on the metal flanges and the metal pads.

13. A manufacturing method of a solder ball disposing surface structure of a package substrate comprising:

providing a core board;

forming a conductive layer on two opposite surfaces of the core board;

respectively forming a first resist layer and a second resist layer on the conductive layer on the two opposite surfaces of the core board, the first and second resist layers respectively having first openings and second openings for exposing a part of a surface of the conductive layer;

respectively forming a first circuit layer and a second circuit layer in the first and second openings of the first and second resist layers by electroplating, wherein the second circuit layer has metal pads;

forming a third resist layer on the first resist layer and the first circuit layer, and forming a fourth resist layer on the second resist layer and the second circuit layer, the fourth resist layer having ring-shaped openings for exposing a part of surfaces of the metal pads;

forming metal flanges on the metal pads by using the conductive layer as a current conductive path for electroplating;

removing the third resist layer, the first resist layer and the conductive layer covered by the first resist layer, the fourth resist layer, the second resist layer, and the conductive layer covered by the second resist layer, thereby exposing the first circuit layer, the second circuit layer and the metal flanges on the metal pads;

forming a first insulative protection layer on the core board and the first circuit layer and forming first openings in the first insulative protection layer for exposing a part of a surface of the first circuit layer as electrical connecting pads; and

forming a second insulative protection layer on the core board, the second circuit layer and the metal pads, and forming second openings in the second insulative protection layer so as to expose a part of surfaces of the metal flanges.

14. The manufacturing method of claim **13**, wherein a size of each of the second openings is not greater than an outer diameter of each of the metal flanges.

15. The manufacturing method of claim **13**, wherein a size of each of the second openings is greater than an outer diameter of each of the metal pads.

16. The manufacturing method of claim **13**, wherein the core board is one of a two-layer or multi-layer circuit board with a dielectric layer on surface thereof, a copper clad laminate board and an insulating board.

17. The manufacturing method of claim **13**, wherein an outer diameter of each of the metal flanges is not greater than that of each of the metal pads.

18. The manufacturing method of claim **13**, further comprising forming a surface treatment layer on the metal flanges and the metal pads.

19. The manufacturing method of claim **18**, further comprising forming conductive elements of solder balls on the surface treatment layer.

20. The manufacturing method of claim **13**, further comprising forming conductive elements of solder balls on the metal flanges and the metal pads.

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