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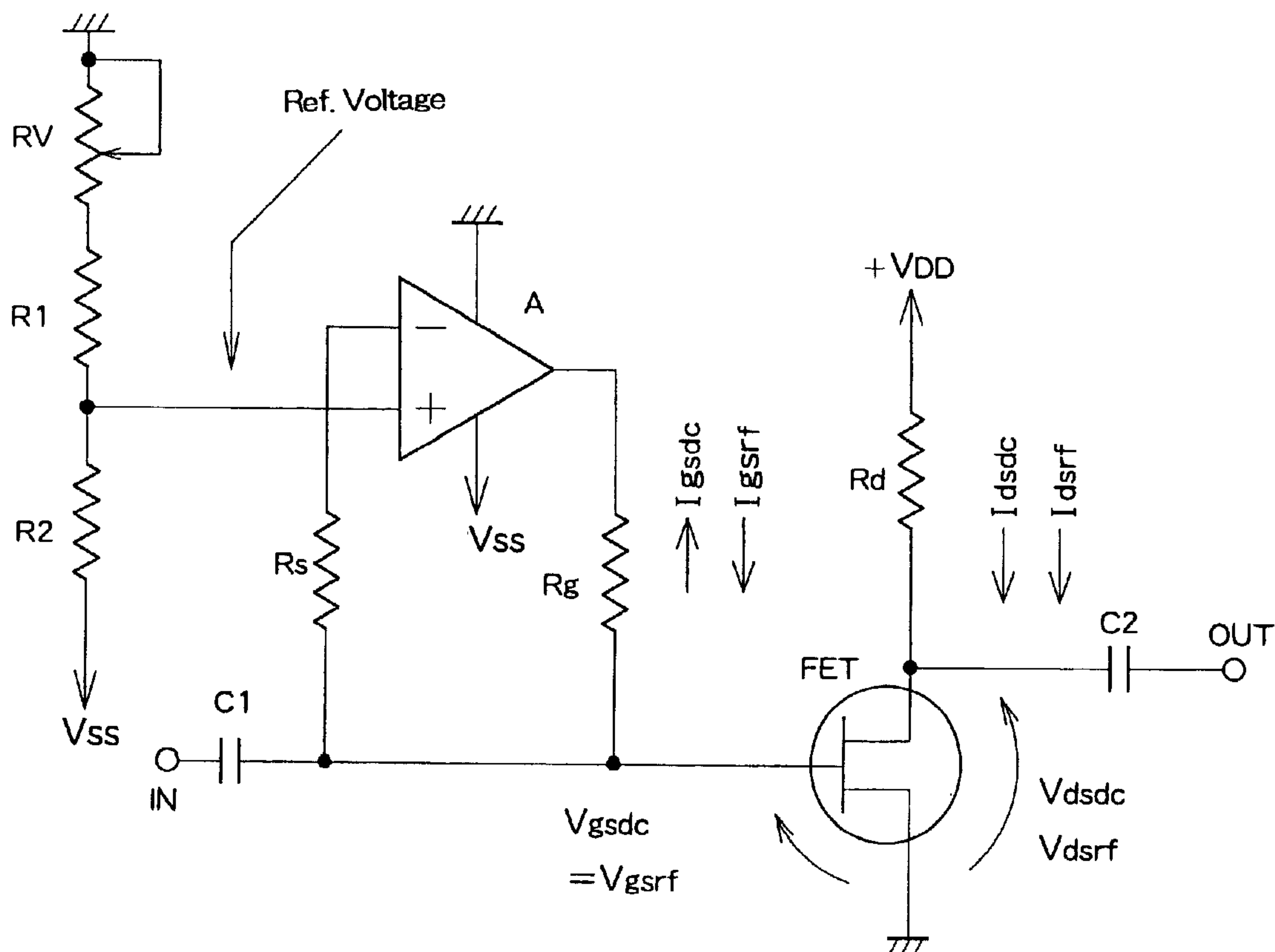
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(54) Titre : CIRCUIT DE POLARISATION DE TEF

(54) Title: FET BIAS CIRCUIT



(57) Abrégé/Abstract:

A circuit for biasing a Field Effect Transistor (FET) is provided. The FET has a gate, a drain, and a source and the circuit comprises a current limiting resistor having a first end and a second end, the first end being connected to the gate; and a closed-loop control circuit connected to the second end, applying and controlling DC voltage to the second end, so that a gate bias voltage that is applied to the gate becomes equal to a reference voltage of a predetermined DC voltage.



## ABSTRACT OF THE DISCLOSURE

A circuit for biasing a Field Effect Transistor (FET) is provided. The FET has a gate, a drain, and a source and the circuit comprises a current limiting resistor having a first end and a second end, the first end being connected to the gate; and a closed-loop control circuit connected to the second end, applying and controlling DC voltage to the second end, so that a gate bias voltage that is applied to the gate becomes equal to a reference voltage of a predetermined DC voltage.

## FET BIAS CIRCUIT

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

5       The present invention relates to a circuit for biasing a field effect transistor (FET).

#### 2. Description of the Related Art

Circuits employing FETs, such as amplifiers, are used in  
10 radio frequency (RF) circuits for radio communications equipment. Fig. 3 shows an example of an RF amplifier using an FET. The FET in the figure is, for example, a GaAs FET. This FET amplifies an input signal that is supplied to the gate from an input terminal IN via a capacitor C1 and supplies an  
15 amplified signal from the drain to an output terminal OUT via a capacitor C2. The drain of the FET is connected to a positive power supply (+VDD) via a resistor Rd, the source is connected to ground, and the gate is connected to a negative power supply (-VSS) via a resistor Rg2.

20       Furthermore, a circuit for biasing the FET in Fig. 3 is a regulated-current bias circuit that constantly maintains a drain bias current Idsdc at a fixed level and comprises a bipolar transistor Tr1, resistors Rb1, Rb2, Rg1, Rg2, and Rd, and a diode D1. One end of resistor Rb1 is connected to the  
25 positive power supply (+VDD) and the other end is connected to the anode of diode D1. One end of resistor Rb2 is connected to the cathode of diode D1 and to the base of transistor Tr1, and the other end is connected to ground. Therefore, the series

circuit formed from resistors Rb1 and Rb2 and diode D1 is a  
dividing circuit for dividing the supply voltage VDD to  
generate voltage Vb and applying it to the base of transistor  
Tr1. The series circuit is also a temperature compensation  
5 circuit for compensating through diode D1 a temperature  
dependency appearing in the base-emitter voltage of transistor  
Tr1 and in turn the emitter current. In relation to this  
compensation operation, it should be noted that the collector  
of transistor Tr1 is connected to the gate of the FET via  
10 resistor Rg1, and the emitter is connected to the drain of the  
FET. Since transistor Tr1 is provided in this sort of  
configuration, the drain bias current Idsdc of the FET is held  
at a fixed value of  $Idsdc = (VDD - Vb - Vbe) / Rd$  mainly due to the  
action of the diode D1 even if a change occurs in the emitter  
15 voltage of transistor Tr1 due to a change in temperature.  
Furthermore, since the gate impedance of the FET, which is  
ideally infinite, is actually a finite value, a minute current  
flows to the gate of the FET. This gate current Igsdc is  
limited by resistors Rg1 and Rg2, which are connected to the  
20 gate of the FET, so that the long-term reliability of the FET  
is maintained. Furthermore, since resistor Rg1 is provided,  
the impedance when viewing the transistor Tr1 from the FET is  
that much higher and the radio frequency amplification  
characteristics become more stable.

25        Regarding the regulation of the drain bias current Idsdc  
as a constant current, refer to Japanese Laid-Open Patent  
Publication No. JP 7-321561. Regarding temperature  
compensation by the diode D1, refer to Japanese Laid-Open

Patent Publication No. JP-5-175747. Furthermore, the gate bias voltage, gate current, drain bias voltage, and drain bias current are respectively denoted in the figure by  $V_{gsdc}$ ,  $I_{gsdc}$ ,  $V_{dsdc}$ , and  $I_{dsdc}$  during no signal input and  $V_{gsrf}$ ,  $I_{gsrf}$ ,  $V_{dsrf}$ , and  $I_{dsrf}$  during signal amplification (when the output signal level is high). In the description hereinafter,  $V_{gsdc}$ ,  $I_{gsdc}$ ,  $V_{dsdc}$ , and  $I_{dsdc}$  are used for the symbols or variable names, unless whenever a distinction is required.

In the circuit shown in Fig. 3, the emitter current of transistor  $Tr1$  is supplied via resistor  $R_d$ . Thus, the power dissipation at resistor  $R_d$  is large compared to the circuit of Fig. 4 to be described hereinafter. Furthermore, since the drain bias current  $I_{dsdc}$  is regulated as a constant current, the circuit of Fig. 3 cannot be used in a class AB or class B amplification mode in which the drain current varies according to the input signal level. Namely, the circuit of Fig. 3 can only be used for class A amplification. Thus, it is difficult to achieve large power amplification at a high efficiency.

A regulated voltage bias circuit that does not have this type of problem is shown in Fig. 4. In the circuit shown in this figure, the output voltage of the constant voltage source  $V_1$  that is implemented from a resistance-type dividing circuit, a voltage regulator, an operational amplifier, and so forth, is applied to the gate of the FET via the resistor  $R_g$ . Since the circuit at the gate side of the FET is completely separate from the circuit at the drain side in the figure, the drain bias current  $I_{dsdc}$  can be more freely set unlike the circuit of Fig. 3. Therefore, the FET can be made to function in a class A,

class AB, or class B configuration. Namely, by configuring the constant voltage source  $V_1$  so that the output voltage can be adjusted and by adjusting the output voltage of the constant voltage source  $V_1$  to an appropriate value, the gate bias voltage  $V_{gsdc}$  can be set to a target value, and in turn the drain bias current  $I_{dsdc}$  can be set to an appropriate value. Thus, the circuit shown in Fig. 4 can be used in various applications from small signal amplification in class A operation to large signal amplification in class AB or class B operation. Furthermore, the gate bias voltage  $V_{gsdc}$  is applied from the constant voltage source  $V_1$  via resistor  $R_g$ . Thus, the gate bias current  $I_{dsdc}$  is limited by resistor  $R_g$  so that the long-term reliability of the FET can be maintained. For the same reason, the impedance is high, when the constant voltage source  $V_1$  is viewed from the FET, to further stabilize the RF amplification characteristics.

However, the above-mentioned conventional circuit has several problems.

First, a compensation circuit having a complex configuration becomes necessary when implementing the circuit shown in Fig. 4. Here, the compensation circuit refers to a circuit for compensating for variations in the gate current  $I_g$  accompanying changes in the input signal level, temperature, and so forth. When the gate current  $I_{gsdc}$  varies, the gate bias voltage  $V_{gsdc}$  and further the drain bias current  $I_{dsdc}$  also varies as a result. More specifically, the amount of change  $\Delta I_{dsdc}$  in the drain bias current  $I_{dsdc}$  can be expressed in the following equation:

$$\begin{aligned}\Delta I_{dsdc} &= (\Delta V_{gsdc1} + \Delta V_{gsdc2}) * (g_m + \Delta g_m) \\ &= (\Delta I_{gsdc1} + \Delta I_{gsdc2}) * (g_m + \Delta g_m) * R_g\end{aligned}$$

In this equation,  $\Delta V_{gsdc1}$  and  $\Delta I_{gsdc1}$  are respectively the amount of change in the gate bias voltage  $V_{gsdc}$  and in the gate current  $I_{gsdc}$  accompanying the change in input signal level,  $\Delta V_{gsdc2}$  and  $\Delta I_{gsdc2}$  are respectively the amount of change in the gate bias voltage  $V_{gsdc}$  and in the gate current  $I_{gsdc}$  accompanying the change in temperature,  $g_m$  is the mutual conductance of the FET, and  $\Delta g_m$  is the amount of change in  $g_m$  accompanying the change in temperature.

Generally,  $\Delta I_{dsdc}$  appearing in the equation is a quadratic function of temperature and  $\Delta g_m$  is a linear function. Thus, with no temperature compensation, the temperature characteristic of the drain bias current  $I_{dsdc}$  approximates the quadratic function characteristic, for example, as shown by the broken line in Fig. 5. Obviously, so as to preferably compensate for this temperature characteristic, a temperature compensation circuit having a quadratic function characteristic is necessary. A temperature compensation circuit having such a characteristic generally has a complex configuration, and the use of such a temperature compensation circuit in configuring an RF amplifier results in an increase in circuit size and in the cost of the amplifier. However, if a temperature compensation circuit having a linear function characteristic is used thereby avoiding a complex circuit configuration, the temperature dependency is not well compensated and persists in the characteristic after temperature compensation, as shown by the solid line in Fig. 5.

During no signal input, the gate bias voltage  $V_{gsdc}$  becomes higher than the output voltage of the constant voltage source  $V_1$  due to the voltage drop at resistor  $R_g$ . Furthermore, when the gate current  $I_{gsdc}$  increases due to a rise in

5 temperature, the voltage drop at resistor  $R_g$  increases. When the voltage drop at resistor  $R_g$  increases, the gate bias voltage  $V_{gsdc}$  rises further. When the gate bias voltage  $V_{gsdc}$  increases, the drain bias current  $I_{dsdc}$  increases. This increase, namely, the increase accompanying the rise in

10 temperature, is denoted by  $\Delta I_{gsdc2}$  in the equation given above, and is a quadratic functional increase. If temperature compensation is not performed or is insufficiently performed, the FET may also become susceptible to thermal runaway caused by the increase  $\Delta I_{gsdc2}$  accompanying the rise in temperature.

15 Furthermore, when a GaAs FET is used, during large signal amplification, the direction of flow of the gate current  $I_{gsdc}$  reverses as shown in Fig. 4. ( $I_{gsrf}$  is a reverse flow.) When the gate current  $I_{gsrf}$  flows from the constant voltage source  $V_1$  to the gate, the gate potential of the FET drops

20 (considerably toward the negative direction) due to the voltage drop at resistor  $R_g$ . As a result, the drain bias current  $I_{dsrf}$  drops, and thus the signal saturation output power of the FET drops during large signal amplification.

The various above-mentioned problems occur due to a

25 combination of the mutual conductance and gate current of the FET depending on the temperature and input signal level, and the resistor  $R_g$  being used. In particular, when resistor  $R_g$  is set to a large value, the change in the gate current  $I_{gsdc}$  and

in turn the change in the drain bias current  $I_{dsdc}$  increase  
accompanying the change in temperature or the change in the  
input signal level. However, it is not preferable to obviate  
resistor  $R_g$  or reduce its value. If resistor  $R_g$  is obviated or  
5 if the value of resistor  $R_g$  is too low, long-term reliability  
cannot be maintained, depending on the type of FET.  
Furthermore, if the value of resistor  $R_g$  is too small, the RF  
operation becomes unstable, depending on the type of FET.

#### 10 SUMMARY OF THE INVENTION

It is therefore an object of the present invention to  
provide an FET bias circuit as a preferable and simple circuit  
capable of operating the FET in class A, class AB, and class B  
configurations and capable of compensating and suppressing  
15 changes in the gate current  $I_{gsdc}$  due to changes in temperature  
or in the level of the input signal to the FET.

In order to achieve this object, the circuit at the gate  
of the FET and the circuit at the drain are separated in the  
present invention so as to be compatible with all of class A,  
20 class AB, and class B, and closed-loop control is performed for  
the gate bias voltage of the FET so that the amount of change  
in the input signal level or in temperature can be easily  
compensated. Namely, the FET bias circuit relating to the  
present invention comprises the current limiting resistor  $R_g$ ,  
25 which has a first end and a second end, and the closed-loop  
control circuit coupled to the current limiting resistor  $R_g$ .  
In the present invention, the first end of the current limiting  
resistor  $R_g$  is connected to the gate of the FET. The closed-

loop control circuit applies and controls DC voltage to the second end of the current limiting resistor  $R_g$ , so that the gate bias voltage  $V_{gsdc}$  of the FET, namely, the voltage appearing at the first end of the current limiting resistor  $R_g$ ,  
5 becomes equal to the reference voltage of a predetermined DC voltage.

According to the present invention, unlike the constant current bias circuit shown in Fig. 3, the circuit at the gate and the circuit at the drain are separate so as to yield an FET  
10 bias circuit that is capable of stable operation in classes where the drain current changes in accordance with the signal input level, and suitable for a wide range of applications from small signal amplification in class A to large signal amplification in class AB or class B. Furthermore, closed-loop  
15 control is performed for the gate bias voltage  $V_{gsdc}$  so that changes in the gate bias voltage  $V_{gsdc}$  and in turn changes in the operating point of the FET (drain bias current  $I_{dsdc}$ ), accompanying changes in the input signal level or temperature, can be limited and suppressed.

20 Furthermore, with the voltage drop at the current limiting resistor  $R_g$  being one cause, a phenomenon where stability of the RF (amplification) characteristic deteriorates or a phenomenon where the saturation output voltage drops when the input signal level is high occurred in the conventional  
25 circuit shown in Fig. 4. In the present invention by comparison, movement of the FET operating point due to variations in the gate current  $I_{gsdc}$  is suppressed by the closed-loop control of the gate bias voltage  $V_{gsdc}$ . Thus, when

designing the circuit constants, the voltage drop at the  
current limiting resistor  $R_g$  can be ignored and the value of  
the current limiting resistor  $R_g$  can be selected and designed  
with priority given to the stability of the RF characteristic,  
5 and the drop in the saturation output voltage described above  
does not occur.

Furthermore, the closed-loop control circuit in the  
present invention can be implemented with a simple circuit  
configuration using an error amplifier. For example, the  
10 reference voltage generation circuit for generating the above-  
mentioned reference voltage can be configured as a dividing  
circuit that can be obtained by connecting a plurality of  
resistors in series. The reference voltage generation circuit  
in this case generates the reference voltage by dividing a DC  
15 voltage of a predetermined value, such as the supply voltage.  
Furthermore, this reference voltage and the gate bias voltage  
of the FET are input by the error amplifier, and a voltage  
equivalent to their difference is applied to the gate of the  
FET via the current limiting resistor  $R_g$ . In this manner, the  
20 FET bias circuit relating to the present invention can be  
implemented using only resistors and an error amplifier, which  
may be configured from an operational amplifier. It should be  
noted that the reference voltage can also be generated by a  
method other than voltage division and the closed-loop control  
25 can be performed using components other than an operational  
amplifier.

Although the change in the drain bias current  $I_{dsdc}$  due  
to the change in the mutual conductance  $g_m$  persists, it is a

linear characteristic with respect to temperature. Thus, in many cases, the FET is prevented from its thermal runaway without temperature compensation. If temperature compensation is to be performed to secure further improved stability, a circuit for such a purpose can easily be configured as a simple, small, and inexpensive circuit having linear function characteristics. In particular, if the closed-loop control circuit is to be configured from the operational amplifier and reference voltage generation circuit as described above, the change in the drain bias current  $I_{dsdc}$  due to the change in the mutual conductance  $g_m$  can be compensated by only setting and selecting the temperature characteristics of the reference voltage generation circuit. For example, in the reference voltage generation circuit which is preferably implemented with a dividing circuit, as at least one of the resistors connected in series, an element, such as a temperature sensitive element, having a complementary temperature characteristics with respect to the temperature characteristics of the mutual conductance of the FET is used, to cancel the temperature characteristics occurring in the drain current of the FET caused by the temperature characteristics of the mutual conductance of the FET.

According to an aspect of the invention, a circuit for biasing a Field Effect Transistor (FET) is provided. The FET has a gate, a drain, and a source and the circuit comprises a current limiting resistor having a first end and a second end, the first end being connected to the gate; and a closed-loop control circuit connected to the second end, applying and controlling DC voltage to the second end, so that a gate bias voltage that is applied to the gate becomes equal to a reference voltage of a predetermined DC voltage.

A circuit for biasing a Field Effect Transistor (FET) is provided. The FET has a gate, a drain, and a source and the circuit comprises a current limiting resistor having a first end and a second end, the first end being connected to the gate; and a closed-loop control circuit connected to the second end, applying and controlling DC voltage to the second end, so that a gate bias voltage that is applied to the gate becomes equal to a reference voltage of a predetermined DC voltage.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a configuration of a radio-frequency amplifier that uses a FET bias circuit relating to an embodiment of the present invention.

Fig. 2 shows a temperature compensation operation in the embodiment.

Fig. 3 is a circuit diagram showing a configuration of a circuit relating to the prior art.

5 Fig. 4 is a circuit diagram showing a configuration of a circuit relating to another prior art.

Fig. 5 shows a temperature compensation operation in the prior art shown in Fig. 4.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described hereinafter with reference to the drawings. An identical component with that in the conventional circuits shown in Figs. 3 and 4 is given an identical reference numeral  
15 and its description is omitted.

Fig. 1 shows an example configuration of an RF amplifier that uses the FET bias circuit relating to an embodiment of the present invention. The circuit shown in this figure is characterized by the circuit at the gate and the circuit at the  
20 drain of the FET being separated each other, a closed-loop control circuit coupled to the gate resistor  $R_g$  being provided, the closed-loop control circuit being configured using an operational amplifier A, and so forth.

A reference voltage is applied to the non-inverted input  
25 terminal of the operational amplifier A and the gate bias voltage  $V_{gsdc}$  of the FET is applied to the inverted input terminal. The output of the operational amplifier A that is generated in accordance with these applied voltages is applied

to the gate of the FET via resistor  $R_g$ . The reference voltage that is input by the operational amplifier A is generated by the reference voltage generation circuit comprising resistors  $R_v$ ,  $R_1$ , and  $R_2$ . More specifically, the supply voltage from the negative power supply ( $-V_{SS}$ ) is divided by these resistors so as to generate the reference voltage at the point connecting the resistors  $R_1$  and  $R_2$ .  $R_v$  is a variable resistor and the adjustment of its resistance enables the reference voltage to be adjusted.

The operational amplifier A operates as a voltage follower. Namely, the voltage that is applied to the inverted input terminal becomes equal to the reference voltage that is applied to the non-inverted input terminal of the operational amplifier A. Described in more detail, the gate current  $I_{gsdc}$  that flows out of the FET, flows into the output terminal of the operational amplifier A via resistor  $R_g$ , and conversely, the gate current  $I_{gsrf}$  that flows into the FET is discharged from the operational amplifier A via resistor  $R_g$ . In any of these cases, a voltage drop develops at the current limiting resistor  $R_g$ . In the present embodiment, since the operational amplifier A controls the gate bias voltage  $V_{gsdc}$  of the FET so as to become equal to the reference voltage, the gate bias voltage  $V_{gsdc}$  is kept constant, independently of the voltage drop.

In this manner, in the present embodiment in which the closed-loop control of the gate bias voltage  $V_{gsdc}$  of the FET is performed, the circuit at the gate of the FET and the circuit at the drain are separate so that, unlike the prior art

shown in Fig. 3, the FET can be operated in any of a class A, class AB, or class B configuration. Furthermore, the change in the gate bias voltage  $V_{gsdc}$  that occurs when the input signal level or the temperature changes can be suppressed by the closed-loop control of the gate bias voltage  $V_{gsdc}$ . Thus, even when the input signal level or the temperature changes, the FET can be operated at a constant gate bias voltage  $V_{gsdc}$ , variations in the drain current  $I_{dsdc}$ , such as due to the input signal level, are prevented, and the movement of the FET operating point can be eliminated.

Furthermore, since the voltage drop at the resistor  $R_g$  can be ignored, the value of resistor  $R_g$  can be selected and designed with priority given to the stability of the RF characteristics, and a drop in the saturation output power that occurred in the circuit shown in Fig. 4 can be prevented.

Furthermore, as described earlier, the mutual conductance  $g_m$  of the FET has a linear temperature characteristic. Therefore, in the case where temperature compensation is not applied to the temperature characteristics, the drain bias current  $I_{dsdc}$  provides linear temperature characteristics as shown by the broken line in Fig. 2. This sort of linear temperature characteristics enables preferable compensation to be achieved with a circuit having a simple configuration.

Using the circuit of the present embodiment as an example, at least one of either resistor  $R_1$  or  $R_2$  forming the reference voltage generation circuit is a temperature sensitive element, and the temperature characteristic of the mutual conductance  $g_m$  of the FET is at least approximately compensated

by the temperature characteristic of the temperature sensitive element. As a result, the characteristic shown by the solid line in Fig. 2, namely, a characteristic having almost no change in the drain bias current  $I_{dsdc}$  with respect to  
5 temperature, can be achieved. Further, the temperature characteristics shown by the broken line in Fig. 2 is a linear characteristic rising toward the right. Thus, in order to achieve the characteristic shown by the solid line, either a temperature sensitive element having a positive temperature  
10 coefficient is used for resistor R1, a temperature sensitive element having a negative temperature coefficient is used for resistor R2, or both are used.

Furthermore, since the temperature characteristic of the drain bias current  $I_{dsdc}$  has a linear characteristic as  
15 described above, thermal runaway of the FET or the resultant damage can be preferably prevented.

Additionally, the present invention can be implemented in a form other than the circuit shown in Fig. 1. First, depending on the FET, a positive power supply is used instead  
20 of the -VSS. Furthermore, although a GaAs FET may be given as the type of FET, the present invention is also applicable to other types of FETs. The operational amplifier A is an example of a comparator amplifier or an error amplifier, and the present invention can generally be implemented using a  
25 comparator amplifier or an error amplifier. In the present embodiment, although resistor  $R_s$  is inserted before the inverted input terminal of the operational amplifier A to suppress the input signal branched to the inverted input

terminal of the operational amplifier A, a coil, a capacitor, or other device may also be used in combination. Furthermore, the closed-loop control circuit for the gate bias voltage  $V_{gsdc}$  may be configured using components other than the resistance-type dividing circuit and the operational amplifier A. For example, a voltage regulator may be used instead of the reference voltage generation circuit that is based on resistance-type voltage dividing. In the case where the voltage regulator is used to generate the reference voltage, the output voltage of the voltage regulator must be set or controlled to decrease with the rise in temperature.

While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A circuit for biasing a field effect transistor (FET) having a gate, a drain, and a source, the circuit comprising:

a current limiting resistor having a first end and a second end, said first end being connected to said gate; and

a closed-loop control circuit connected to said second end, said control circuit controlling a DC voltage and applying said voltage to said second end, wherein said voltage sets a gate bias voltage applied to said gate, said closed loop control circuit having:

a reference voltage generation circuit that generates a reference voltage; and

an error amplifier that inputs the reference voltage and said gate bias voltage and applies a voltage equivalent to the difference of both inputs to said gate via said current limiting resistor.

2. The circuit according to claim 1 wherein: said reference voltage generation circuit has complementary temperature characteristics with respect to the temperature characteristics of mutual conductance of said FET so as to cancel the temperature characteristics occurring in drain current of said FET caused by temperature characteristics of mutual conductance of said FET.

3. A circuit for biasing a FET having a gate, a drain, and a source, the circuit comprising:

a gate resistor that is connected to the gate of the FET; and

a closed-loop control circuit coupled to said gate resistor, for controlling voltage applied to the gate of the

FET through the gate resistor, such that a predetermined voltage is maintained at the gate of the FET, wherein the closed-loop control unit comprises a reference voltage generation circuit that generates a reference voltage, and an error amplifier that inputs the reference voltage and a gate bias voltage and provides a voltage equivalent to the difference of both inputs to said gate via said gate resistor;

said reference voltage generation circuit having complementary temperature characteristics with respect to temperature characteristics of mutual conductance of said FET so as to cancel the temperature characteristics occurring in drain currents of said FET caused by said temperature characteristics of mutual conductance.

4. The according to claim 3 further comprising a second resistor coupled to said error amplifier by its inverting input port and said gate of said FET, such that said second resistor suppressing an input signal branched to said inverted input port of said error amplifier.

5. A circuit for temperature compensation, the circuit comprising:

a single FET having a gate, source, and drain;

a gate resistor that is connected to the gate of the FET; and

a closed-loop control circuit coupled to said gate resistor, for controlling voltage applied to the gate of the FET through the gate resistor, such that a predetermined voltage is maintained at the gate of the FET so as to cancel temperature characteristics occurring in said single FET, wherein the closed-loop control unit comprises a reference voltage generation circuit that generates a reference voltage, and an error amplifier that inputs the reference

voltage and a gate bias voltage and provides a voltage equivalent to the difference of both inputs to said gate via said gate resistor;

said reference voltage generation circuit having complementary temperature characteristics with respect to temperature characteristics of mutual conductance of said FET so as to cancel the temperature characteristics occurring in drain currents of said FET caused by said temperature characteristics of mutual conductance.

6. A circuit for temperature compensation, the circuit comprising:

a single FET having a gate, source, and drain;

a gate resistor that is connected to the gate of the FET;

a closed-loop control circuit coupled to said gate resistor, for controlling voltage applied to the gate of the FET through the gate resistor, such that a predetermined voltage is maintained at the gate of the FET so as to cancel temperature characteristics occurring in said single FET, wherein said closed-loop control circuit includes a reference voltage generation circuit that generates a reference voltage, and an error amplifier that inputs the reference voltage and a gate bias voltage and provides a voltage equivalent to the difference of both inputs to said gate via said gate resistor,

said reference voltage generation circuit having complementary temperature characteristics with respect to temperature characteristics of mutual conductance of said FET so as to cancel the temperature characteristics occurring in drain currents of said FET caused by said temperature characteristics of mutual conductance; and

a second resistor coupled to said error amplifier by its inverting input port and said gate of said FET, such

that said second resistor suppressing an input signal branched to said inverted input port of said error amplifier.

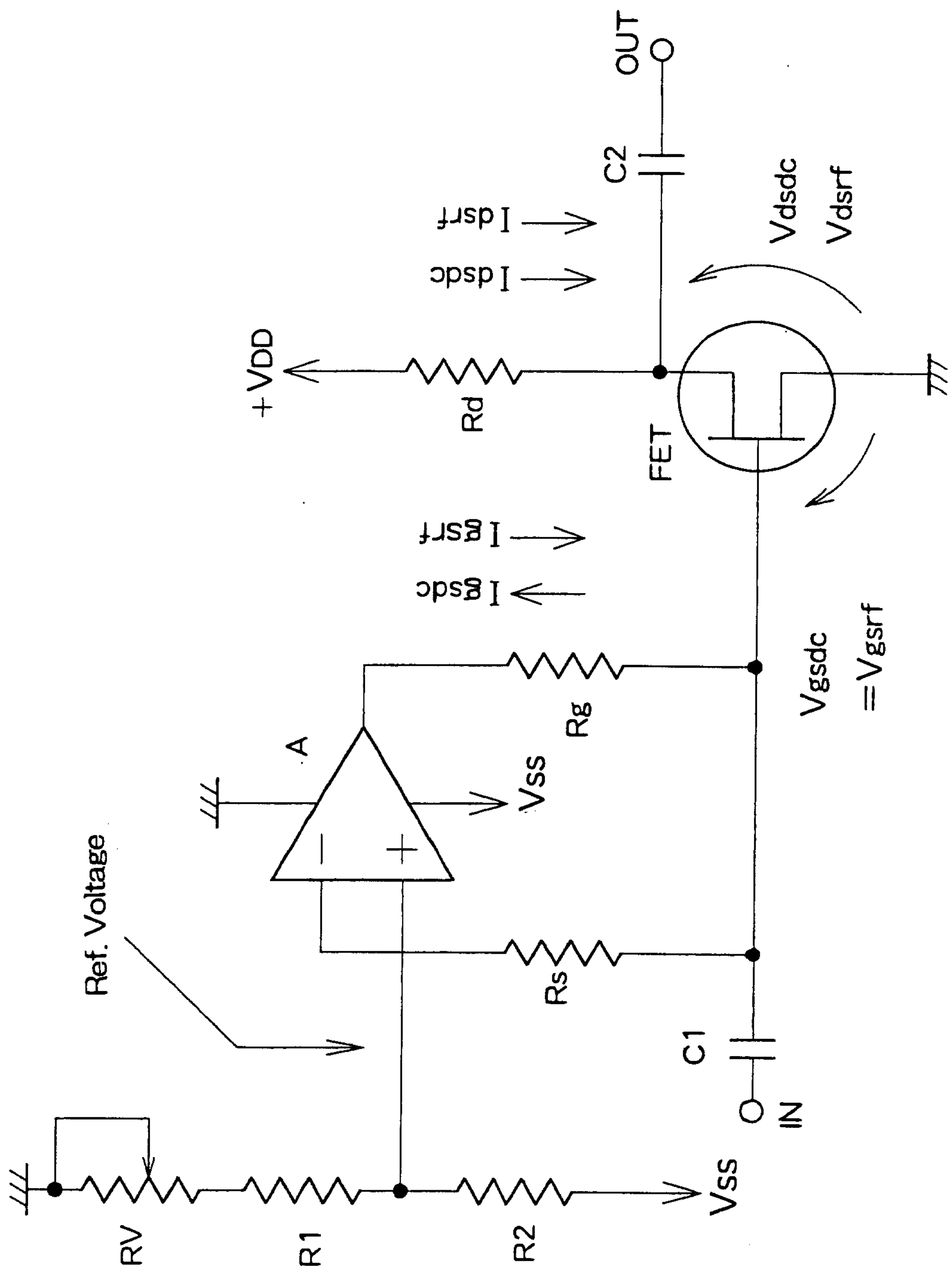


Fig. 1

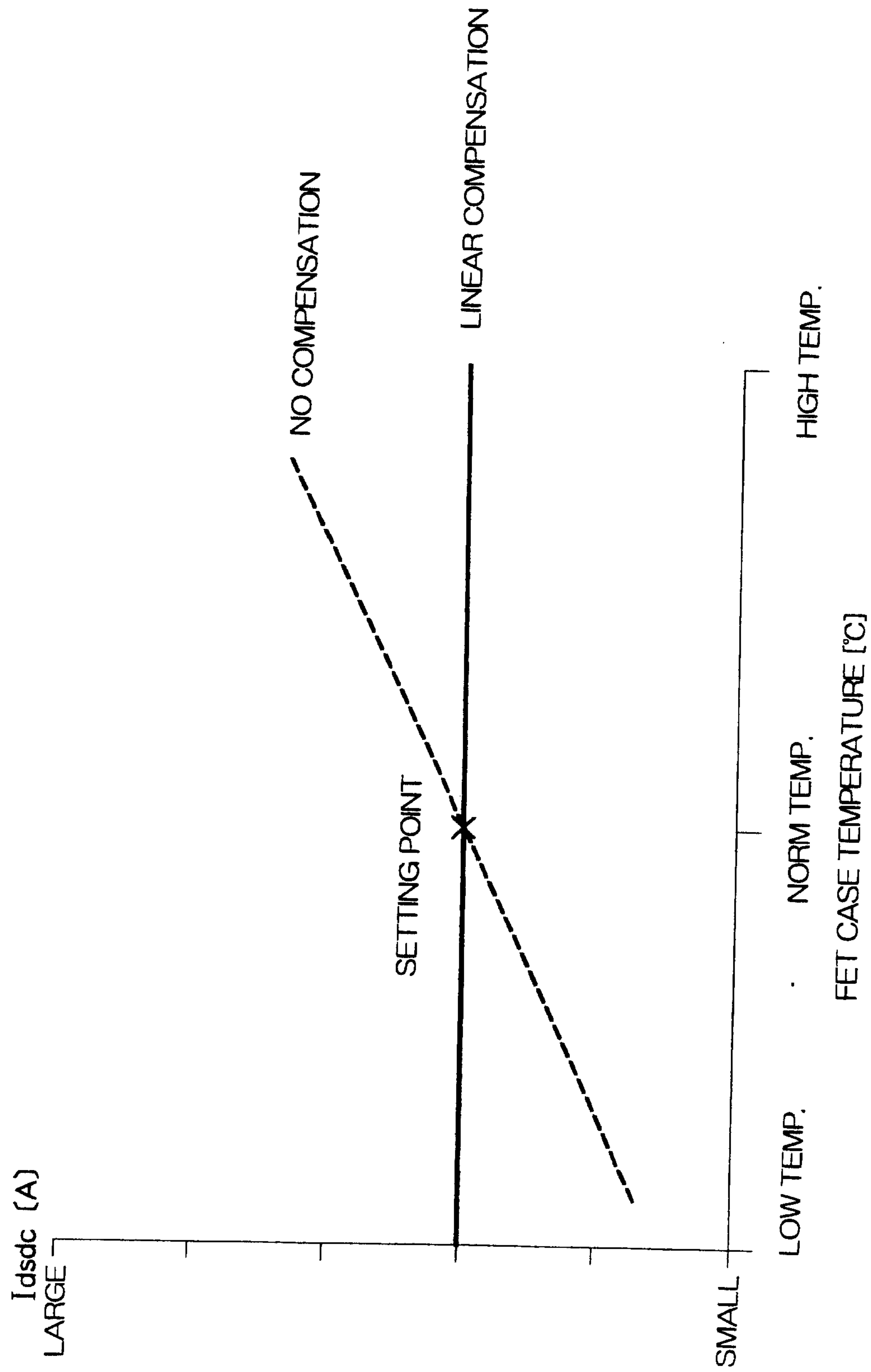
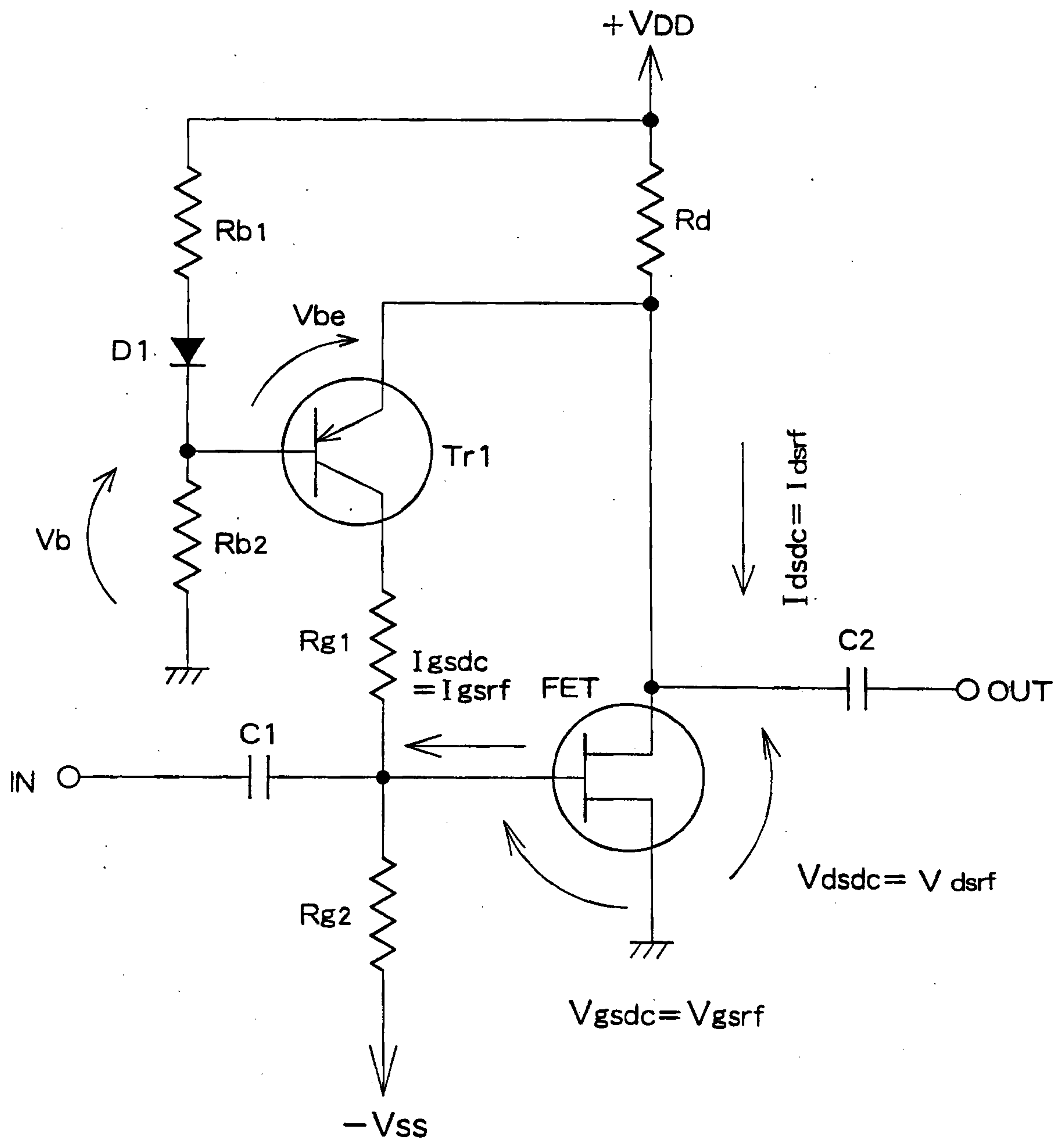


Fig. 2

**Fig. 3**

Prior Art

Gowling Lafleur Henderson LLP

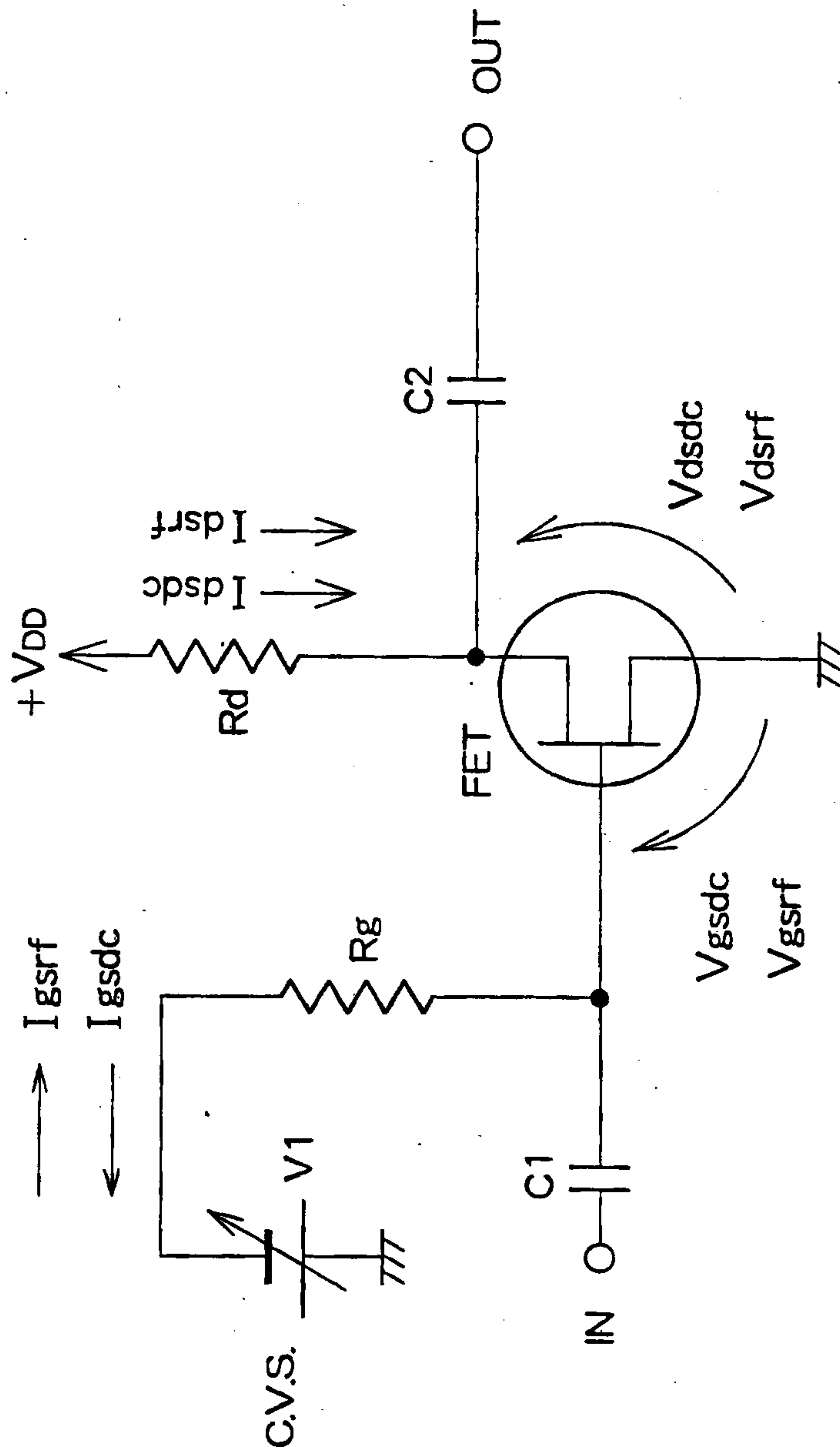


**Fig. 4** Prior Art

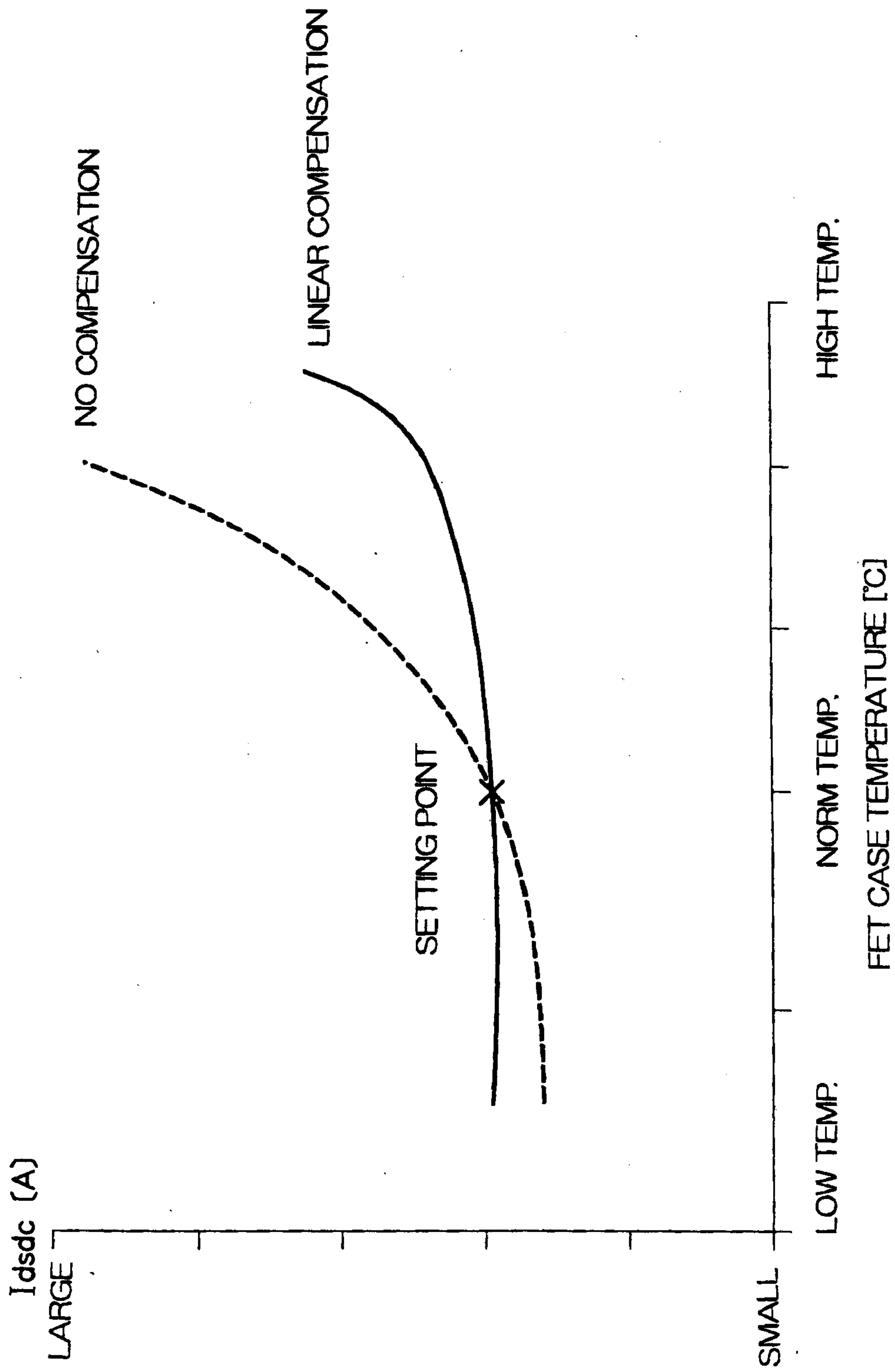


**Fig. 5** Prior Art

