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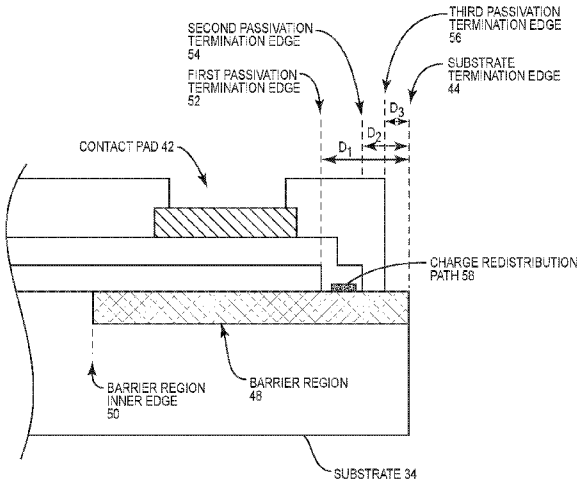

FIG. 8

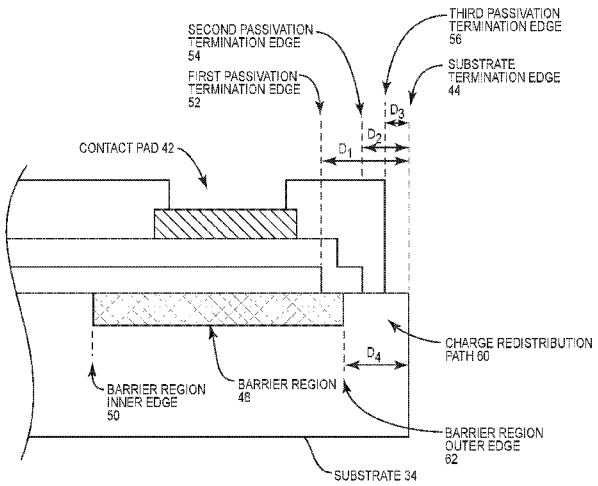

FIG. 12

(57) Abstract: A semiconductor die includes a substrate, a first passivation layer over the substrate, and a second passivation layer over the first passivation layer and the substrate. The substrate has boundaries defined by a substrate termination edge. The first passivation layer is over the substrate such that it terminates at a first passivation termination edge that is inset from the substrate termination edge by a first distance. The second passivation layer is over the first passivation layer and the substrate such that it terminates at a second passivation termination edge that is inset from the substrate termination edge by a second distance. The second distance is less than the first distance such that the second passivation layer overlaps the first passivation layer.

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SEMICONDUCTOR DIE WITH IMPROVED RUGGEDNESS

Field of the Disclosure

[0001] The present disclosure is related to semiconductor devices, and in particular to semiconductor devices with increased ruggedness and methods for making the same.

Background

[0002] Numerous semiconductor devices can be fabricated together on a semiconductor die. For purposes of illustration, Figure 1 shows a conventional semiconductor die 10. The conventional semiconductor die 10 includes a substrate 12, a first passivation layer 14 over the substrate 12, a second passivation layer 16 over the first passivation layer 14, a third passivation layer 18 over the second passivation layer 16, and a number of contact pads 20. The boundaries of the substrate 12 are defined by a substrate termination edge 22. The substrate 12 includes an active area 24 in which a number of semiconductor devices (not shown) may be provided, for example, by one or more implanted regions and one or more metallization layers, and a barrier region 26 around the active area 24. The barrier region 26 electrically isolates the active area 24 from the substrate termination edge 22 and thus the surrounding environment. The barrier region 26 is generally provided as an implant that reduces the conductivity of the substrate 12, but can also be an etched mesa or shallow trench isolation (STI). Normally, the barrier region 26 extends from an inside barrier region termination edge 28 to the substrate termination edge 22, forming a barrier around the perimeter of the conventional semiconductor die 10.

[0003] The first passivation layer 14 is provided over the active area 24 and extends over the barrier region 26 to a passivation termination edge 30. The second passivation layer 16 is over the first passivation layer 14 and similarly extends to the passivation termination edge 30. The third passivation layer 18 is over the second passivation layer 16 and similarly extends to the passivation termination edge 30. The contact pads 20 may be provided on the second

passivation layer 16 and be exposed to the outside environment via one or more openings in the third passivation layer 18. While not shown, metallization layers within the first passivation layer 14 and the second passivation layer 16 may couple the contact pads to one or more semiconductor devices in the active area 24. The passivation termination edge 30 is inset from the substrate termination edge 22 by a certain distance D.

[0004] The first passivation layer 14, the second passivation layer 16, and the third passivation layer 18 are provided to isolate the semiconductor devices in the active area 24 from the surrounding environment, both electrically and physically. However, when the conventional semiconductor die 10 is in a humid environment and subject to high temperatures and/or bias voltages, one or more of the first passivation layer 14, the second passivation layer 16, and the third passivation layer 18 may delaminate from their underlying layer, allowing moisture to penetrate into the active area 24. This may cause failure of the conventional semiconductor die 10. This problem is exacerbated by an electric field created by operating one or more semiconductor devices in the active area 24, which may be quite high at the passivation termination edge 30. This electric field may draw moisture from the passivation termination edge 30 towards the active area 24 and thus cause failure of the conventional semiconductor die 10 as discussed above.

[0005] In light of the above, there is a need for a semiconductor die with improved ruggedness and methods for manufacturing the same.

Summary

[0006] The present disclosure is related to semiconductor devices, and in particular to semiconductor devices with increased ruggedness and methods for making the same. In one embodiment, a semiconductor die includes a substrate, a first passivation layer over the substrate, and a second passivation layer over the first passivation layer and the substrate. The substrate has boundaries defined by a substrate termination edge. The first passivation layer is over the substrate such that it terminates at a first passivation termination edge that is

inset from the substrate termination edge by a first distance. The second passivation layer is over the first passivation layer and the substrate such that it terminates at a second passivation termination edge that is inset from the substrate termination edge by a second distance. The second distance is less than the first distance such that the second passivation layer overlaps the first passivation layer. By overlapping the second passivation layer and the first passivation layer, the ruggedness of the semiconductor die can be significantly increased, since moisture can be prevented from penetrating the first passivation layer and the second passivation layer.

[0007] In one embodiment, a method for manufacturing a semiconductor die includes the steps of providing a substrate, providing a first passivation layer over the substrate, and providing a second passivation layer over the first passivation layer. The substrate has boundaries defined by a substrate termination edge. The first passivation layer is over the substrate such that it terminates at a first passivation termination edge that is inset from the substrate termination edge by a first distance. The second passivation layer is provided over the first passivation layer and the substrate such that it terminates at a second passivation termination edge that is inset from the substrate termination edge by a second distance. The second distance is less than the first distance such that the second passivation layer overlaps the first passivation layer. By overlapping the second passivation layer and the first passivation layer, the ruggedness of the semiconductor die can be significantly increased, since moisture can be prevented from penetrating the first passivation layer and the second passivation layer.

[0008] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0009] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0010] Figure 1 illustrates a conventional semiconductor die.

[0011] Figures 2 through 13 illustrate semiconductor die according to various embodiments of the present disclosure.

[0012] Figure 14 is a flow chart describing a method for manufacturing a semiconductor die according to various embodiments of the present disclosure.

Detailed Description

[0013] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0014] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0015] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no

intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0016] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0017] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0018] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the

relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0019] Figure 2 shows a semiconductor die 32 according to one embodiment of the present disclosure. The semiconductor die 32 includes a substrate 34, a first passivation layer 36 over the substrate 34, a second passivation layer 38 over the first passivation layer 36 and the substrate 34, a third passivation layer 40 over the second passivation layer 38, and a number of contact pads 42. The boundaries of the substrate 34 are defined by a substrate termination edge 44. The substrate 34 includes an active area 46 in which a number of semiconductor devices (not shown) may be provided, for example, by one or more implanted regions and one or more metallization layers, and a barrier region 48 around the active area 46. The barrier region 48 electrically isolates the active area 46 from the substrate termination edge 44 and thus the surrounding environment. The barrier region 48 may be provided as an implanted region (e.g., a region of implanted nitrogen, hydrogen, helium, magnesium, zirconium, krypton, argon, and/or iron) that reduces the conductivity of the substrate 34, and may extend from a barrier region inner edge 50 to the substrate termination edge 44. The semiconductor devices may include any type of devices such as diodes, high electron mobility transistors (HEMTs), field-effect transistors (FETs), metal-oxide semiconductor field-effect transistors (MOSFETs), and the like.

[0020] The first passivation layer 36 is provided over the active area 46 and extends over the barrier region 48 to a first passivation termination edge 52. The second passivation layer 38 is over the first passivation layer 36 and the substrate 34 and extends to a second passivation termination edge 54. The third passivation layer 40 is over the second passivation layer 38 and similarly extends to the second passivation termination edge 54. The contact pads 42 may be provided on the second passivation layer 38 and be exposed to the outside environment via one or more openings in the third passivation layer 40. While not shown, metallization layers within the first passivation layer 36 and the second passivation layer 38 may couple the contact pads to one or more semiconductor devices in the active area 46.

[0021] The first passivation termination edge 52 is inset from the substrate termination edge 44 by a first distance D_1. In various embodiments, the first distance D_1 may be between 1µm and 150µm. The second passivation termination edge 54 is inset from the substrate termination edge 44 by a second distance D_2. In various embodiments, the second distance D_2 may be between 0.5µm and 50µm. Notably, the second distance D_2 is less than the first distance D_1 such that the second passivation layer 38 and the third passivation layer 40 overlap the first passivation layer 36. Accordingly, the first passivation termination edge 52 is shielded from the surrounding environment by the second passivation layer 38 and the third passivation layer 40. Providing the first passivation layer 36, the second passivation layer 38, and the third passivation layer 40 in this manner increases the ruggedness of the semiconductor die 32 by preventing moisture ingress into the active area 46. In one embodiment, a difference between the first distance D_1 and the second distance D_2 is greater than 0.5µm and less than 100µm. In general, the difference between the first distance D_1 and the second distance D_2 may be greater than x and less than y. In various embodiments, x may be 1µm, 2µm, 3µm, 4µm, 5µm, 6µm, 7µm, 8µm, 9µm, 10µm, and up to but not including 50µm. For any of these embodiments y may be 50µm, 60µm, 70µm, 80µm, 90µm, and up to 100µm.

[0022] While only three passivation layers are shown, the principles discussed herein may be applied to any number of passivation layers without departing from the principles of the present disclosure. Further, the first passivation layer 36, the second passivation layer 38, and the third passivation layer 40 may comprise multiple layers themselves. Finally, the principles of the present disclosure may be applied to as little as two passivation layers. That is, the third passivation layer 40 is optional in the embodiment discussed above. Additionally, while the substrate 34 is shown as a single layer, the substrate 34 may include multiple layers (e.g., a carrier layer and one or more epitaxial layers on top of the carrier layer). In these embodiments, the barrier region 48 may be provided through one or more of the epitaxial layers, but not the carrier layer. In one embodiment, the substrate 34 may comprise gallium nitride (GaN). In other

embodiments, the substrate 34 may comprise silicon (Si), silicon carbide (SiC), or any other semiconductor material system.

[0023] In one embodiment, the first passivation layer 36, the second passivation layer 38, and the third passivation layer 40 comprise stoichiometric and non-stoichiometric formulations of alumina, silica, silicon nitride, silicon oxynitride, silicon dioxide, and/or zirconium oxide. Further, the composition of the first passivation layer 36, the second passivation layer 38, and the third passivation layer 40 may alternate in some embodiments. Separately applying the passivation layers and/or alternating the composition of the passivation layers may reduce the presence of defects (e.g., pinholes) in the layers that traverse more than one of the layers to prevent exposing the active area 46 to the outside environment.

[0024] Figure 3 shows a top-down view of the semiconductor die 32 illustrating the relative positions of the first passivation termination edge 52 and the second passivation termination edge 54 with respect to the substrate termination edge 44 according to one embodiment of the present disclosure. As illustrated, the first passivation termination edge 52 and the second passivation termination edge 54 are inset from the perimeter of the semiconductor die 32 such that the second passivation termination edge 54 is nested inside the substrate termination edge 44 and the first passivation termination edge 52 is nested within the second passivation termination edge 54.

[0025] Figure 4 shows the semiconductor die 32 according to an additional embodiment of the present disclosure. The semiconductor die 32 shown in Figure 4 is substantially the same as that shown in Figure 2, except that the third passivation layer 40 in Figure 4 extends over the second passivation layer 38 to a third passivation termination edge 56, which is inset from the substrate termination edge 44 by a third distance D_3. The third distance D_3 is less than the second distance D_2, such that the third passivation layer 40 overlaps the first passivation layer 36 and the second passivation layer 38. Doing so may further increase the ruggedness of the semiconductor die 32, as it may provide a barrier between the second passivation termination edge 54 and the surrounding

environment, and provides an additional barrier between the first passivation termination edge 52 and the surrounding environment. Because the passivation layers may be separately provided and/or alternate in composition, the layers may resist delamination in different conditions, which may prevent moisture ingress over a wide range of environmental conditions.

[0026] In the embodiment shown in Figure 4, the first distance D_1 may be larger, such that it may be between 1.5µm and 250µm. The second distance D_2 may be between 1µm and 150µm. The third distance may be between 0.5µm and 50µm. In one embodiment, a difference between the first distance D_1 and the second distance D_2 is greater than 5µm and less than 50µm. Similarly, a difference between the second distance D_2 and the third distance D_3 is greater than 0.5µm and less than 50µm. In general, the difference between the first distance D_1 and the second distance D_2, and the difference between the second distance D_2 and the third distance D_3 may be greater than x and less than y. In various embodiments, x may be 1µm, 2µm, 3µm, 4µm, 5µm, 6µm, 7µm, 8µm, 9µm, 10µm, and up to but not including 50µm. For any of these embodiments y may be 50µm, 60µm, 70µm, 80µm, 90µm, and up to 100µm.

[0027] Figure 5 shows a top-down view of the semiconductor die 32 illustrating the relative positions of the first passivation termination edge 52, the second passivation termination edge 54, and the third passivation termination edge 56 with respect to the substrate termination edge 44 according to one embodiment of the present disclosure. As illustrated, the first passivation termination edge 52, the second passivation termination edge 54, and the third passivation termination edge 56 are inset from the perimeter of the semiconductor die 32 such that the third passivation termination edge 56 is nested inside the substrate termination edge 44, the second passivation termination edge 54 is nested inside the third passivation termination edge 56, and the first passivation termination edge 52 is nested inside the second passivation termination edge 54.

[0028] As discussed above, the buildup of an electric field at the termination edge of any of the passivation layers may contribute to moisture and/or ion

ingress as it may attract particles towards the active area 46 and thus encourage delamination thereof. In an effort to mitigate this effect, Figure 6 shows an enlarged view of one side of the semiconductor die 32 shown in Figure 2 further including a charge redistribution path 58. The charge redistribution path 58 is provided as a metal layer on the substrate 34 between the first passivation termination edge 52 and the second passivation termination edge 54. While not shown, in some embodiments the charge redistribution path 58 may be provided inside the first passivation termination edge 52 or may traverse across the first passivation termination edge 52 and/or the second passivation termination edge 54. In one embodiment, the charge redistribution path 58 may be provided around the perimeter of the semiconductor die 32 and coupled to a fixed potential such as ground.

[0029] In addition to mitigating the ingress of moisture and/or ions to the active area of the semiconductor die 32, the charge redistribution path 58 may provide other operational benefits as well. While the charge redistribution path 58 shown in Figure 6 forms a ring around the perimeter of the semiconductor die 32, the charge redistribution path 58 may be provided in any area in which charge redistribution may be beneficial (e.g., to avoid moisture and/or ion ingress) and thus may be provided in any shape and at any location on the semiconductor die (e.g., over a portion of the active area, bisecting the active area, etc.). In some embodiments, the charge redistribution path 58 forms a closed path, while in other embodiments the charge redistribution path 58 may remain open. Further, while the charge redistribution path 58 is shown as a metal layer on the substrate 34 between the substrate 34 and the first passivation layer 36, the charge redistribution path 58 may be provided on the opposite side of the substrate 34 (opposite the first passivation layer 36), on the first passivation layer 36, on the second passivation layer 38, on the third passivation layer 40, or on any other layer without departing from the principles described herein. In various embodiments, the location of the charge redistribution path 58 may be different in different areas of the device. For example, one lateral edge of the semiconductor die 32 may be reserved for gate

contacts of semiconductor devices in the active area 46 thereof and thus be referred to as a "gate side," while an opposite lateral edge of the semiconductor die may be reserved for drain contacts of semiconductor devices in the active area 46 thereof and thus be referred to as a "drain side." Since the electric field in these different portions of the semiconductor die 32 may be different, the charge redistribution path 58 may be provided in a first pattern and in a first location on one of the substrate 34, the first passivation layer 36, the second passivation layer 38, the third passivation layer 40, or any other layer on the gate side of the semiconductor die 32 and provided in a second pattern and in a second location on one of the substrate 34, the first passivation layer 36, the second passivation layer 38, the third passivation layer 40, or any other layer on the drain side of the semiconductor die. In general, the particular pattern and location of the charge redistribution path 58 may be different for different areas of the semiconductor die 32, as the field in these different areas may be different and thus may need to be redistributed in different ways to increase the performance of the semiconductor die 32.

[0030] Figure 7 shows a top-down view of the semiconductor die 32 including the charge redistribution path 58 according to one embodiment of the present disclosure. As shown, the charge redistribution path 58 is inset from the perimeter of the semiconductor die 32 between the first passivation termination edge 52 and the second passivation termination edge 54. Providing the charge redistribution path 58 as shown in Figures 6 and 7 reduces the electric field at the first passivation termination edge 52 and the second passivation termination edge 54, which in turn reduces moisture and ion ingress and increases the ruggedness of the semiconductor die 32. The charge redistribution path 58 may be a metal layer comprising aluminum, alloys of titanium, silicon, nickel, and platinum, alloys of titanium, aluminum, nickel, and gold, alloys of titanium nickel, and aluminum, alloys of germanium, nickel, and aluminum, and any other metal system used to make electrical contact to the accompanying active devices.

[0031] Figure 8 shows an enlarged view of one side of the semiconductor die 32 shown in Figure 4 further including the charge redistribution path 58 according

to one embodiment of the present disclosure. The charge redistribution path 58 is provided as a metal layer on the substrate 34 between the first passivation termination edge 52 and the second passivation termination edge 54. While not shown, in some embodiments the charge redistribution path 58 may be provided inside the first passivation termination edge 52, may be provided between the second passivation termination edge 54 and the third passivation termination edge 56, or may traverse across the first passivation termination edge 52, the second passivation termination edge 54, and the third passivation termination edge 56. The charge redistribution path 58 may be provided around the perimeter of the semiconductor die 32 and coupled to a fixed potential such as ground.

[0032] Figure 9 shows a top-down view of the semiconductor die 32 including the charge redistribution path 58 according to one embodiment of the present disclosure. As shown, the charge redistribution path 58 is inset from the perimeter of the semiconductor die 32 between the first passivation termination edge 52 and the second passivation termination edge 54. Providing the charge redistribution path 58 as shown in Figures 8 and 9 reduces the electric field at the first passivation termination edge 52, the second passivation termination edge 54, and the third passivation termination edge 56, which in turn reduces moisture ingress and increases the ruggedness of the semiconductor die 32. The charge redistribution path 58 may be a metal layer comprising aluminum, alloys of titanium, silicon, nickel, and platinum, alloys of titanium, aluminum, nickel, and gold, alloys of titanium nickel, and aluminum, alloys of germanium, nickel, and aluminum, and any other metal system used to make electrical contact to the accompanying active devices.

[0033] Figure 10 shows an enlarged view of one side of the semiconductor die 32 shown in Figure 2 further including a charge redistribution path 60 according to one embodiment of the present disclosure. The charge redistribution path 60 is preferably provided as a conductive (i.e., not implanted or conductively implanted) region of the substrate 34 outside of the barrier region 48. That is, rather than extending between the barrier region inner edge 50 and

the substrate termination edge 44, the barrier region 48 extends between the barrier region inner edge 50 and a barrier region outer edge 62, which is inset from the substrate termination edge 44 by a third distance D_3. The region comprising the charge redistribution path 60 may in part also be implanted with conductive dopant to have conductivity higher than that of the surface conducting part of the active area. The third distance D_3 may be less than the first distance D_1 between the first passivation termination edge 52 and the substrate termination edge 44 and more than the second distance D_2 between the second passivation termination edge 54 and the substrate termination edge 44. The conductive region of the substrate 34 forming the charge redistribution path 60 may be coupled to ground through the substrate 34 or by a direct contact to a topside grounded or non-zero biased contact pad. For example, the surface conductive region of the substrate 34 may be connected to ground through a contact pad on the backside of the substrate 34 (not shown). This may be achieved by additional masking when implanting the barrier region 48, as discussed below. The charge redistribution path 60 may be provided in any number of shapes and as a closed or open path without departing from the principles herein.

[0034] Figure 11 shows a top-down view of the semiconductor die 32 including the charge redistribution path 60 according to one embodiment of the present disclosure. As shown, the charge redistribution path 60 is on the outside of the barrier region 48 as a conductive or not implanted region. While not shown, the barrier region outer edge 62 may be provided inside the first passivation termination edge 52 (i.e., the third distance D_3 may be greater than the first distance D_1) or at any other point between the first passivation termination edge 52 and the second passivation termination edge 54. Providing the charge redistribution path 60 as shown in Figures 10 and 11 reduces the electric field at the first passivation termination edge 52 and the second passivation termination edge 54, which in turn reduces moisture ingress and increases the ruggedness of the semiconductor die 32. While the charge redistribution path 60 may be a region that is not implanted, it may also be

implanted as a conductive region, for example, using silicon (Si), calcium (Ca), Oxygen (O), germanium (Ge), or carbon (C).

[0035] Figure 12 shows an enlarged view of one side of the semiconductor die 32 shown in Figure 4 further including the charge redistribution path 60 according to one embodiment of the present disclosure. The charge redistribution path 60 is provided as a conductive (i.e., not implanted) region of the substrate 34 outside the barrier region 48. That is, rather than extending between the barrier region inner edge 50 and the substrate termination edge 44, the barrier region 48 extends between the barrier region inner edge 50 and a barrier region outer edge 62, which is inset from the substrate termination edge 44 by a fourth distance D_4. The fourth distance D_4 may be less than the first distance D_1 between the first passivation termination edge 52 and the substrate termination edge 44 and more than the second distance D_2 between the second passivation termination edge 54 and the substrate termination edge 44. The conductive region of the substrate 34 forming the charge redistribution path 60 may be coupled to ground through the substrate 34. For example, the conductive region of the substrate 34 may be connected to ground through a contact pad on the backside of the substrate 34 (not shown).

[0036] Figure 13 shows a top-down view of the semiconductor die 32 including the charge redistribution path 60 according to one embodiment of the present disclosure. As shown, the charge distribution path 60 is on the outside of the barrier region 48 as a conductive or not implanted region. While not shown, the barrier region outer edge 62 may be provided inside the first passivation termination edge 52 (i.e., the fourth distance D_4 may be greater than the first distance D_1), may be provided between the second passivation termination edge 54 and the third passivation termination edge 56 (i.e., the fourth distance D_4 may be greater than the third distance D_3 and less than the second distance D_2), or may be provided at any other point between the first passivation termination edge 52 and the second passivation termination edge 54. Providing the charge redistribution path 60 as shown in Figures 12 and 13 reduces the electric field at the first passivation termination edge 52, the second passivation termination

edge 54, and the third passivation termination edge 56, which in turn reduces moisture ingress and increases the ruggedness of the semiconductor die 32. While the charge redistribution path 60 may be a region that is not implanted, it may also be implanted as a conductive region, for example, using silicon (Si), calcium (Ca), Oxygen (O), germanium (Ge), or carbon (C).

[0037] While the charge redistribution paths are discussed above with respect to semiconductor die, the principles described herein may also be applied to other devices such as monolithic microwave integrated circuits.

[0038] Figure 14 is a flow diagram illustrating a method for manufacturing a semiconductor die according to one embodiment of the present disclosure. First, a substrate is provided (step 100). A barrier region is then provided around an active region in the substrate (step 102). This may involve, for example, implanting a region of the substrate such that it is no longer conductive. This may be accomplished by implanting the substrate with nitrogen (N), hydrogen (H), helium (He), magnesium (Mg), zirconium (Zr), krypton (Kr), argon (Ar), and Iron (Fe), but can also be an etched mesa or shallow trench isolation (STI). In embodiments in which a charge redistribution path is provided as a conductive or not implanted region outside the barrier region, this may include additional masking when implanting the barrier region such that it terminates at a barrier region outer edge that is inset from a substrate termination edge. In other embodiments, this may include providing additional implantation outside the barrier region to make this region more conductive. This may be accomplished by implanting the substrate with silicon (Si), calcium (Ca), Oxygen (O), germanium (Ge), or carbon (C). A number of semiconductor devices are then provided in the active area of the semiconductor die (step 104). This may involve, for example, implanting various regions within the active area, providing metal layers for contacts, and other steps that will be appreciated by those skilled in the art. If the charge redistribution path is not provided as a conductive region outside the barrier region, but instead provided as a metal layer on the substrate, the charge redistribution path is then provided (step 106). This may involve masking and depositing a metal layer on the surface of the substrate as

discussed above. A first passivation layer is then provided over the substrate (step 108). As discussed above, the first passivation layer may terminate at a first passivation termination edge. A second passivation layer is then provided over the first passivation layer and the substrate (step 110). As discussed above, this second passivation layer may terminate at a second passivation termination edge, which is between the first passivation termination edge and the substrate termination edge such that the second passivation layer overlaps the first passivation layer. The third passivation layer may then be provided over the second passivation layer (step 112). As discussed above, the third passivation layer may terminate at the second passivation termination edge, or may terminate at a third passivation termination edge that is between the second passivation termination edge and the substrate termination edge.

[0039] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A semiconductor die comprising:
   - a substrate, the substrate having boundaries defined by a substrate termination edge;
   - a first passivation layer over the substrate, the first passivation layer terminating at a first passivation termination edge that is inset from the substrate termination edge by a first distance; and
   - a second passivation layer over the first passivation layer and the substrate, the second passivation layer terminating at a second passivation termination edge that is inset from the substrate termination edge by a second distance, wherein the second distance is less than the first distance such that the second passivation layer overlaps the first passivation layer.

2. The semiconductor die of claim 1 further comprising a third passivation layer over the second passivation layer and the substrate, the third passivation layer terminating at a third passivation termination edge that is inset from the substrate by a third distance, wherein the third distance is less than the second distance such that the third passivation layer overlaps the second passivation layer.

3. The semiconductor die of claim 2 wherein the substrate comprises:
   - an active area in which one or more active devices are provided; and
   - a barrier region surrounding the active area and configured to electrically isolate the active area from the substrate termination edge, wherein:
     - the barrier region terminates at a barrier region termination edge that is inset from the substrate termination edge by a fourth

distance, wherein the fourth distance is greater than the third distance; and

- a charge redistribution path is formed by a region between the barrier region termination edge and the substrate termination edge.

4. The semiconductor die of claim 3 wherein the region forming the charge redistribution path is implanted with dopants to increase the conductivity thereof.

5. The semiconductor die of claim 3 wherein the charge redistribution path is coupled to a fixed potential.

6. The semiconductor die of claim 3 wherein the fourth distance is greater than the second distance.

7. The semiconductor die of claim 2 further comprising a charge redistribution path, the charge redistribution path comprising a metal layer under the second passivation layer between the first passivation termination edge and the second passivation termination edge.

8. The semiconductor die of claim 7 wherein the charge redistribution path is coupled to a fixed potential.

9. The semiconductor die of claim 1 wherein the substrate comprises:

- an active area in which one or more active devices are provided; and
- a barrier region surrounding the active area and configured to electrically isolate the active area from the substrate termination edge, wherein:
  - the barrier region terminates at a barrier region termination edge that is inset from the substrate termination edge by a third distance, wherein the third distance is greater than the second distance; and

- a charge redistribution path is formed by a region between the barrier region termination edge and the substrate termination edge.

10. The semiconductor die of claim 9 wherein the region forming the charge redistribution path is implanted with dopants to increase the conductivity thereof.

11. The semiconductor die of claim 9 wherein the charge redistribution path is coupled to a fixed potential.

12. The semiconductor die of claim 1 further comprising a charge redistribution path, the charge redistribution path comprising a metal layer under the second passivation layer between the first passivation termination edge and the second passivation termination edge.

13. The semiconductor die of claim 12 wherein the charge redistribution path is coupled to a fixed potential.

14. A method for manufacturing a semiconductor die comprising:

- providing a substrate, the substrate having boundaries defined by a substrate termination edge;
- providing a first passivation layer over the substrate such that the first passivation layer terminates at a first passivation termination edge that is inset from the substrate termination edge by a first distance; and
- providing a second passivation layer over the first passivation layer and the substrate such that the second passivation layer terminates at a second passivation termination edge that is inset from the substrate termination edge by a second distance, wherein the second distance is less than the first distance such that the second passivation layer overlaps the first passivation layer.

15. The method of claim 14 further comprising providing a third passivation layer over the second passivation layer and the substrate, the third passivation layer terminating at a third passivation termination edge that is inset from the substrate by a third distance, wherein the third distance is less than the second distance such that the third passivation layer overlaps the second passivation layer.

16. The method of claim 15 further comprising providing a barrier region in the substrate, wherein the barrier region:

- surrounds an active region in which one or more active devices are provided;
- electrically isolates the active region from the substrate termination edge; and
- terminates at a barrier region termination edge that is inset from the substrate termination edge by a fourth distance that is greater than the third distance such that a charge redistribution path is formed by a region between the barrier region termination edge and the substrate termination edge.

17. The method of claim 16 wherein the fourth distance is greater than the second distance.

18. The method of claim 15 further comprising providing a charge redistribution path as a metal layer under the second passivation layer between the first passivation termination edge and the second passivation termination edge.

19. The method of claim 16 further comprising coupling the charge redistribution path to a fixed potential.

20. The method die of claim 14 further comprising providing a barrier region in the substrate, wherein the barrier region:

- surrounds an active region in which one or more active devices are provided;
- electrically isolates the active region from the substrate termination edge; and
- terminates at a barrier region termination edge that is inset from the substrate termination edge by a fourth distance that is greater than the third distance such that a charge redistribution path is formed between a region between the barrier region termination edge and the substrate termination edge.

21. The method of claim 14 further comprising providing a charge redistribution path as a metal layer under the second passivation layer between the first passivation termination edge and the second passivation termination edge.

22. The method of claim 21 further comprising coupling the charge redistribution path to a fixed potential.

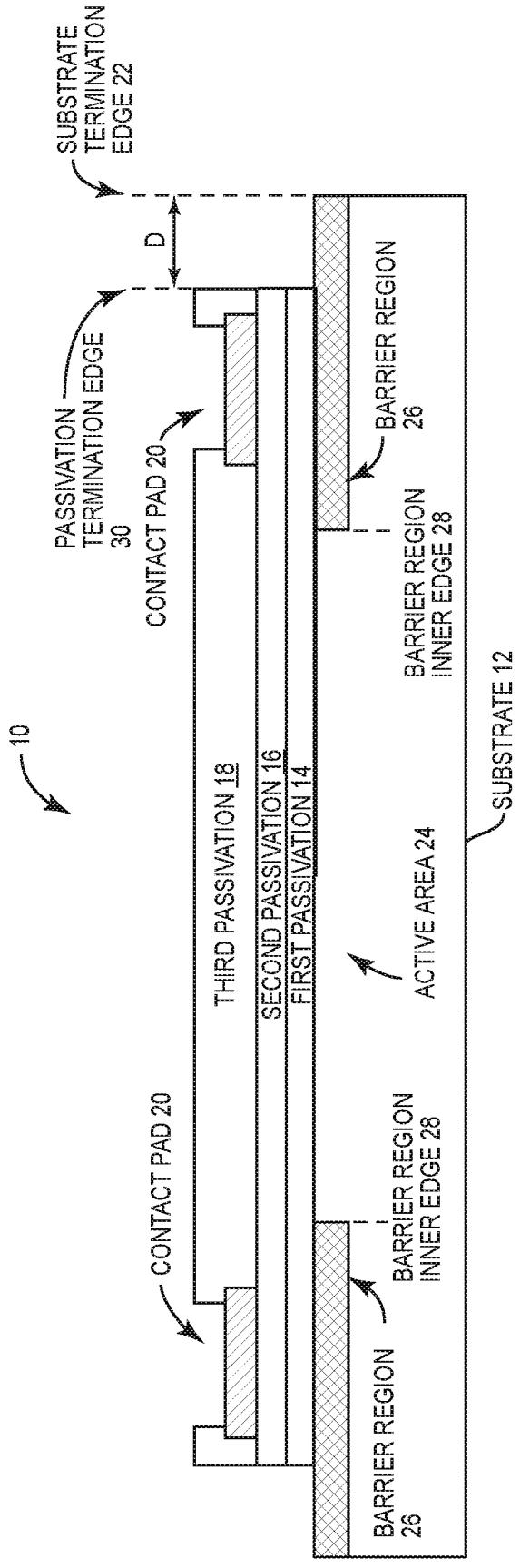
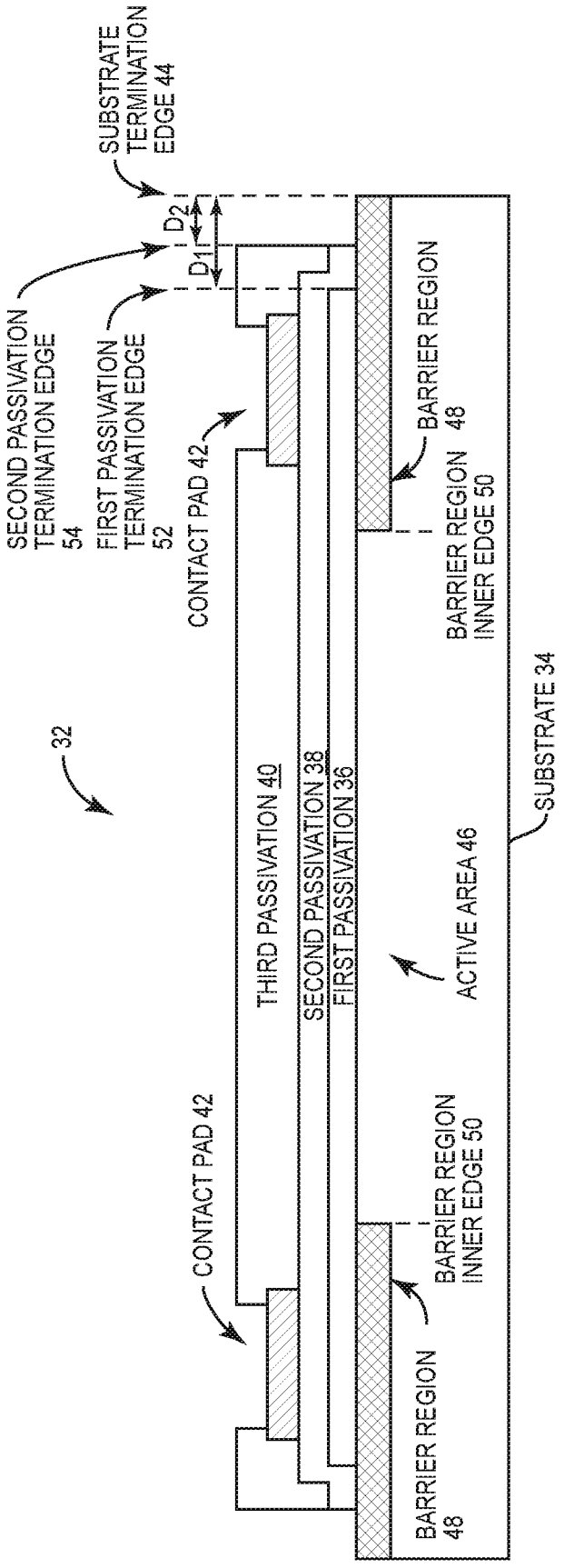


FIG. 1
(RELATED ART)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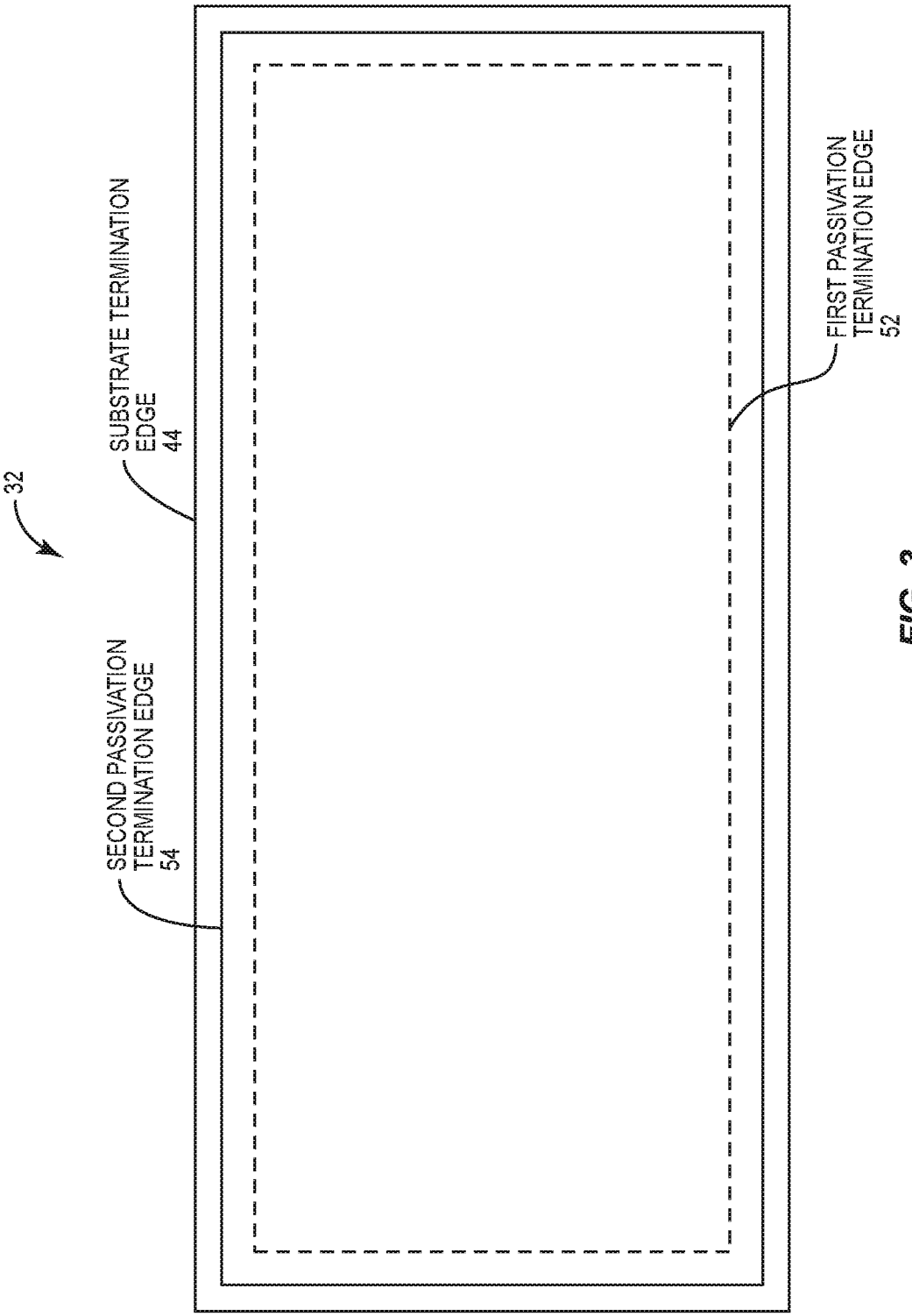
BARRIER REGION 48
BARRIER REGION INNER EDGE 50
32
THIRD PASSIVATION 40
SECOND PASSIVATION 38
FIRST PASSIVATION 36
ACTIVE AREA 46
SUBSTRATE 34
CONTACT PAD 42
BARRIER REGION INNER EDGE 50
BARRIER REGION 48

FIG. 2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FIRST PASSIVATION TERMINATION EDGE 52
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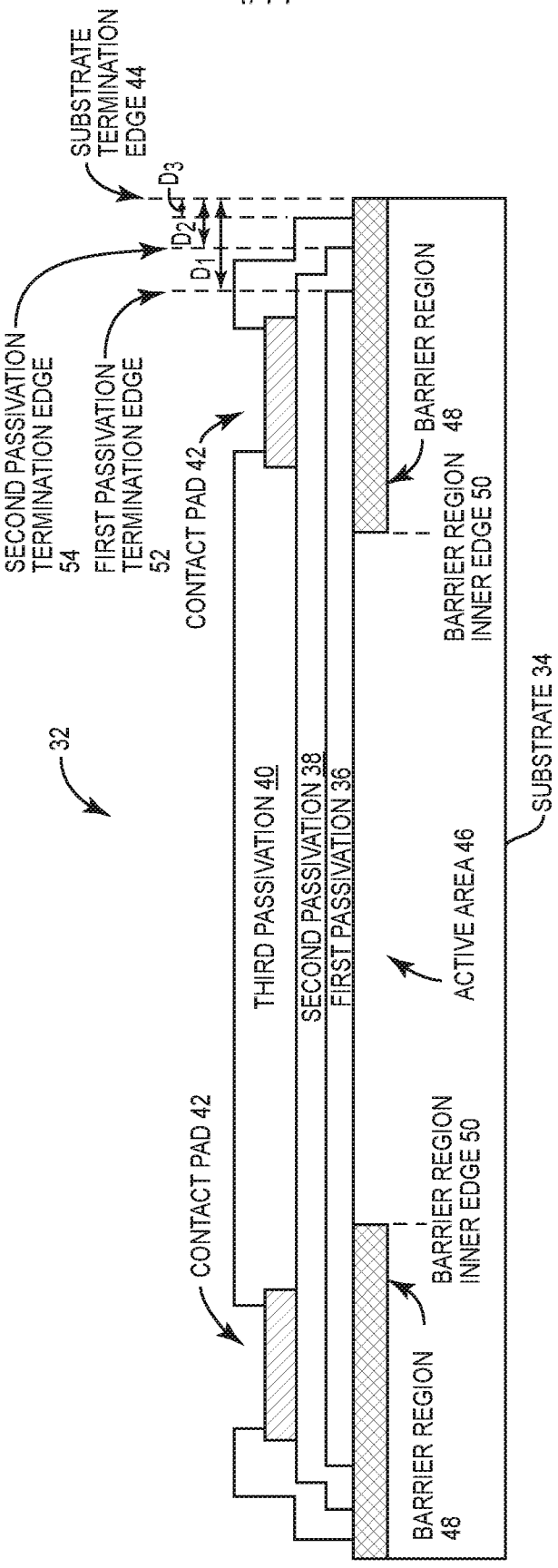
FIG. 3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D2
D1
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FIRST PASSIVATION TERMINATION EDGE 52
CONTACT PAD 42
BARRIER REGION 48
BARRIER REGION INNER EDGE 50
32
THIRD PASSIVATION 40
SECOND PASSIVATION 38
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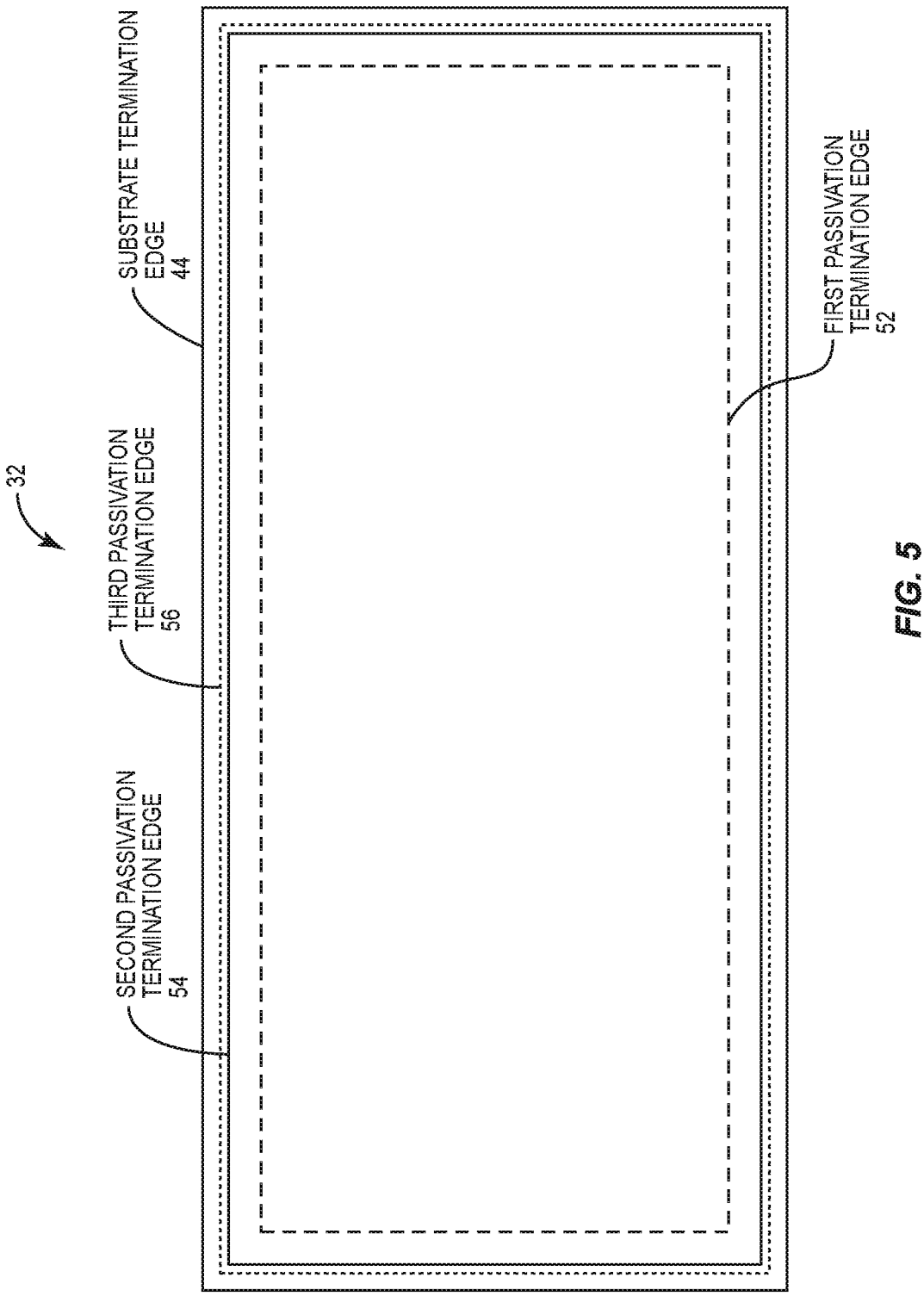
ACTIVE AREA 46
SUBSTRATE 34
CONTACT PAD 42
BARRIER REGION INNER EDGE 50
BARRIER REGION 48

FIG. 4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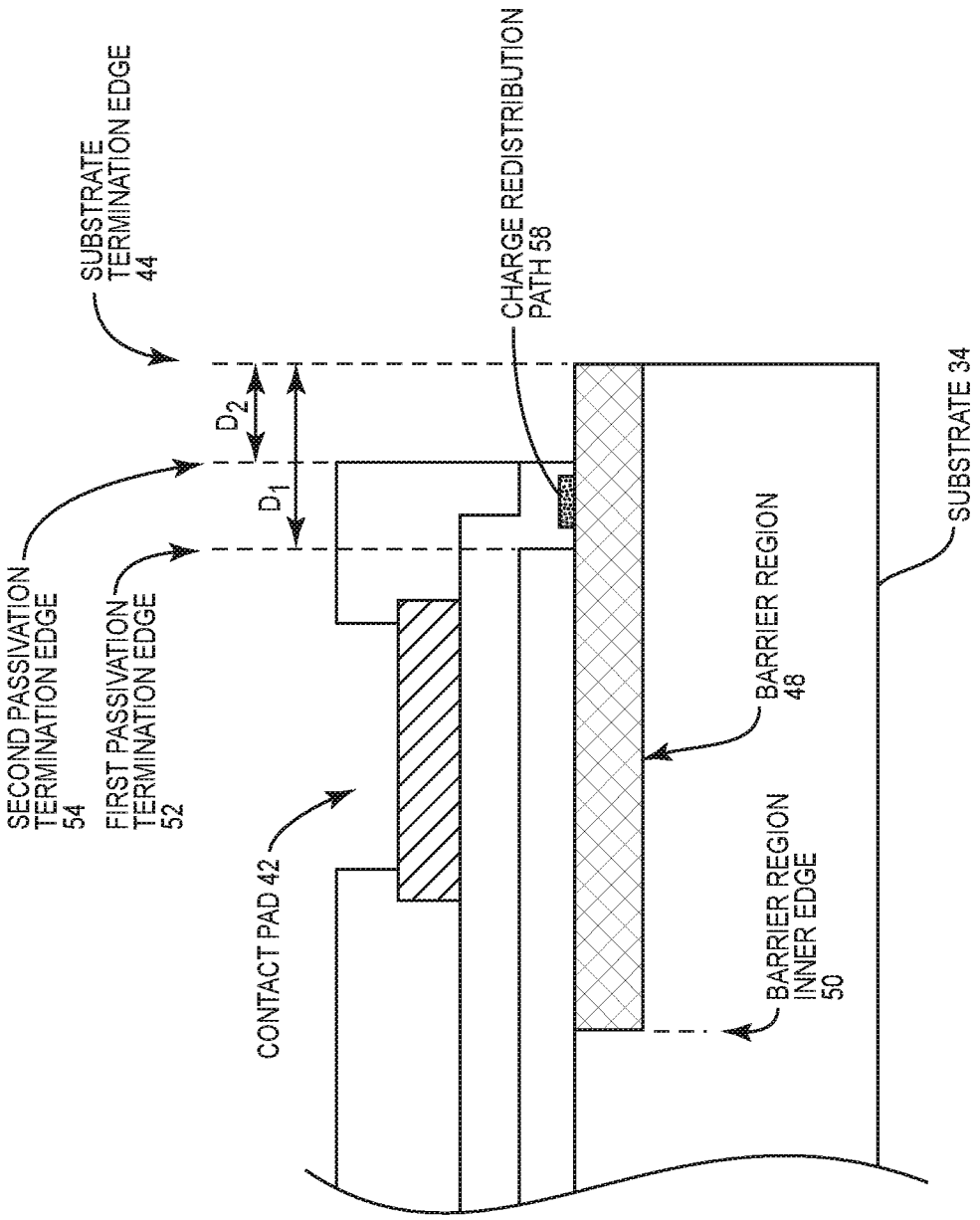
SECOND PASSIVATION TERMINATION EDGE 54
FIRST PASSIVATION TERMINATION EDGE 52

FIG. 5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SUBSTRATE 34
D_2
D_1
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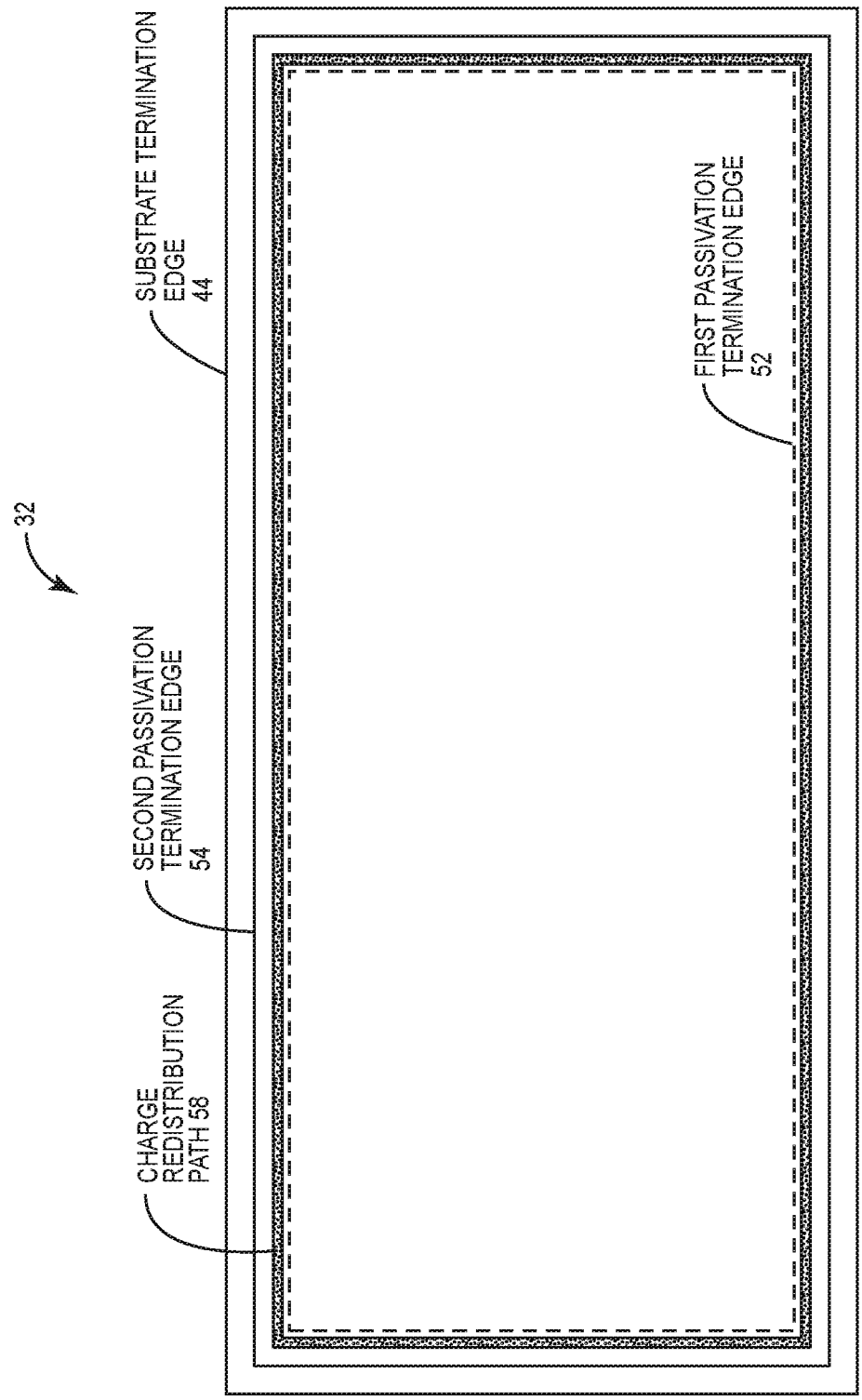
BARRIER REGION 48
CONTACT PAD 42
BARRIER REGION INNER EDGE 50

FIG. 6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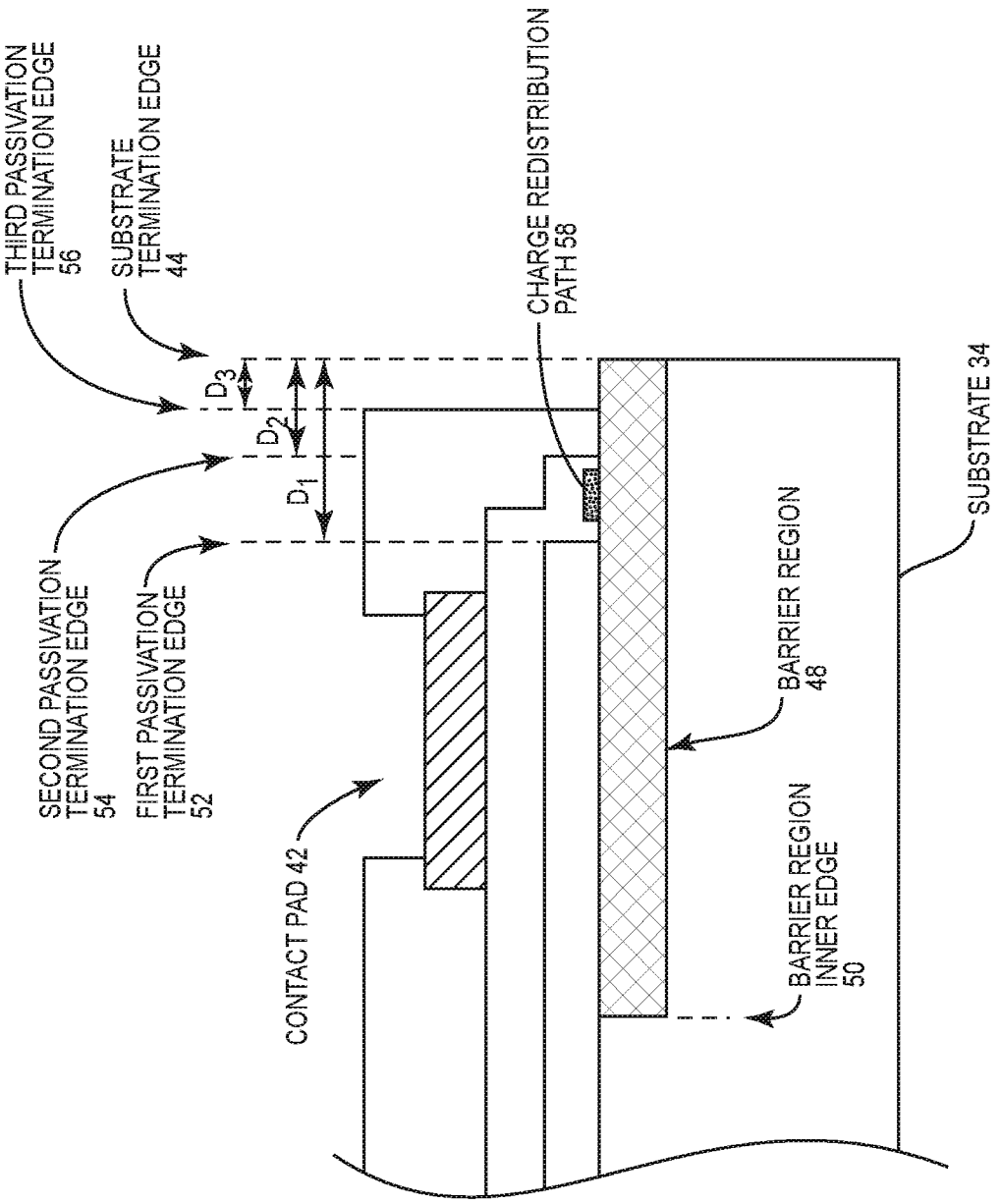
FIRST PASSIVATION TERMINATION EDGE 52
SECOND PASSIVATION TERMINATION EDGE 54
CHARGE REDISTRIBUTION PATH 58

FIG. 7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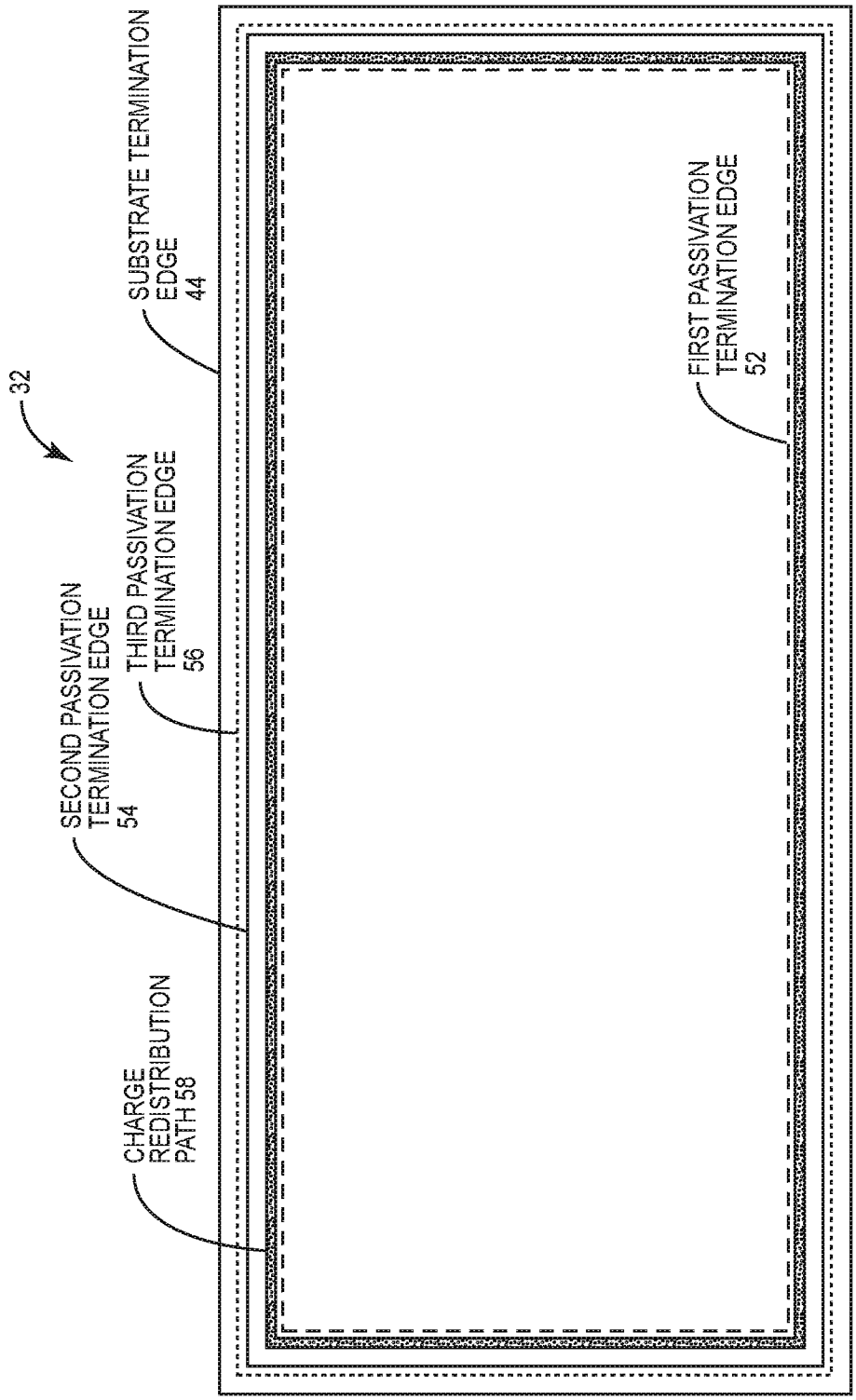
FIRST PASSIVATION TERMINATION EDGE 52
CONTACT PAD 42
BARRIER REGION INNER EDGE 50
BARRIER REGION 48
SUBSTRATE 34
D1
D2
D3

FIG. 8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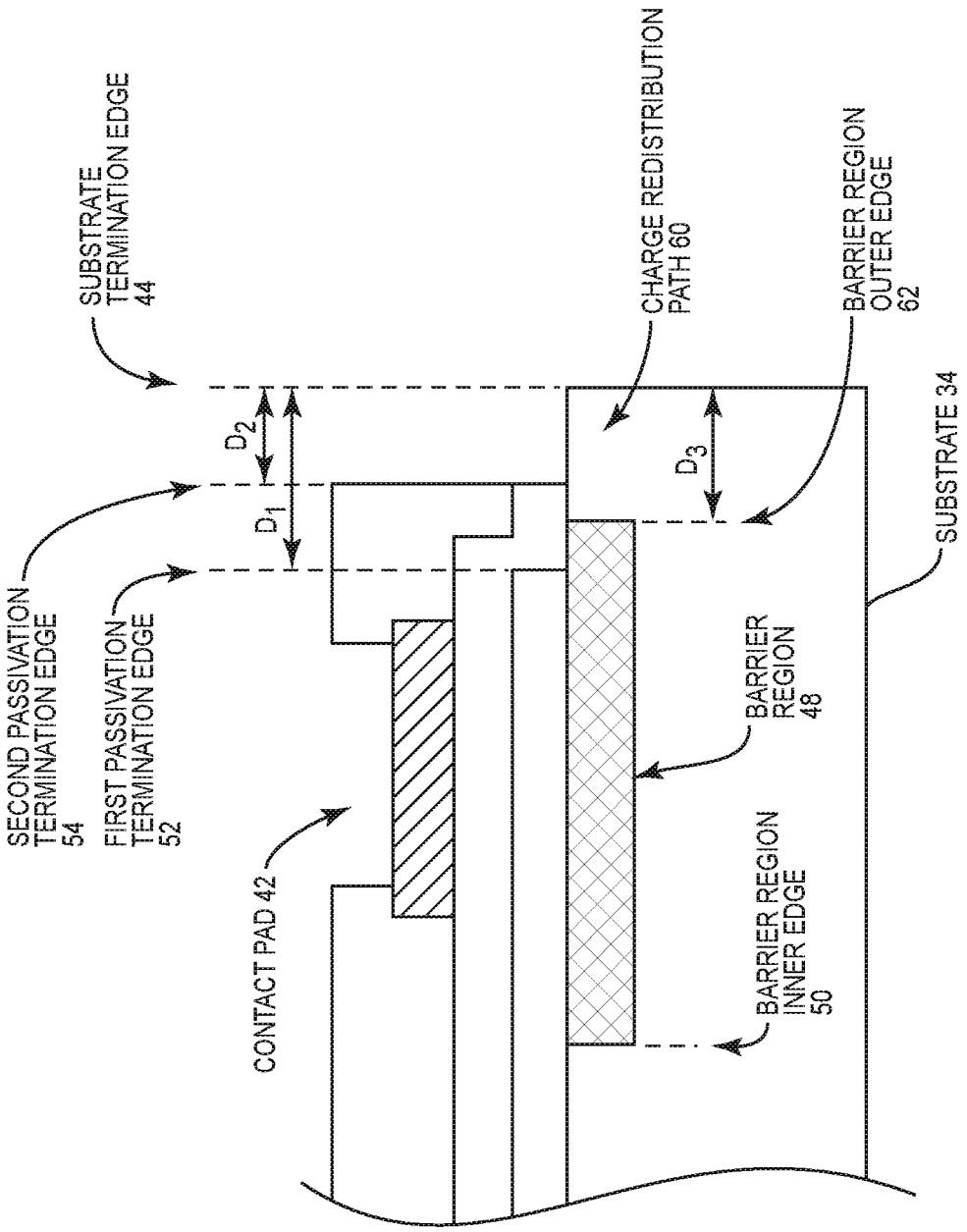
SECOND PASSIVATION TERMINATION EDGE 54
CHARGE REDISTRIBUTION PATH 58

FIG. 9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D_1
D_3
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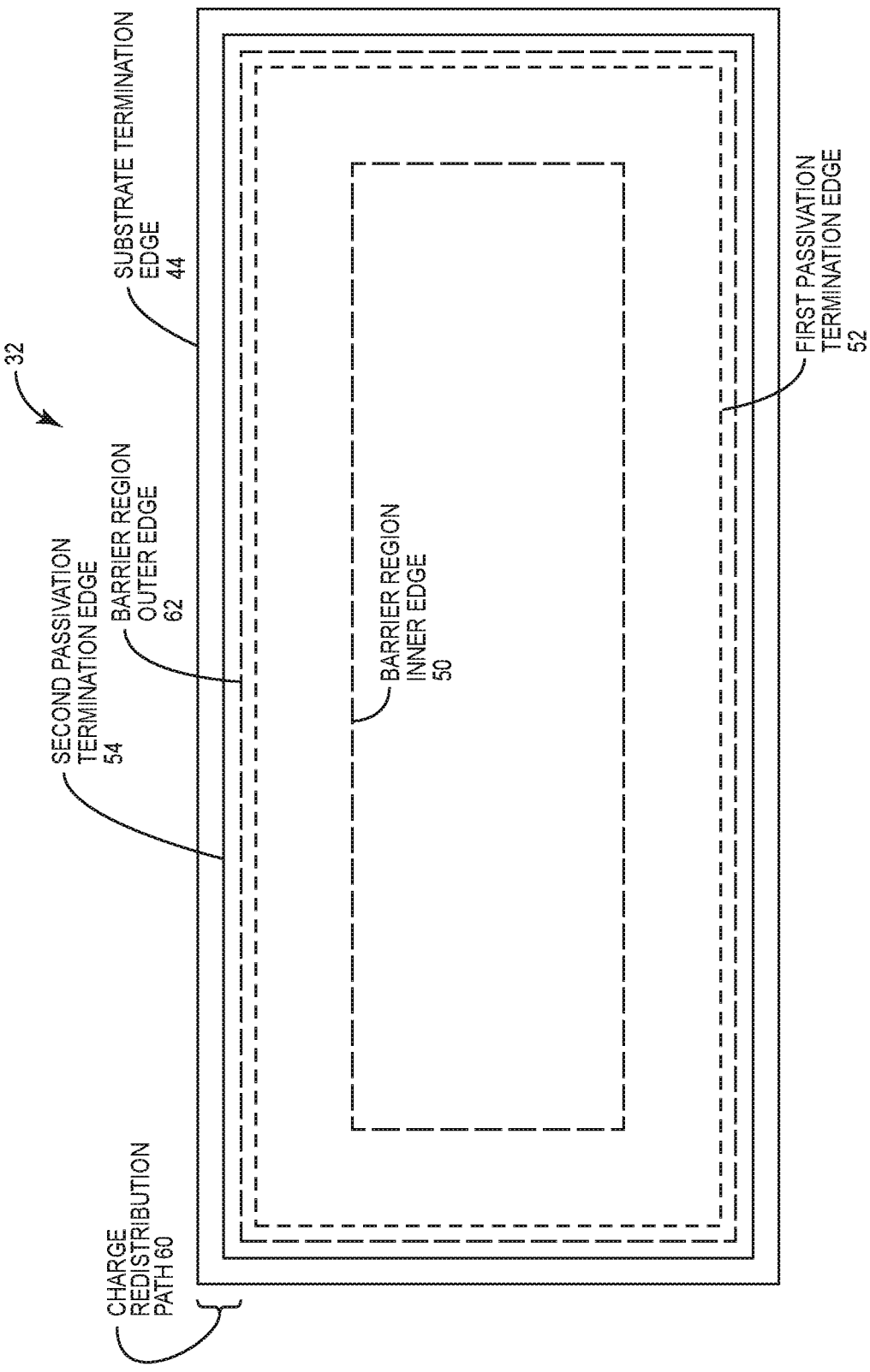
FIRST PASSIVATION TERMINATION EDGE 52
BARRIER REGION 48
CONTACT PAD 42
BARRIER REGION INNER EDGE 50

FIG. 10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FIRST PASSIVATION TERMINATION EDGE 52
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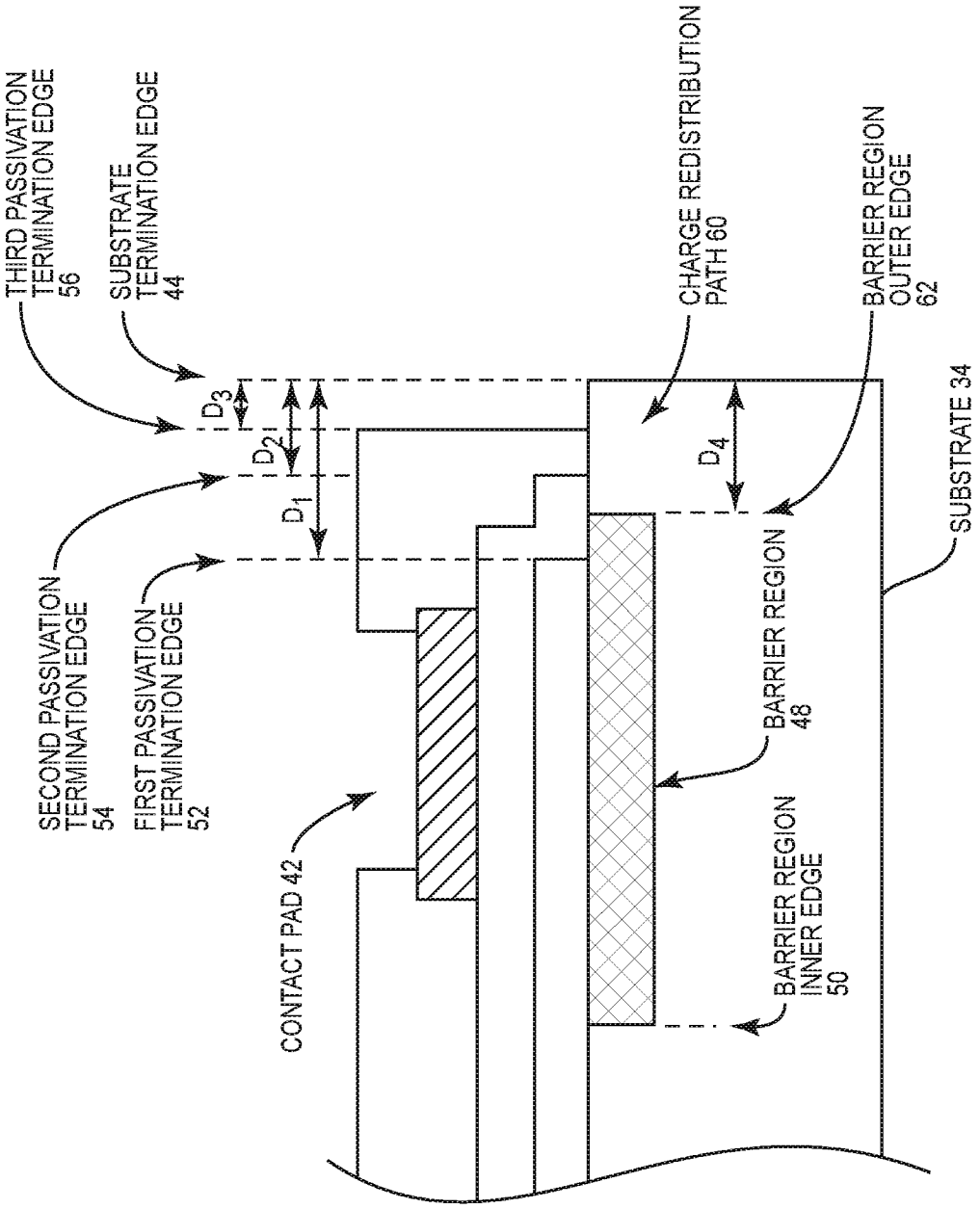
SECOND PASSIVATION TERMINATION EDGE 54
BARRIER REGION INNER EDGE 50
CHARGE REDISTRIBUTION PATH 60

FIG. 11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SUBSTRATE TERMINATION EDGE 44
CHARGE REDISTRIBUTION PATH 60
BARRIER REGION OUTER EDGE 62
SUBSTRATE 34
D_3
D_2
D_1
D_4
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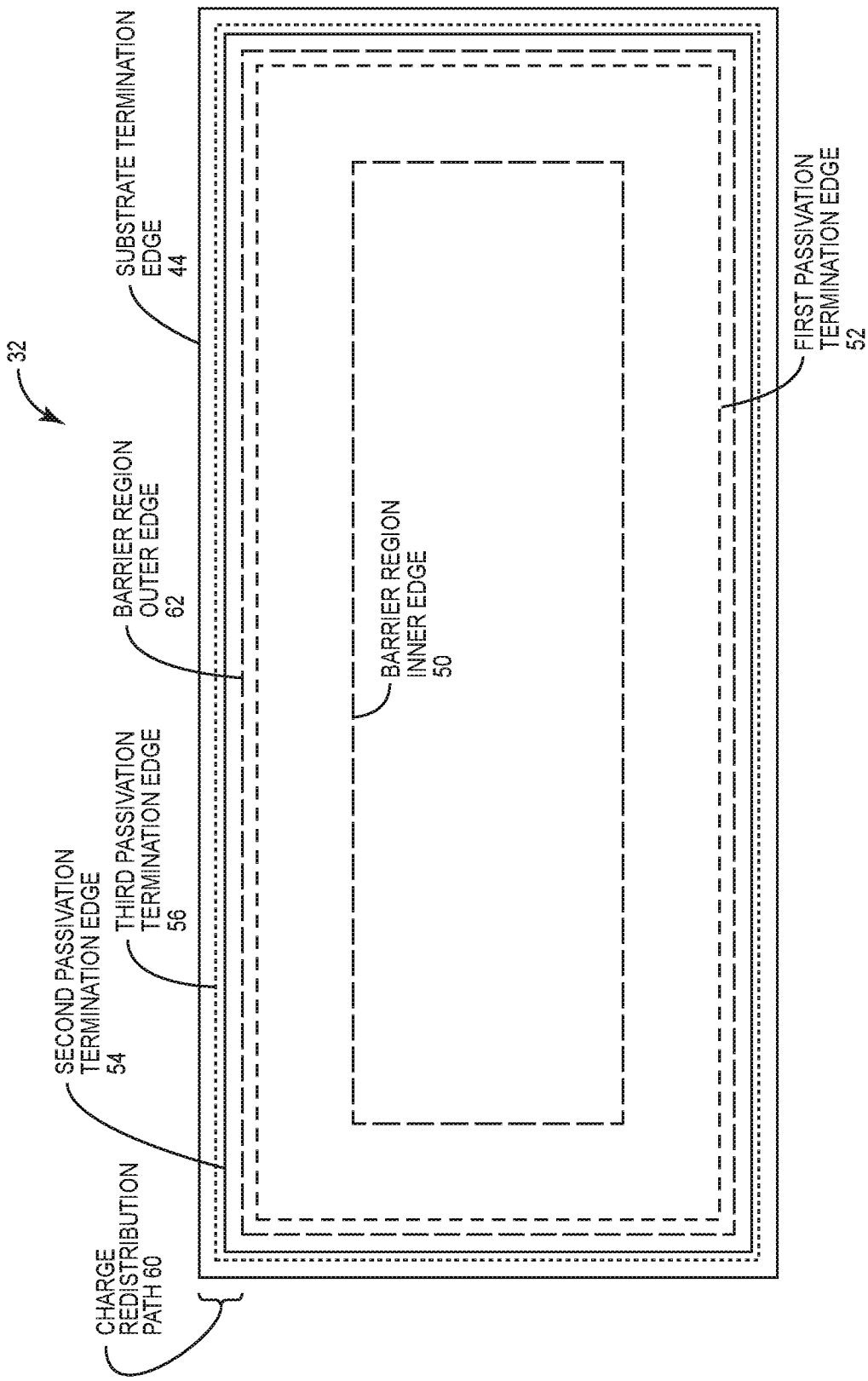
FIRST PASSIVATION TERMINATION EDGE 52
BARRIER REGION 48
CONTACT PAD 42
BARRIER REGION INNER EDGE 50

FIG. 12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THIRD PASSIVATION TERMINATION EDGE 56
SECOND PASSIVATION TERMINATION EDGE 54
CHARGE REDISTRIBUTION PATH 60

FIG. 13

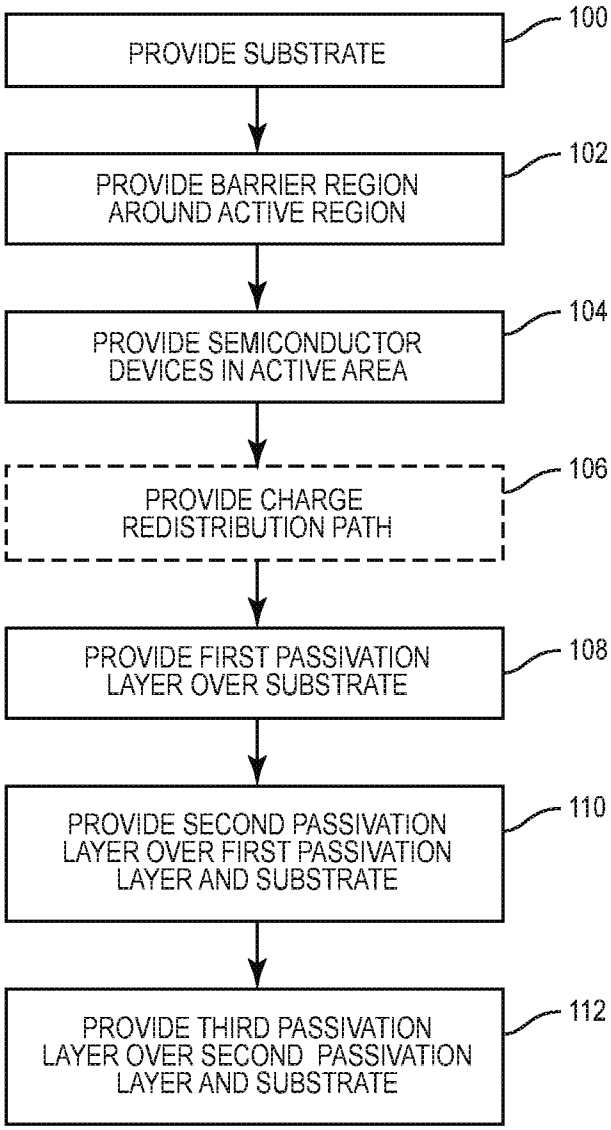
PROVIDE SUBSTRATE
100
PROVIDE BARRIER REGION AROUND ACTIVE REGION
102
PROVIDE SEMICONDUCTOR DEVICES IN ACTIVE AREA
104
PROVIDE CHARGE REDISTRIBUTION PATH
106
PROVIDE FIRST PASSIVATION LAYER OVER SUBSTRATE
108
PROVIDE SECOND PASSIVATION LAYER OVER FIRST PASSIVATION LAYER AND SUBSTRATE
110
PROVIDE THIRD PASSIVATION LAYER OVER SECOND PASSIVATION LAYER AND SUBSTRATE
112

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/058836

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/31 H01L29/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/299890 A1 (MATOCHA KEVIN [US] ET AL) 9 October 2014 (2014-10-09) paragraph [0078] - paragraph [0094]; figure 11 paragraph [0009] paragraph [0058] - paragraph [0070] -----	1-22
X	US 2010/025820 A1 (SUEKAWA EISUKE [JP]) 4 February 2010 (2010-02-04) paragraph [0005]; figure 1 paragraph [0030] - paragraph [0035] -----	1,9-14, 20-22
X	WO 2016/166808 A1 (MITSUBISHI ELECTRIC CORP [JP]) 20 October 2016 (2016-10-20) paragraph [0041] - paragraph [0059]; figures 1-10 -----	1-6, 9-11, 14-17, 19,20
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2019	22/01/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hirsch, Alexander

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/058836

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/303260 A1 (NIEDERNOSTHEIDE FRANZ JOSEF [DE] ET AL) 22 October 2015 (2015-10-22) paragraph [0004]; figures 1-8 paragraph [0031] paragraph [0050] - paragraph [0089] -----	1,2, 9-15, 20-22

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/058836

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 5477681 B2	23-04-2014
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		KR 20100012792 A	08-02-2010
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WO 2016166808 A1	20-10-2016	CN 107534061 A	02-01-2018
		DE 112015006450 T5	28-12-2017
		JP 6241572 B2	06-12-2017
		JP WO2016166808 A1	08-06-2017
		US 2018138272 A1	17-05-2018
		WO 2016166808 A1	20-10-2016
US 2015303260 A1	22-10-2015	CN 105047714 A	11-11-2015
		DE 102014005879 A1	22-10-2015
		US 2015303260 A1	22-10-2015