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(54) **Title**: SEMICONDUCTOR SOCKET

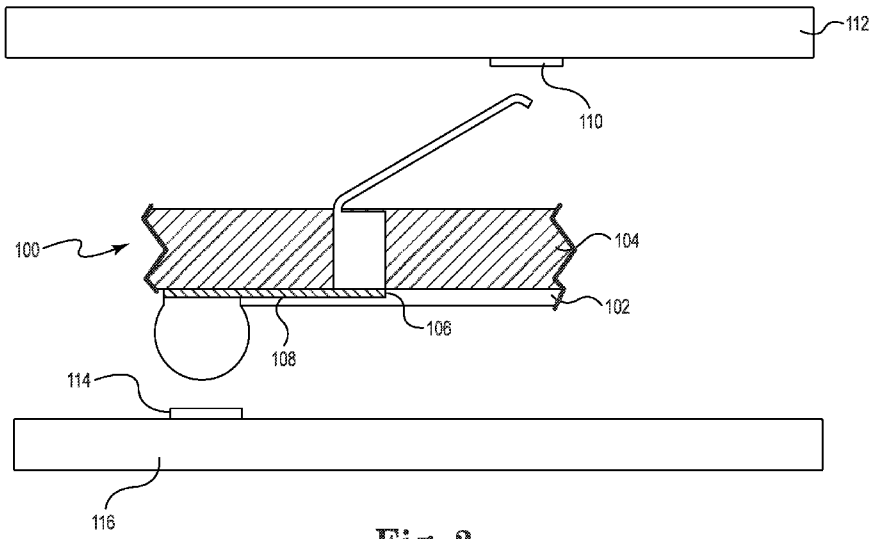

Fig. 2

(57) **Abstract**: A semiconductor socket including a substrate with a plurality of through holes extending from a first surface to a second surface. A plurality of discrete contact members are located in the plurality of the through holes. The plurality of contact members each include a proximal end accessible from the second surface, and a distal end extending above the first surface. At least one dielectric layer is bonded to the second surface of the substrate with recesses corresponding to target circuit geometry. A conductive material deposited in at least a portion of the recesses to form conductive traces redistributing terminal pitch of the proximal ends of the contact members.

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SEMICONDUCTOR SOCKET

Technical Field

[0001] The present application relates to a high performance semiconductor socket that forms an electrical interconnect between an integrated circuit and another circuit member.

Background of the Invention

[0002] Traditional integrated circuit (IC) sockets are generally constructed of an injection molded plastic insulator housing which has stamped and formed copper alloy contact members stitched or inserted into designated positions within the housing. The designated positions in the insulator housing are typically shaped to accept and retain the contact members. The assembled socket body is then generally processed through a reflow oven which melts and attaches solder balls to the base of the contact member. During final assembly, the socket can be mounted onto a printed circuit assembly. The printed circuit assembly may be a printed circuit board (printed circuit board), the desired interconnect positions on the printed circuit board are printed with solder paste or flux and the socket is placed such that the solder balls on the socket contacts land onto the target pads on the printed circuit board. The assembly is then reheated to reflow the solder balls on the socket assembly. When the solder cools it essentially welds the socket contacts to the printed circuit board, creating the electrical path for signal and power interaction with the system.

[0003] During use, the socket receives one or more IC packages and connects each terminal on the IC package to the corresponding terminal on the printed circuit board. The terminals on the IC package are held against the contact members by applying a load to the package, which is expected to maintain intimate contact and reliable circuit connection throughout the life of the system. No permanent connection is required so that the IC package can be removed or replaced without the need for reflowing solder connections.

[0004] These types of sockets and interconnects have been produced in high volume for many years. As systems advance to next generation architectures, these traditional devices have reached mechanical and electrical limitations that mandate alternate approaches.

[0005] As processors and electrical systems evolve, several factors have impacted the design of traditional sockets. Increased terminal count, reductions in the terminal pitch (i.e., the distance between the contacts), and signal integrity have been main drivers that impact the socket and contact design. As terminal count increases, the IC packages get larger due to the additional space needed for the terminals. As the IC package grows larger the relative flatness of the IC package and corresponding printed circuit board becomes more important. A certain degree of compliance is required between the contacts and the terminal pads to accommodate the topography differences and maintain reliable connections.

[0006] IC package manufacturers tend to drive the terminal pitch smaller so they can reduce the size of the IC package and reduce the flatness effects. As the terminal pitch reduces, however, the surface area available to place a contact is also reduced, which limits the space available to locate a spring or a contact member that can deflect without touching a neighbor.

[0007] In order to maximize the length of the spring so that it can deflect the proper amount without damage, the thickness of the insulating walls within the plastic housing is reduced. Thinner walls increase the difficulty of molding as well as the latent stress in the molded housing that can cause warping due to heat applied during solder reflow.

[0008] For mechanical reasons, longer contact members traditionally have been preferred because they have desirable spring properties. Long contact members, however, tend to reduce the electrical performance of the connection by creating a parasitic effect that impacts the signal as it travels through the contact. Other factors, such as contact resistance, impact self heating as current passes through, for example, power delivery contacts. Also, the small space between contact members can cause distortion as a nearby contact member influences a neighboring contact member, which is known as cross talk.

[0009] Traditional sockets and methods of fabricating the same are able to meet the mechanical compliance requirements of today's needs, but they have reached an electrical performance limit. Next generation systems will operate above 5 GHz and beyond and the existing interconnects will not achieve acceptable performance levels without significant revision.

Brief Summary of the Invention

[0010] The present disclosure is directed to semiconductor sockets that enable next generation electrical performance. A semiconductor socket according to the present disclosure may include a substrate and a plurality of discrete contact members positioned and secured in a plurality of holes through the substrate. Some of the embodiments can include a high performance interconnect architecture within a socket.

[0011] The contact members can be simple beam structures made of conventional materials, but omit the normal retention features that add parasitic mass and distort or degrade the integrity of the signal as it passes through the contact member. This approach provides a reliable connection to the package terminals and creates a platform to add electrical and mechanical enhancements to the substrate of the socket to address the challenges of next generation interconnect requirements. The lack of contact member retention features greatly reduces the complexity of the contact members and the tooling required to produce them.

[0012] Once embodiment is directed to a semiconductor socket including a substrate with a plurality of through holes extending from a first surface to a second surface. A plurality of discrete contact members are located in the plurality of the through holes. The plurality of contact members each include a proximal end accessible from the second surface, and a distal end extending above the first surface. At least one dielectric layer is bonded to the second surface of the substrate with recesses corresponding to target circuit geometry. A conductive material deposited in at least a portion of the recesses to form conductive traces redistributing terminal pitch of the proximal ends of the contact members.

[0013] Conductive plating is optionally applied to at least a portion of the conductive traces. The conductive material can be one of sintered conductive particles or a conductive ink. A compliant material is optionally located between the substrate and at least a portion of the circuit geometry.

[0014] At least one electrical device is printed on one of a dielectric layer or the substrate and electrically coupled to at least a portion of the circuit geometry. The conductive traces in the circuit geometry comprise preferably have substantially rectangular cross-sectional shapes. The present printing process permits a conductive material, a non-conductive material, and a semi-conductive material to be printed on a single layer.

[0015] The semiconductor socket optionally includes at least one external dielectric layer extending beyond the substrate. External routing on the external dielectric layer electrically couples to a portion of the circuit geometry. The external routing can be electrically coupled to one of a power management system, a ground plane, or another semiconductor socket.

[0016] The substrate is optionally a plurality of layers. In one embodiment, the substrate includes at least one additional circuitry plane. The additional circuitry plane can be one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

[0017] The present disclosure is also directed to an electrical assembly including a semiconductor device electrically coupled to the distal ends of the contact members, and a circuit member with a plurality of contact pads electrically coupled to the proximal ends of the contact members. The circuit member can be one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

[0018] The present disclosure is also directed to a method of forming a semiconductor socket. A plurality of discrete contact members are inserted into a plurality of through holes in a substrate. The contact members include proximal ends accessible from a second surface of the substrate and distal ends extending above a first surface of the substrate. At least one dielectric layer is selectively printed on the second surface of the substrate to create recesses corresponding to a target circuit geometry. A conductive material is deposited in a plurality of the recesses to form conductive traces redistributing terminal pitch of the proximal ends of the contact members. The conductive material is preferably printed in the recesses.

[0019] The substrate containing the contact members may be inverted to expose the proximal ends of the contact members that will electrically couple with the printed circuit board. This surface of the substrate and the array of exposed proximal ends of the contact members may be processed to achieve contact retention, to add mechanical features to improve the reliability of the solder joint to the printed circuit board, and to provide a platform to add passive and active circuit features to improve electrical performance or internal function and intelligence.

[0020] Once the substrate is loaded with contact members, the substrate can be processed as a printed circuit or semiconductor package to add functions and electrical enhancements not found in traditional connectors. In one embodiment, electrical devices and conductive traces are printed onto the substrate using, for example, inkjet printing technology, aerosol printing technology, or other printing technology. The ability to enhance the substrate such that it mimics aspects of the IC package and the printed circuit board allows for reductions in complexity for the IC package and the printed circuit board while improving the overall performance of the semiconductor socket.

[0021] The printing processes permits the fabrication of functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0022] The use of additive printing processes permits the material set in a given layer to vary. Traditional printed circuit board and circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer can greatly enhance electrical performance.

[0023] The present method and apparatus can permit dramatic simplification of the contact members and the substrate of the socket housing. The preferably featureless contact members reduce parasitic effects of additional metal features normally present for contact member retention. The present method and apparatus can be compatible with existing high volume manufacturing techniques. Adding functions to the socket housing permits reductions in the cost and complexity of the IC package and/or the printed circuit board.

[0024] In another embodiment, mechanical decoupling features are added to the contact member retention structure. The semiconductor socket can be configured to electrically and mechanically couple to contact pads on the printed circuit board, thereby reducing cost and eliminating at least one reflow cycle that can warp or damage the substrate.

Brief Description of the Several Views of the Drawing

[0025] Figure 1 is a cross-sectional view of a semiconductor socket in accordance with an embodiment of the present disclosure.

[0026] Figure 2 is a cross-sectional view of a semiconductor socket with printed conductive traces in accordance with another embodiment of the present disclosure.

[0027] Figure 3 is a cross-sectional view of an alternate semiconductor socket in accordance with another embodiment of the present disclosure.

[0028] Figure 4 is a cross-sectional view of a semiconductor socket with a compliant layer located between a substrate and a conductive trace in accordance with another embodiment of the present disclosure.

[0029] Figure 5 is a cross-sectional view of a semiconductor socket with multiple layers of conductive traces in accordance with another embodiment of the present disclosure.

[0030] Figure 6 is a cross-sectional view of a semiconductor socket with a printed ground plane in accordance with another embodiment of the present disclosure.

[0031] Figure 7 is a cross-sectional view of a semiconductor socket with conductive traces electrically coupling a plurality of contact members to location external to the substrate in accordance with another embodiment of the present disclosure.

[0032] Figure 8 is a cross-sectional view of two semiconductor sockets electrically coupled by conductive traces in accordance with another embodiment of the present disclosure.

[0033] Figures 9 is cross-sectional views of a semiconductor socket including other electrical devices in accordance with other embodiments of the present disclosure.

[0034] Figures 10 is cross-sectional views of an alternate semiconductor socket including other electrical devices in accordance with other embodiments of the present disclosure.

[0035] Figure 11 is a cross-sectional view of a semiconductor socket with capacitive coupling features in accordance with another embodiment of the present disclosure.

Detailed Description of the Invention

[0036] A semiconductor socket in accordance with the present disclosure permits fine contact-to-contact spacing (pitch) on the order of less than 1.0 millimeter (1×10^{-3} meter), and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch semiconductor sockets are especially useful for communications, wireless, and memory devices. The disclosed low cost, high signal performance semiconductor sockets, which have low profiles and can be soldered to the system PC board, are particularly useful for desktop and mobile PC applications.

[0037] The disclosed semiconductor sockets may permit IC devices to be installed and uninstalled without the need to reflow solder. The solder-free electrical connection of the IC devices is environmentally friendly.

[0038] Figure 1 is a side cross-sectional view of a portion of a semiconductor socket 50 in accordance with an embodiment of the present disclosure. A substrate 52 includes an array of through holes 54 that extend from a first surface 56 to a second surface 58. Recesses 60 are formed in the second surface 58 that overlaps with the through holes 54. In one embodiment, the substrate 52 is the bottom of a socket housing adapted to receive an IC device, such as for example, IC device 92. Although the substrate 52 is illustrated as a generally planar structure, a semiconductor socket according to the present disclosure may include one or more recesses for receiving IC devices and a cover assembly for retaining the IC devices to the substrate 52, such as disclosed in U.S. Pat. Nos. 7,101,210 (Lin et al.); 6,971,902 (Taylor et al.); 6,758,691 (McHugh et al.); 6,461,183 (Ohkita et al.); and 5,161,983 (Ohno et al.), which are hereby incorporated by reference.

[0039] The substrate 52 may be constructed of any of a number of dielectric materials that are currently used to make sockets, semiconductor packaging, and printed circuit boards. Examples may include UV stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert

and resistant to fire. Other suitable plastics include phenolics, polyesters, and Ryton® available from Phillips Petroleum Company.

[0040] The substrate 52 may also be constructed from metal, such as aluminum, copper, or alloys thereof, with a non-conductive surface, such as an anodized surface. In another embodiment, a metal substrate can be overmolded with a dielectric polymeric material. For example, a copper substrate may be placed in a mold and plastic may be injected around it.

[0041] In embodiments where the substrate 52 is a coated metal, the substrate 52 can be grounded to the electrical system, thus providing a controlled impedance environment. Some of contact members 62 can be grounded by permitting them to contact an uncoated surface of the metal housing.

[0042] The substrate 52 may also include stiffening layers, such as metal, ceramic, or alternate filled resins, to be added to maintain flatness where a molded or machined part might warp. The substrate 52 may also be multi-layered (having a plurality of discrete layers).

[0043] A plurality of discrete contact members 62 are inserted into recesses 60 so distal portions 64 extend out through the holes 54. In the illustrated embodiment, the distal portions 64 are simple cantilever beams located above the first surface 56. The distal portions 64 preferably have a generally uniform cross section. The cross-sectional shape can be rectangular, square, circular, triangular, or a variety of other shapes.

[0044] Proximal portions 66 are preferably configured to reside in the recesses 60. In one embodiment, proximal portions 66 form an interference fit with recesses 60. The contact members 62 can be deposited into the recesses 60 using a variety of techniques, such as for example stitching or vibratory techniques.

[0045] The contact members 62 are preferably constructed of copper or similar metallic materials such as phosphor bronze or beryllium-copper. The contact members are preferably plated with a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple layers thereof. In some embodiments the contact members 62 are encapsulated except the distal and proximal ends. Examples of suitable encapsulating materials include Sylgard® available from Dow Coming Silicone of Midland, Mich. and Master Sil 713 available from Master Bond Silicone of Hackensack, N.J. Suitable contact members are disclosed in U.S. Pat.

Nos. 6,247,938 (Rathburn) and 6,461,183 (Ohkita et al.), which are hereby incorporated by reference.

[0046] In one embodiment, bend 70 is formed after insertion to retain the contact members 62 to the substrate 52. The bend 70 also permits distal portions 64 to flex when coupled to contact pad 90 on first circuit member 92.

[0047] Bend 72 in distal portion 64 is optionally provided to enhance coupling with the contact pads 90 on the first circuit member 92. The contact members 62 may have a variety of shapes, such as reversing the bend 72 or basic vertical structures. Proximal portion 66 can be electrically coupled to contact pads 94 on a second circuit member 96 using a variety of techniques, including solder, pressure, and the like. As used herein, the term "circuit member" refers to, for example, a packaged integrated circuit device, an unpackaged integrated circuit device, a printed circuit board, a flexible circuit, a bare-die device, an organic or inorganic substrate, a rigid circuit, or any other device capable of carrying electrical current.

[0048] With contact members 62 inserted, the substrate 52 is optionally inverted to expose the proximal ends 66 located within the recess 60. The proximal ends 66, the recesses 60 and the second surface 58 can then be subjected to additional processing as discussed in the various embodiments detailed below. Solder ball 74 is optionally formed on proximal portion 66 of the contact member 62, as discussed in greater detail below.

[0049] Figures 2 and 3 illustrate alternate semiconductor sockets 100 in accordance with an embodiment of the present disclosure. Dielectric material 102 is printed on the substrate 104 to create recesses or trenches 106. The recesses 106 in the dielectric material 102 are then metalized to create conductive traces 108. The use of a printed dielectric material 102 to form recesses 106 in which the conductive traces 108 are formed has application to any of the embodiments disclosed herein.

[0050] In the illustrated embodiments, the conductive traces 108 are additional circuitry that create an offset or redistribution of the pitch between terminals 110 on the semiconductor device 112 and contact pads 114 on the circuit member 116.

[0051] Metalizing can be performed by printing conductive particles followed by a sintering step, by printing conductive inks, or a variety of other techniques. The metalizing material is preferably of copper or similar metallic materials such as phosphor bronze or beryllium-copper. The resulting conductive traces 108 are

optionally plated to improve conductive properties. The plating is preferably a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple layers thereof.

[0052] The dielectric material 102 may be constructed of any of a number of materials that provide electrostatic dissipation or to reduce cross-talk between adjacent conductive traces 108. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers 102, 104 from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0053] In one embodiment, the conductive traces 108 are formed by depositing a conductive material in a first state in the recesses 106 in the dielectric material, and then processed to create a second more permanent state. For example, the metallic powder is printed and subsequently sintered, or the curable conductive material flows into the recesses 106 and is subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. "Curable" refers to an uncured material having the potential to be cured, such as for example by the application of a suitable energy source.

[0054] The recesses 106 permit control of the location, cross section, material content, and aspect ratio of the conductive traces 108. Maintaining the conductive traces 108 with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses 106 to control the aspect ratio of the conductive traces 108 results in a more rectangular or square cross-section of the conductive traces 108, with the corresponding improvement in signal integrity.

[0055] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 106. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 106. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 106 not occupied

by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 106.

[0056] In another embodiment, a thin conductive foil is pressed into the recesses 106, and the edges of the recesses 106 acts to cut or shear the conductive foil. The process locates a portion of the conductive foil in the recesses 106, but leaves the negative pattern of the conductive foil not wanted outside and above the channels for easy removal. Again, the foil in the channels are preferably post plated to add material to increase the thickness of the conductive traces 108 and to fill any voids left between the conductive foil and the recesses 106.

[0057] Figure 4 illustrates semiconductor socket 130 with a compliant layer 132 supporting the conductive traces 134 in accordance with an embodiment of the present disclosure. Compliant layer 132 is preferably printed on substrate 136, followed by dielectric layer 138 creating recesses 140 for forming the conductive traces 134. The conductive traces 134 are formed as discussed herein. The compliant layer 132 serves to decouple thermal and mechanical stress between the substrate 136 and the circuit member 142.

[0058] Figure 5 illustrates semiconductor socket 150 with multi-layered printed conductive traces in accordance with an embodiment of the present disclosure. Dielectric layers 152A, 152B, 152C,152D (collectively "152") are successively printed on substrate 154. Each layer 152 is selectively printed to create recesses into which circuit traces 156 and/or contact pads 158 are formed to redistribute the pitch 160 of contact members 162. In one embodiment, layer 152B optionally include a compliant material.

[0059] Figure 6 illustrates semiconductor socket 170 with conductive traces 172 serving as a ground plane 174 in accordance to an embodiment of the present disclosure. Dielectric layer 176 is printed so conductive traces 172 connect multiple contact members 178A, 178B. Forming the ground plane 174 on substrate 180 enhances performance and reduces ground connections to circuit member 182.

[0060] Figure 7 is a cross-sectional view of a semiconductor socket 190 according to another embodiment where the conductive traces 192 formed on substrate 194 are used to connect to another circuit, such as for example, a power management circuit. The conductive traces 192 extend beyond a perimeter edge of the substrate 194 to an external connection 196 that does not flow through circuit member 198. In one embodiment, the conductive traces 192 are supported by a

dielectric material, such as for example a polymeric film used to manufacture flexible circuits. The conductive traces 192 can deliver, condition, and manage power from the external connection 196 separate from power provided by the circuit member 198. The conductive traces are preferably formed using the printing technology discussed herein.

[0061] Figure 8 is a variation of Figure 7 that uses the conductive traces 192 to electrically couple two or more semiconductor sockets 190A and 190B. Each circuit member 190A, 190B includes a semiconductor device 200A, 200B. The conductive traces 192 permit socket-to-socket connection of the semiconductor devices 200A, 200B external to the circuit member 198. The conductive traces 192 are preferably supported by a flexible polymeric film.

[0062] Figure 9 illustrates semiconductor socket 220 with electrical devices 222, such as for example, internal decoupling capacitors, located on substrate 224 in accordance with an embodiment of the present disclosure. Printed conductive traces 226 electrically couple the electrical devices 222 to one or more of the contact members 228. The electrical devices 222 can be added as discrete components or printed materials, reducing the need for discrete components on the first and second circuit members 230, 232.

[0063] The electrical devices 222 can be a power plane, ground plane, capacitor, resistor, filters, signal or power altering and enhancing device, memory device, embedded IC, RF antennae, and the like. The electrical devices 222 can be located on either surface of the substrate 224, or embedded therein. The electrical devices 222 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0064] Locating such electrical devices 222 on the semiconductor socket 220 improves performance and enables a reduction in the cost of the integrated circuit 230, the socket 220, and the printed circuit board 232. Integrated circuit manufactures are limited by the pitch that the printed circuit board 232 can accommodate and still keep the printed circuit board to four layers. The integrated circuit makers can manufacture the package 230 with a smaller pitch, but with the pin counts is so high that the printed circuit board 232 likely requires additional layers in order to route all of the signals. The present semiconductor socket 220 permits

integrated circuit manufactures to reduce the pitch of the contacts 234 on the package 230, and perform any required signal routing in the semiconductor socket 220, rather than in the printed circuit board 232 or by adding daughter boards to the system.

[0065] Integrated circuit manufactures also are limited by current socket designs when designing the configuration of contacts 234 on the package 230. Performing the routing in the present semiconductor socket 220 permits quick and inexpensive changes. Similarly, locating the electrical devices 222 in the semiconductor socket 220 permits integrated circuit manufactures to reduce or eliminate the capacitors currently located on the package 230 and printed circuit board 232. This shift can greatly reduce cost and simplify the package 230 and printed circuit board 232, while improving performance.

[0066] One of the reasons the contact members on prior art sockets are so long (typically about 3 millimeters) is to provide clearance for the capacitors on the package 230 and the printed circuit board 232 when the integrated circuit is put into the socket. Locating the electrical devices 222 in the present semiconductor socket 220 permits the contact members 228 to be shorter, which will improve electrical performance.

[0067] The availability of printable silicon inks provides the ability to print electrical devices 222 and conductive traces 226, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[0068] The electrical devices 222 and conductive traces 226 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference.

[0069] Printing process are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0070] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0071] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[0072] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0073] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The

substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0074] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0075] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic/organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0076] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[0077] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0078] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[0079] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0080] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0081] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0082] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[0083] Figure 10 illustrates an alternate semiconductor socket 240 with internal decoupling capacitance 242 in accordance with an embodiment of the present disclosure. The decoupling capacitance 242 can be an discrete embedded or printed electrical device. Contact member 244 provides the electrical connection to the capacitor located on the semiconductor device 246 and solder ball 248 provides the electrical connection to the capacitor located on printed circuit board 250.

[0084] Figure 11 is a cross-sectional view of semiconductor socket 270 with various capacitive coupling features in accordance with another embodiment of the present disclosure. A capacitive coupling feature 272A is embedded in layer 274 of the substrate 275. A capacitive coupling feature 272B is located on second surface 276 of the layer 274. The capacitive coupling features 272A, 272B are positioned to electrically couple with contact pad 278 on first circuit member 280.

[0085] Capacitive coupling feature 282A is embedded in layer 284 of the substrate 275. Capacitive coupling feature 282B is located on first surface 286 of the layer 284. The capacitive coupling features 282C is embedded in layer 288. All three capacitive coupling features 282A, 282B, 282C are positioned to electrically couple with contact pad 290 on the second circuit member 292. The various capacitive coupling features in the embodiment of Figure 11 are optionally formed using inkjet printing technology, aerosol printing technology, or other printing technology.

[0086] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the invention . The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the invention.

[0087] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the

practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[0088] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[0089] Other embodiments of the invention are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the invention. Thus, it is intended that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[0090] Thus the scope of this invention should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean “one and only one” unless explicitly so stated, but rather “one or more.” All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be

encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A semiconductor socket comprising:

a substrate comprising a plurality of through holes extending from a first surface to a second surface;

a plurality of discrete contact members located in the plurality of the through holes, the plurality of contact members each comprising a proximal end accessible from the second surface, and a distal end extending above the first surface;

at least one dielectric layer bonded to the second surface of the substrate with recesses corresponding to target circuit geometry; and

a conductive material deposited in at least a portion of the recesses comprising conductive traces of a circuit geometry redistributing terminal pitch of the proximal ends of the contact members.

2. The semiconductor socket of claim 1 comprising conductive plating on at least a portion of the conductive traces.

3. The semiconductor socket of claim 1 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.

4. The semiconductor socket of claim 1 comprising a compliant material located between the substrate and at least a portion of the circuit geometry.

5. The semiconductor socket of claim 1 comprising at least one printed electrical device on one of a dielectric layer or the substrate and electrically coupled to at least a portion of the circuit geometry.

6. The semiconductor socket of claim 1 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

7. The semiconductor socket of claim 1 wherein a conductive material, a non-conductive material, and a semi-conductive material are printed on a single layer.

8. The semiconductor socket of claim 1 comprising:

at least one external dielectric layer extending beyond the substrate; and

external routing on the external dielectric layer electrically coupled to a portion of the circuit geometry.

9. The semiconductor socket of claim 8 wherein the external routing is electrically coupled to one of a power management system, a ground plane, or another semiconductor socket.

10. The semiconductor socket of claim 1 comprising a plurality of recesses in the second surface of the substrate that at least partially overlap with the plurality of through holes, the recesses comprise a cross-sectional area greater than a cross-sectional area of the through holes.

11. The semiconductor socket of claim 1, wherein the substrate comprises a plurality of layers.

12. The semiconductor socket of claim 1, wherein the substrate comprises at least one additional circuitry plane.

13. The semiconductor socket of claim 12 wherein the at least one additional circuitry plane comprises one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

14. The semiconductor socket of claim 1 comprising:

a semiconductor device electrically coupled to the distal ends of the contact members; and

a circuit member with a plurality of contact pads electrically coupled to the proximal ends of the contact members.

15. The semiconductor socket of claim 14 wherein the circuit member is selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

16. A method of forming a semiconductor socket comprising:

providing a substrate with a plurality of through holes extending from a first surface to a second surface;

inserting a plurality of discrete contact members in the plurality of through holes, the contact members comprising proximal ends accessible from the second surface and distal ends extending above the first surface;

printing at least one dielectric layer selectively on the second surface of the substrate to create recesses corresponding to a target circuit geometry; and

depositing a conductive material in a plurality of the recesses to form conductive traces redistributing terminal pitch of the proximal ends of the contact members.

17. The method of claim 16, comprising depositing a compliant layer between the second surface and a portion of the conductive traces.

18. The method of claim 16 comprising applying conductive plating to at least a portion of the conductive traces.

19. The method of claim 16 comprising printing the recesses with a substantially rectangular cross-sectional shape.

20. The method of claim 16 wherein the step of depositing the conductive material comprises one or more of printing a conductive material in the recesses and sintering the conductive material or printing a conductive ink in the recesses.

21. The method of claim 16 comprising:

printing at least one electrical device on the semiconductor socket; and

electrically coupling the electrical device to the circuit geometry.

22. The method of claim 21 wherein the electrical device is selected from one of transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, optical fibers, printed optical quality material, coaxial structures, or printed micro strip RF circuits.

23. The method of claim 16 comprising printing one or more of a non-conductive material or a semi-conductive material in one or more of the recesses.

24. The method of claim 16 comprising the steps of:

locating pre-formed conductive materials in one or more of the recesses; and

plating the recesses to form conductive traces with cross-sectional shapes corresponding to a cross-sectional shape of the recesses.

25. The method of claim 16 comprising the steps of:

pressing conductive foil into at least a portion of the recesses;

shearing the conductive foil along edges of the recesses;

removing excess conductive foil not located in the recesses; and

plating the recesses to form conductive traces with substantially rectangular cross-sectional shapes.

26. The method of claim 16 comprising:

printing at least one external dielectric layer that extends beyond the substrate; and

printing external routing on the external dielectric layer electrically coupled to a portion of the circuit geometry.

27. The method of claim 26 comprising electrically coupling the external routing to one of a power management system, a ground plane, or another semiconductor socket.

28. The method of claim 16 comprising printing at least one additional circuitry plane on the second surface of the substrate.

29. The method of claim 28 wherein the at least one additional circuitry plane comprises one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

30. The method of claim 16 comprising:

electrically coupling a semiconductor device to the distal ends of the contact members; and

electrically coupling a circuit member to the proximal ends of the contact members.

31. The method of claim 30 wherein the circuit member is selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

32. The method of claim 26, further comprising:

printing a plurality of electrical devices on the substrate; and

electrically coupling each of the plurality of electrical devices to at least one of the plurality of contact members.

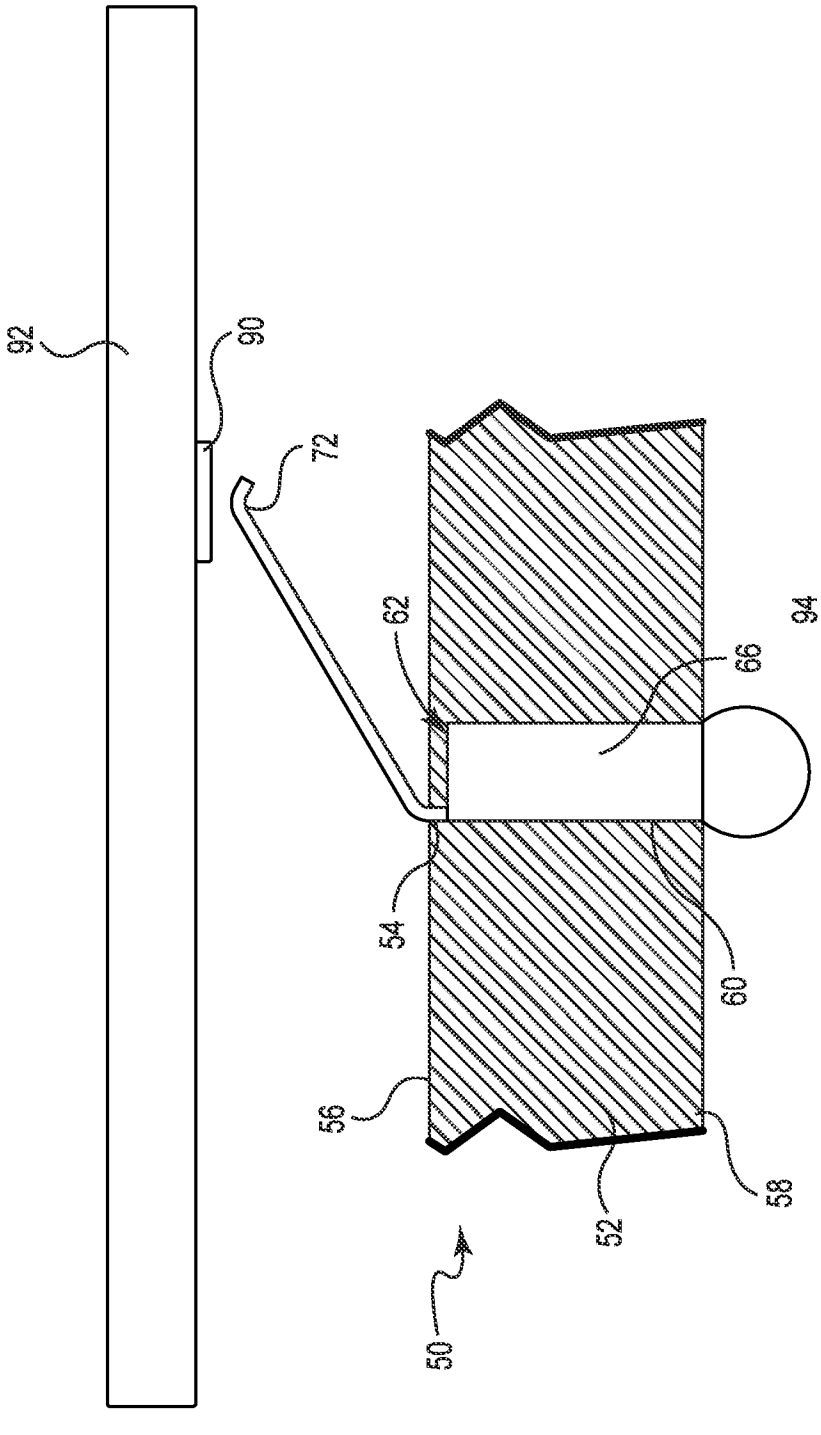


Fig. 1

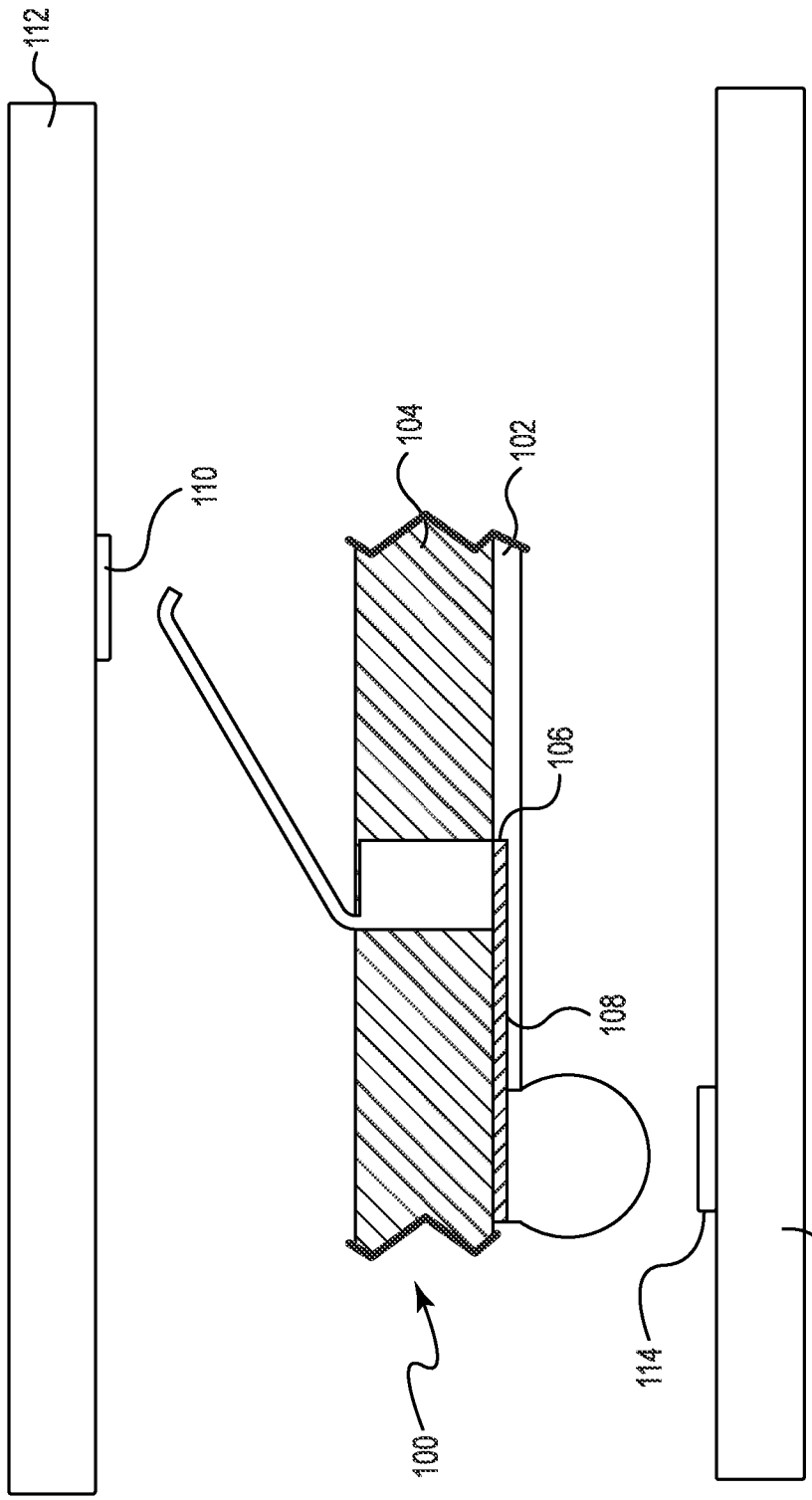


Fig. 2

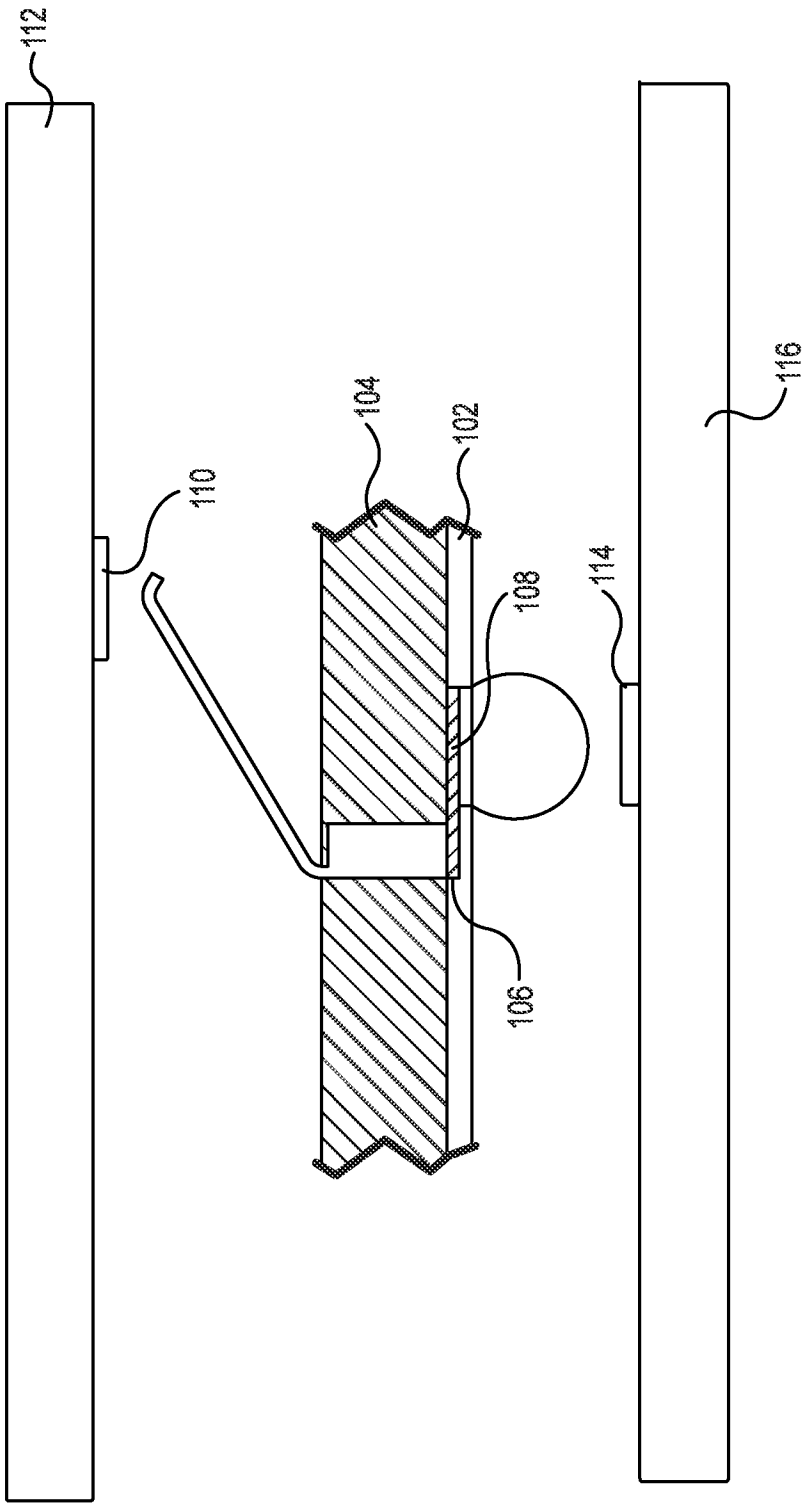


Fig. 3

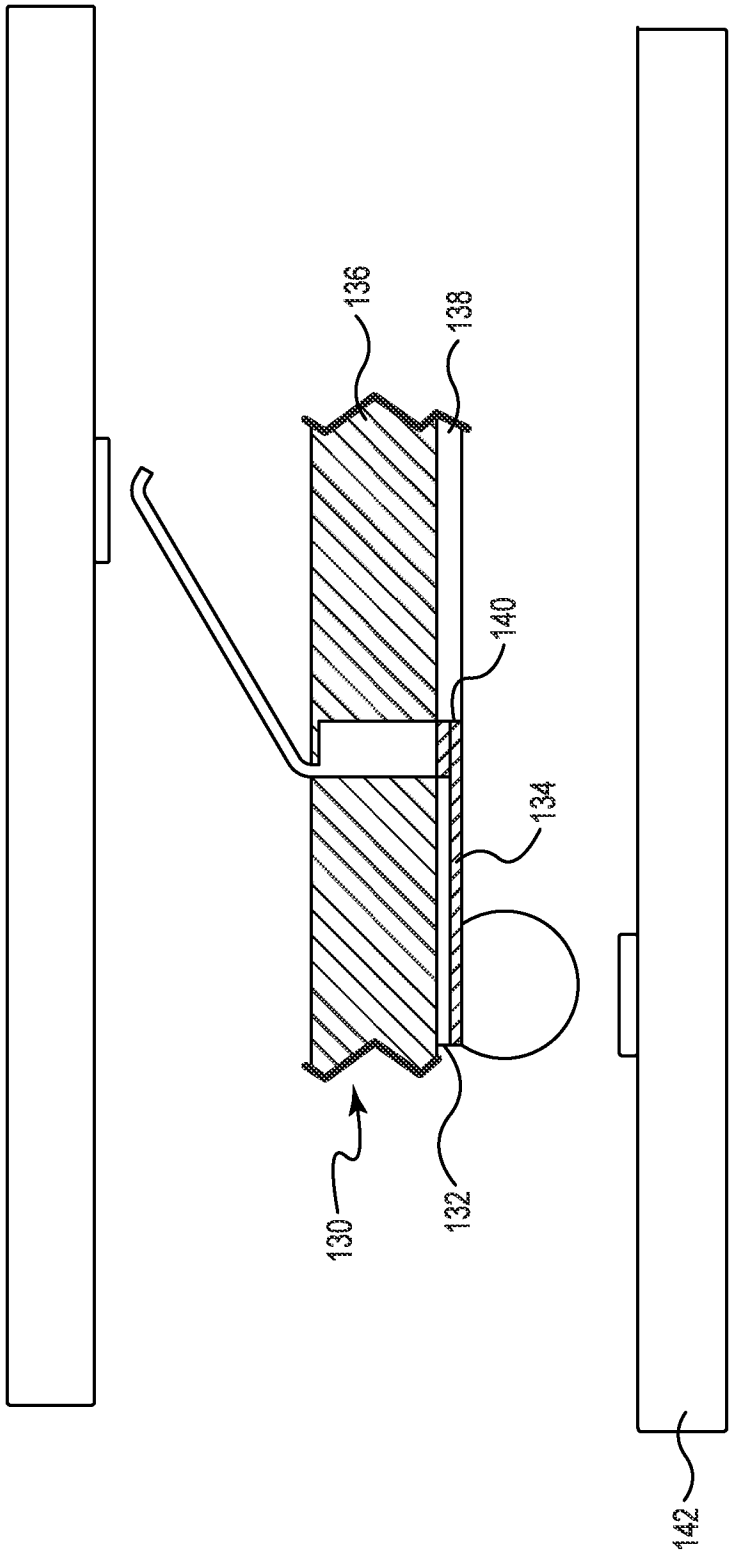


Fig. 4

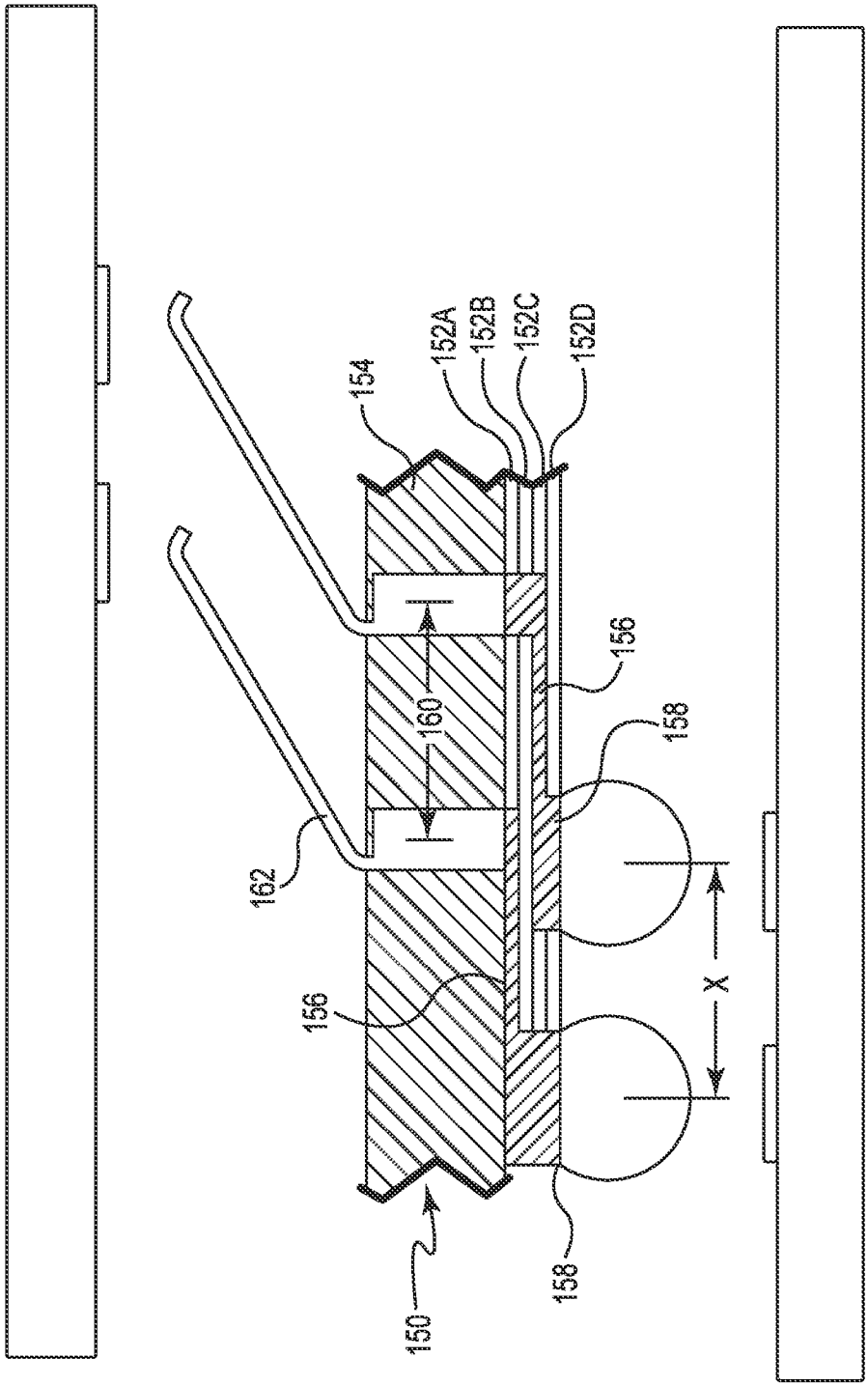


Fig. 5

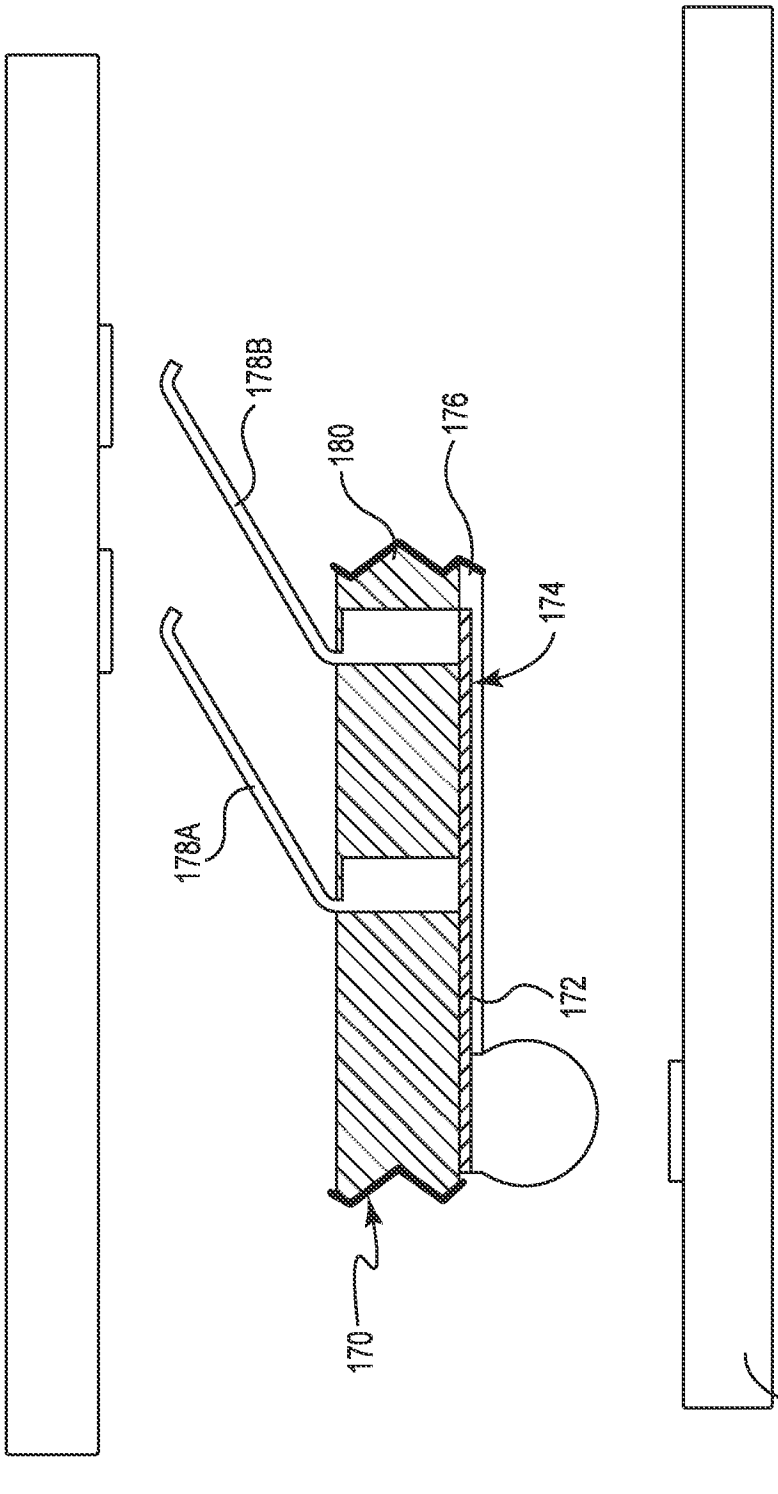


Fig. 6

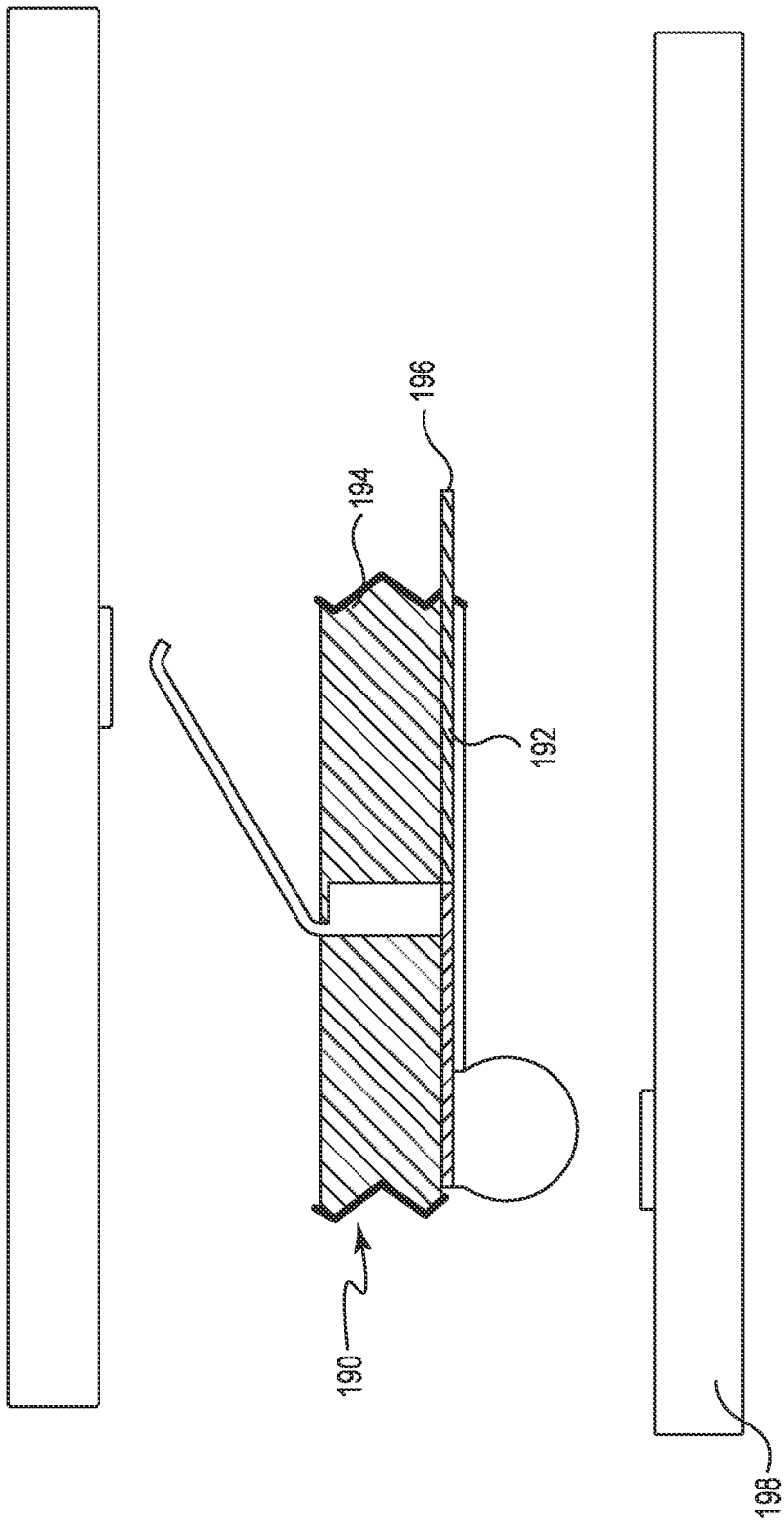


Fig. 7

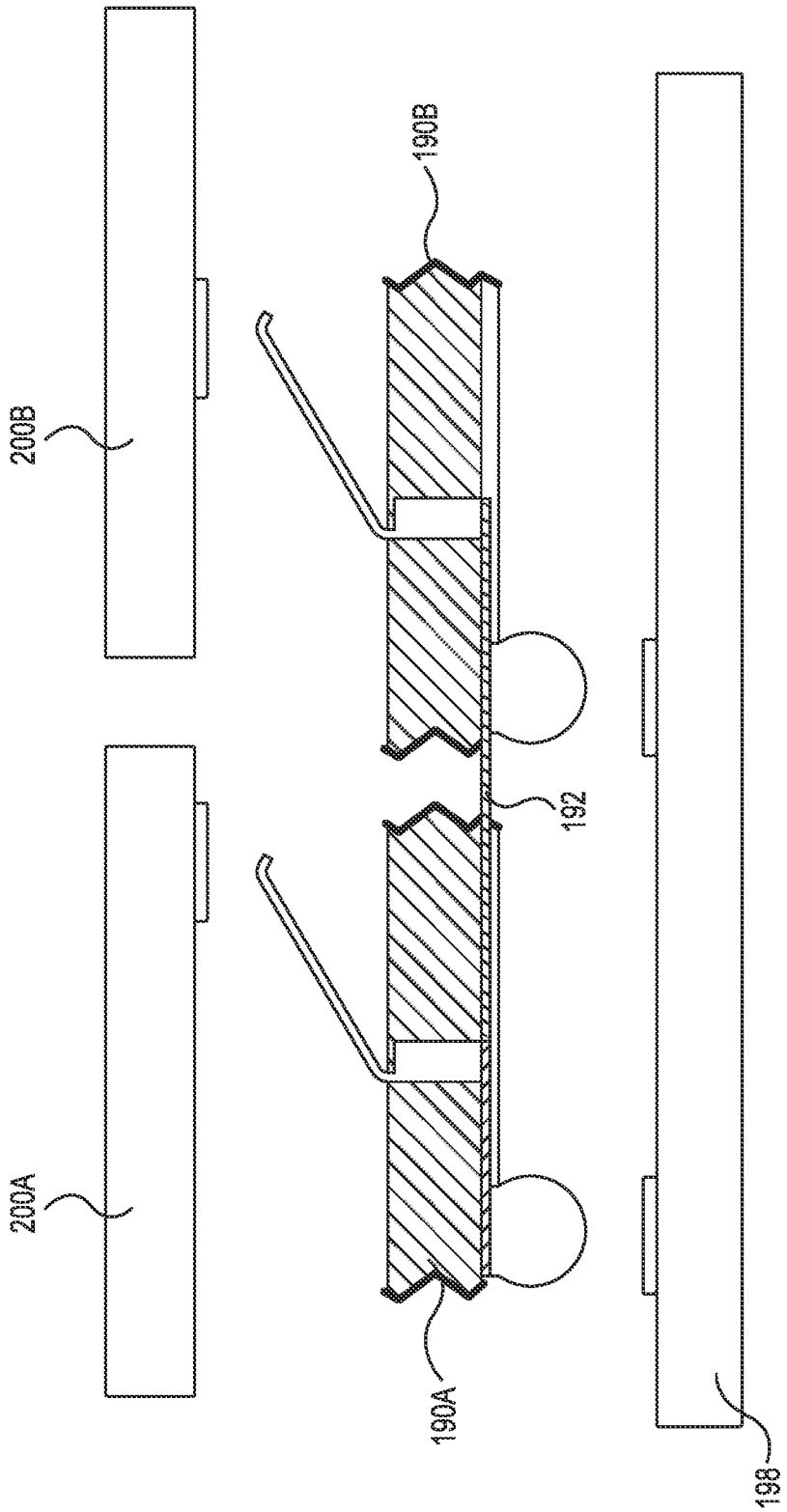


Fig. 8

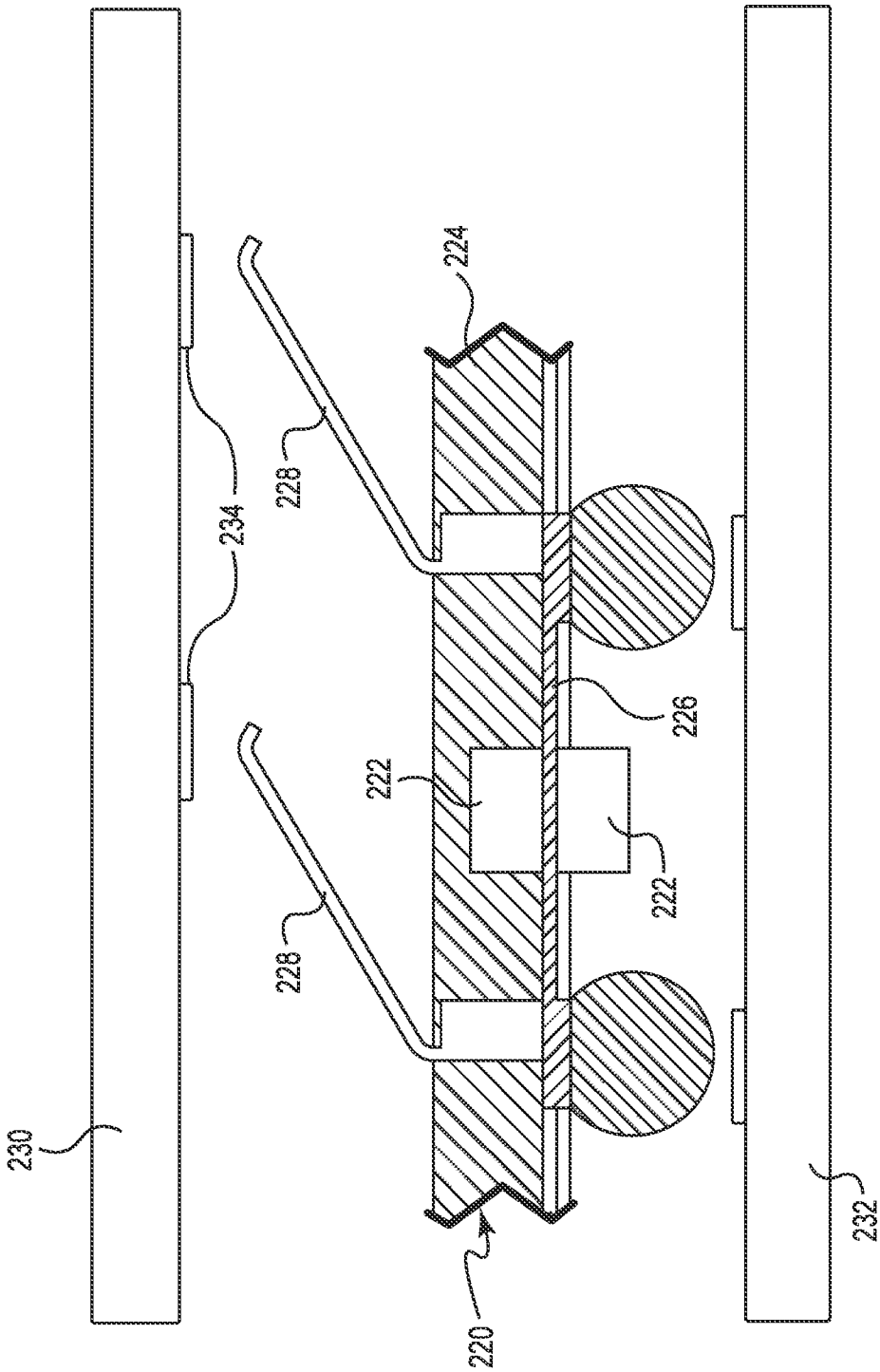


Fig. 9

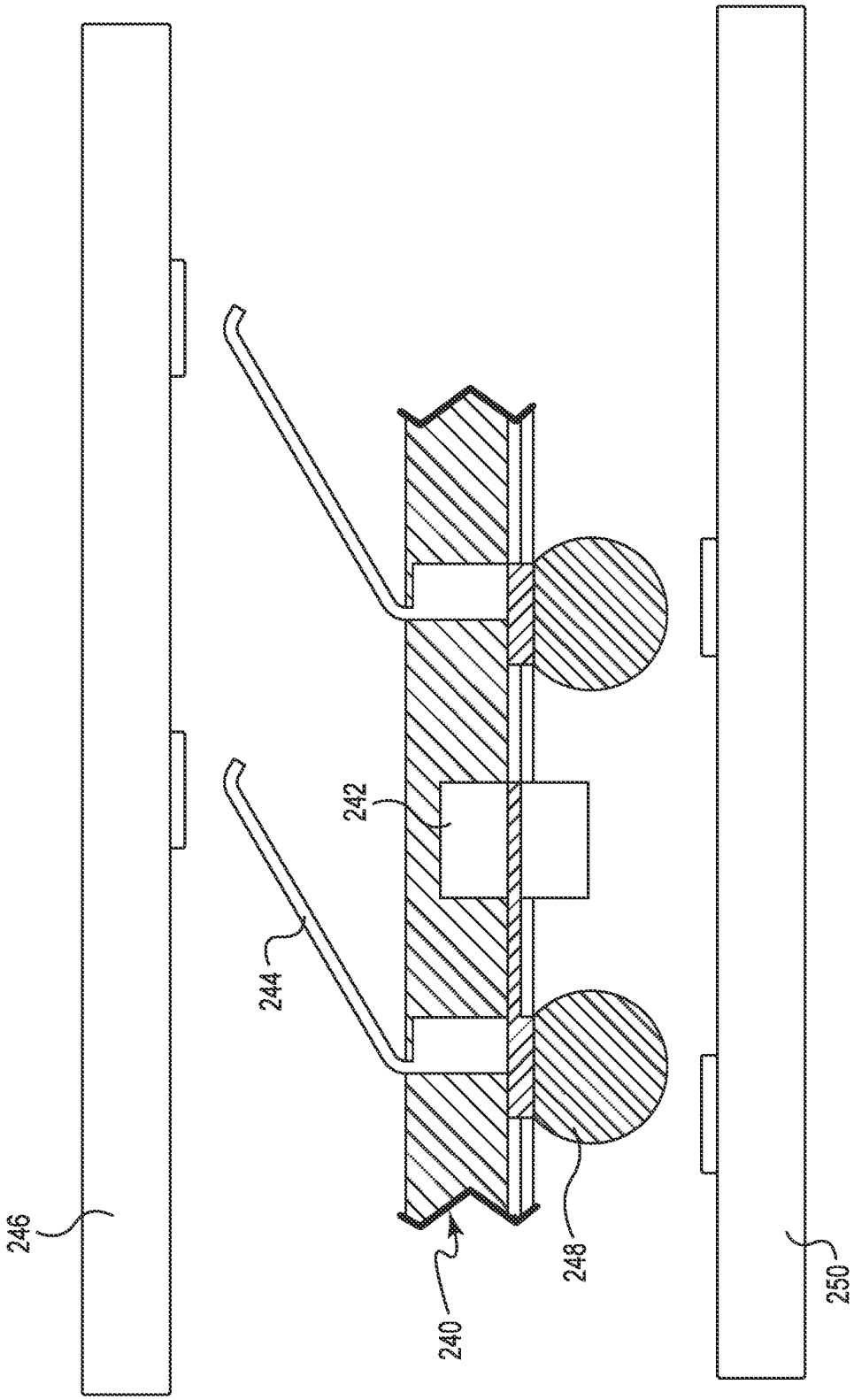
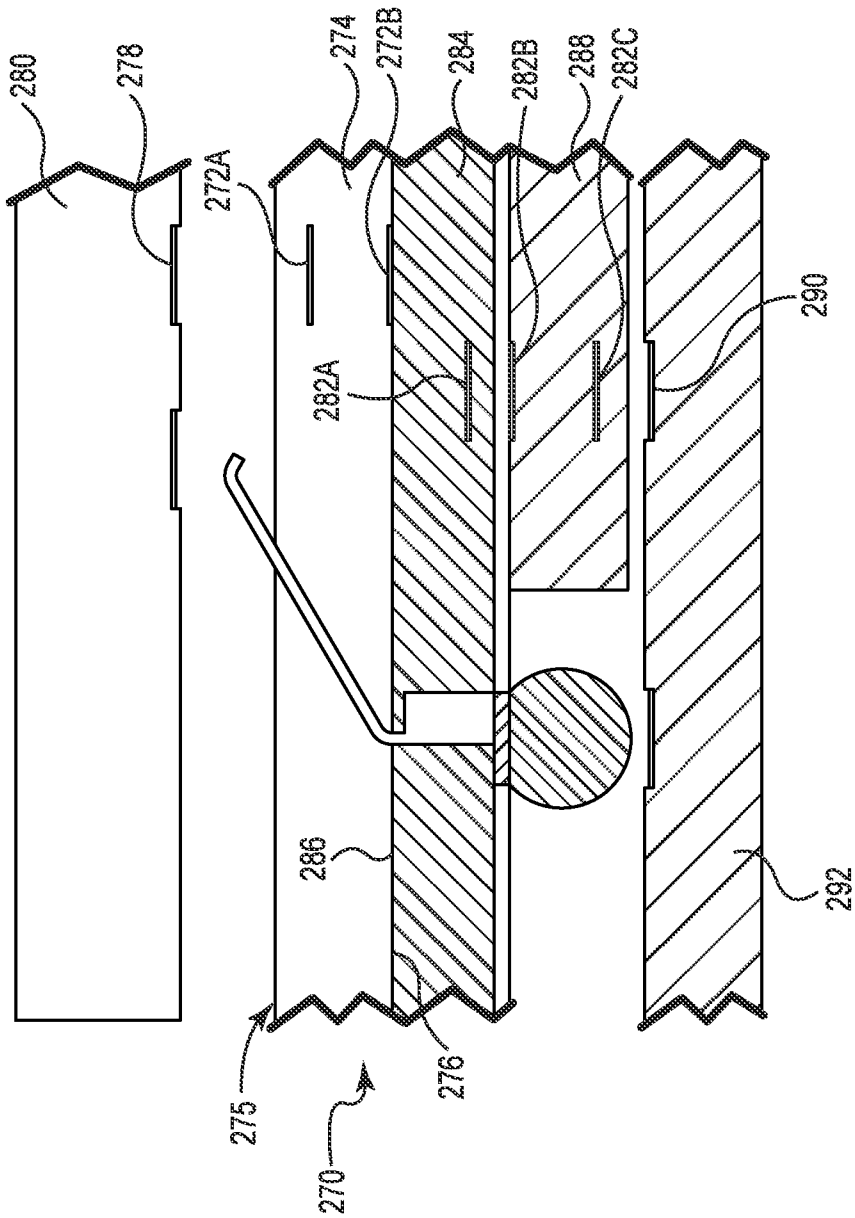


Fig. 10


280
278
274
272B
284
282B
288
282C
272A
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282A
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292
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276
270

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/038606

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05K 1/11 (2010.01)
USPC - 439/66
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01R 12/14, 20, 22, 24, 28; H05K 1/11 (2010.01)
USPC - 439/65-67, 78, 81, 84

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, GooglePatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 7,326,064 B2 (RATHBURN et al) 05 February 2008 (05.02.2008) entire document	1-2, 4, 6, 8-15 ---------- 3, 5, 7, 16-32
Y	US 6,506,438 B2 (DUTHALER et al) 14 January 2003 (14.01.2003) entire document	3, 5, 7, 16-32
Y	US 5,819,579 A (ROBERTS) 13 October 1998 (13.10.1998) entire document	25
A	US 6,830,460 B1 (RATHBURN) 14 December 2004 (14.12.2004) entire document	1-32

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2010	18 AUG 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)